Instrumentation of Particle Physics Experiments

HUCHENG CHEN

BROOKHAVEN NATIONAL LABORATORY

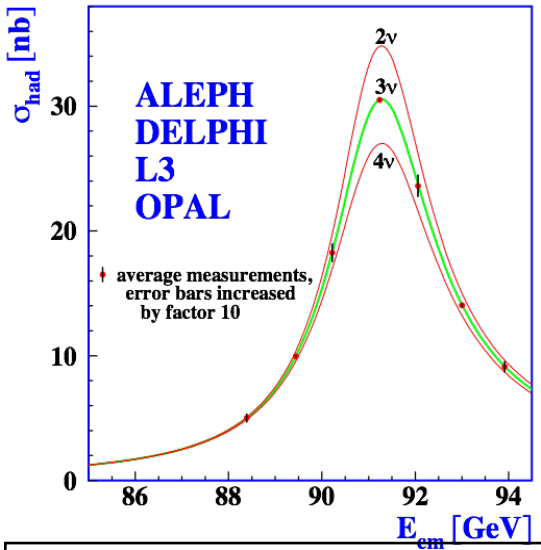
WHEPS – WEIHAI HIGH ENERGY PHYSICS SCHOOL 2015

Lecture 4 – Accelerator Based Neutrino Experiments and Cold Electronics Development

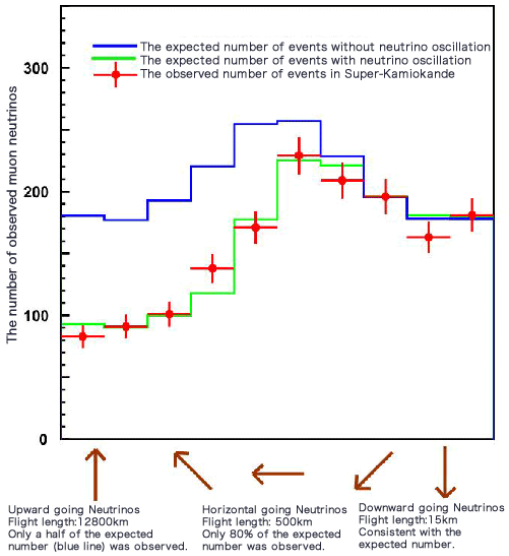
- Accelerator Based Neutrino Experiments in US
  - Short Baseline Neutrino Program
  - Long Baseline Neutrino Program
- Cold Electronics Development
  - A Brief History of Cold Electronics
  - Advantages of Cold Electronics
  - R&D on CMOS Cold Electronics
  - Electronics Lifetime at 300K and 77K

Three Neutrino Paradigm

- Early 1990s:
  - Measurement of the lineshape of the Z^0 at LEP and SLC in the early 1990s puts tight constraint of three (2.984±0.008) light neutrinos that couple to the Z^0
  - At the time no proof that neutrinos have mass
- 1998:
  - Measurement of atmospheric neutrinos in Super-Kamiokande conclusively demonstrates neutrino oscillations and therefore neutrinos have mass



Phys.Rept.427:257-454,2006 (http://arxiv.org/abs/hep-ex/0509008)



More Neutrinos?

- Hints from several experiments at shorter baselines cannot be explained by the the three neutrino mixing paradigm
  - Reactor experiments at very short baseline
  - Radioactive source experiments
  - LSND experiment

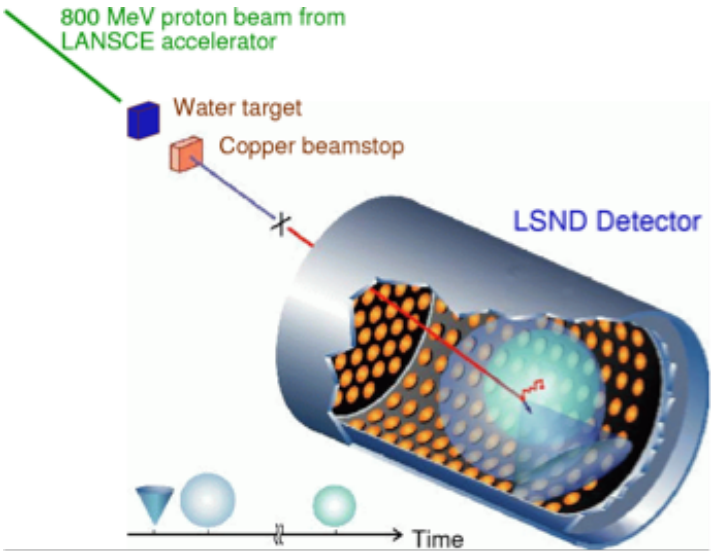
Table 14.1: Sensitivity of different oscillation experiments.

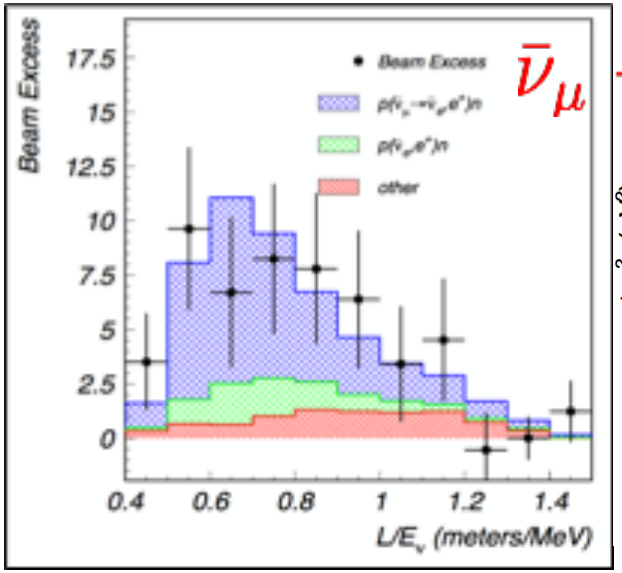
	Source	Type of ν	$\overline{E}$[MeV]	L[km]	$\min(\Delta m^2)[\mathrm{eV}^2]$
	Reactor	$\overline{\nu}_e$	~ 1	1	$\sim 10^{-3}$
	Reactor	$\overline{\nu}_e$	~ 1	100	$\sim 10^{-5}$
Short-baseline	Accelerator	$\nu_\mu, \overline{\nu}_\mu$	$\sim 10^3$	1	~ 1
	Accelerator	$\nu_\mu, \overline{\nu}_\mu$	$\sim 10^3$	1000	$\sim 10^{-3}$
	Atmospheric ν's	$\nu_{\mu,e}, \overline{\nu}_{\mu,e}$	$\sim 10^3$	10^4	$\sim 10^{-4}$
	Sun	ν_e	~ 1	1.5×10^8	$\sim 10^{-11}$

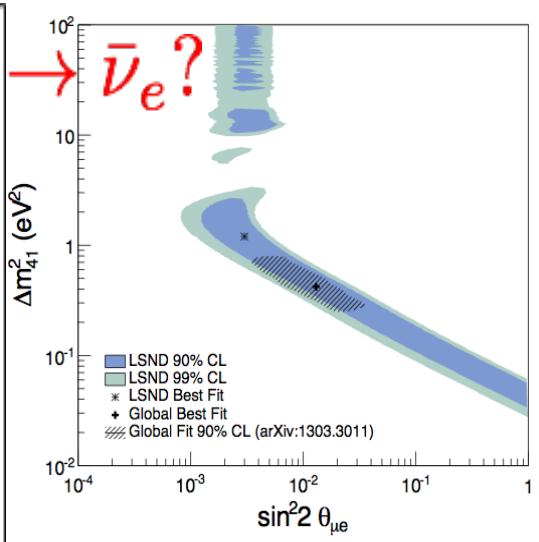
PDG - http://pdg.lbl.gov/2014/reviews/rpp2014-rev-neutrino-mixing.pdf

Liquid Scintillator Neutrino Detector (LSND)

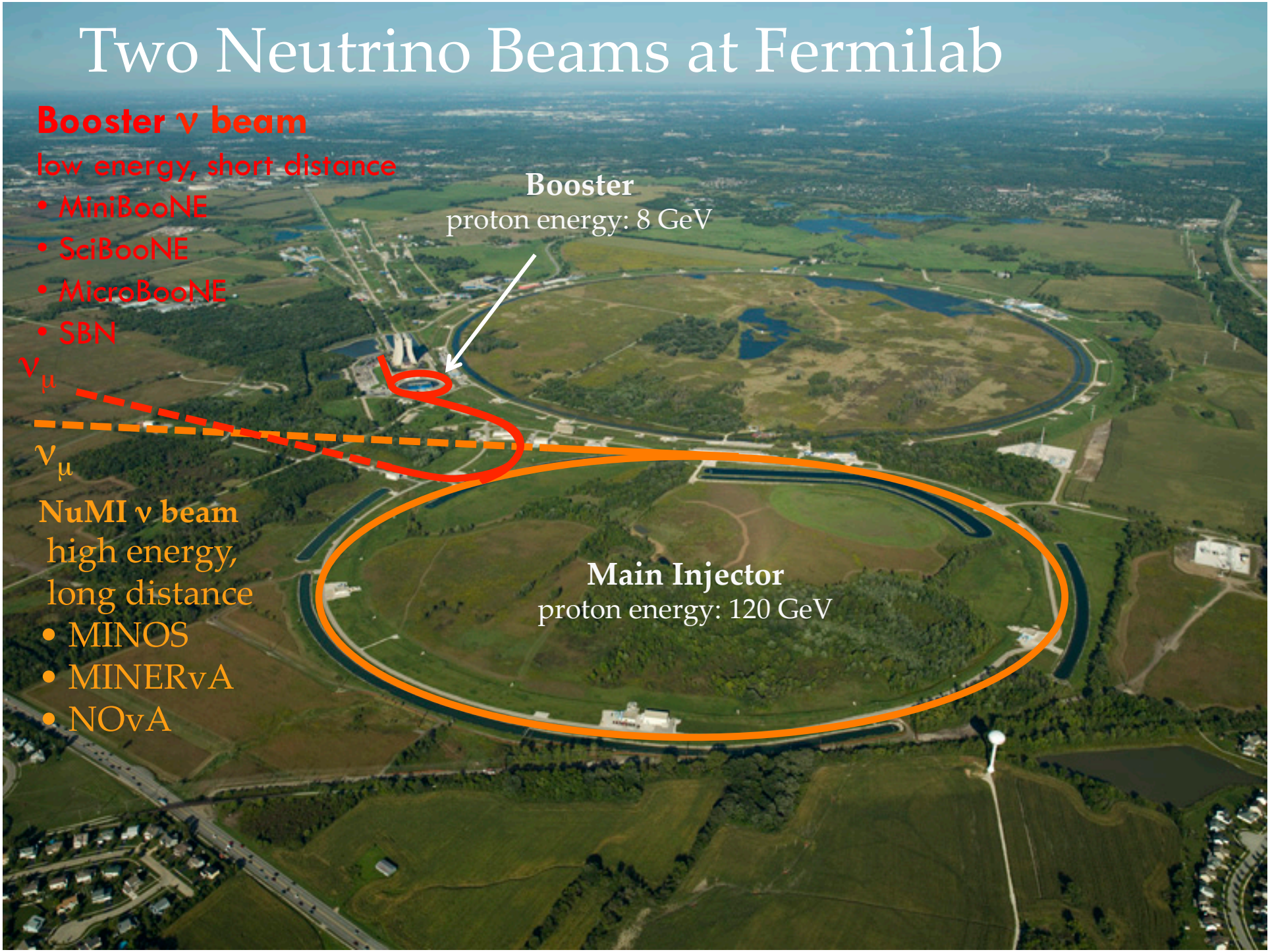
- Low energy $\bar{\nu}_\mu$ beam from DAR using LANSCE proton beam at LANL
- Detect 3.8σ excess of $\bar{\nu}_e$ via inverse beta decay in liquid scintillator detector
- If interpreted as mixing: not consistent with L/E of the three neutrino paradigm:
  - L/E ~ 1 km/GeV
- Could this be evidence of mixing through a sterile sector?







Two Neutrino Beams at Fermilab



Fermilab Short-Baseline: Booster Neutrino Beam (BNB)

- Well understood ν flux with peak at ~700 MeV
  - Hadron production data (HARP experiment @ CERN)
  - 10+ years of study by MiniBooNE and SciBooNE
- Detectors at ~500m yield L/E ~ 1 km/GeV
- Robust target and single horn system: 375 million pulses on last horn
- Beam near surface (~10m):
  - \+ Modest civil construction cost
  - – Cosmic backgrounds

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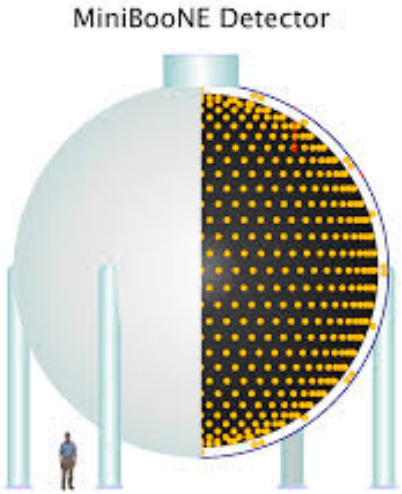
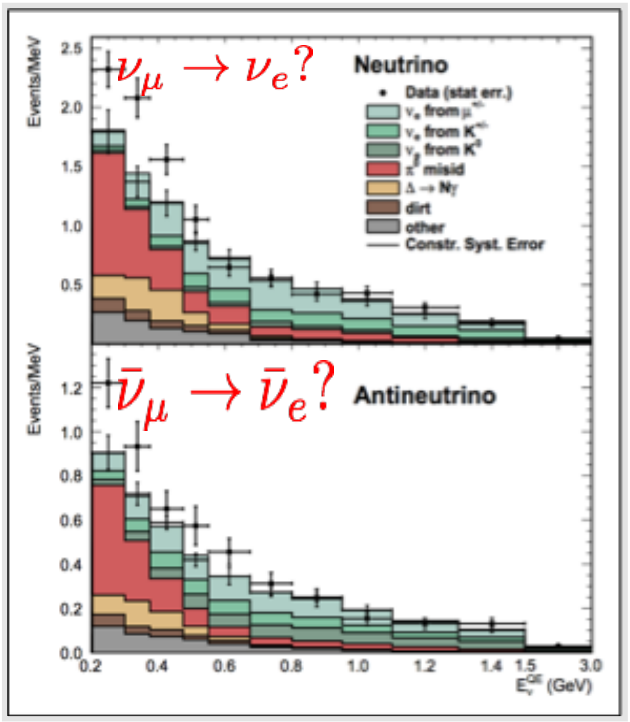
PDG - http://pdg.lbl.gov/2014/reviews/rpp2014-rev-neutrino-mixing.pdf

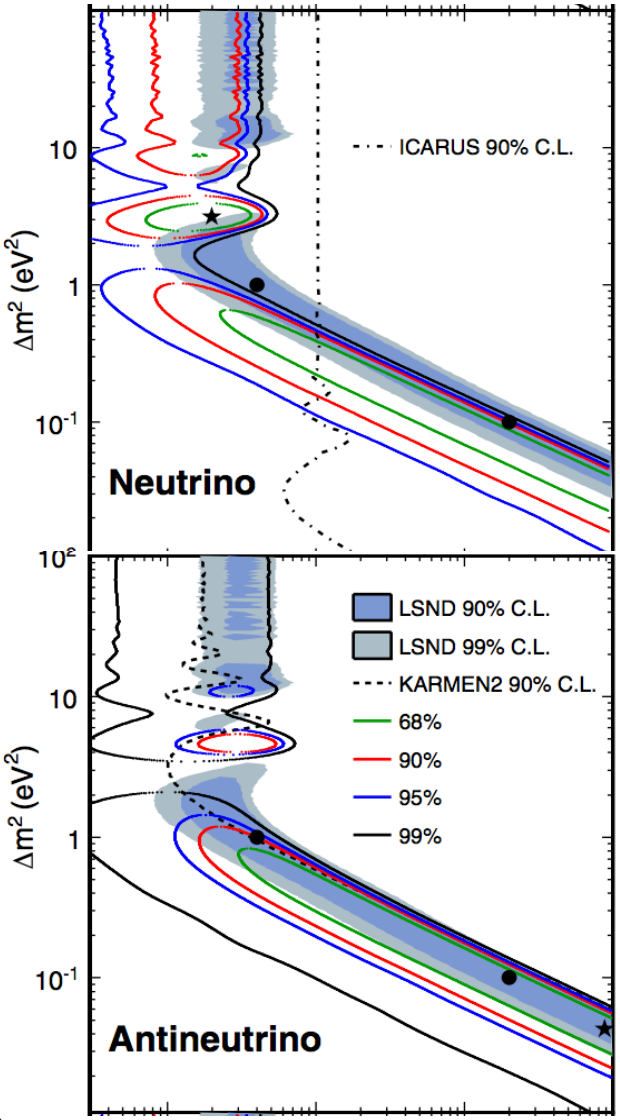
First Generation on BNB: MiniBooNE



Follow up on LSND with different E_ν and baseline but same L/E

Low energy excess:
- Not good fit to LSND result
- Is it e or γ?





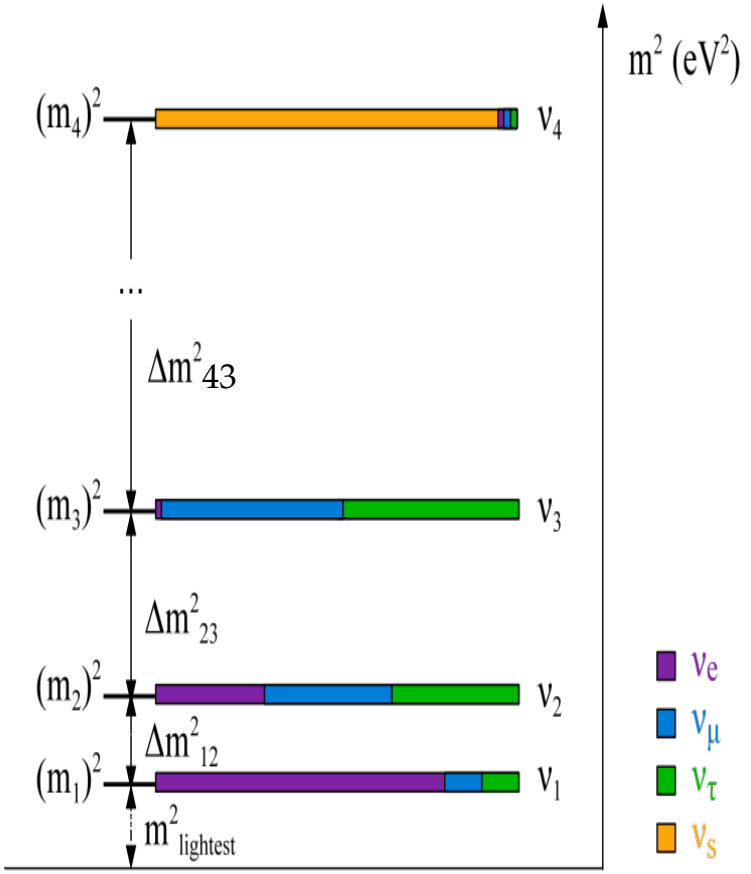
Phys.Rev.Lett. 110 (2013) 161801
(http://arxiv.org/pdf/1303.2588v2.pdf)

The Sterile Neutrino Picture

Experiment	Type	Channel	Significance
LSND	DAR	$\bar{\nu}_\mu \to \bar{\nu}_e$ CC	3.8σ
MiniBooNE	SBL accelerator	$\nu_\mu \to \nu_e$ CC	3.4σ
MiniBooNE	SBL accelerator	$\bar{\nu}_\mu \to \bar{\nu}_e$ CC	2.8σ
GALLEX/SAGE	Source - e capture	ν_e disappearance	2.8σ
Reactors	Beta-decay	$\bar{\nu}_e$ disappearance	3.0σ

K. N. Abazajian et al. "Light Sterile Neutrinos: A Whitepaper", arXiv: 1204.5379 [hep-ph], (2012)

- For comparisons work with 3 + 1 models. However, models with a single ν_s don't describe all of the data



The discovery of a light sterile neutrino would monumental for particle physics and cosmology

Brief History of Fermilab SBN Program

2003-13 - 1st gen. BNB experiments: MiniBooNE and SciBooNE

2015-18 - 2nd gen. BNB experiment: MicroBooNE - address the MiniBooNE low energy excess (e or γ)

2009-13 - Proposals to address short-baseline anomalies using multiple LAr TPCs:

- X ICARUS@CERN: no ν beam at CERN
- X LAr1@FNAL: rejected by PAC and P5 – too expensive

Jan. 2014 – Two new proposals to Fermilab PAC for next phase at BNB:

- P-1052: ICARUS@FNAL: Updated ICARUS-T600 detector plus new T150 as near detector on the BNB for oscillation searches.
- P-1053: LAr1-ND*: LAr1-ND + MicroBooNE (possibly followed by 1kton scale far detector).

2014 – Proponents of ICARUS, LAr1-ND, and MicroBooNE, plus representatives from FNAL, INFN and CERN, work together to develop a coherent SBN physics program.

* Recent name change: LAr1-ND ➔ Short-Baseline Near Detector (SBND)

The SBN Proposal

- Returned to the January 2015 PAC meeting with an updated proposal:

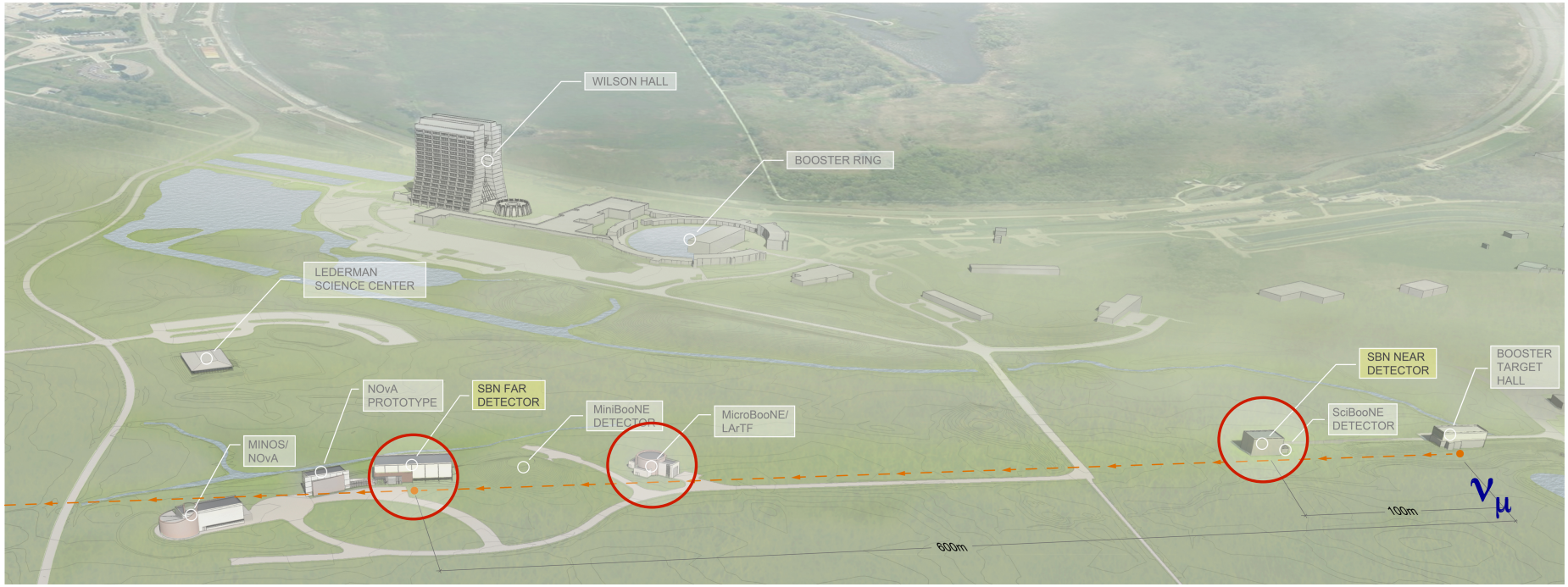
A Proposal for a Three Detector Short-Baseline Neutrino Oscillation Program in the Fermilab Booster Neutrino Beam

Submitted jointly by ICARUS, MicroBooNE and SBND (LAr1-ND)
http://arxiv.org/abs/1503.01520

- Measure ν_e appearance and ν_μ disappearance in one program
- Detailed analysis for program sensitivities (e.g.):
  - Cosmogenic and beam based backgrounds ("Dirt" events)
  - Systematics from flux minimized by use of near detector
  - Detector systematics reduced by use of common technology
- To address cosmics from surface operation need: overburden, fast light detection and external cosmic tagger systems
- Technology development for LBNF/DUNE
- Granted Stage 1 approval by Fermilab director in February

Operate in 2018

SBN Program – Three detectors with one mission



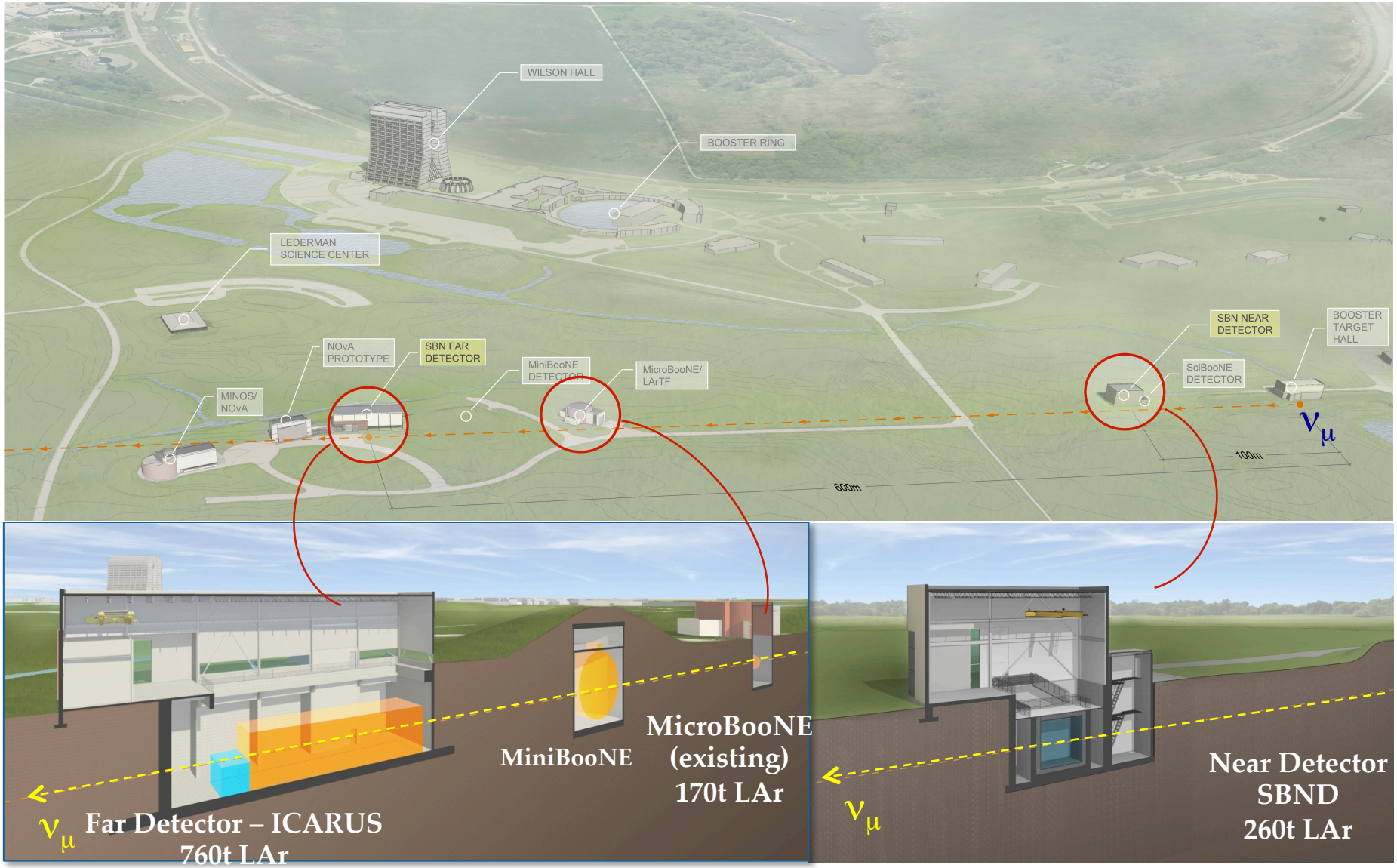
	ICARUS	MicroBooNE	SBND	Produce
ν_μ Disappearance	Fewer ν_μ ?	Fewer ν_μ ?	ν_μ	ν_μ
ν_e Appearance	More ν_e?	More ν_e?	~1% ν_e	~1% ν_e

110m

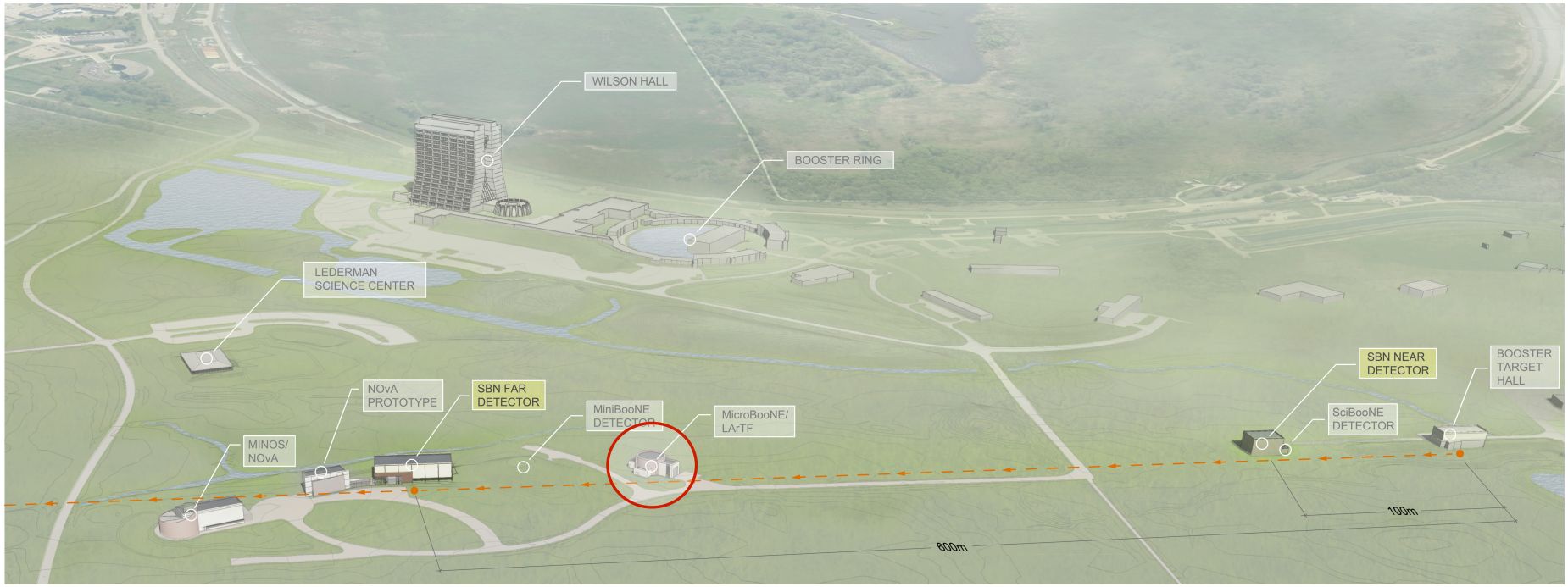
470m

600m

Three detectors with one technology: Liquid Argon TPC



SBN Middle Detector: MicroBooNE



MicroBooNE Experiment

- 170 ton LAr TPC in the Fermilab Booster Neutrino Beamline

- MicroBooNE is also an important first step in the SBN program

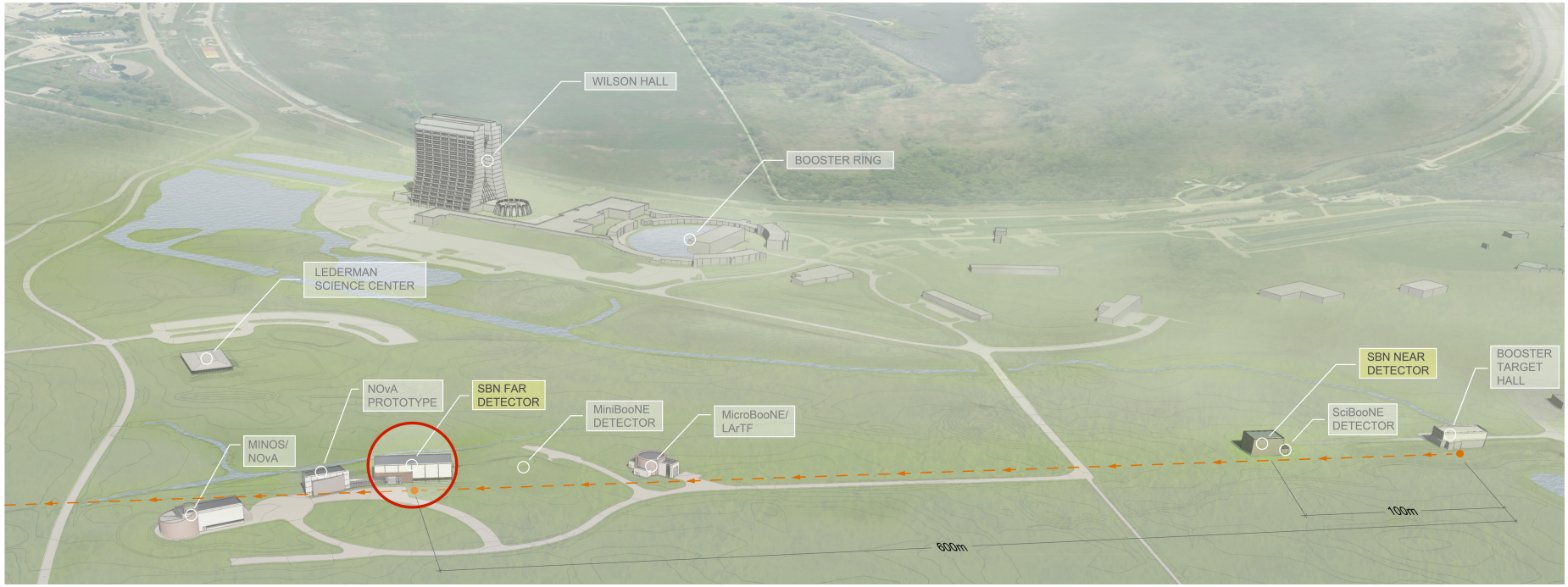
- <u>physics goals</u>:
  - *address MiniBooNE low energy excess*
  - *make 1st low energy neutrino cross section measurements on Ar*

- <u>technical advances</u>:
  - *argon fill without evacuation* (*1st demonstrated in LAPD*)
  - *cold front-end electronics*
  - *long drift (2.5m)*
  - *near surface operation*
  - *automated reconstruction*

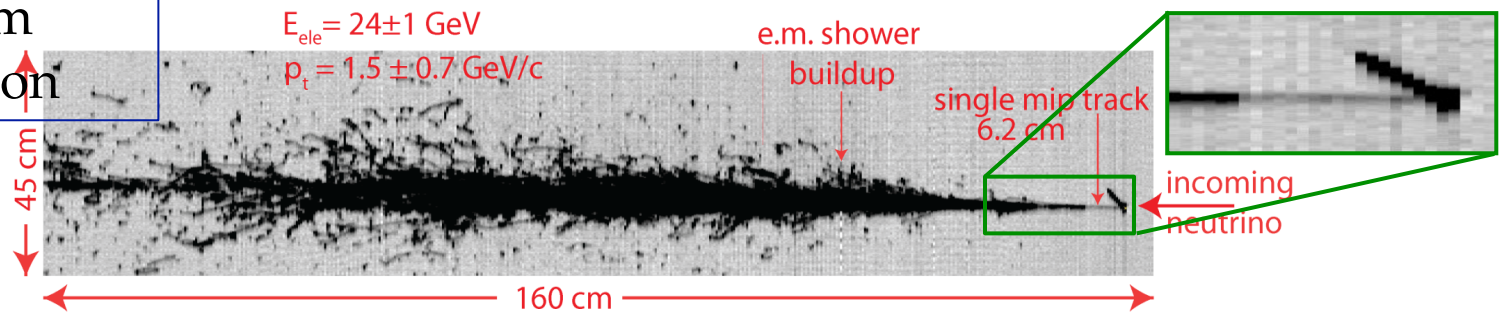
MicroBooNE Status

- *1st phase of cryo system exercised last spring*
- *detector completed, installed, and cabled in LArTF last year*
- *CD-4 granted in December 2014*
- *2nd phase of cryogenics system installed*
- *commissioning in progress!*
- *reading out the detector and exercising the DAQ*
- *biased the wire planes; discovered a set of noisy channels (<1% of the wires)*
- *Booster horn replacement will be completed in summer*
- *detector purge started April 20th*
- *first cosmic event recorded on August 6th*

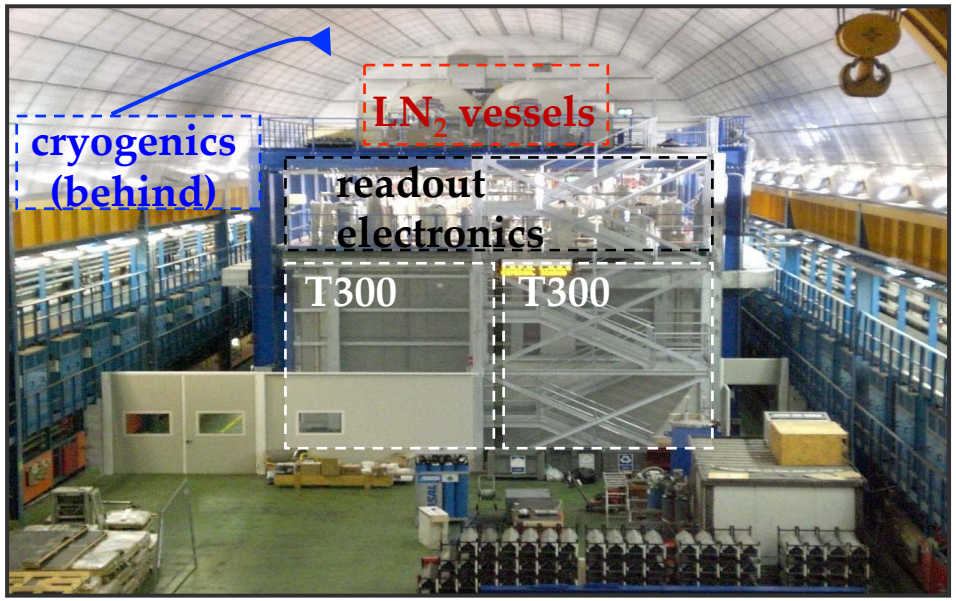
SBN Far Detector: ICARUS

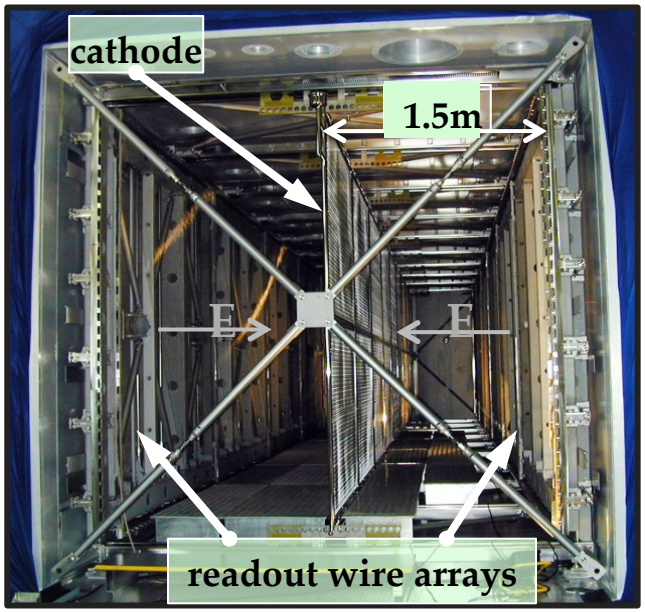


ICARUS Electron candidate from LNGS operation



Far Detector: ICARUS-T600



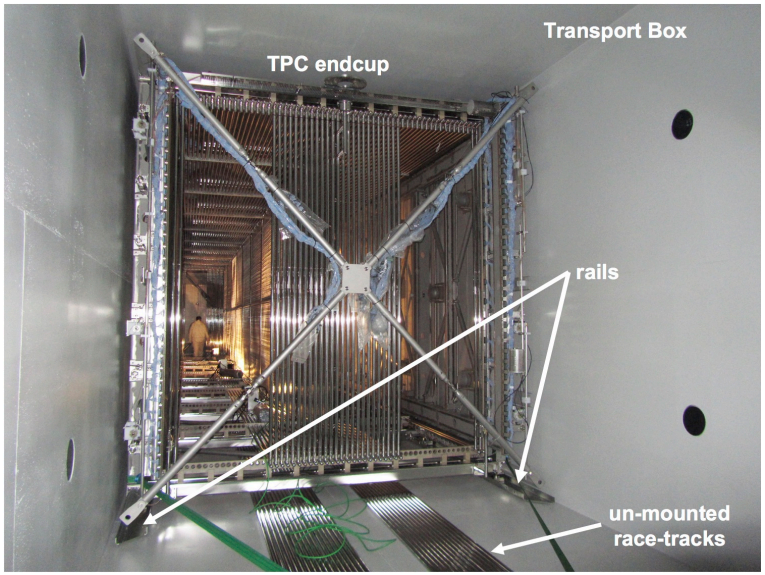


- Two identical modules (T300):
  - 3.6x3.9x19.6m^3 each
  - LAr active mass: ~476 t
  - Drift length = 1.5 m (1 ms)
  - Very high LAr purity achieved (t_{ele} ~ 15ms)

- Two TPCs per module
  - 3 readout wire planes at 0, ±60°
  - ~ 54000 wires, 3 mm pitch and plane spacing
  - Charge measurement on collection plane
- PMTs for scint. light detection
  - 8" tubes (20 in one module, 54 on other)
  - VUV sensitive (128nm) with TPB wavelength shifter coating

ICARUS T600 Transport to CERN

- Move to CERN completed December 2014



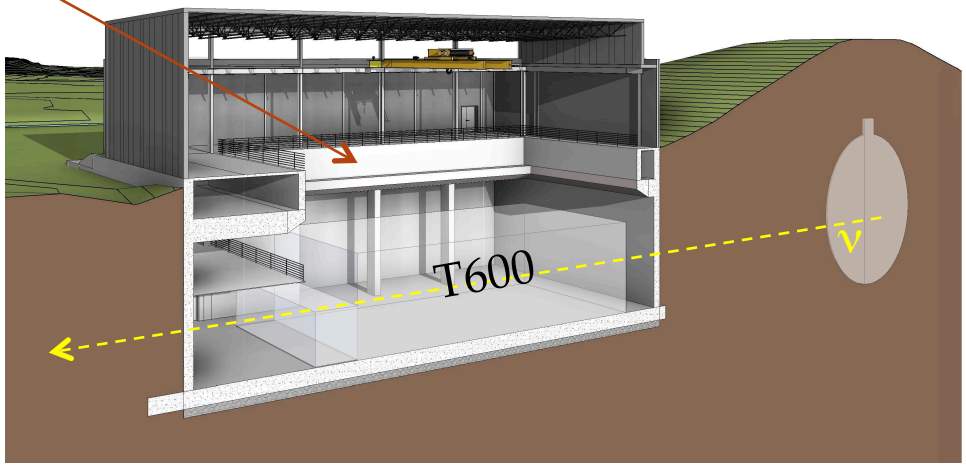
ICARUS-T600: Refurbishing at CERN

- ICARUS-WA104 collaboration to refurbish TPCs at CERN:
  - New cryostats with improved insulation
  - New cabling
  - Upgrade TPC electronics: testing both new warm electronics and possible use of BNL cold amplifier (MicroBooNE, LArIAT)
- For SBN surface operation need improved cosmic rejection:
  - Improved light detection: more PMTs (180/ module) and faster electronics (~ns resolution)
  - External cosmic tagger system (e.g. scint.)
- Schedule
  - ✓ Move from Gran Sasso to CERN Dec 2014
  - ✓ Refurbishing started Jan 2015
  - TPCs delivered to FNAL as soon as the building is available, currently foreseen as early 2017

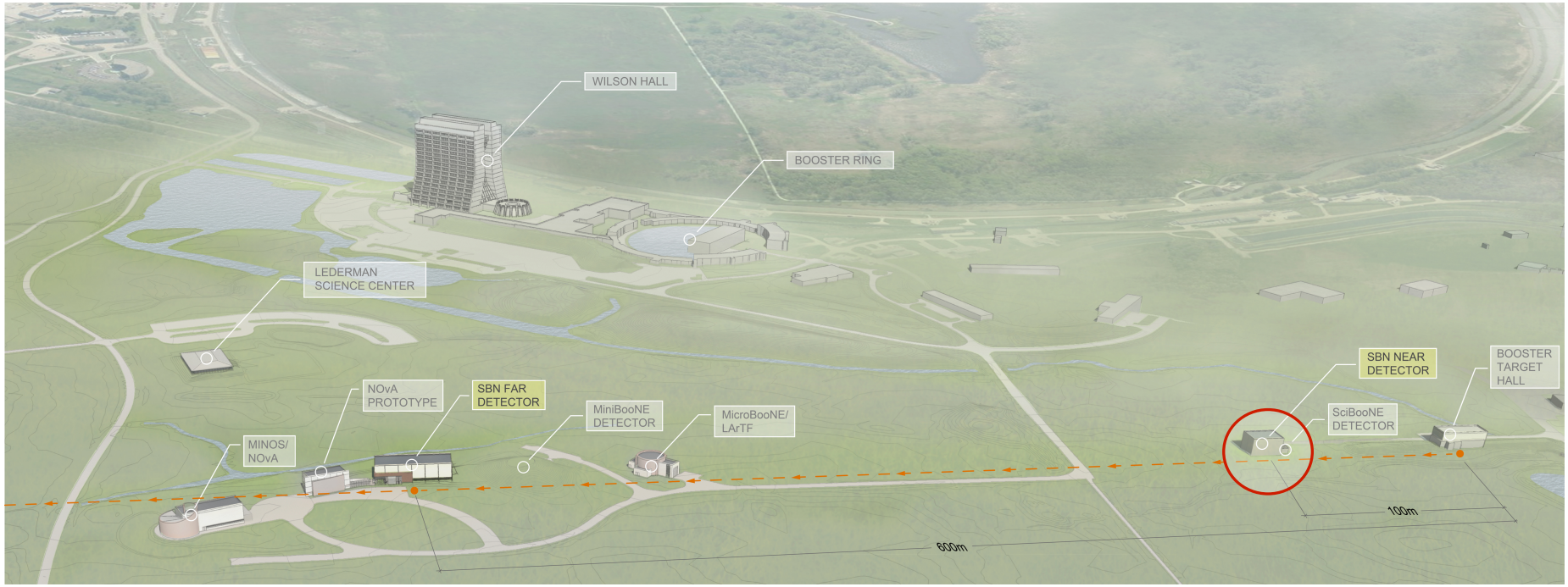
Far Detector Building

- Preliminary design started summer 2014
- Close cooperation between ICARUS, CERN and Fermilab on design requirements and review
- Designed for 3m concrete overburden over detector to mitigate cosmogenic backgrounds for near surface operation

- Timeline:
  - ✓ March 2015 - Design complete
  - ✓ April 2015 - Construction contract bidding (complete May 2015)
  - ✓ August 2015 - Construction start
  - Nov 2016 - Beneficial occupancy



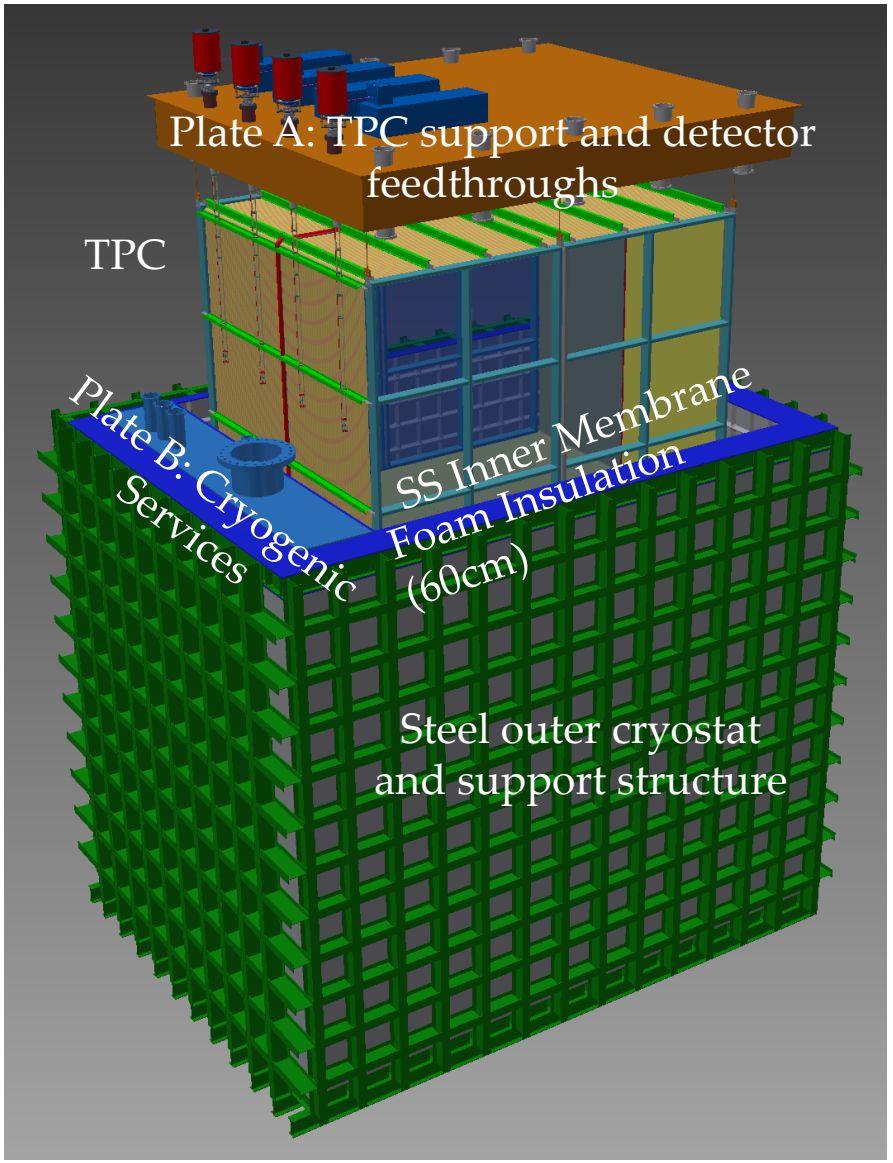
SBN Near Detector: SBND



- Build on experience from ICARUS, MicroBooNE, DUNE 35 ton prototype
- Opportunity for prototyping DUNE designs
  - TPC construction techniques (US NSF – STFC)
  - TPC Electronics (US DOE/NSF)
  - Light detection (tbd)
  - Cryostat technology (CERN-Fermilab)
  - Cryogenics systems (CERN-Fermilab)
  - Laser Calibration (SNSF)
  - Cosmic Tagger System (SNSF)

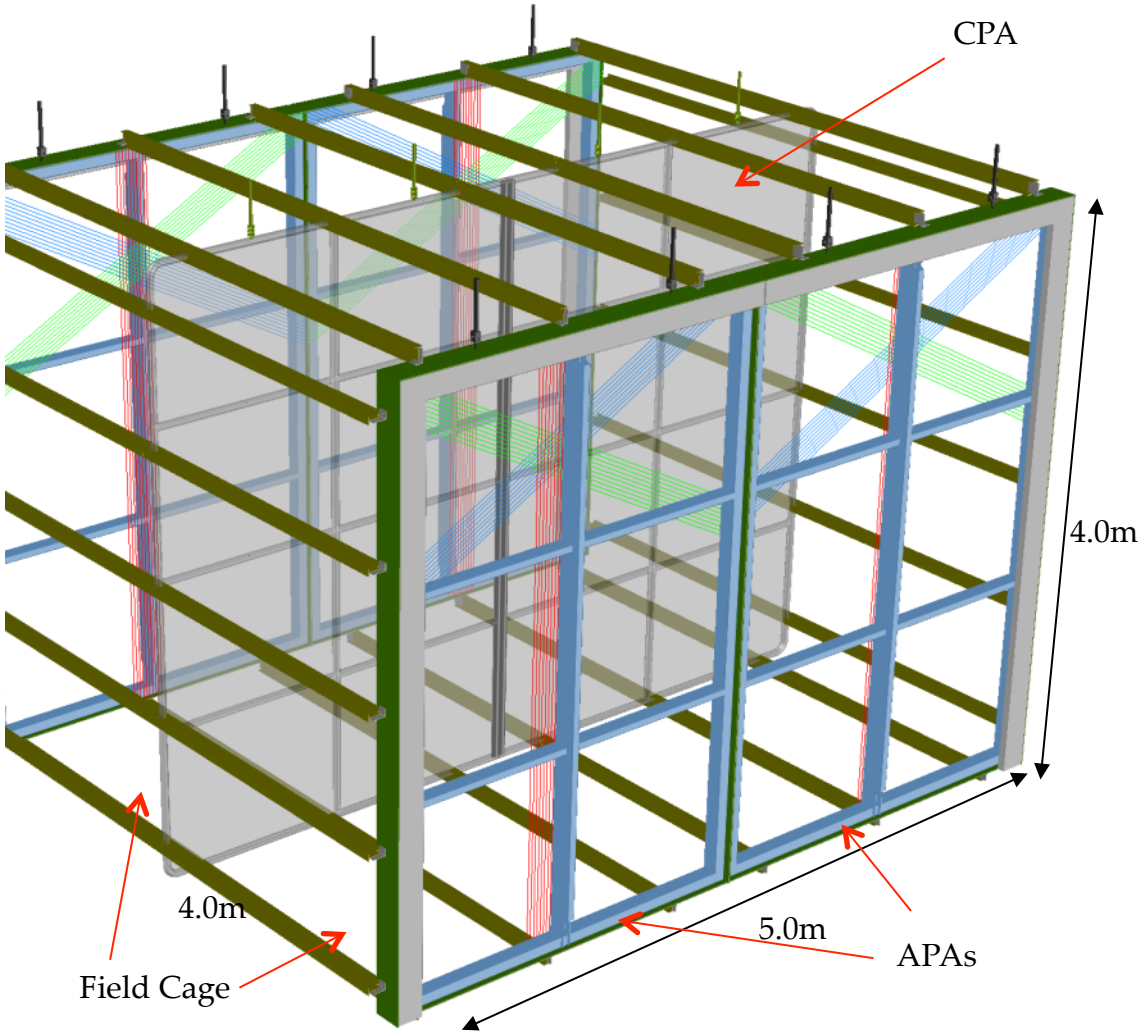
SBND Cryostat + TPC

- Membrane cryostat: same as planned for the DUNE far detector
  - Two worldwide vendors serving the LNG industry (IHI-Japan, GTT-France)
- Series of cryostats being jointly developed by CERN and Fermilab
  - ✓ LBNE 35t (IHI)
  - WA105-182 dual-phase (50t) (GTT)
  - SBND (GTT through CERN)
  - WA105 dual-phase (GTT)
  - DUNE single-phase for CERN testbeam (GTT)
  - Full size LBNF 10-40kt
- Collaboration between Fermilab and CERN



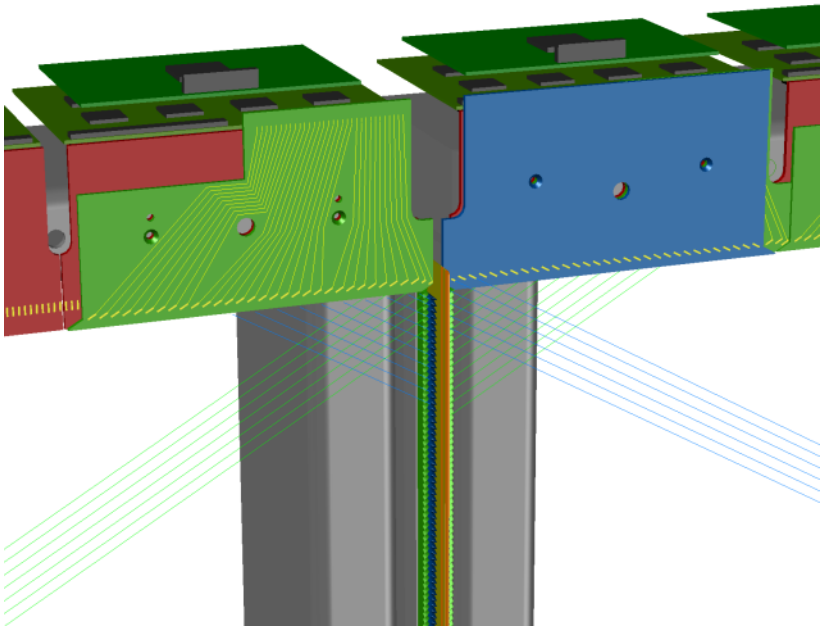
SBND TPC Design

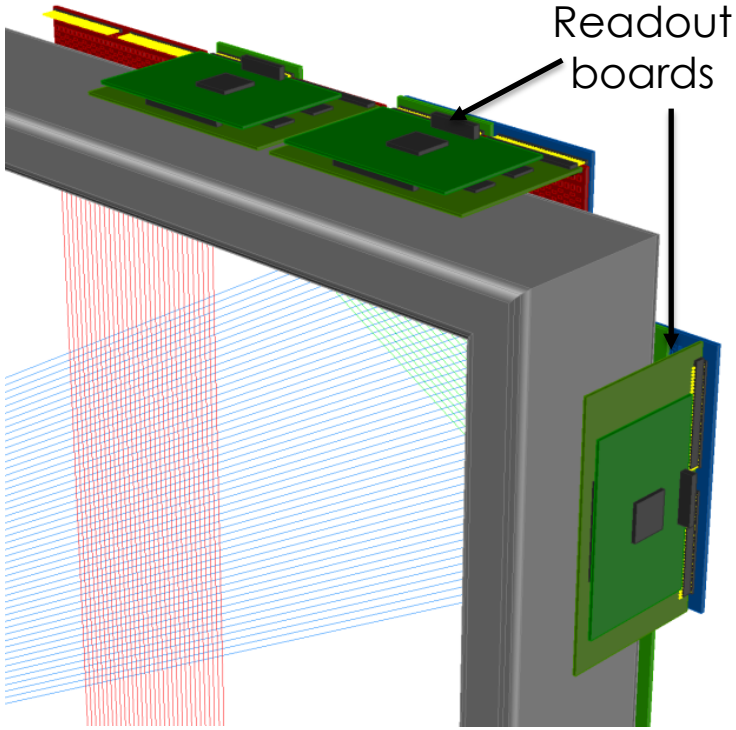
- Started with current DUNE single phase design
- Active volume: 5m (beam) x 4m (width) x 4m (height)
- Central cathode plane assembly (CPA), two anode plane assemblies (APA) on either side w/ 2m drift distance each.
- Single sided APA wire planes joined at edge to reduce readout channels
- Light detectors mounted behind APAs on frames

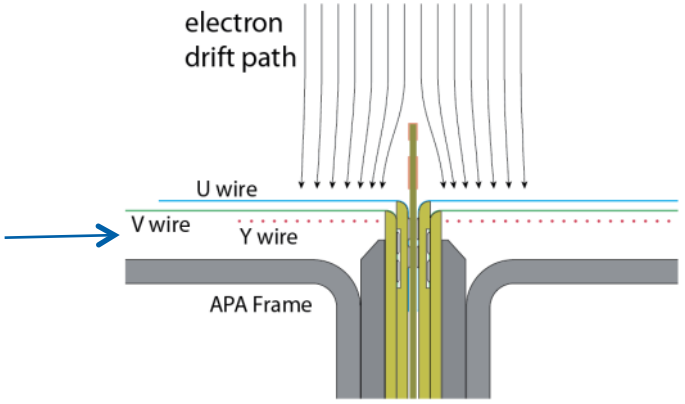


SBND: Anode Plane Assemblies

The SBND APA is a hybrid between that of MicroBooNE and DUNE



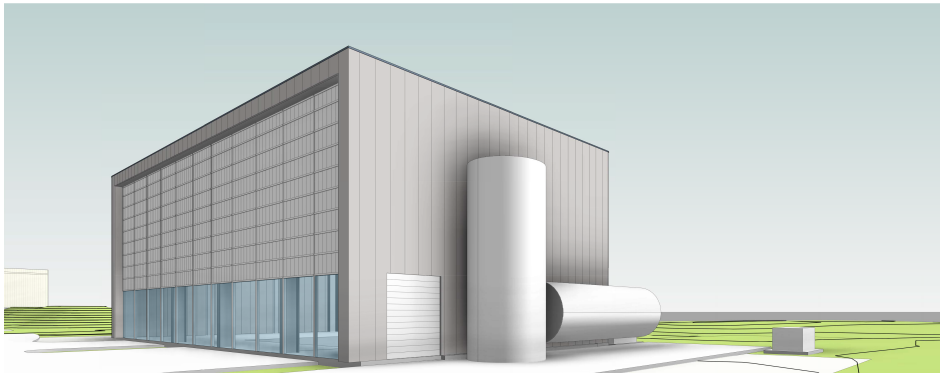


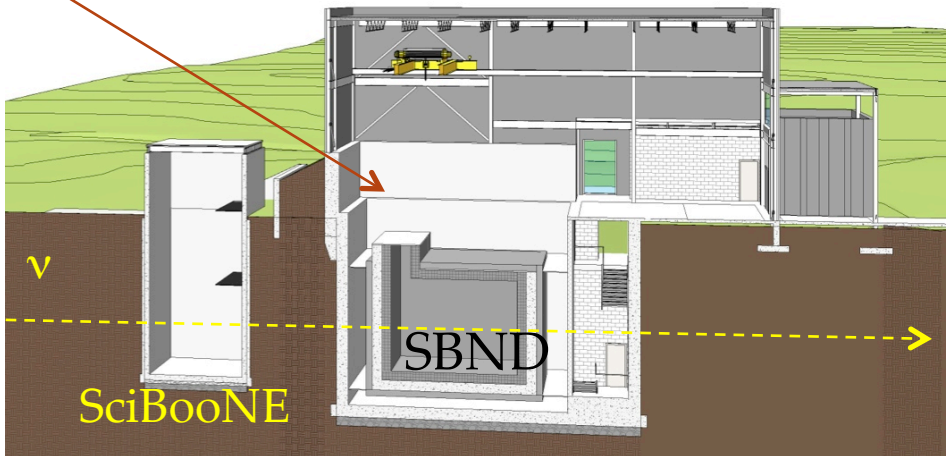


Innovation example: Bias board between adjacent APAs to eliminate dead region

Near Detector Building

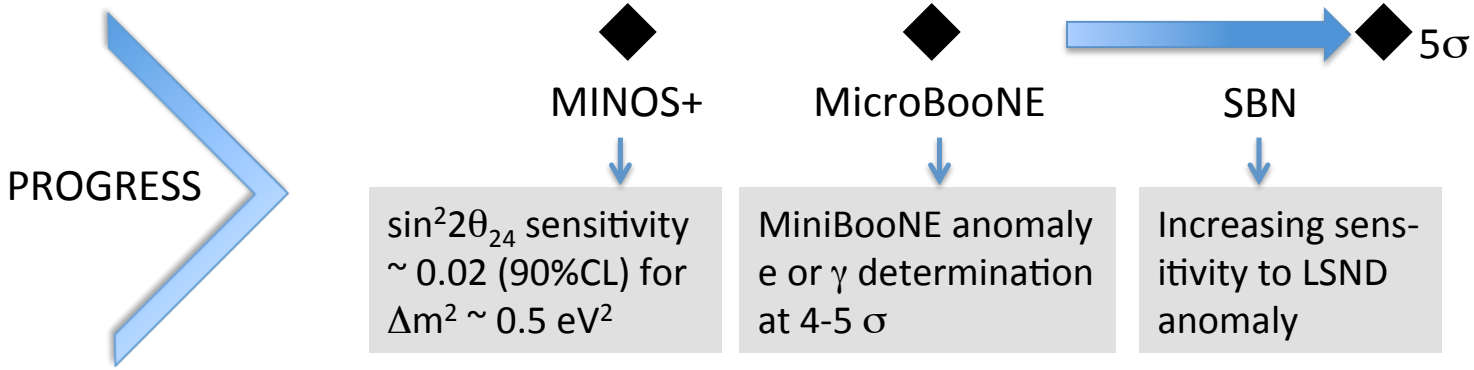
- Design started January 2015
- Designed for 3m concrete overburden inside building to mitigate cosmogenic backgrounds for near surface operation
- Timeline:
  - ✓ March 2015 - 60% Design complete
  - ✓ June 2015 - Design complete
  - – Aug-Sept 2015 - Construction start
  - – Nov 2016 - Beneficial occupancy





SBN Program Timeline

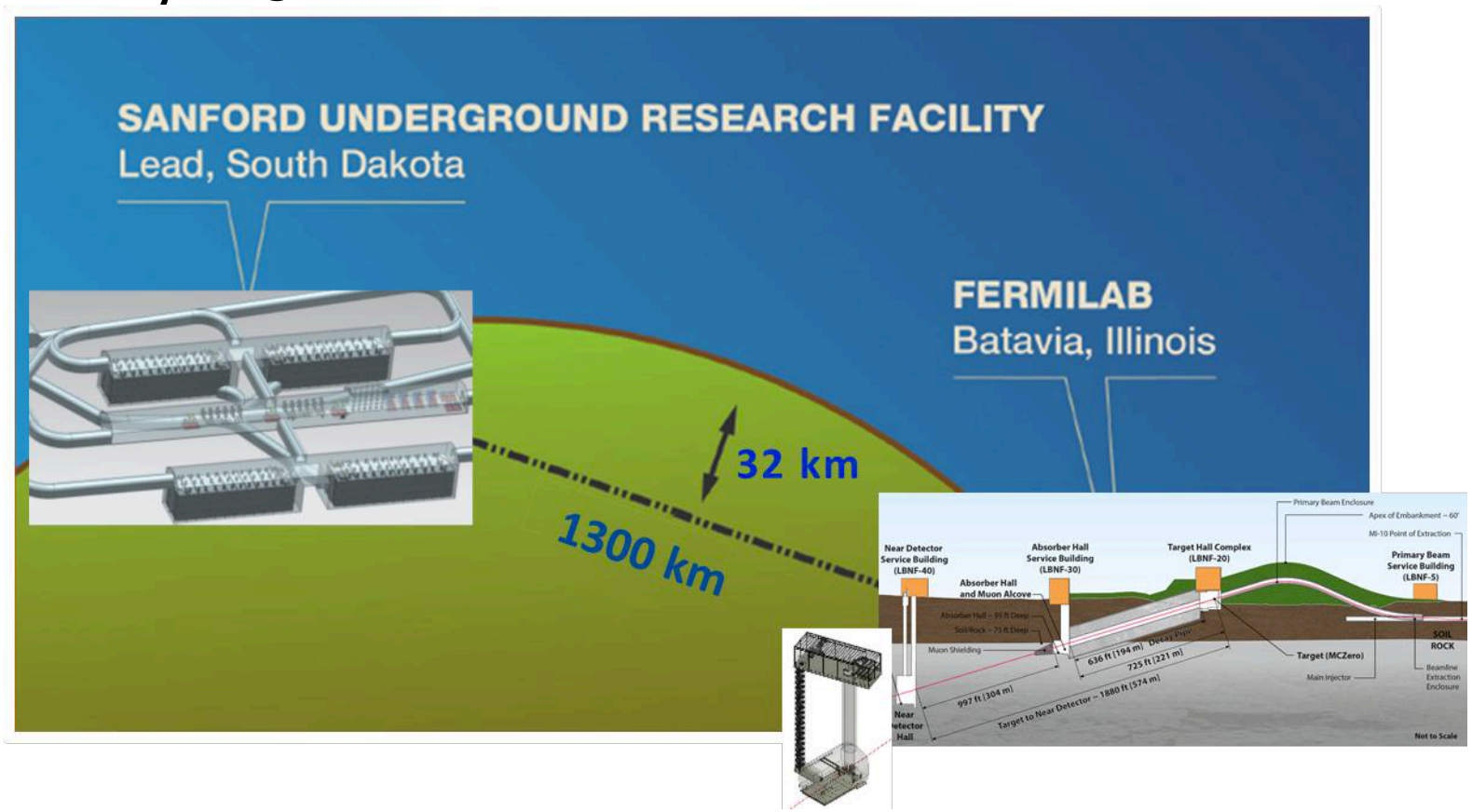
EPOC	EXPT	2015	2016	2017	2018	2019	2020	
NOW	MINOS+	RUN						
NOW	MicroBooNE		RUN 1		RUN - SBN			
NEXT	SBND		BUILD + INSTALL *		RUN - SBN			
NEXT	ICARUS		REFURBISH+INSTALL*		RUN - SBN			
NEXT+	?						decide	????



* Important contributions from CERN Neutrino Platform and European funding agencies (INFN, STFC, SNSF)

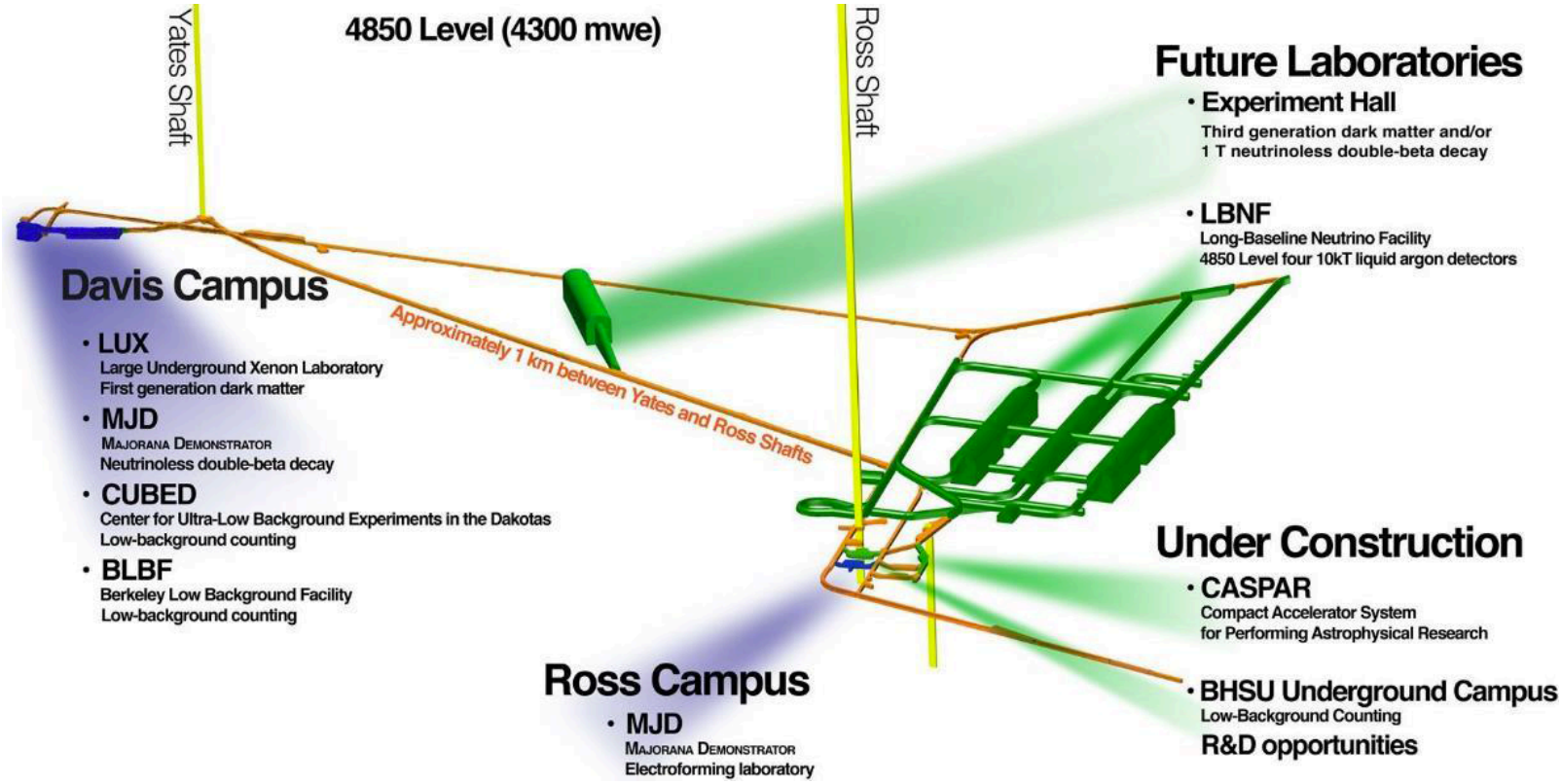
Source of information: January 2015 Fermilab PAC meeting; presentations & Report:

LBNF/DUNE



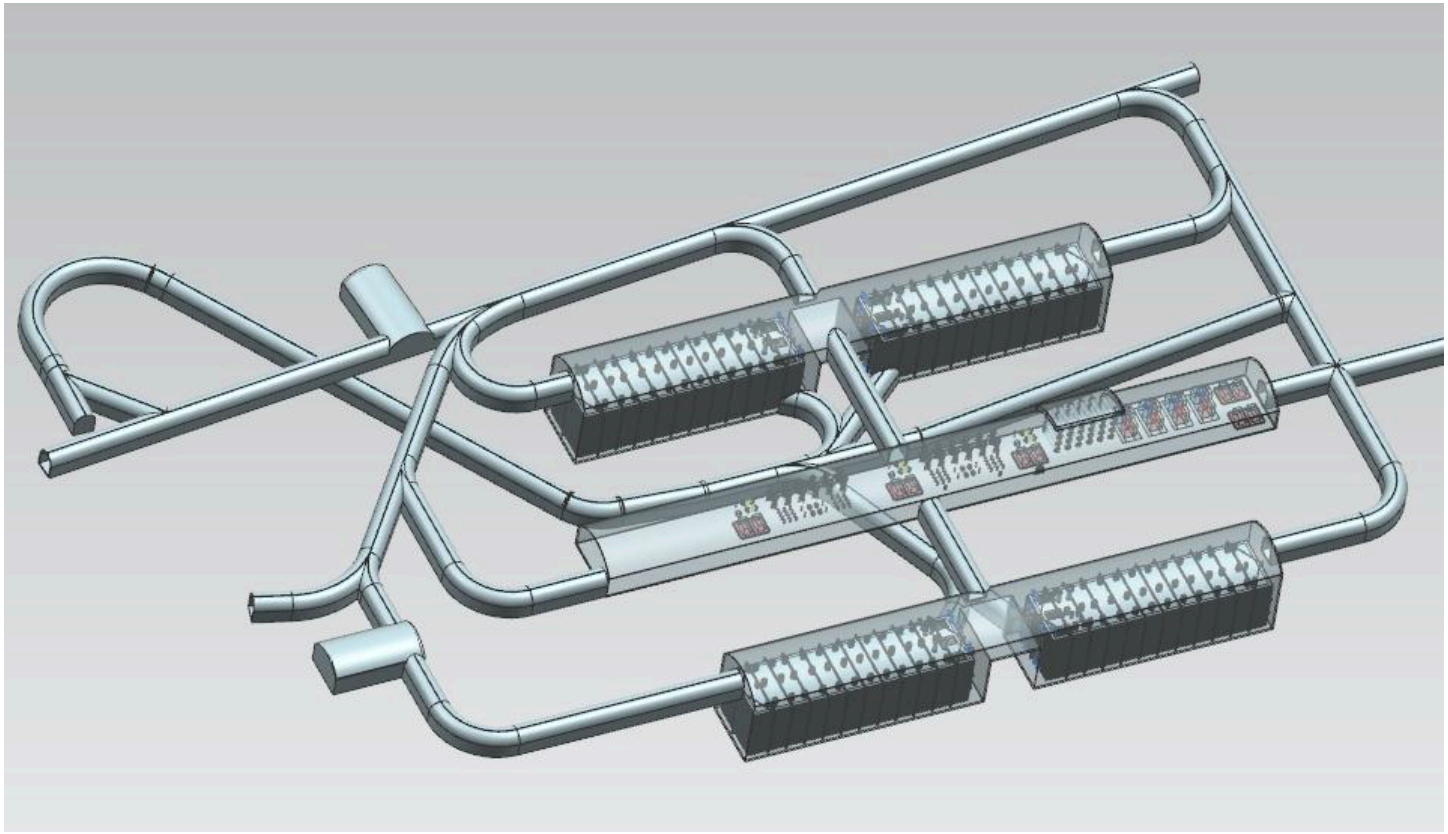
- Neutrino beam from FNAL to Homestake
  - 1,300 km long baseline
  - 1.2 MW (→ 2.3 MW)

LBNF



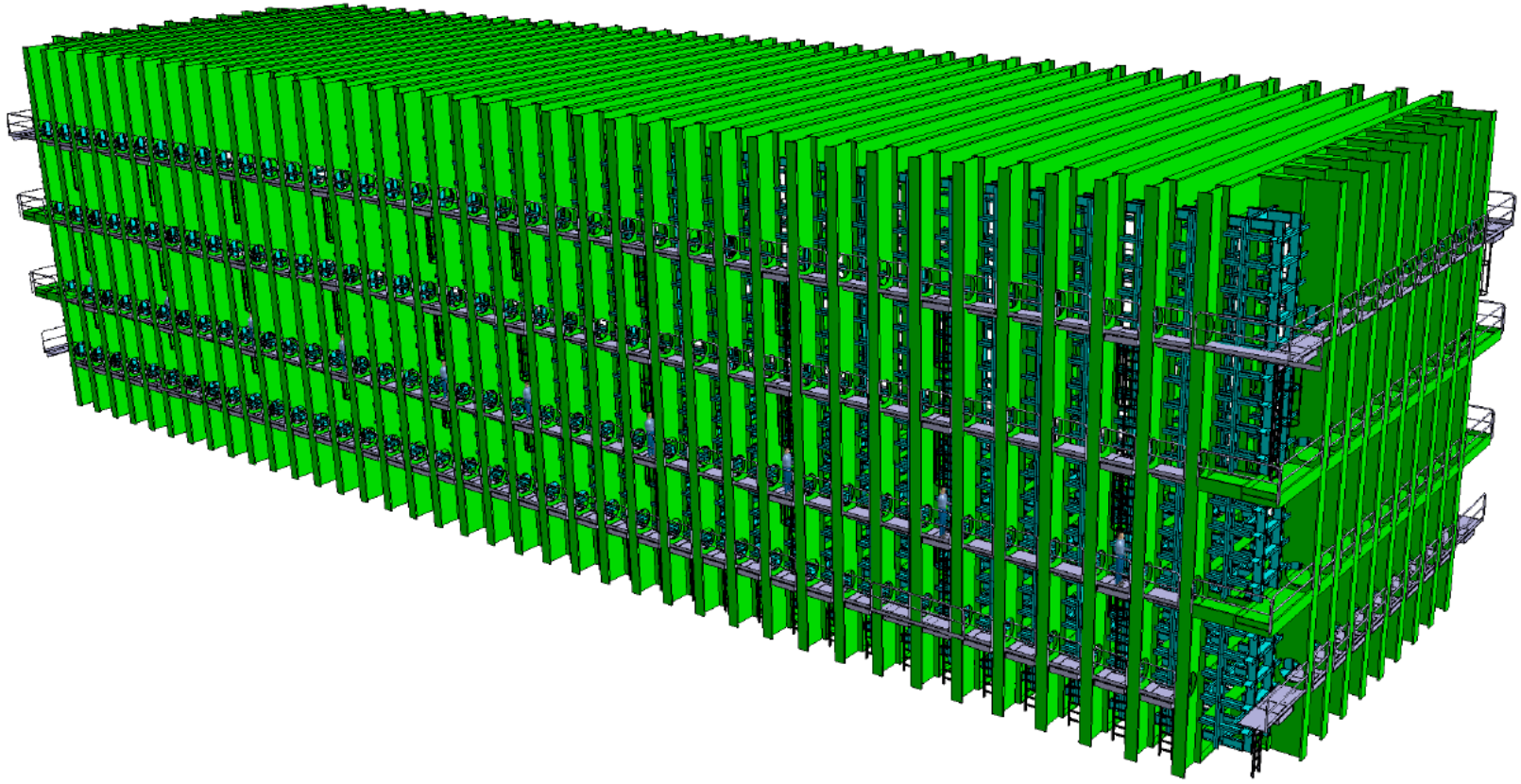
- Long Baseline Neutrino Facility
  - Conventional facilities at both the near and far sites
  - Cryogenics infrastructure to support the DUNE LAr-TPC detectors at SURF
  - An intense neutrino beam aimed at the far site

LBNF – Far Detector Cavern Configuration



- Two parallel caverns each have two 10 kt detector pits with a laydown space in between
- The CF utilities and cryogenics are in a separate parallel cavern, to alleviate conflicts with cryostat & detector install

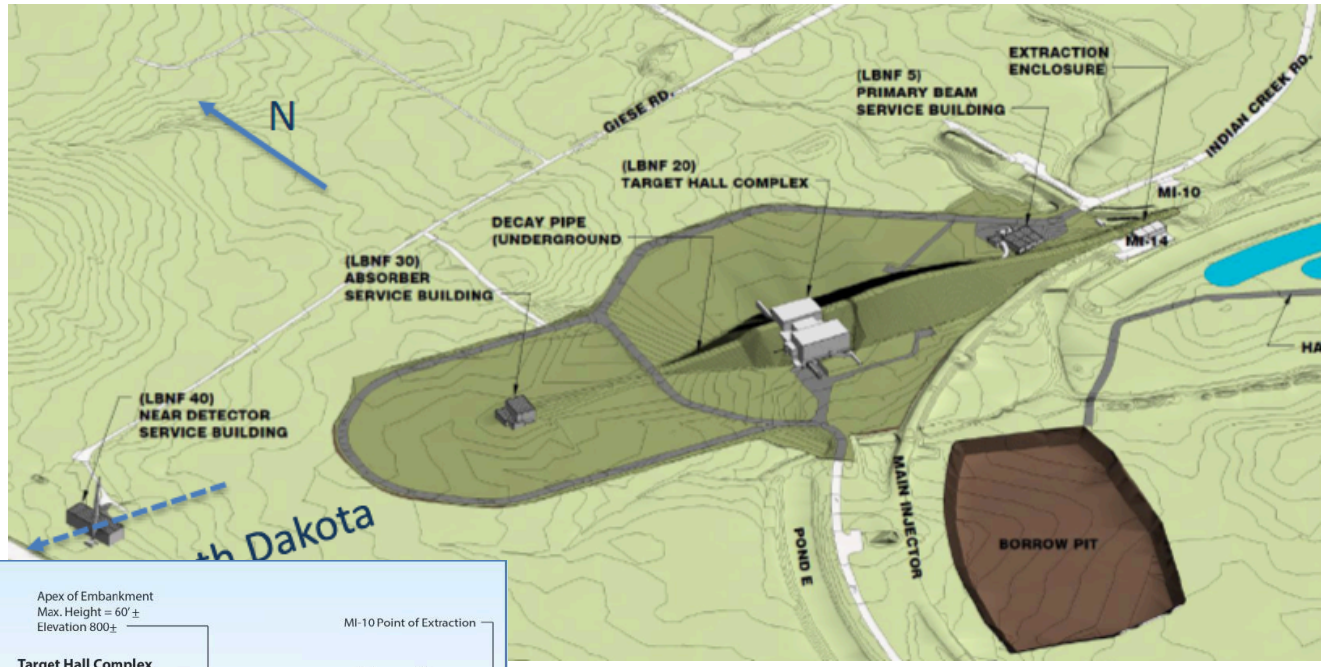
LBNF – Free-standing cryostat steel frame support

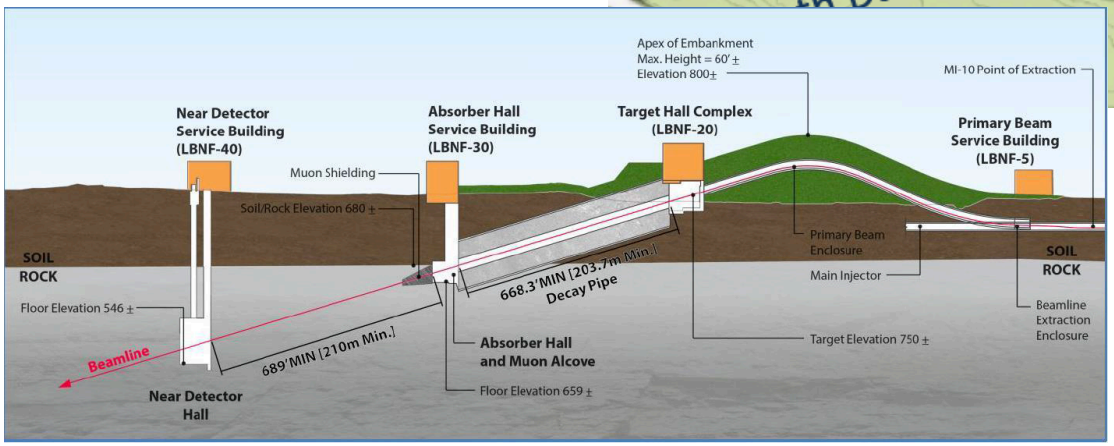


- Design accommodates both single-and dual-phase detectors
- Similar designs are being used by the Short-Baseline Neutrino program and for LAr-TPC prototypes at CERN

Neutrino Beam at Fermilab & the Near Detector Facility

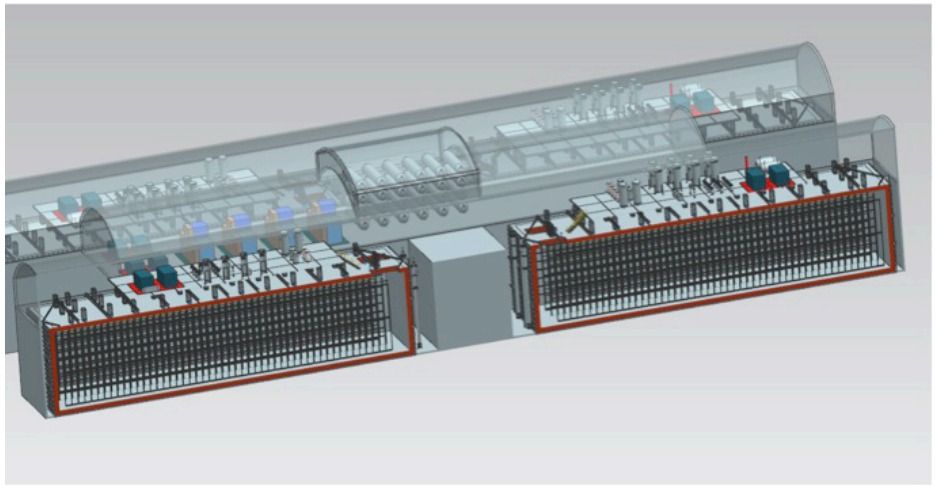
- Embankment allows placement of the target close to grade to reduce risk of tritium production in the aquifer





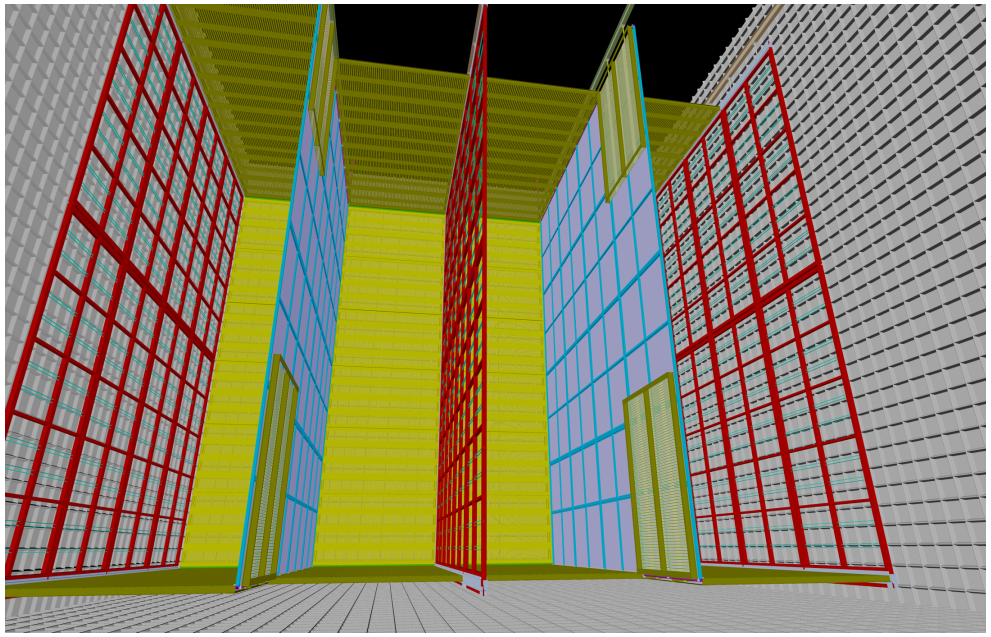
DUNE Detector

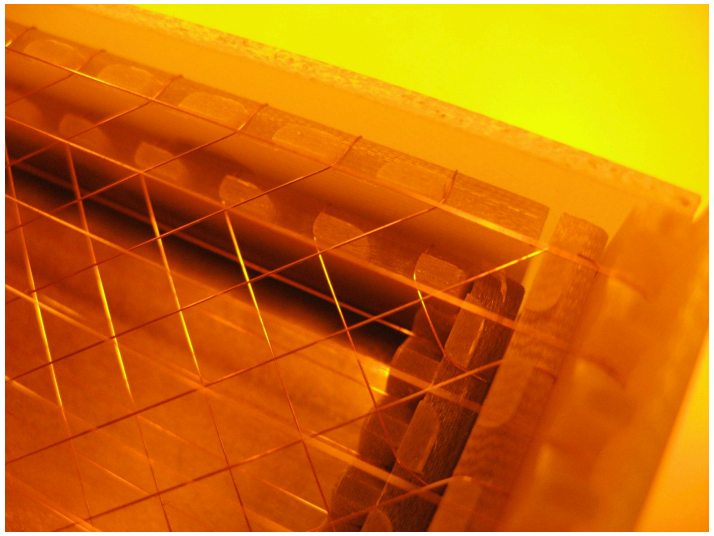
- Far Detector
  - Pattern recognition
  - Energy measurement
  - Energy range: few MeV – few GeV
  - LAr-TPC
    - Exquisite imaging capability in 3D
      - ~ few mm scale
    - Excellent energy measurement capability
      - Total active calorimeter



DUNE Far Detector

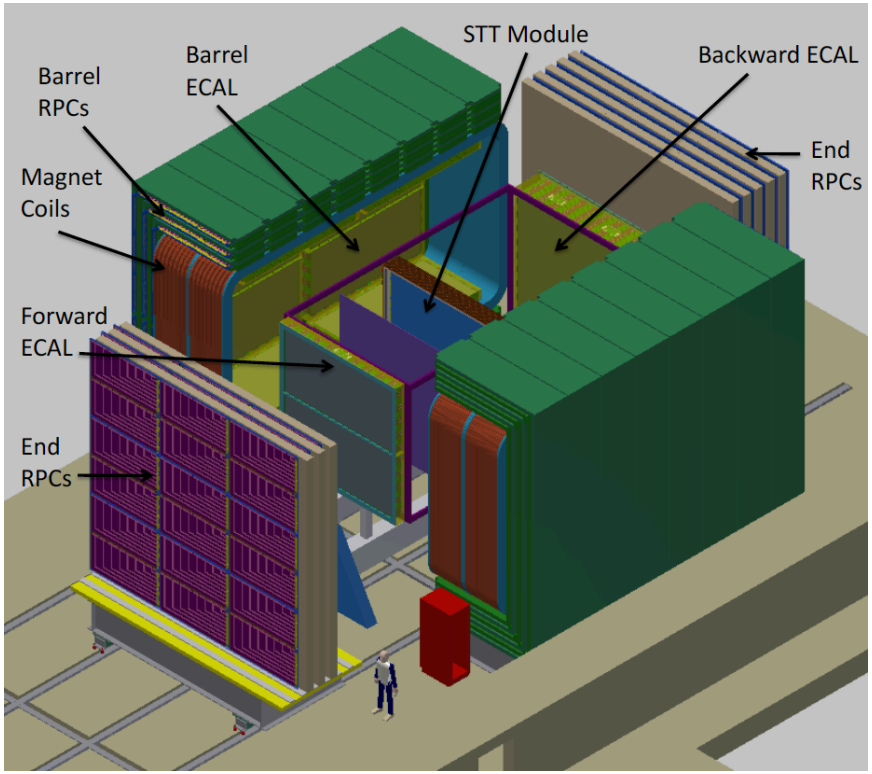
- 4 x 10 kt FD module
  - Active volume: 12m x 14m x 58m
  - 150 Anode Plane Assemblies
    - 6.3m high x 2.3m wide
  - 200 Cathode Plane Assemblies
    - 3m high x 2.3m wide
  - A:C:A:C:A arrangement
  - Cathodes at -180kV for 3.5m drift
  - APAs have wrapped wires – read out both sides
  - Each side has one collection wire plane & two induction planes





DUNE Detector

- Near Detector
  - Constrain systematic uncertainties in LBL oscillation analysis
  - Near detector must be able to constrain ν cross sections & ν flux
- The NOMAD-inspired Fine-Grained Tracker (FGT)
  - Central straw-tube tracking system
  - Lead-scintillator sampling ECAL
  - Large-bore warm dipole magnet
  - RPC-based muon tracking systems
- Constraints on cross sections and the neutrino flux
- A rich self-contained non-oscillation neutrino physics program

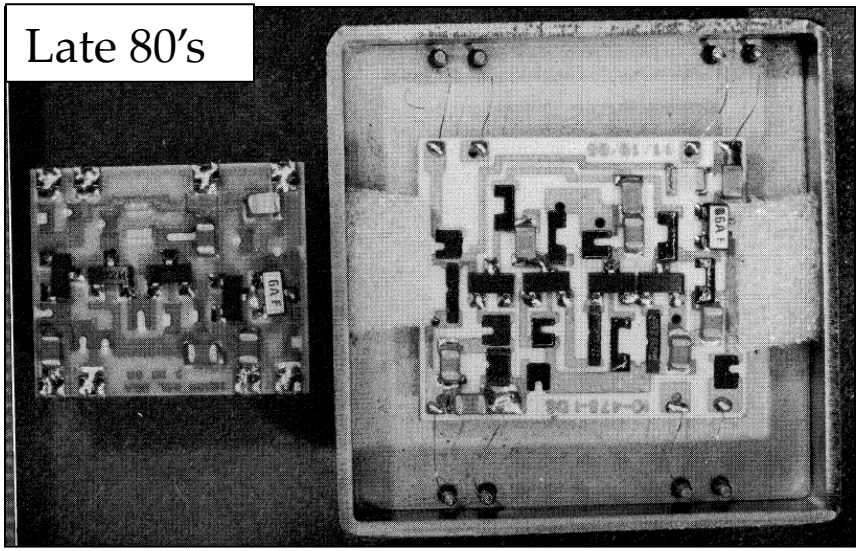


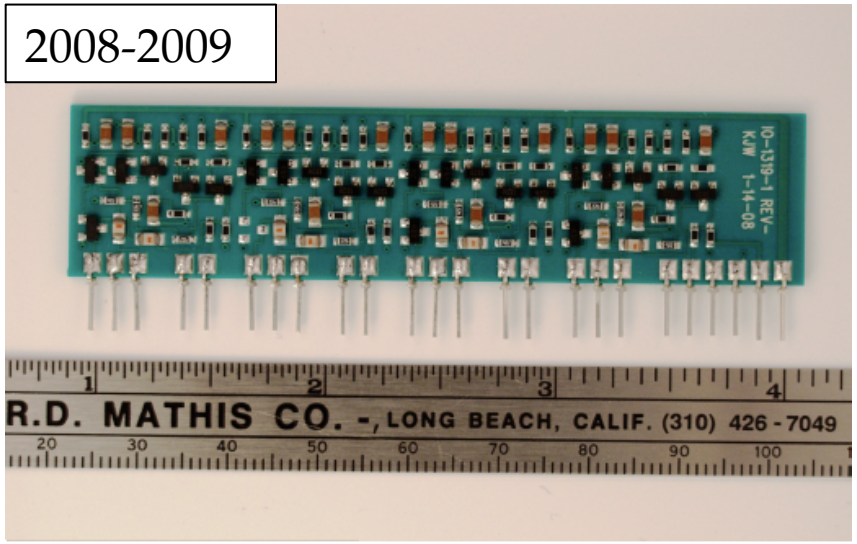
Cold Electronics Development

- A Brief History of Cold Electronics
- Advantages of Cold Electronics
- R&D on CMOS Cold Electronics
- Electronics Lifetime at 300K and 77K

Cold Electronics Development

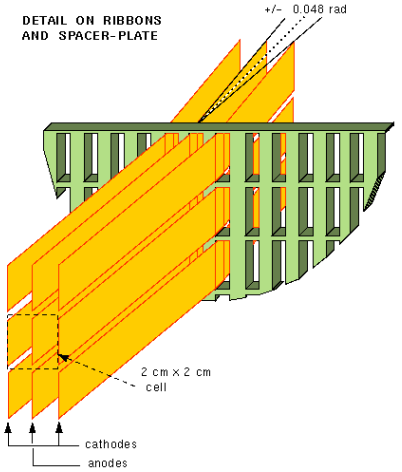
- Cryogenics Front-end based on JFET
- Technology mature and available as of today
  - Reliability issues require a careful choice of component and high reliability assembly
  - Ceramic hybrid with co-fired traces and surface mount components properly tested
- Helios-NA34
  - Liquid Argon calorimeter
  - 576 preamplifiers
  - Operation: 4 years, multiple cool-downs
  - Failure: 1 caused by mechanical contact
- Several years of experience
  - MicroBooNE front-end design started from JFET as well

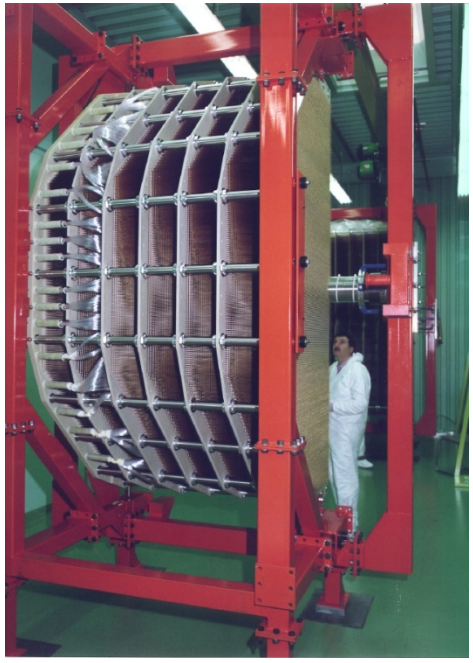




Cryogenics Front-end based on JFET

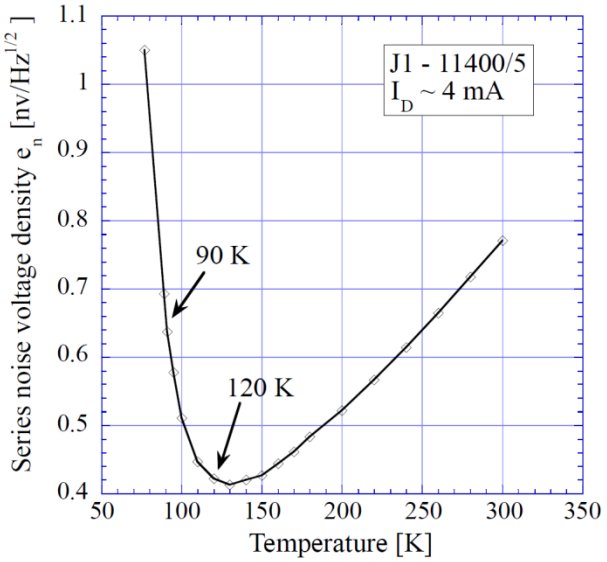
- NA48/NA62
  - Liquid Krypton calorimeter
  - Preamplifiers in LKr: **13,212** channels; surface mounted components
  - Operated at very high voltage
    - Tested up to 7kV, operated in 3kV
  - Failures
    - ~50 because of a HV accident in 1998
    - ~25 cold electronics failures after 1998
    - failure rate is < 0.2% in 17 years
    - The last failure recorded was more than 7 years ago
  - Always kept at cryogenic temperature since 1998
  - Operation
    - **17 years** so far
    - Plan to run until 2018, expected to be in operation for **20 years**

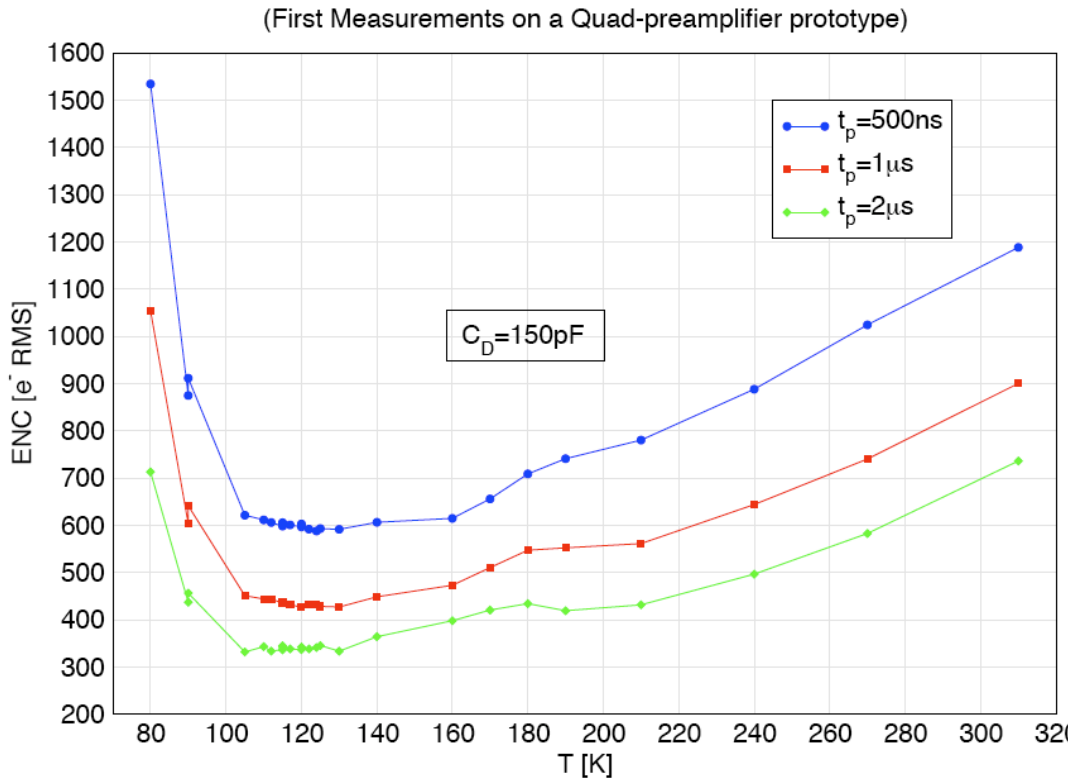




Performance of Cold Electronics (JFET)

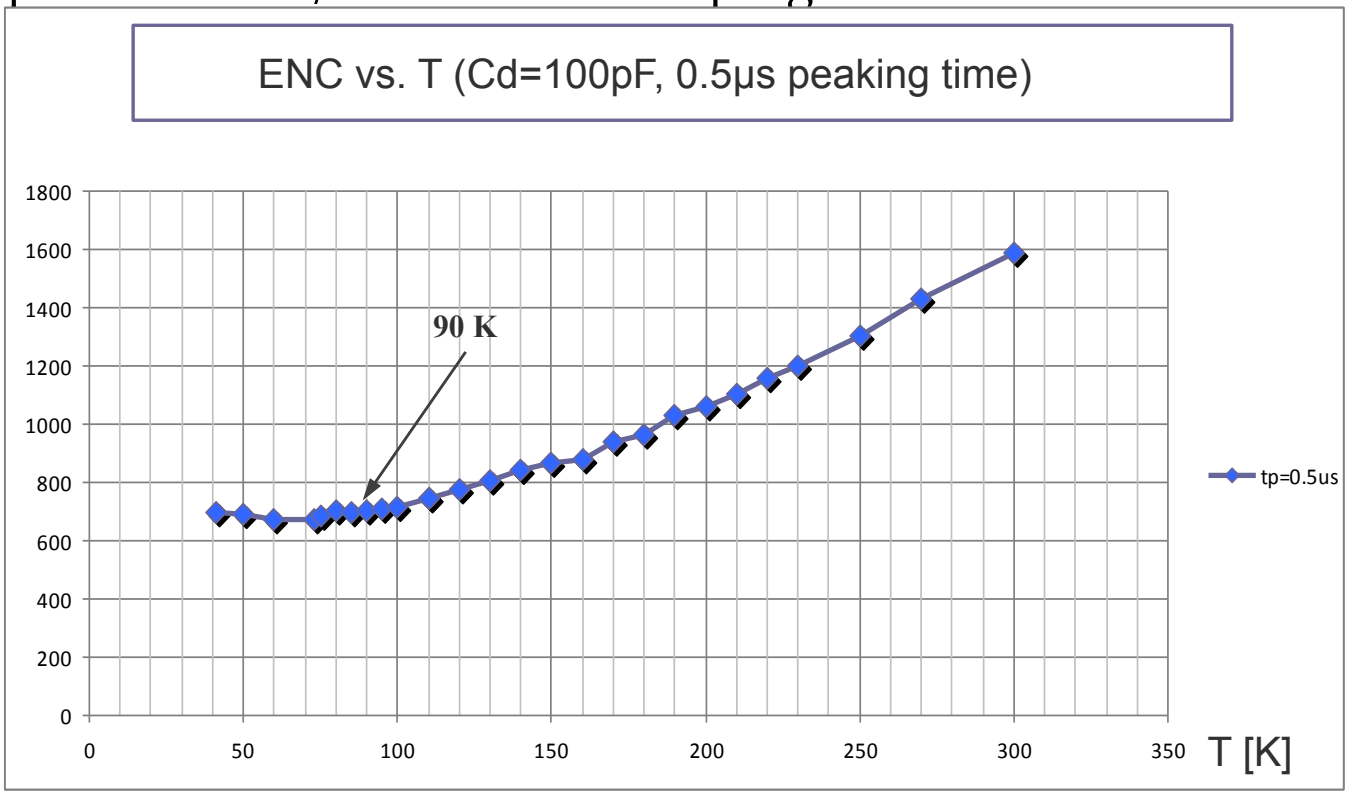
- JFET based preamplifier designed for MicroBooNE
- Bulk mobility and transconductance increase as temperature decreases, carrier freeze out causes ENC increasing when temperature lower than ~100K





Performance of Cold Electronics (CMOS)

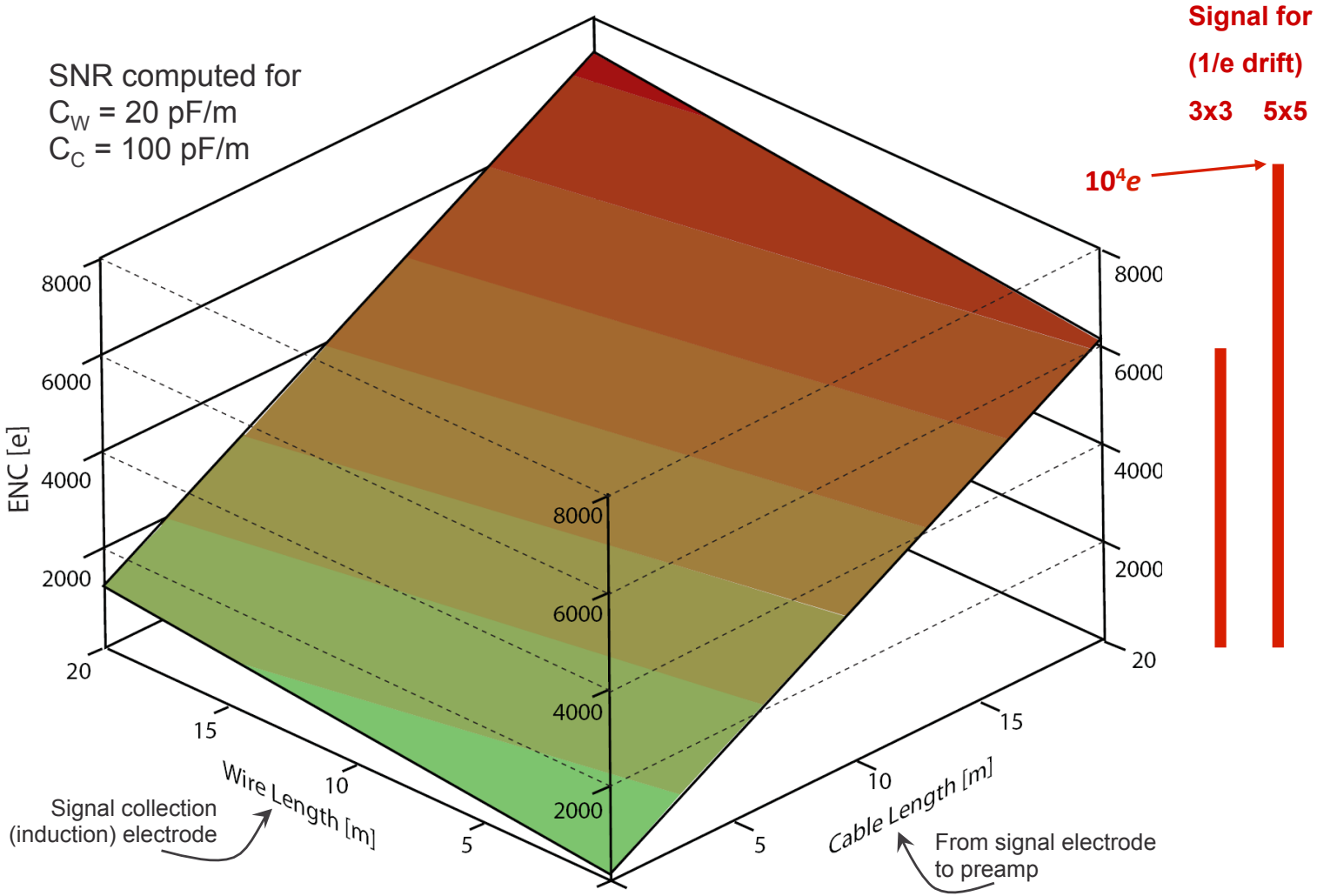
- Test result of existing ASIC in 0.25 *μm (not designed for LAr)*
- CMOS in LAr has less than half the noise as that at room temperature, higher mobility and higher transconductance/current ratio
- MicroBooNE has adopted the cryogenic CMOS analog front end ASIC developed for LBNF/DUNE LAr TPC program



Motivation of Cold Electronics

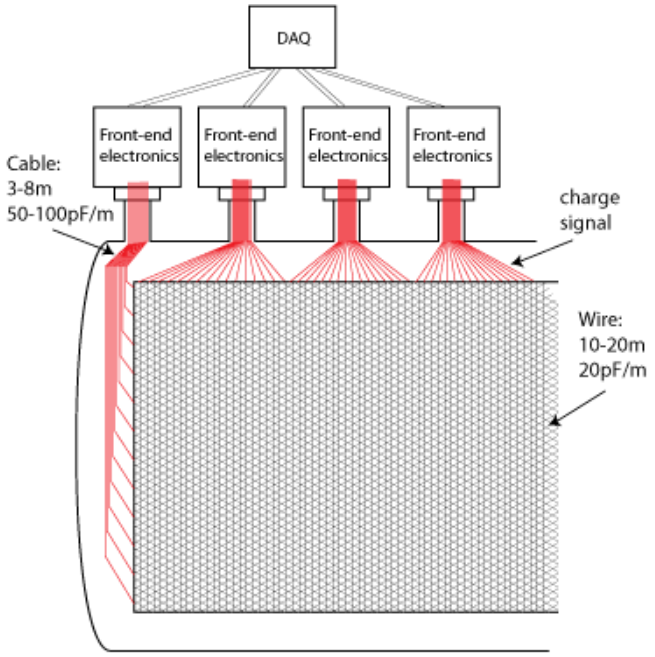
- Readout electronics developed at BNL for low temperatures (77K-300K) is an enabling technology for noble liquid and mixed phase detectors for neutrino and dark matter research
  - Cold electronics decouples the electrode and cryostat design from the readout design. With electronics integral with detector electrodes the noise is independent of the fiducial volume (signal cable lengths), and much lower than with warm electronics
    - The amplifier serial input noise, $e^2 \propto C_d^2/g_m$, linearly increases with detector and cable capacitance, C_d, and decreases with input stage transconductance, g_m
  - Signal multiplexing results in large reduction in the quantity of cables (less outgassing) and the number of feedthroughs/cryostat penetrations
- R&D of CMOS cold electronics started in 2008
  - We had started thinking about LAr TPCs, before the final decision for LAr TPC (and not for Water Cherenkov) for LBNF/DUNE had been made
  - MicroBooNE started with plans for JFET's and, the FE ASIC caught up with MicroBooNE delays

Advantages of Cold Electronics



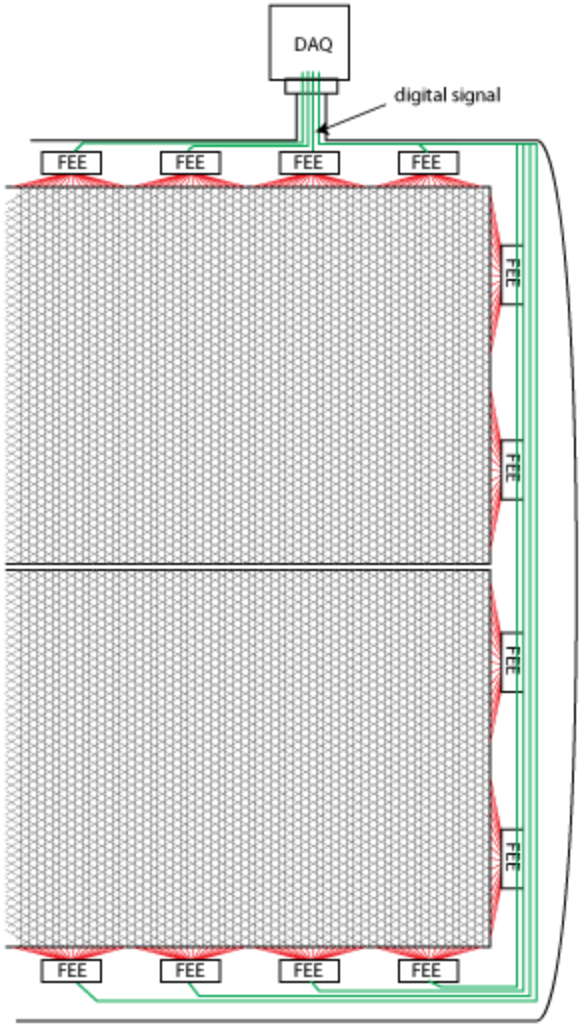
Advantages of Cold Electronics

- A typical readout configuration with warm electronics: long cables connect the sense wires to the FEE, resulting in large electronics noise. To reduce the cable length, one has to implement cold feedthroughs below the liquid level, which increases the cryostat complexity.

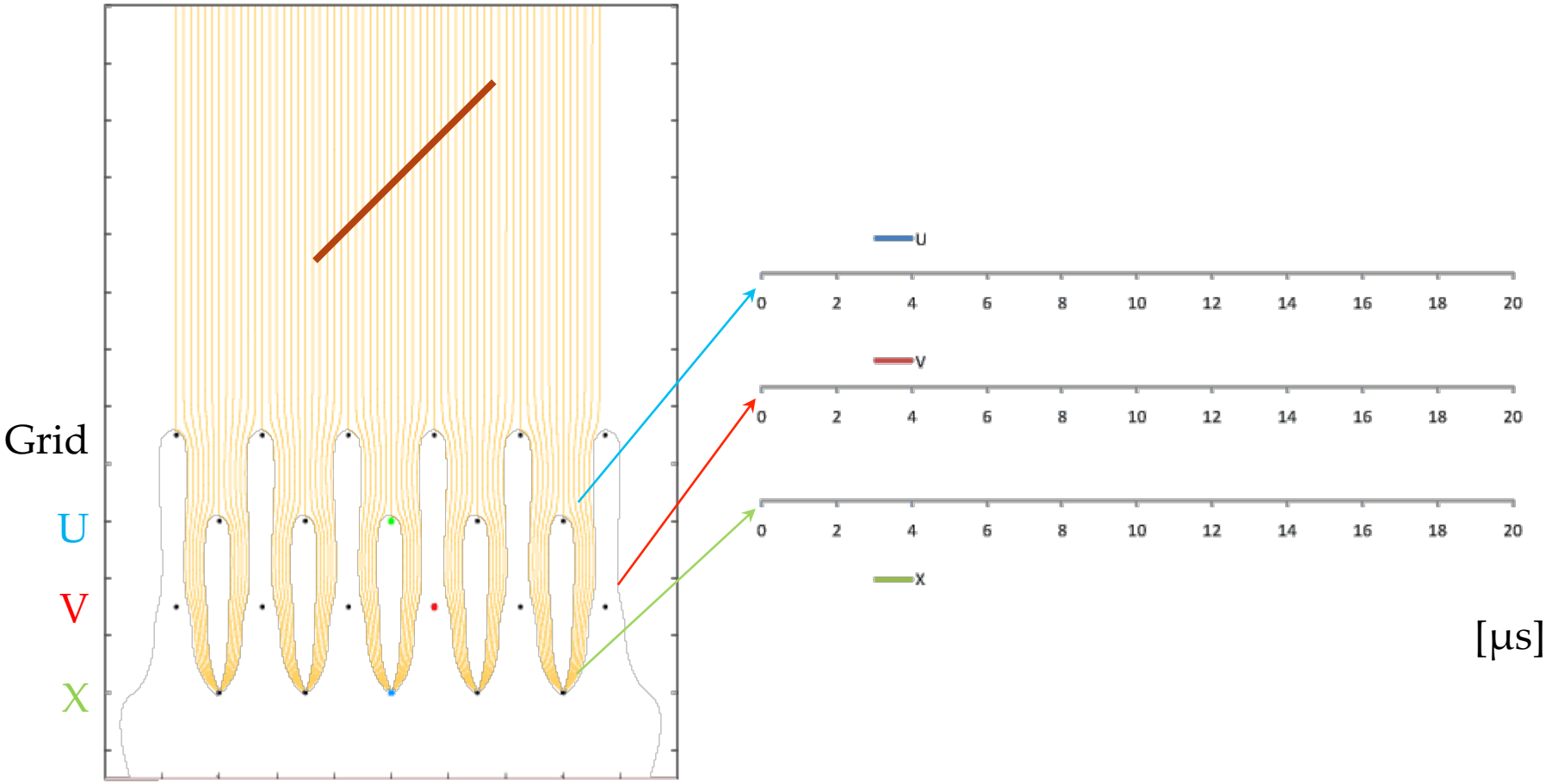


Advantages of Cold Electronics

- Having front-end electronics in the cryostat, close to the wire electrodes yields the best SNR
- Highly multiplexed circuits with fewer digital output lines not only greatly reduce the number of cryostat penetrations, but also give the designers of both the TPC and the cryostat the freedom to choose the optimum configurations



Signal Formation: Induced Signals from a Track Segment



DUNE style wire arrangement: 3 instrumented wire planes + 1 grid plane
Raw current waveforms convolved with a 0.5μs gaussian (~1/2 drift length) to mimic diffusion

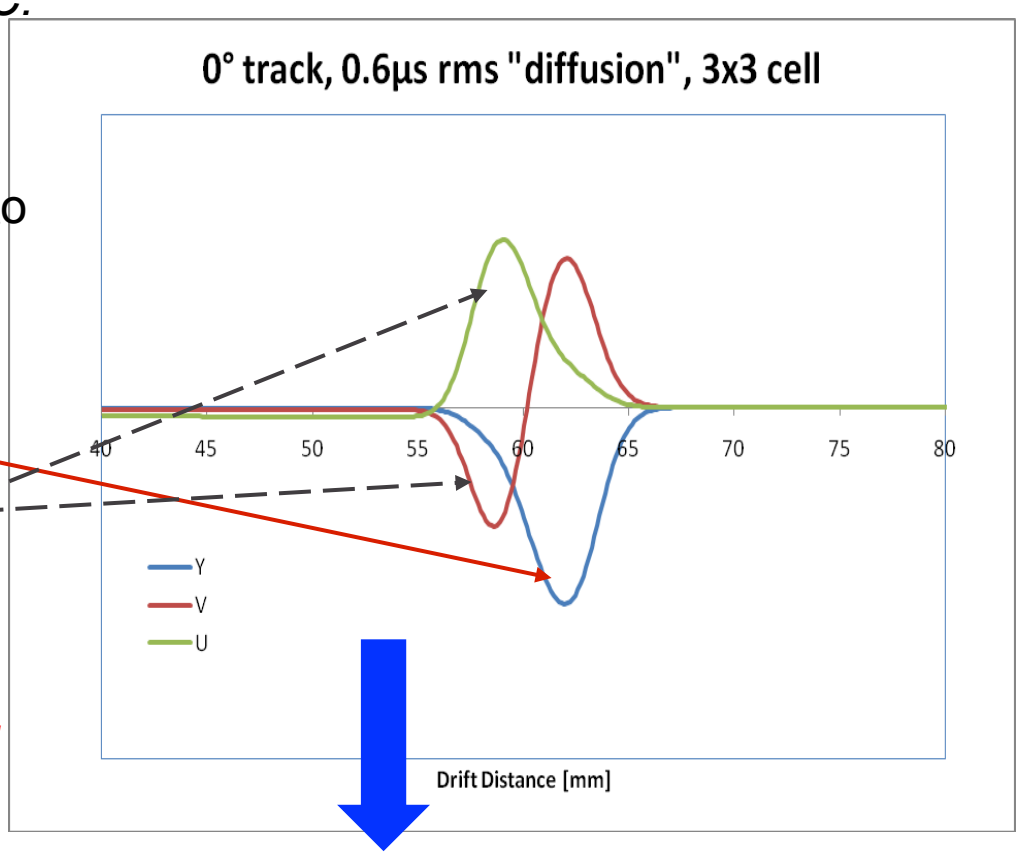
Signals in LArTPC

Charge signal:

- A 3mm MIP track should create *210keV/mm x 3mm /23.6eV/e = 4.3fC.*
- After a 1/3 initial recombination loss: *~2.8fC*
- Assume the drift path to equal the charge life time, reducing the signal to 1/e≈0.368.
- The expected signal for *3mm* wire spacing is then ≈*1fC=6250 e*, … and for *5mm, ≈10^4 e*, for ***the "collection signal"***.
- The induction signals are smaller

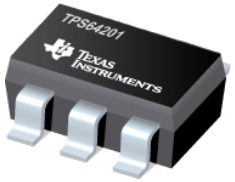
- The ***time scale*** of TPC signals is determined by the ***wire plane spacing*** and ***electron drift velocity***, *(~1.5 mm/μs at 500 V/cm)*.

Induced Current Waveforms on 3 Sense Wire Planes:



Sampling rate ***≤ 2 Ms/s***

Cold Electronics

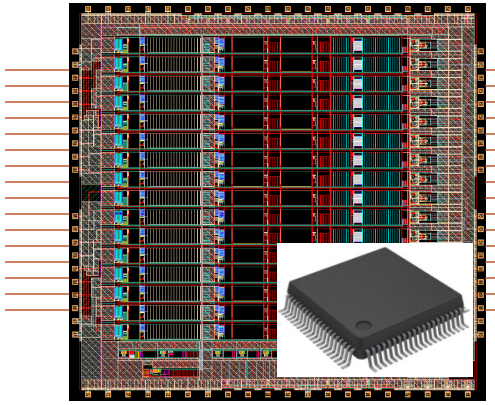


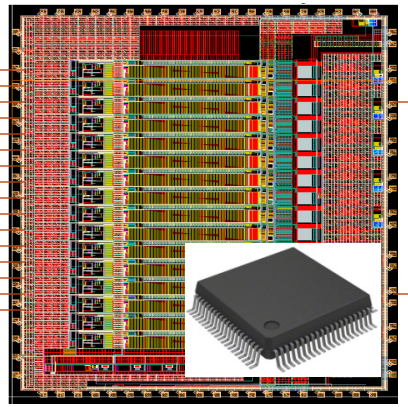
voltage regulation
(COTS)
(< 100mV dropout)

front-end ASIC
~ 5mW/ch.

ADC ASIC
~ 5mW/ch.

FPGA (COTS)
~ 8mW/ch.



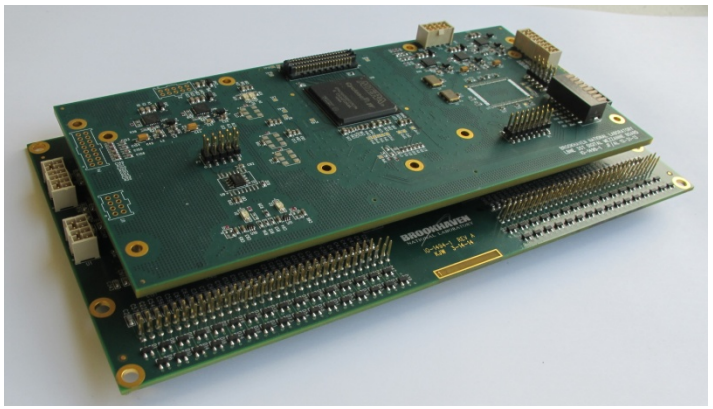


overall 128:2
multiplexing

8 x

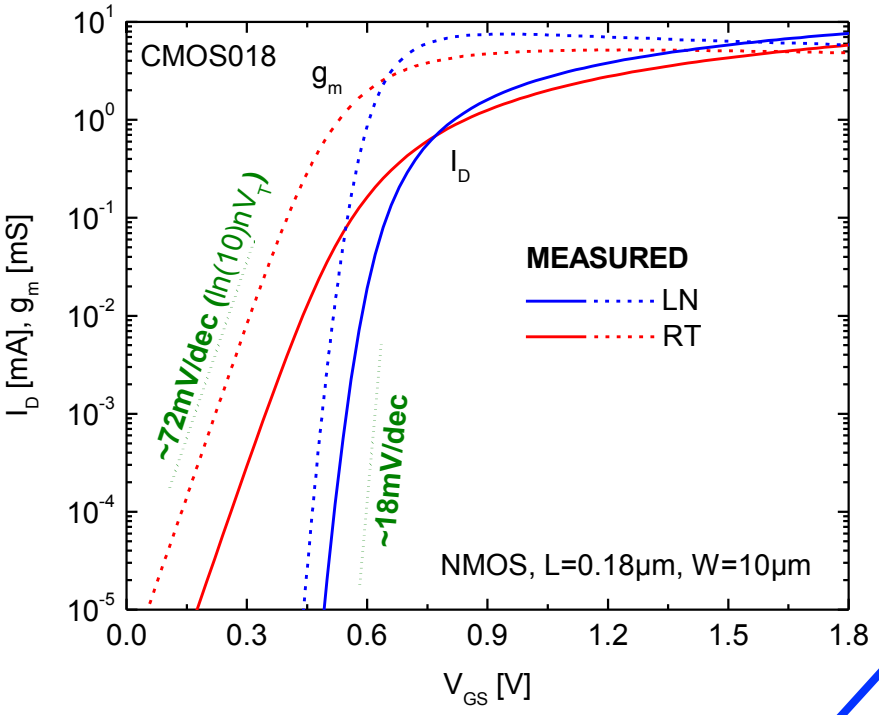
1 x

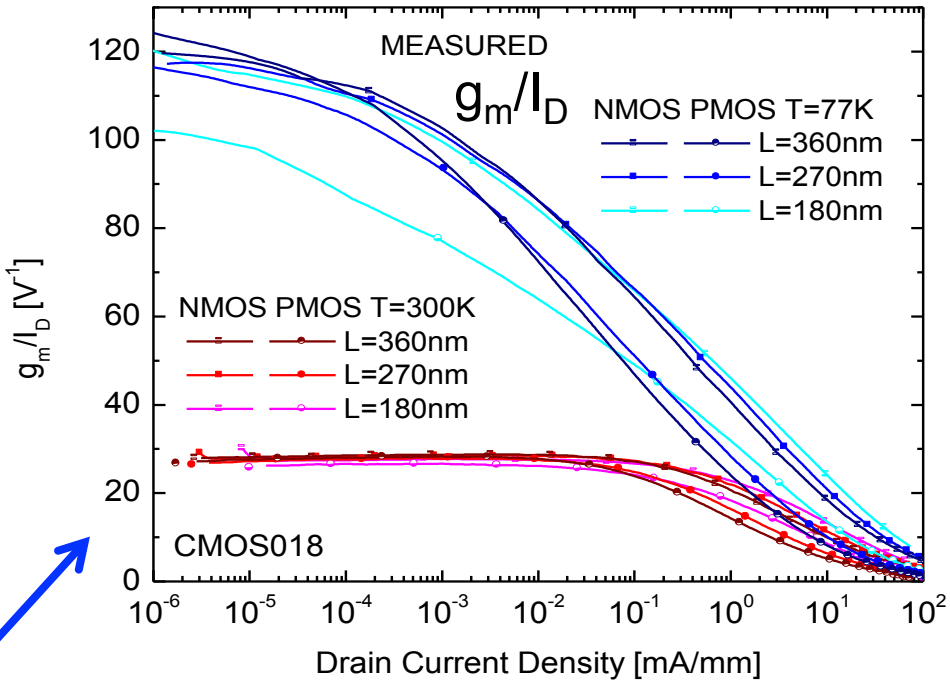
A Complete Front End Readout Chain



front-end cold
module
serving 128 wires
~ 2.4 W

CMOS Characteristics in LAr



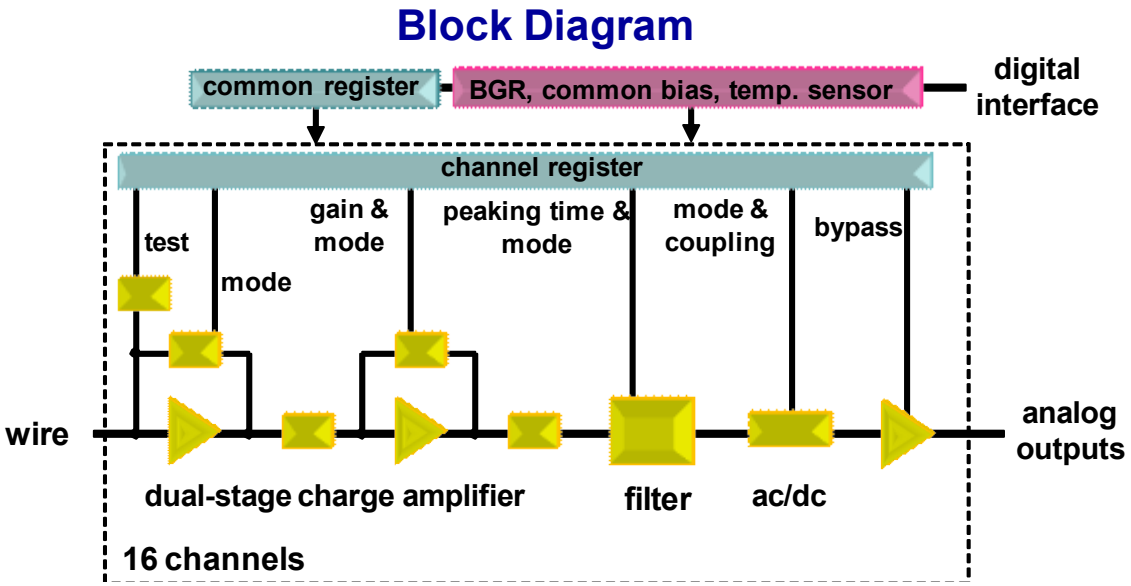


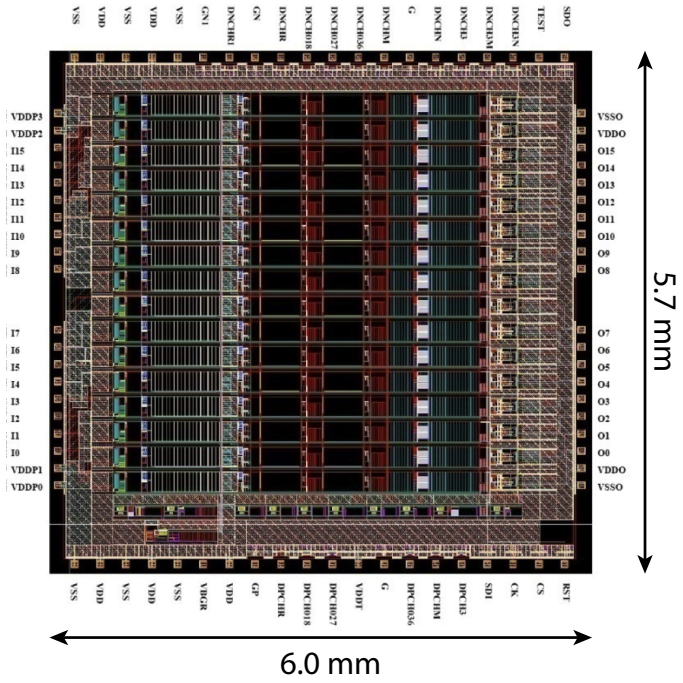
Transconductance/ drain current

$$\frac{g_m}{I_D} \rightarrow \frac{q}{nk_BT} = \begin{cases} \sim 30 \ \ at \ \ T = 300K \\ \sim 116 \ \ at \ \ T = 77K \end{cases}$$

At 77-89K, charge carrier ***mobility*** in silicon *increases* and ***thermal fluctuations*** *decrease* with ***kT/e***, resulting in a ***higher gain***, ***higher*** g_m/I_D, ***higher speed*** and ***lower noise***.

Front-End ASIC

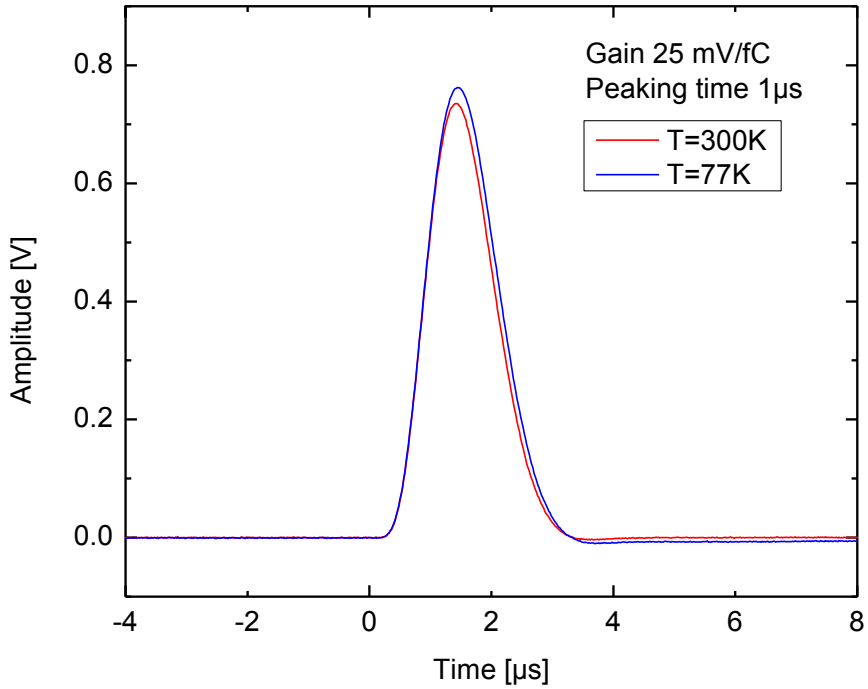




- 16 channels, programmable
- charge amplifier, high-order filter
- adjustable gain: 4.7, 7.8, 14, 25 mV/fC
  (charge 55, 100, 180, 300 fC)
- adjustable filter time constant
  (peaking time 0.5, 1, 2, 3 μs)
- selectable collection/non-collection mode
  (baseline 200, 900 mV)
- selectable dc/ac coupling (100μs)

- rail-to-rail analog signal processing
- band-gap referenced biasing
- temperature sensor (~ 3mV/°C)
- 136 registers with digital interface
- ~ 5.5 mW/channel (input MOSFET 3.9 mW)
- single MOSFET test structures
- ~ 15,000 MOSFETs
- designed for 77K-300K operation
- designed for long lifetime
- tech. CMOS 180 nm, 1.8 V, 6M, MIM, SBRES

FE ASIC - Programmability



Bandgap Reference

$$V_{BGR} \approx \begin{cases} 1.185\ V \ \text{ at } \ 300\ ^{\circ}K \\ 1.164\ V \ \text{ at } \ 77\ ^{\circ}K \end{cases}$$

variation ≈ 1.8 %

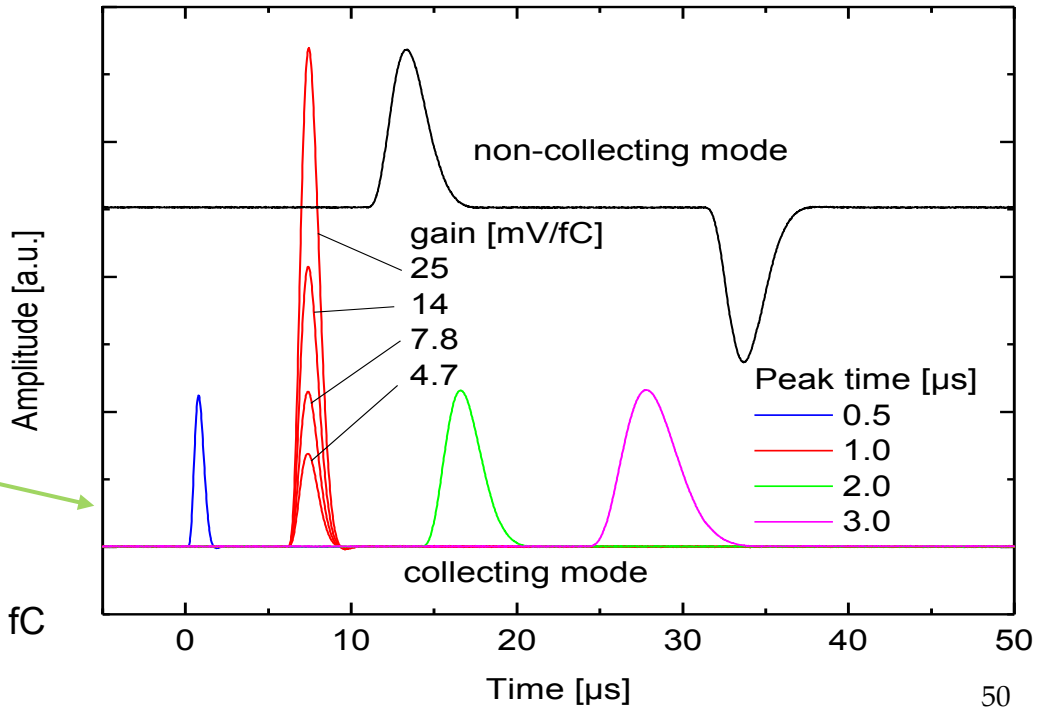
Temperature Sensor

$$V_{TMP} \approx \begin{cases} 867.0\ mV \ \text{ at } \ 300\ ^{\circ}K \\ 259.3\ mV \ \text{ at } \ 77\ ^{\circ}K \end{cases}$$

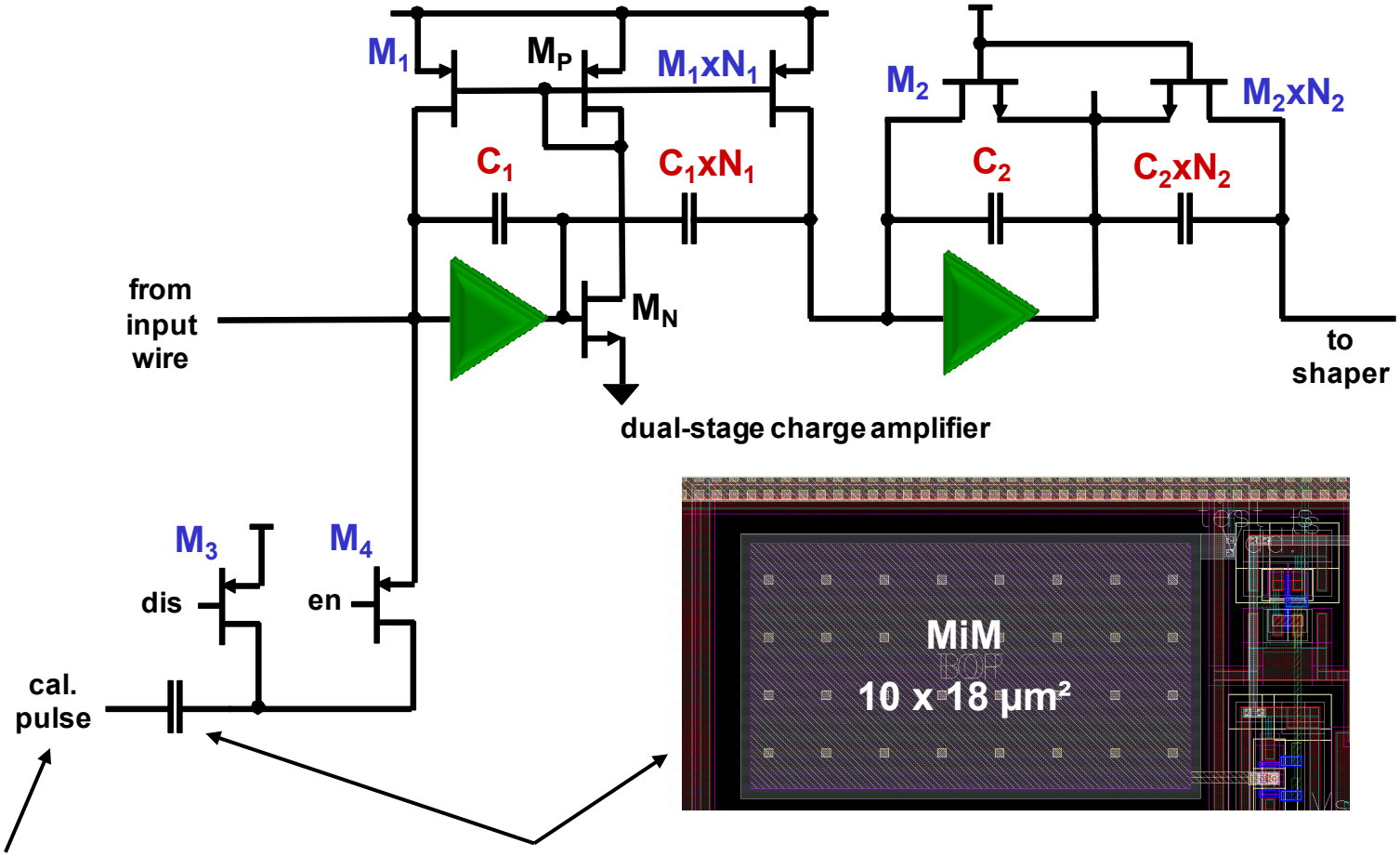
~ 2.86 mV / °K

Adjustable gain, peaking time and baseline

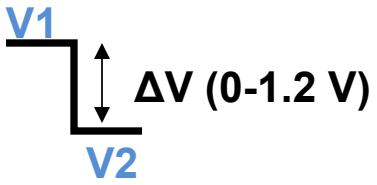
maximum charge 55, 100, 180, 300 fC



FE ASIC - Calibration Circuit



external pulse generator



injection capacitor (per-channel enable)

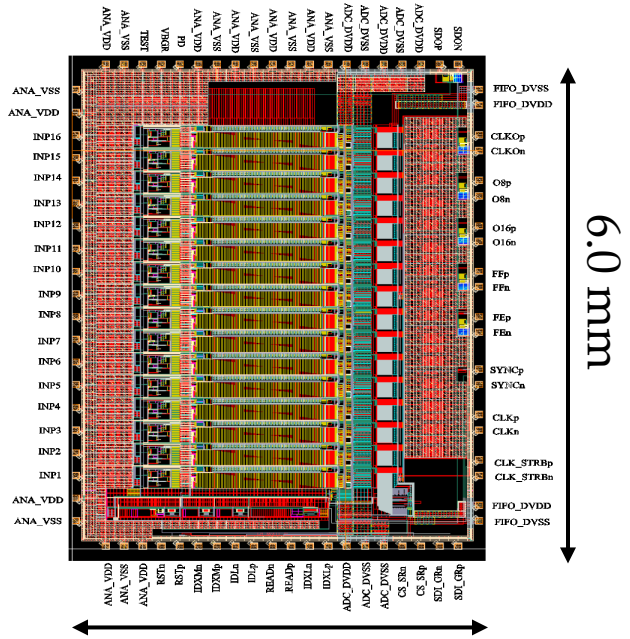
- nominal value: 198 fF
- same-run non-uniformity 0.25 % rms
- run-to-run non-uniformity 2.5 % rms
- measured: 184 fF at 300 K
  183 fF at 77 K (0.5 %)

$$\Delta Q = C_{inj} \cdot \Delta V$$

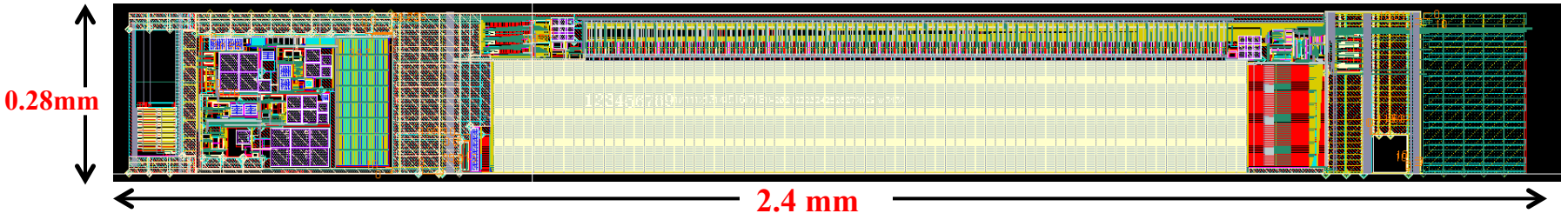
$$\downarrow$$

0-230 fC

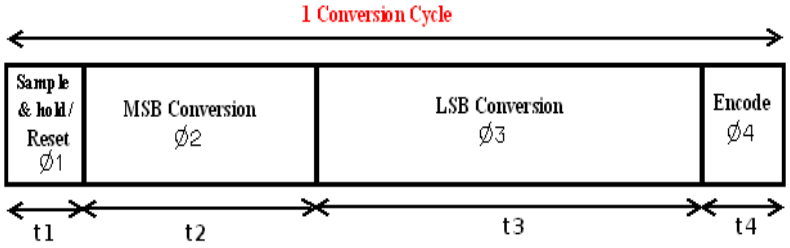
ADC ASIC



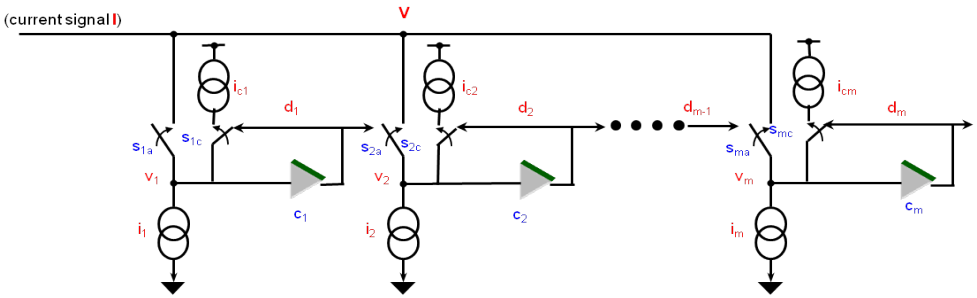
- 16 channels, programmable
- sample/hold
- 12-bit ADC at 2MS/s sampling rate
- current-mode domino architecture
- FIFO 192s bit wide x 32 bits deep
- multiplexer 8:1 or 16:1
- serializer 12:1
- adjustable offsets
- ~4.5 mW/ch.
- power-down modes
- ~ 300,000 MOSFETs
- designed for 77-300Koperation
- designed for long lifetime
- tech. CMOS 180nm, 1.8 V, 6M, MIM, SBRES



ADC Operation & Functions



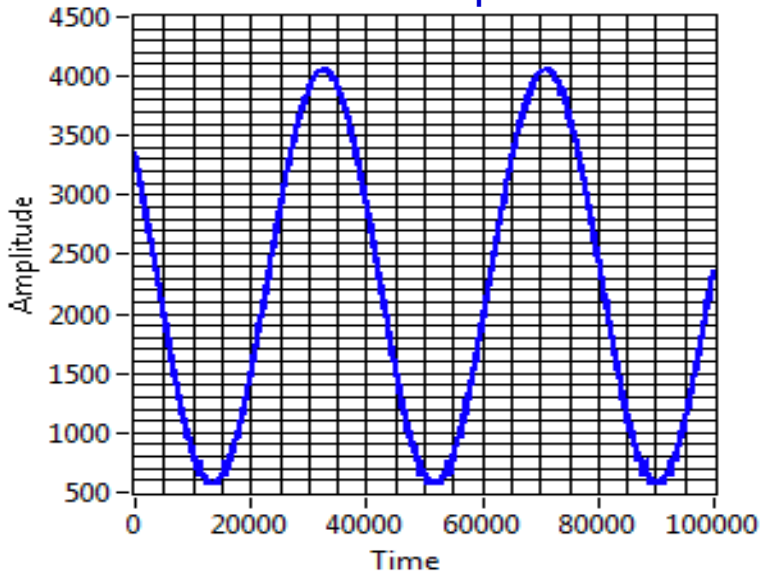
4-phase ADC conversion
- sampling / reset
- MSBs Conversion
- LSBs Conversion
- encoding

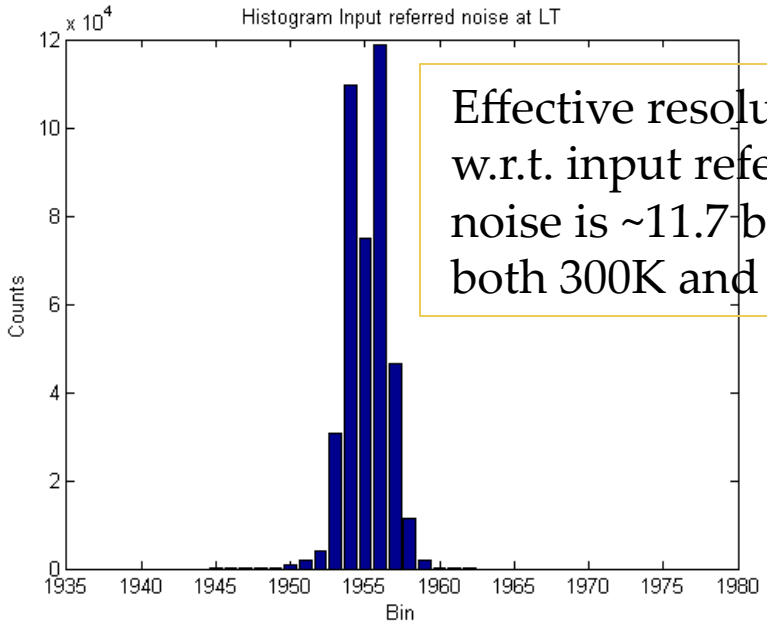


Current-mode domino architecture, 2 steps

MSB: 6 bits → 1 MSB cell = 64 LSB cells
- 1 LSB cell = 500 nA
- 1 MSB cell = 32 uA

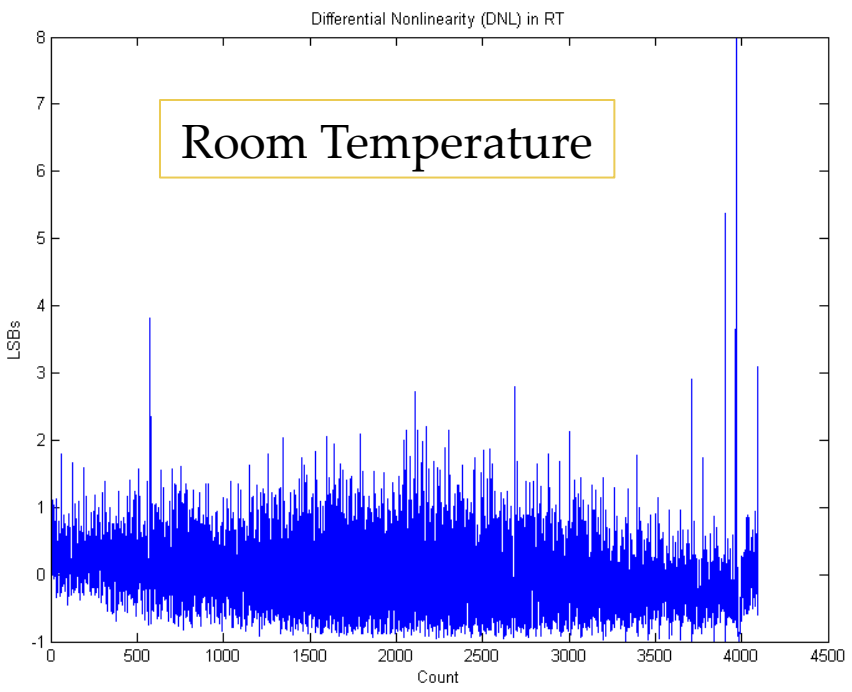
Sinusoidal sampled in LN

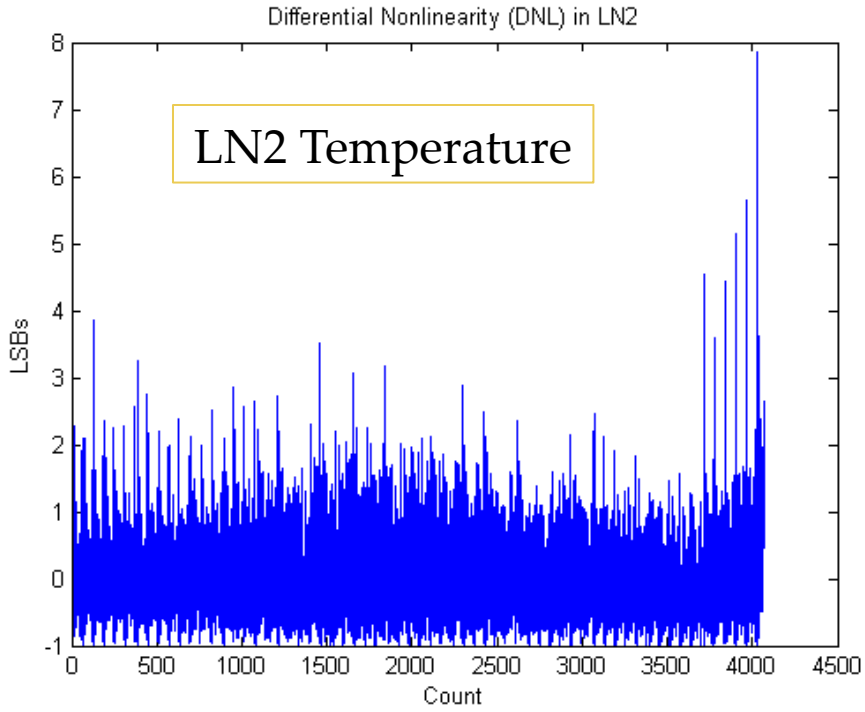




Effective resolution w.r.t. input referred noise is ~11.7 bits at both 300K and 77K

ADC ASIC

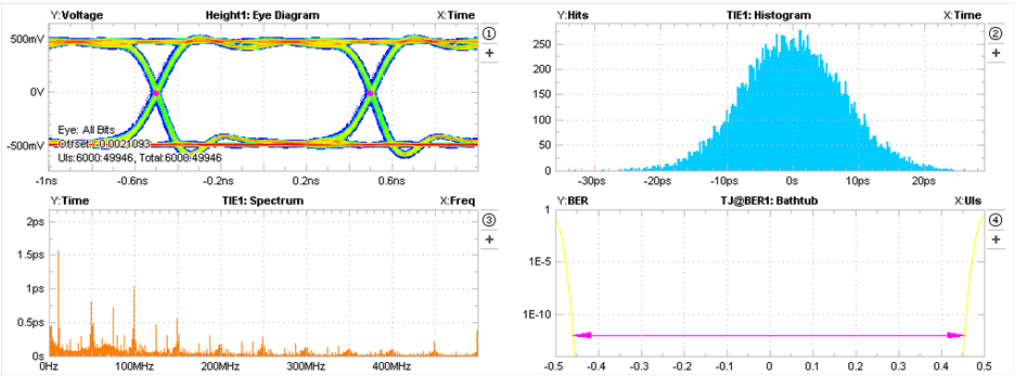


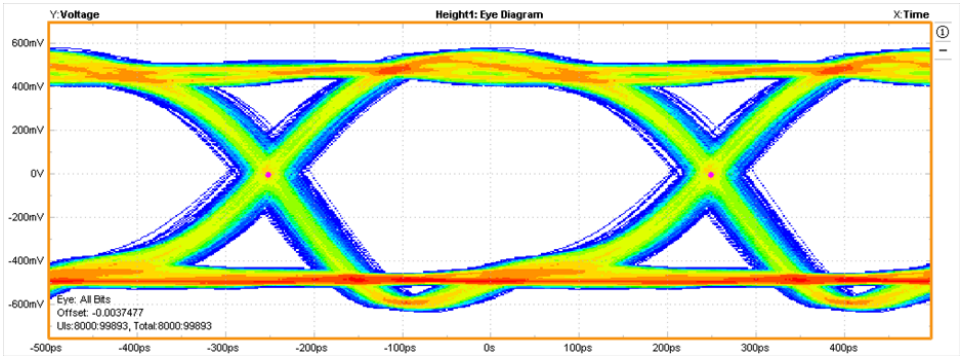


- Differential non-linearity (DNL) is less than 4 LSBs for 99% ADC bins at both 300K and 77K
  - Higher DNL every 64 ADC bins is understood, and improvement has been implemented

Cold FPGA

Qualified FPGA for Cold Operation

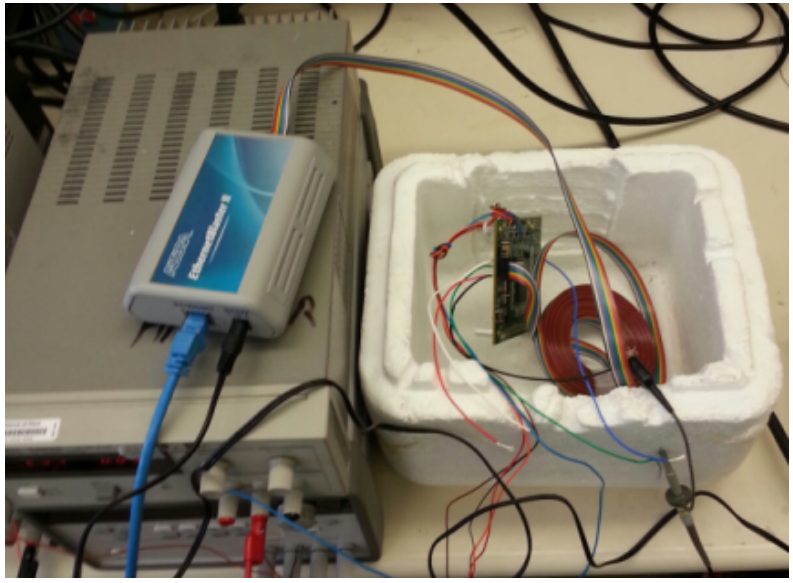




- Test of Cyclone IV GX Transceiver Starter Board in LN_2
  - Transceiver works well at both 1Gbit/s and 2Gbit/s
  - Height
    - 839mV @ 1Gbit/s
    - 823mV @ 2Gbit/s
  - Eye Width
    - 914ps @ 1Gbit/s
    - 357ps @ 2Gbit/s
  - On board SRAM works with BIST
    - 18-Mb SRAM from ISSI IS61VPS102418A-250TQL
    - Cyclone IV GX is running with Nios II processor and utilization of ~80% fabric resources

Cold FPGA

Vendor	Family	Technology	Speed of GTX [Gbps]	# of GTX	Memory [Mbit]	Core Voltage [V]	Status	
ALTERA	Arria GX	90nm	3.125	4 - 12	1.2 - 4.5	1.2	Tested by BNL	✔
ALTERA	Arria II	40nm	6.375	8 - 24	2.9 - 16.4	0.9	Tested by BNL	✗
ALTERA	Stratix II GX	90nm	6.375	4 - 20	1.4 - 6.7	1.2	Tested by SMU	✔
ALTERA	Cyclone IV E	60nm	N/A	N/A	0.3 - 3.9	1.0, 1.2	Tested by BNL	✔
ALTERA	Cyclone IV GX	60nm	3.125	2 - 8	0.5 - 6.5	1.2	Tested by BNL	✔
ALTERA	Cyclone V GX	28nm	3.125	4 - 12	1.2 - 12.2	1.1	Tested by BNL	✗
XILINX	Virtex 5	65nm	6.5	0 - 24	0.9 - 18.6	1.0	Tested by BNL	✗



EPCS4	4Mbit	✔
EPCS16	16Mbit	✔
EPCS64	64Mbit	✗
EPCS128	128Mbit	✗
EPCQ16	16Mbit	✔
EPCQ32	32Mbit	✔
EPCQ64	64Mbit	✔
EPCQ128	128Mbit	✔

- FPGA Configuration Methods Tested in LN2
  - JTAG through ~50 feet of single ended cable
  - FPGA flash programming through I2C EPCS/EPCQ

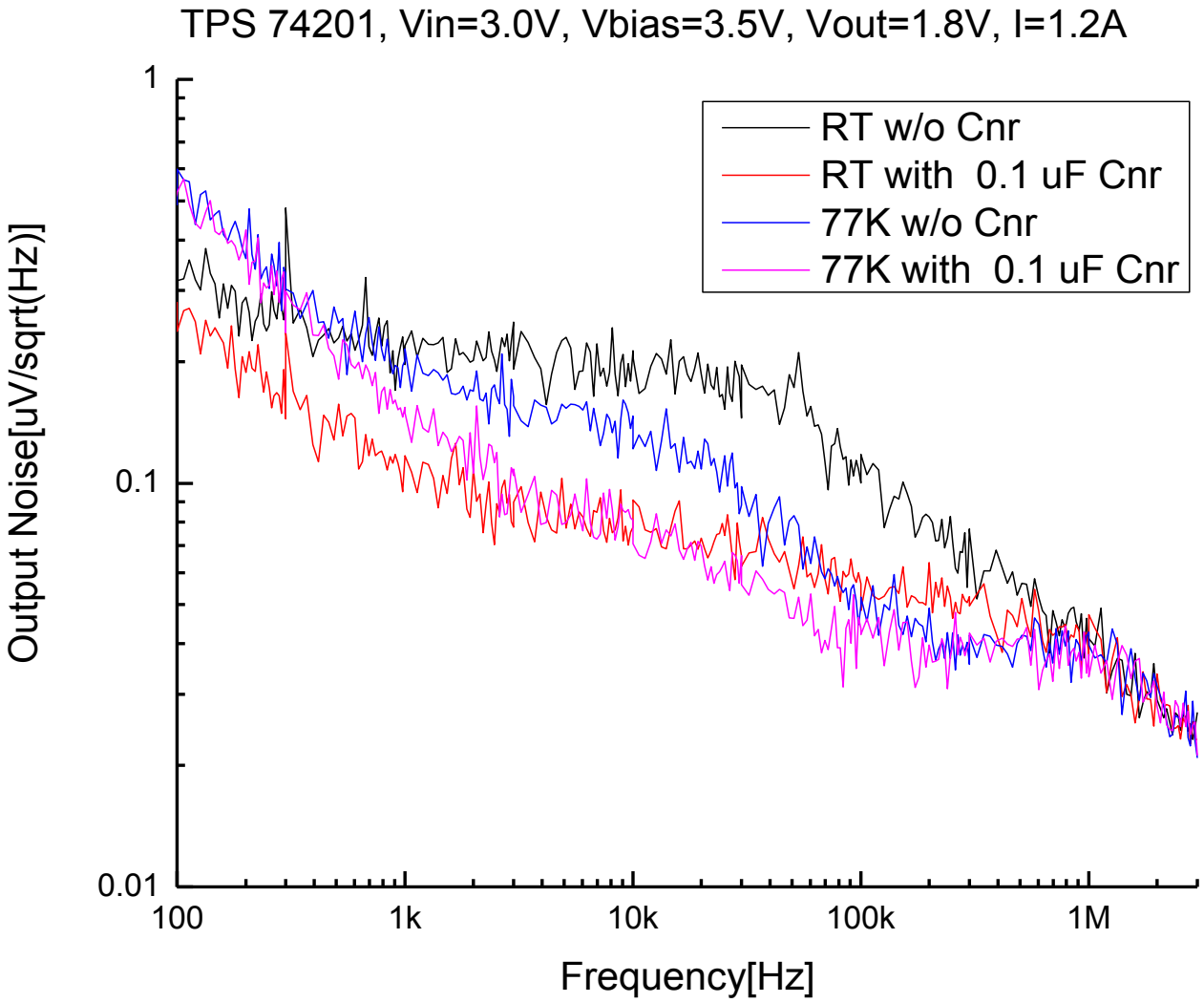
Cold Regulator

Vendor	Part Number	Iout	Vout	Vin	Note
ADI	ADP1708	1A	0.8V to 5.0V	2.5V to 5.5V	
ADI	ADP1741	2A	0.75V to 3V	1.6V to 3.6V	
ADI	ADP124ACPZ-1.8	500mA	1.8V	2.3V to 5.5V	
ADI	ADP130AUJZ-1.8	350mA	1.8V	2.3V to 3.6V	
ADI	ADP170AUJZ-1.8	300mA	1.8V	2.0V to 3.6V	
Globaltech	GS2915L18F	150mA	1.8V	2.3V to 6.0V	
Intersil	ISL9021	250mA	0.9V to 3.3V	1.5V to 5.5V	
Intersil	ISL80113	3A	0.8V to 3.3V	1V to 3.6V	
Linear	LTC3026	1.5A	0.4V to 2.6V	1.14V to 5.5V	
Linear	LTM4616	16A	0.6V to 5V	2.7V to 5.5V	POL Converter
Linear	LTM4619	8A	0.8V to 5V	4.5V to 26.5V	POL Converter
Maxim	MAX8517	1A	0.5V to 3.4V	1.425V to 3.6V	
National	LP38502TJ-ADJ	1.5A	0.6V to 5V	2.7V to 5.5V	
TI	TPS73701	1A	1.2V to 5V	2.2V to 5.5V	
TI	TPS78601	1.5A	1.2V to 5.5V	2.7V to 5.5V	
TI	TPS78618	1.5A	1.8V	2.7V to 5.5V	
TI	TPS78625	1.5A	2.5V	3.0V to 5.5V	
TI	TPS74201	1.5A	0.8V to 3.6V	0.9V to 5.5V	

- Cryogenic test of commercial voltage regulators that could be used to power LAr TPC cold electronics
- Stable and low-noise regulation, low dropout (low power) are critical

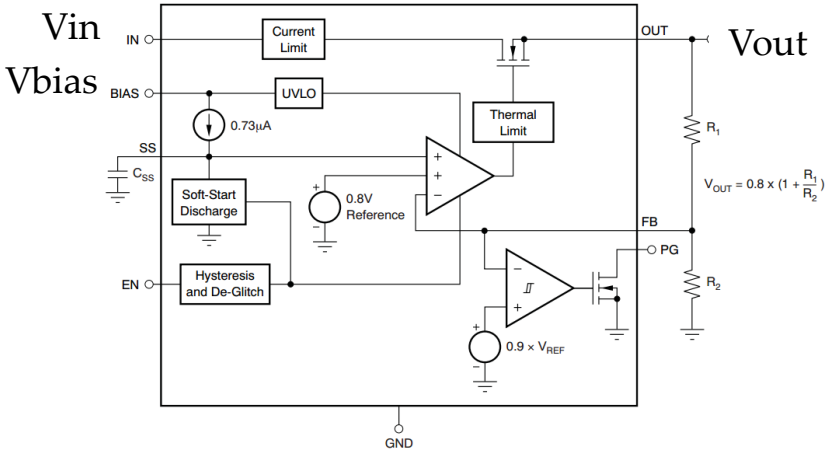
Cold Regulator - Noise

TI TPS74201: Output Noise Spectral Density

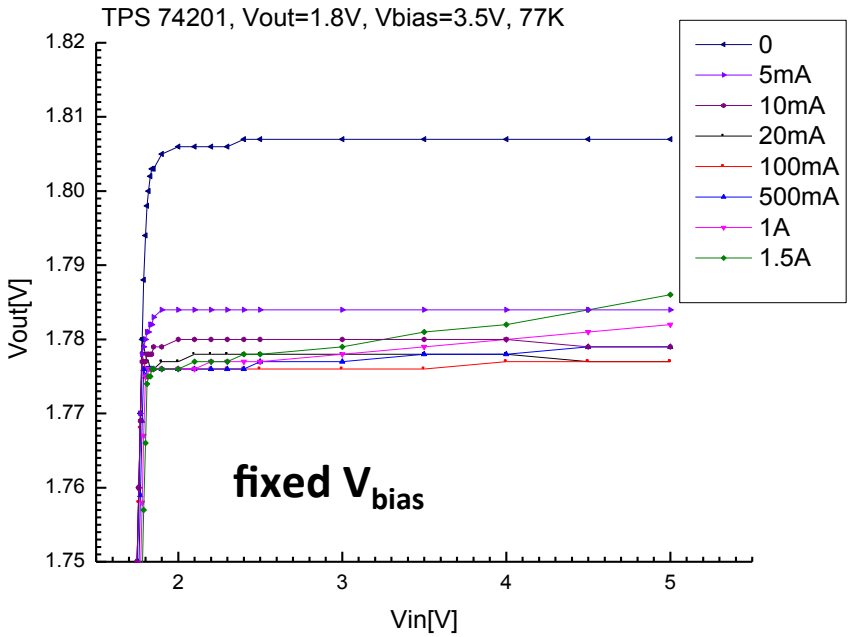


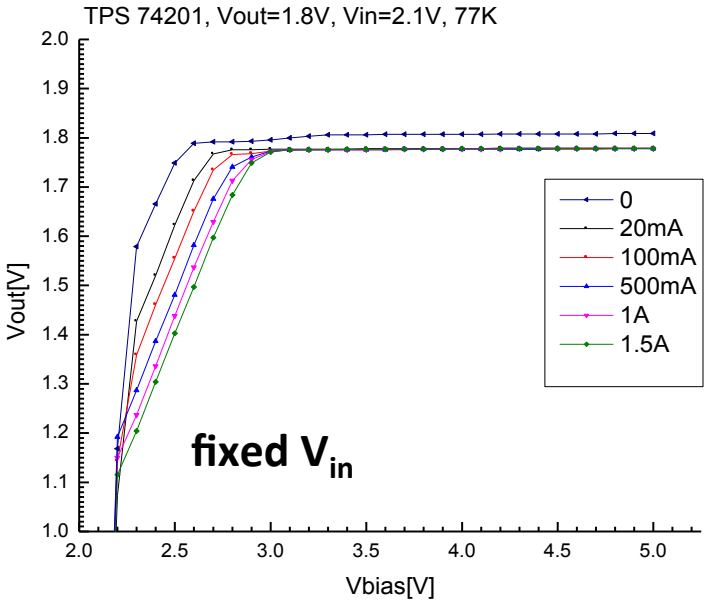
Cold Regulator Qualification

TI TPS74201

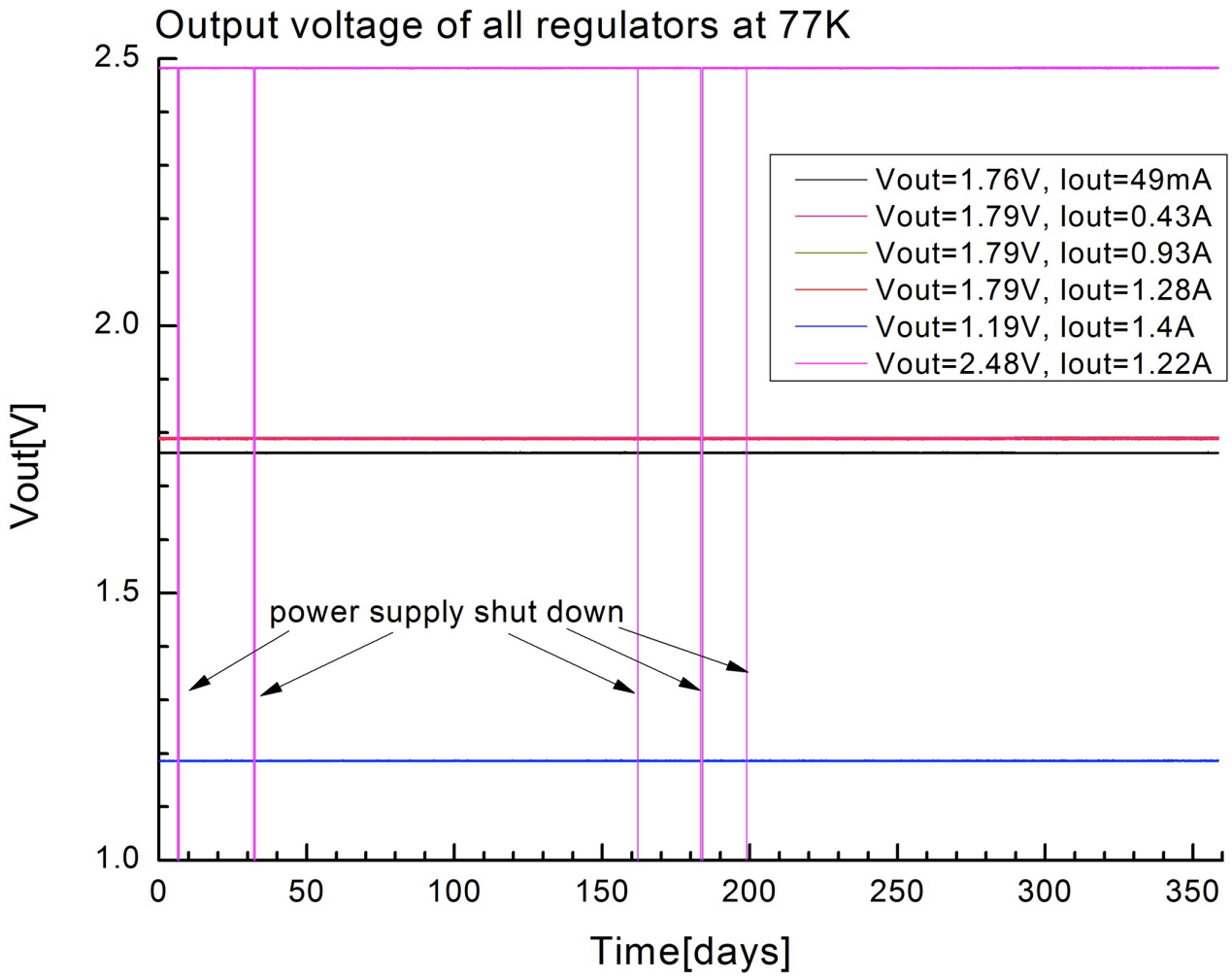


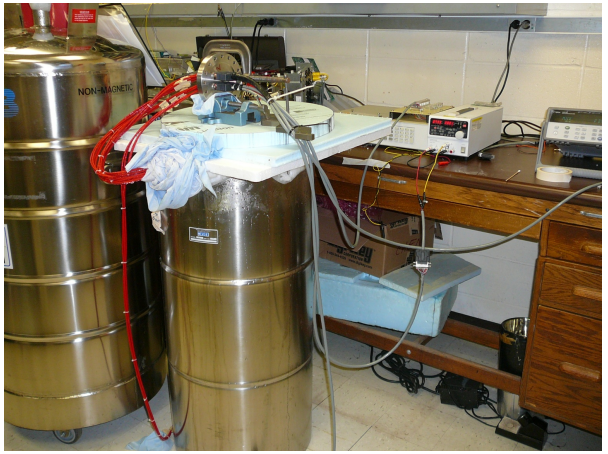
- TI TPS742xx voltage regulator family has been identified working well at cryogenic temperature recently
- 1.5A max I_{out}, 0.8V-3.6V adjustable V_{out}, and separate V_{in} makes it an ideal candidate for all of the cold electronics chain





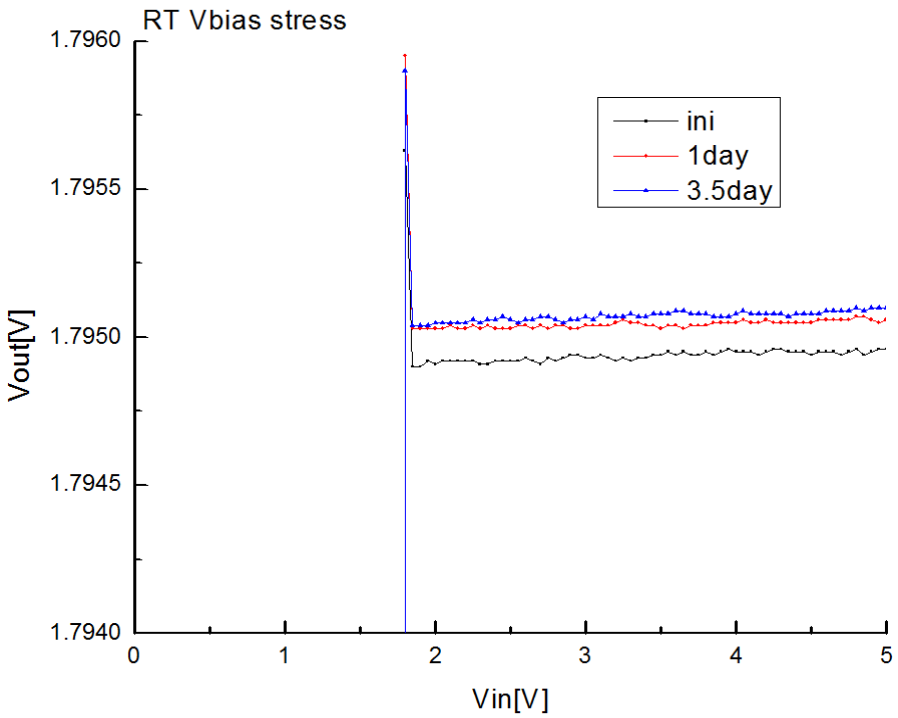
Cold Regulator - Lifetime

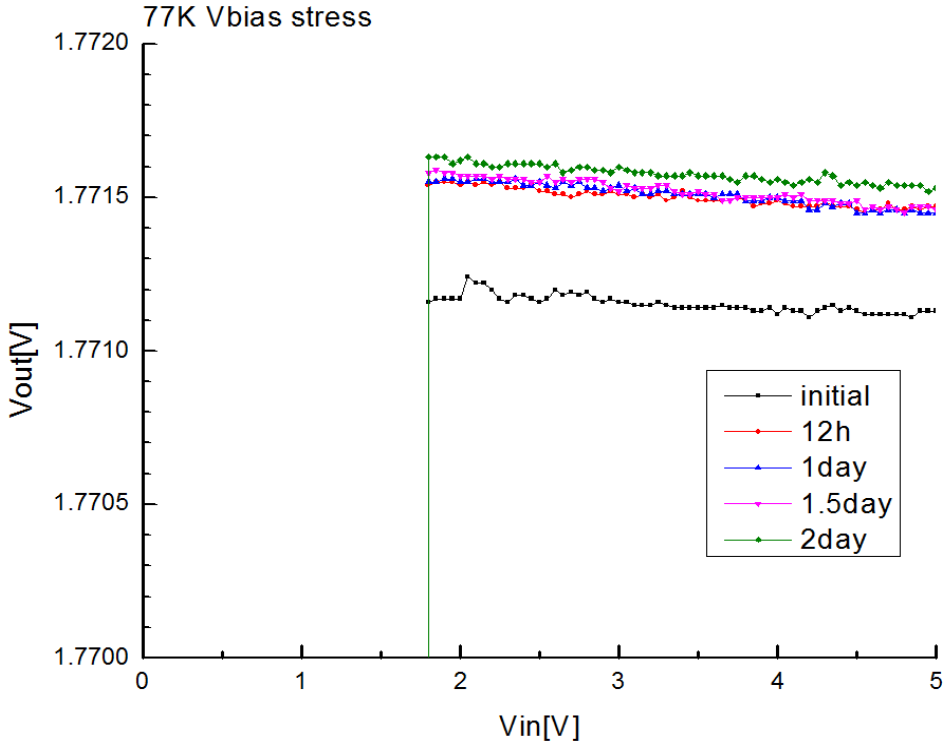




- A long term test of several **TPS74201 in LN2** has been going on **since June 24th, 2013**
- Voltage regulators are working normally for ~ 24 months, the test has been wrapped up in June 2015

Cold Regulator – Lifetime/Stress





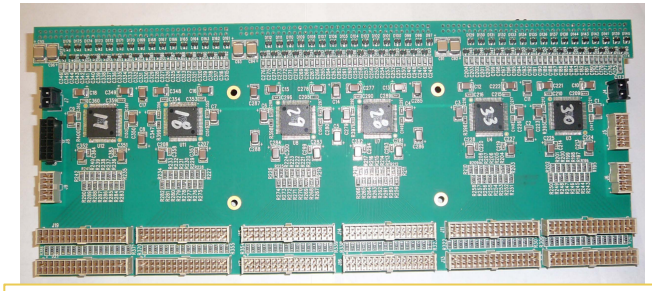
	Vin stress(Vbias=4V, Iload=0.9A)		Vbias stress(Vin=2.1V, Iload=50mA)	
	RT	77K	RT	77K
Maximum Stress Condition	Vin=8V	Vin=11V	Vbias=12V	Vbias=12V

- Preliminary tests show negligible degradation with voltage stress much higher than nominal
  - Compare 12V to nominal 3.6V, 8V to nominal 1.8V
- Systematic lifetime characterization will continue through the next months

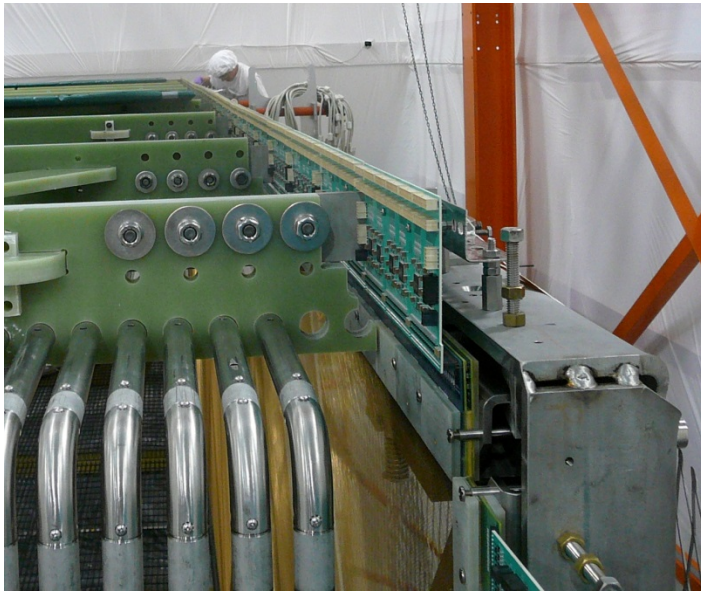
Performance as ASIC is submerged in LN_2

Analog FE ASIC in MicroBooNE

8,256 channels instrumented with FE ASICs

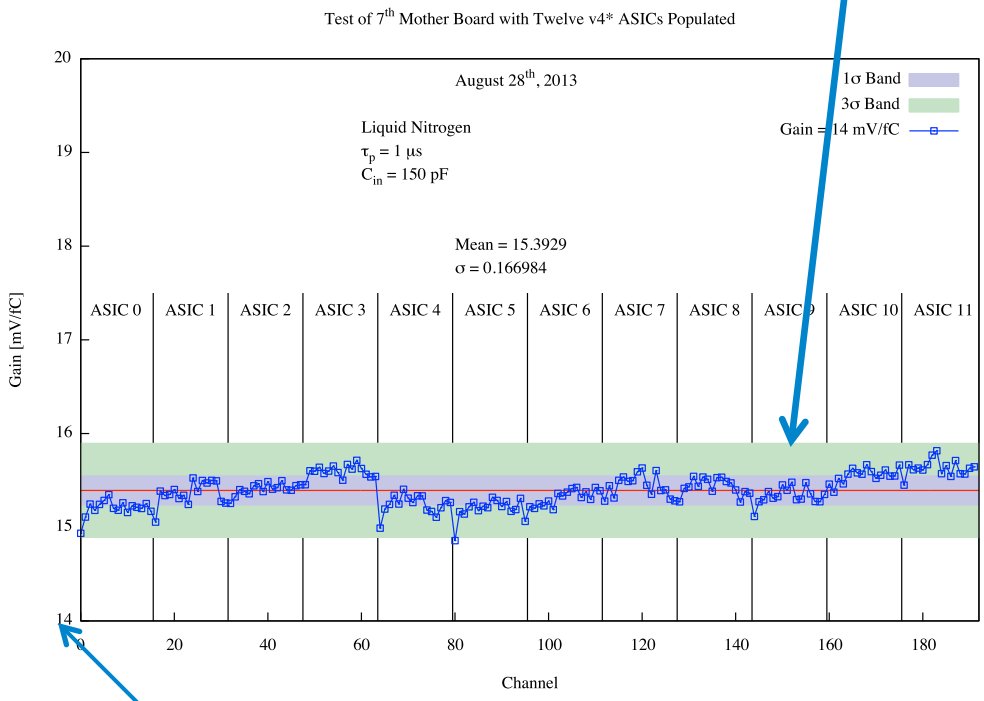


MicroBooNE cold mother board with 12 analog FE ASICs (192 channels)



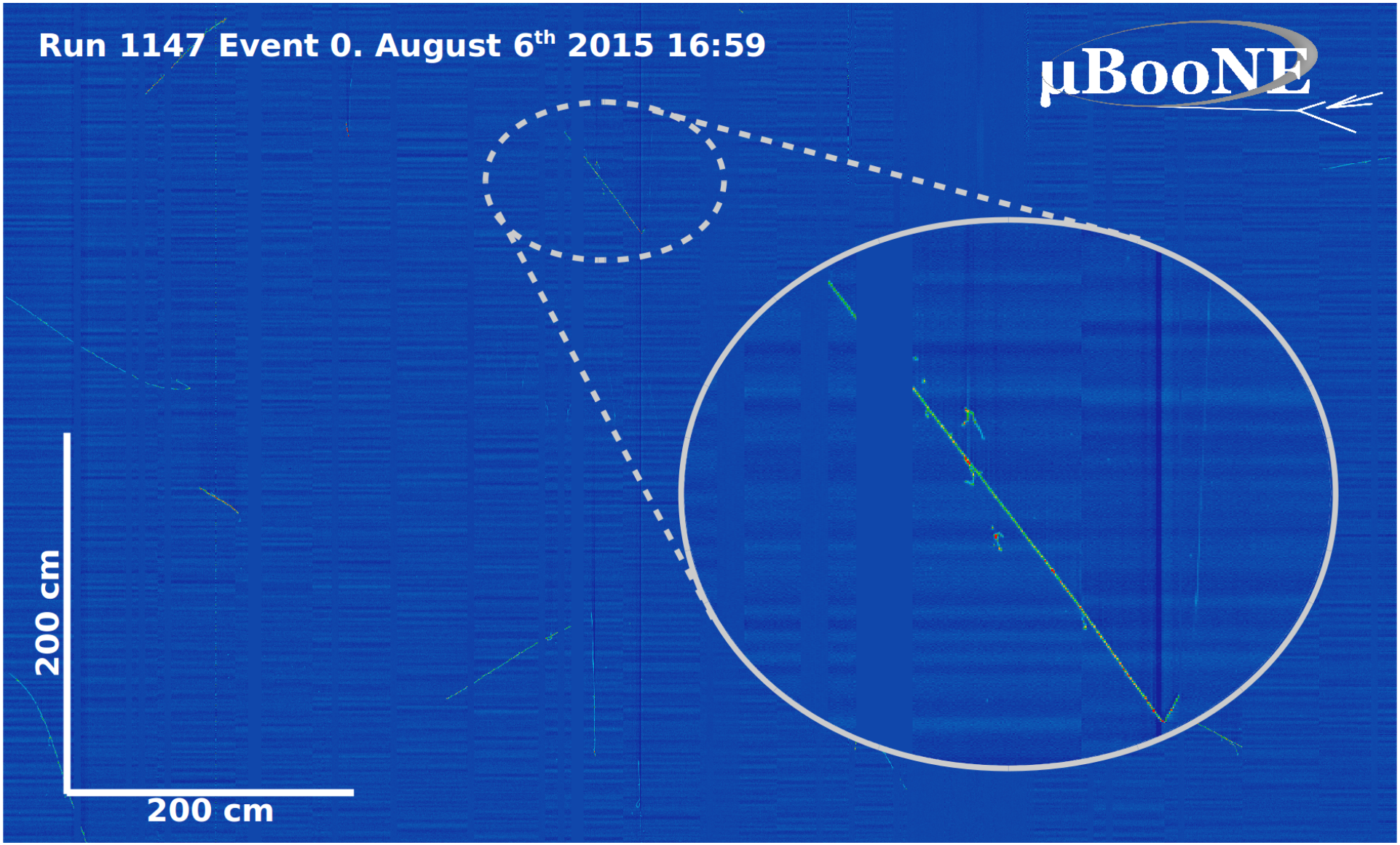
50 cold mother boards (8,256 channels) are installed on MicroBooNE TPC

$\sigma_{gain} \approx 1\%$

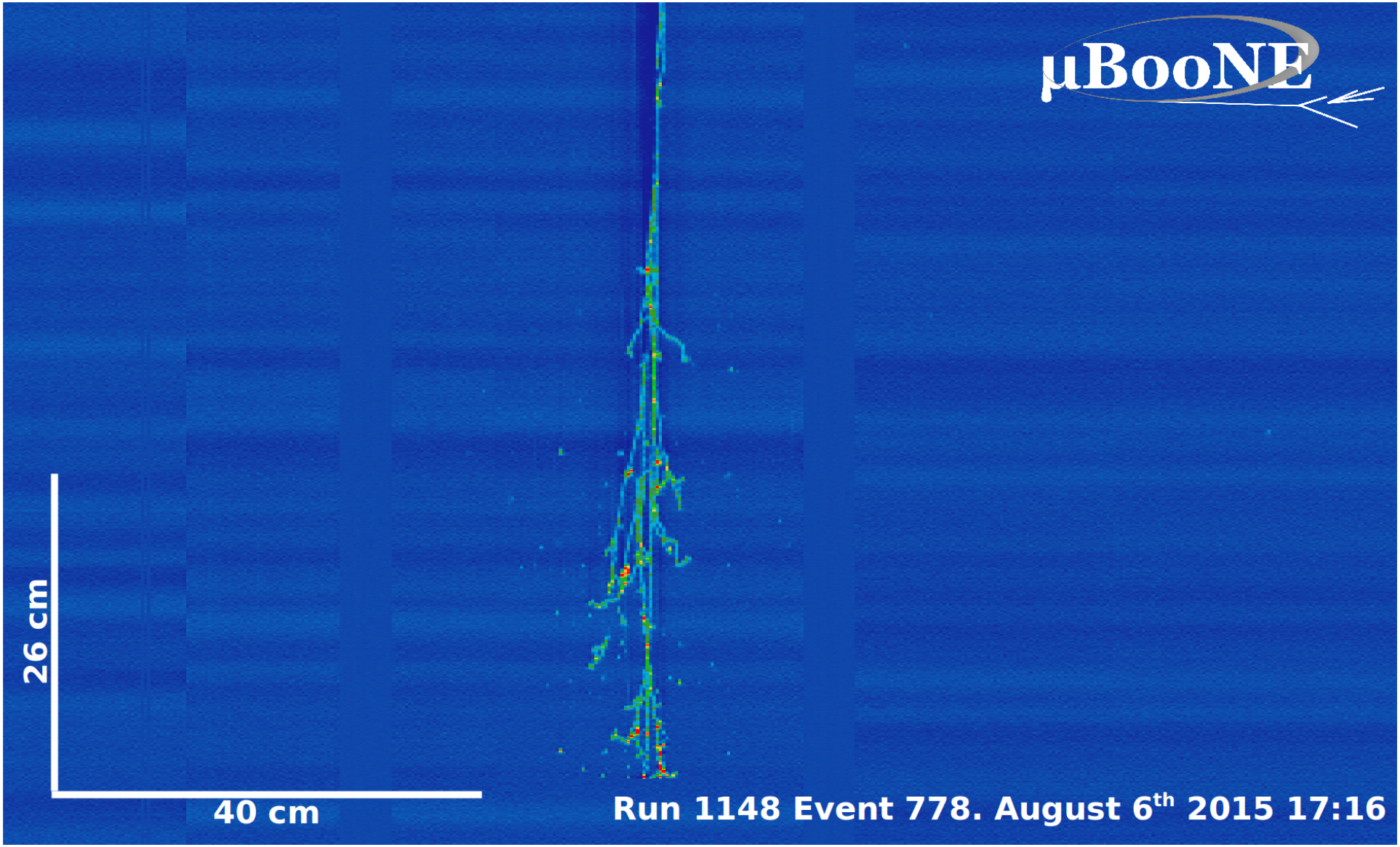


Note: Offset scale

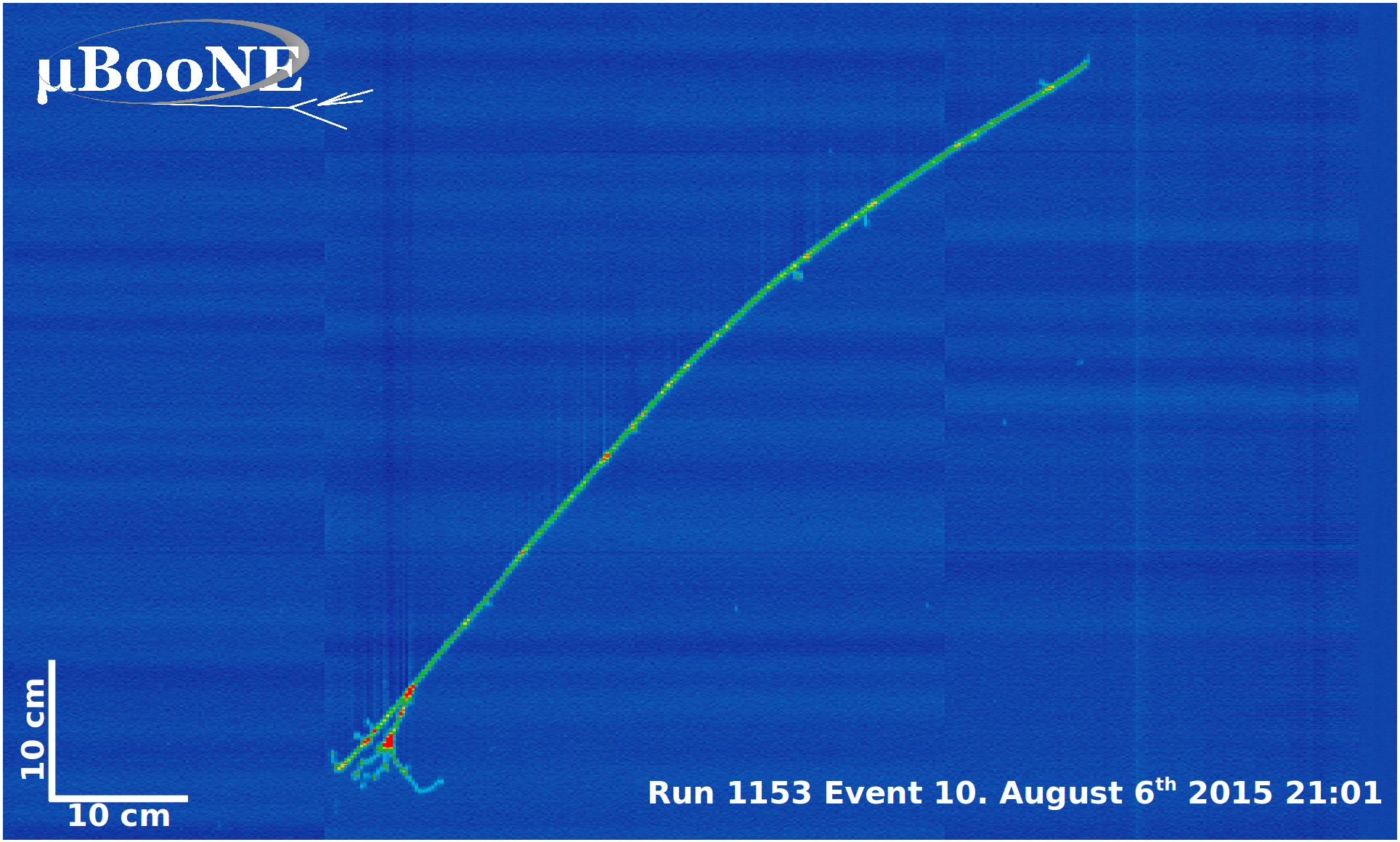
Cosmic Rays Events in MicroBooNE @ 230V/cm



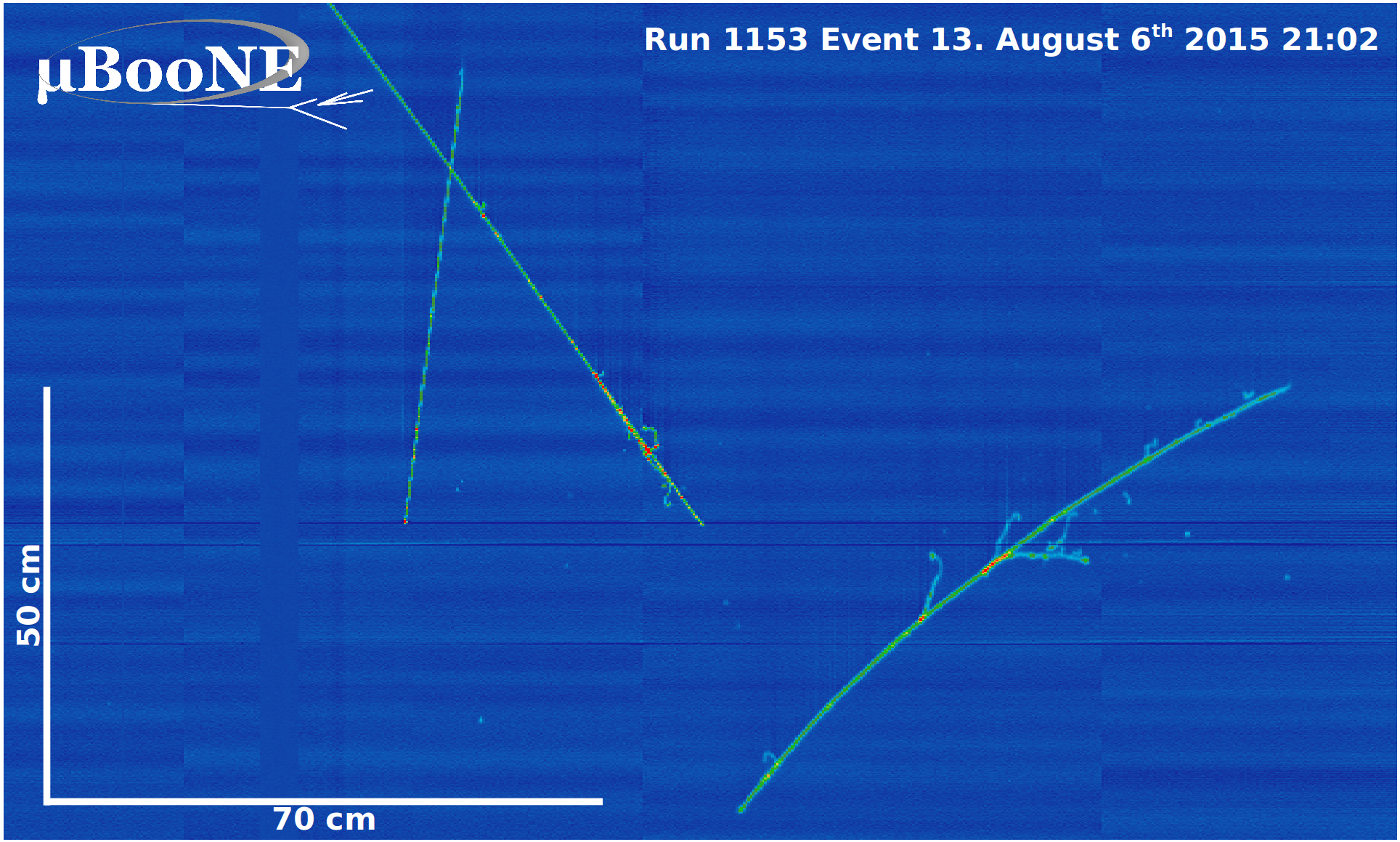
Cosmic Rays Events in MicroBooNE @ 230V/cm



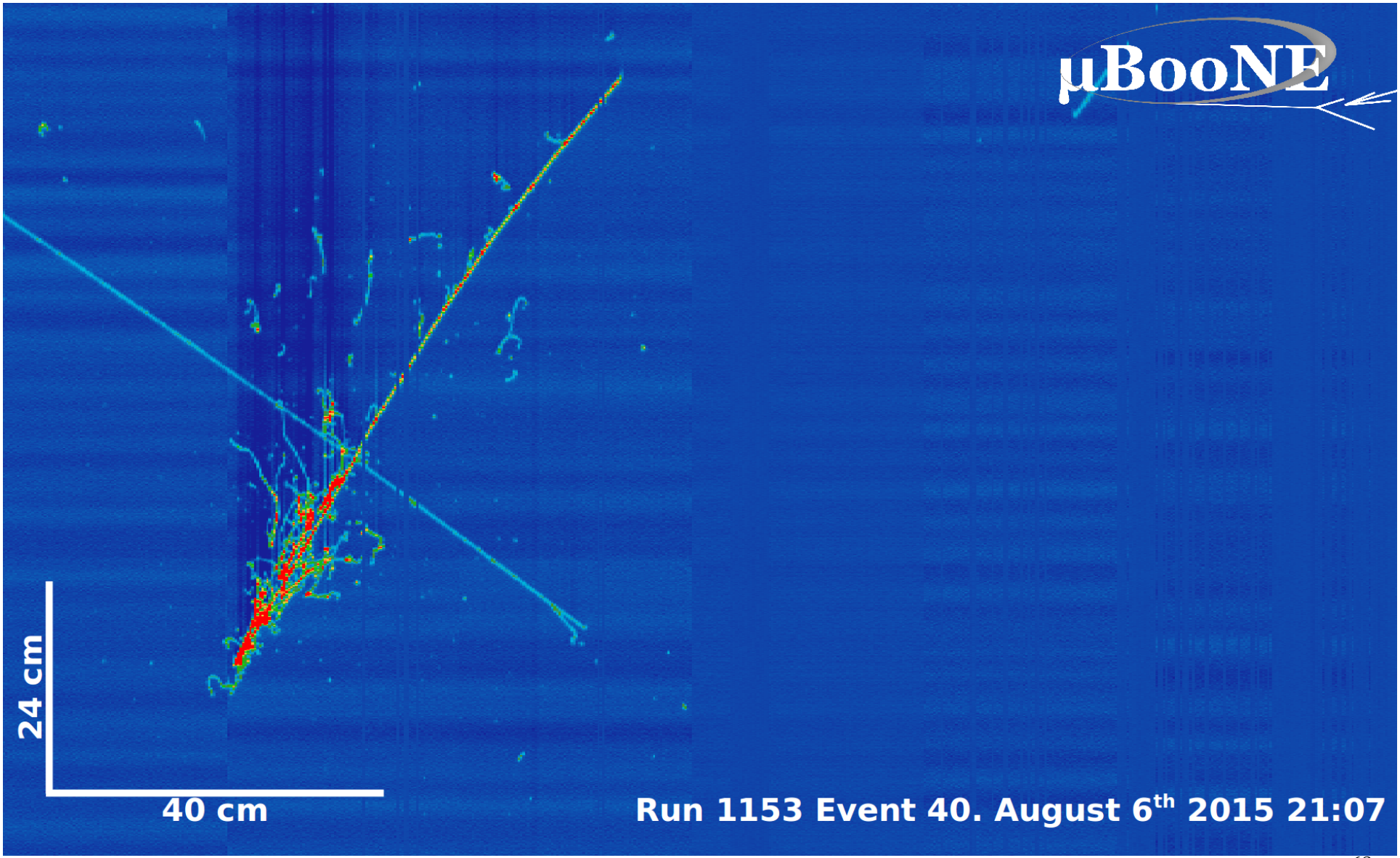
Cosmic Rays Events in MicroBooNE @ 230V/cm



Cosmic Rays Events in MicroBooNE @ 230V/cm

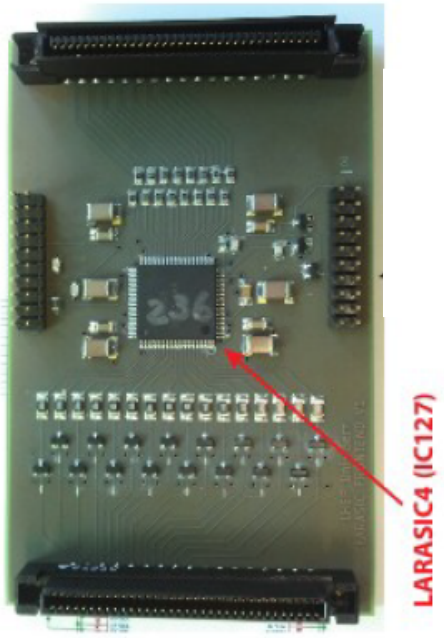


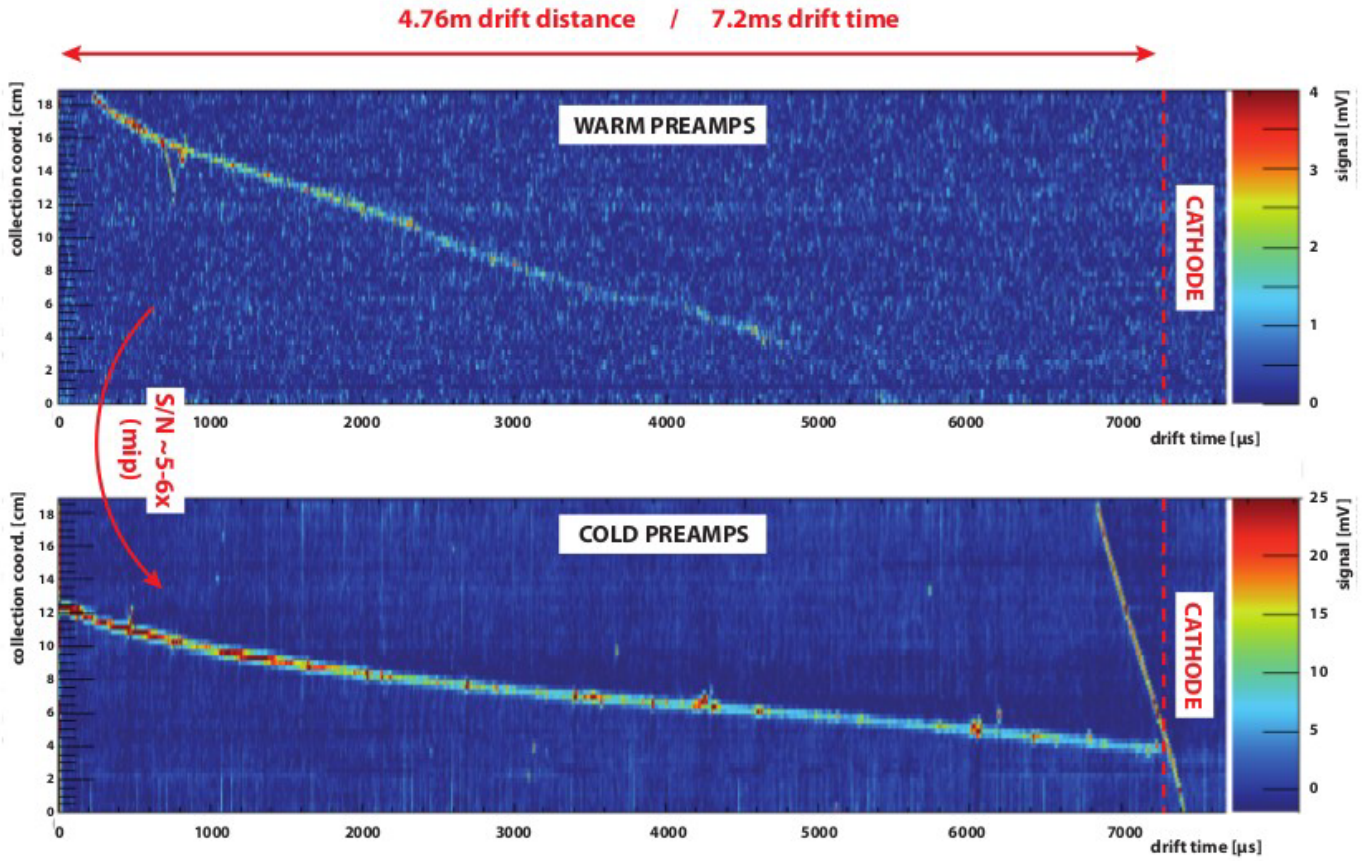
Cosmic Rays Events in MicroBooNE @ 230V/cm



Analog FE ASIC in ARGONTUBE (Bern)

5-6x Improvement on S/N



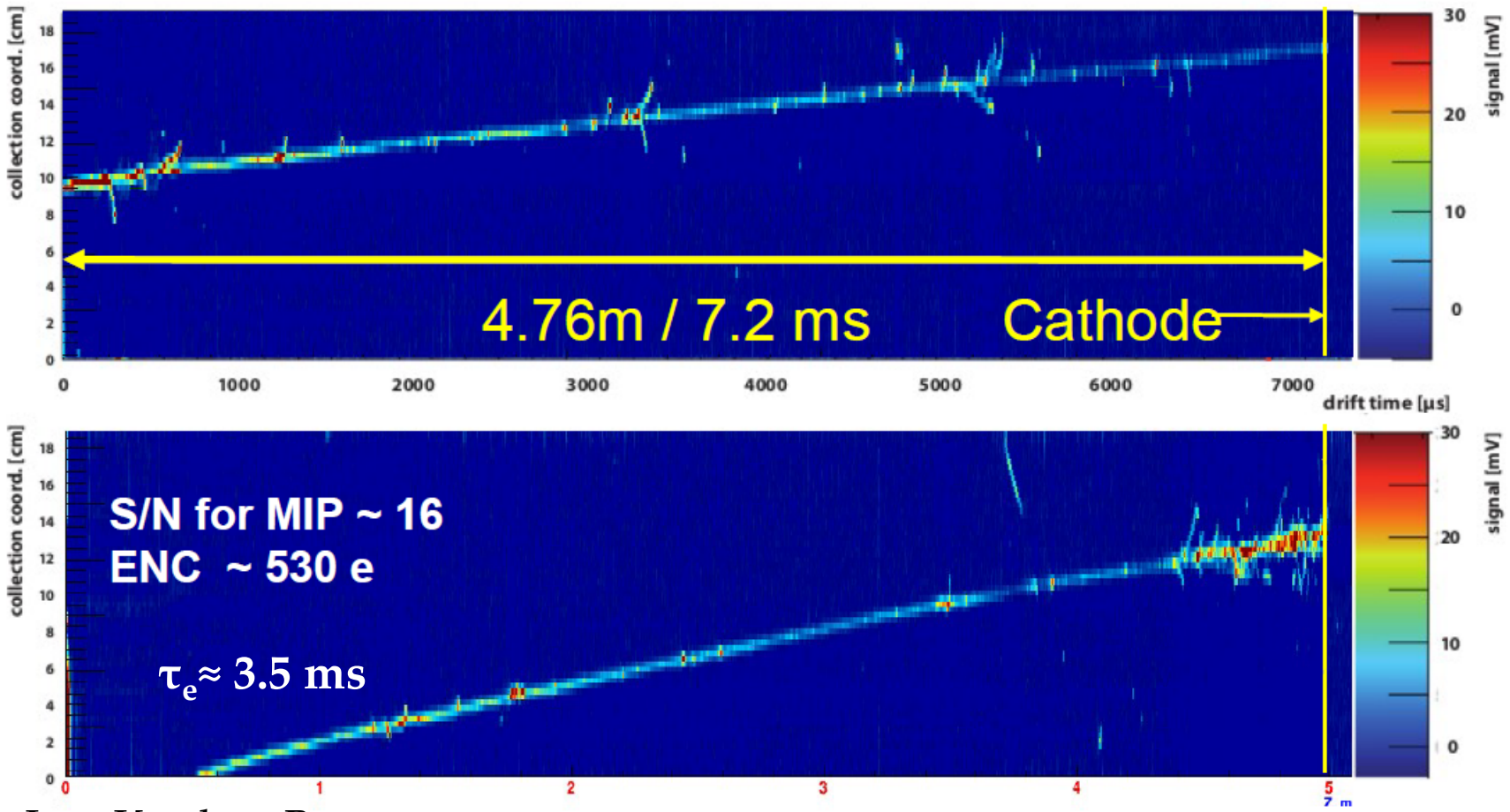


- N.B. different color scale on two plots
- Courtesy of Igor Kreslo @ University of Bern

Testing MicroBooNE cold preamps with ARGONTUBE

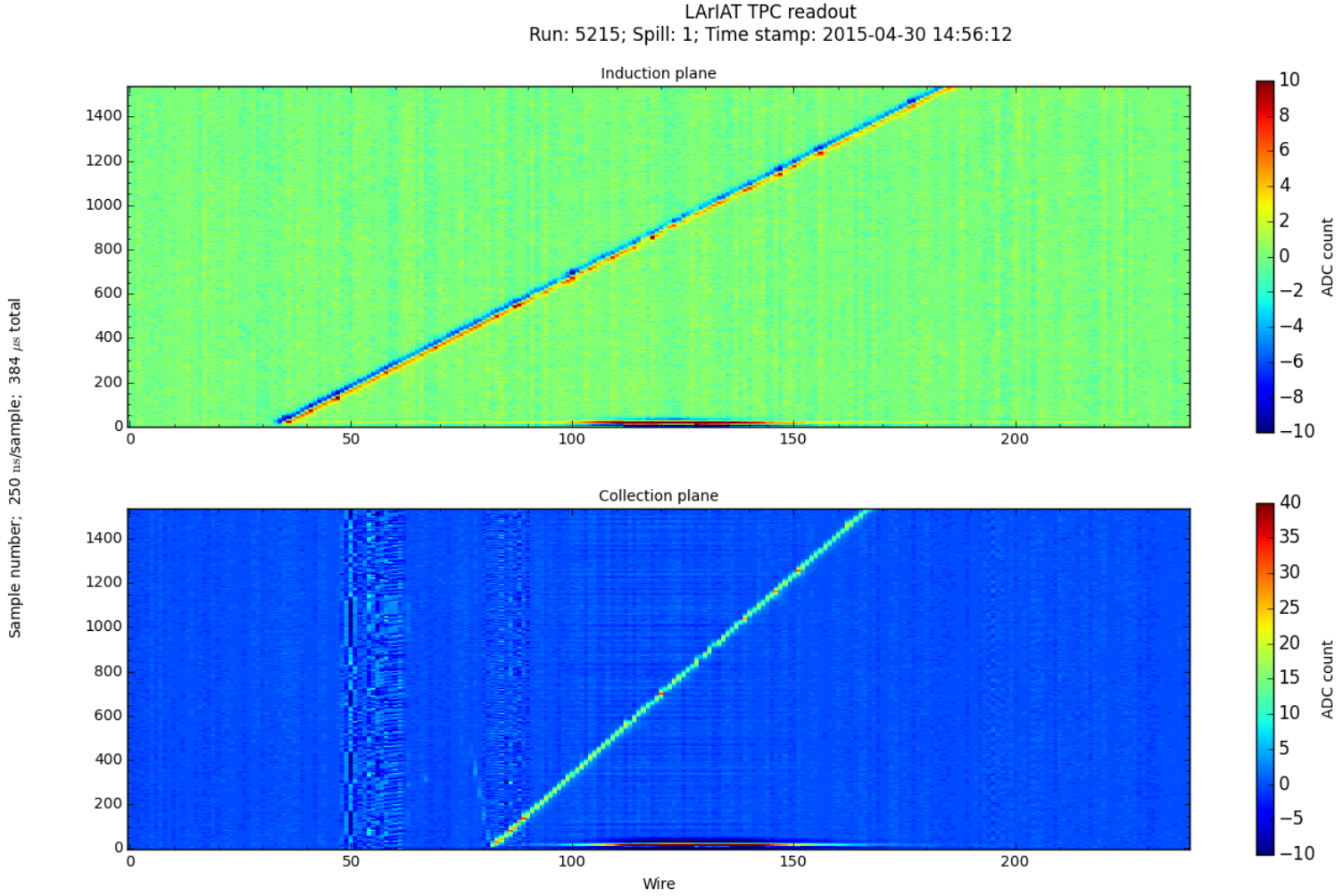
~ 5 m long electrons drift in LAR: first time!

twice MicroBooNE drift lentgh, < ½ E-field



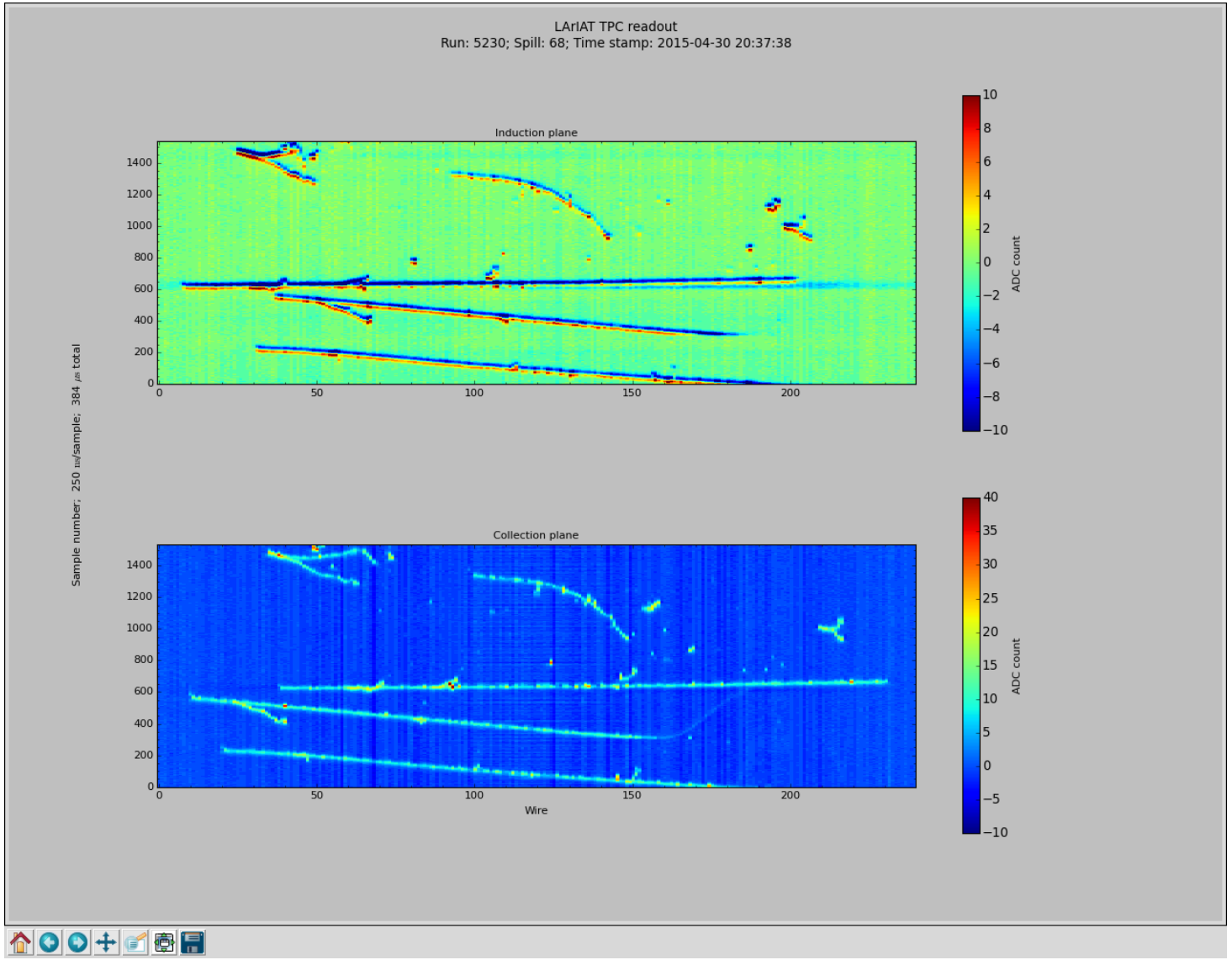
From: Igor Kreslo @ Bern

Analog FE ASIC in LArIAT



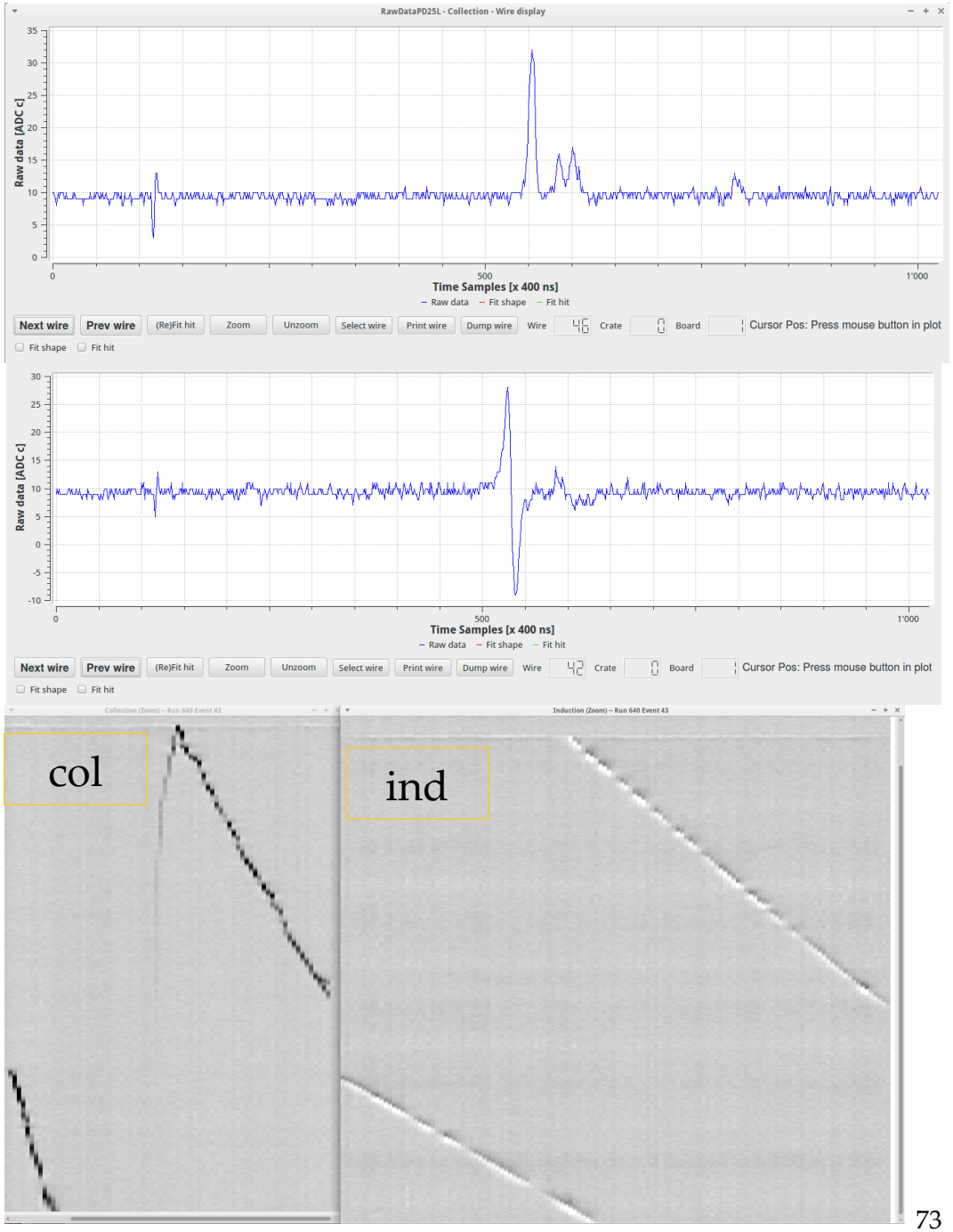
- S/N reaches ~50/1 (from Carl Bromberg @ MSU)

LArIAT Beam Event



Analog FE ASIC in ICARUS 50l TPC

- ICARUS 50l TPC
  - Warm integration test in the week of March 30th at CERN
  - Cold data taking in the week of April 20th at CERN:
    - **The signals were observed and the tracks reconstructed on the first day of cooling down!**



Electronics lifetime at 300K and 77K

- Lifetime vs temperature due to ***aging*** process
  - CMOS in ***dc*** operation: Analog FE ASIC
  - CMOS in ***ac*** operation: Logic circuits and FPGAs

Principal findings and design guidelines

- A study of hot-electron effects on the device lifetime has been performed for the TSMC NMOS 180nm technology node at 300K and 77K. Two different measurements were used: accelerated lifetime measurement under severe electric field stress by the drain-source voltage (Vds), and a separate measurement of the substrate current (Isub) as a function of $1/V_{ds}$. The former verifies the canonical very steep slope of the inverse relation between the lifetime and the substrate current , $\tau \propto I_{sub}^{-3}$, and the latter confirms that below a certain value of Vds *a lifetime margin of several orders of magnitude can be achieved for the cold electronics TPC readout. The low power ASIC design for MicroBooNE and DUNE falls naturally into this domain, where hot-electron effects are negligible*

- *Lifetime of digital circuits (ac operation) is extended by the inverse duty factor* $4/(f_{clock} t_{rise})$ *compared to dc operation.* This factor is large (>100) for deep submicron technology and clock frequency needed for TPC

CMOS in **dc** operation: Analog FE ASIC Introduction (1)

- *Lifetime due to aging*: A limit defined by a chosen level of monotonic degradation in e.g., drain current, transconductance, due to a well understood mechanism. The device "fails" if a chosen parameter gets out of the specified circuit design range. This aging mechanism does not result in sudden device failure
- At high temperatures (300-420K) there are several sudden failure mechanisms strongly temperature dependent [e.g., electromigration $\propto (I/T)^2 \exp(-a/T)$], which become negligible at low temperatures
- *Physics-of-failure* modeling for CMOS technology in LAr is reduced to study of hot-electron effects as the dominant remaining mechanism
- Thermal expansion/contraction is studied separately

Introduction (2)

- It is known that CMOS operation at cryogenic temperatures offers considerable advantages as compared to room temperature operation, with respect to *speed, transconductance/drain current ratio (subthreshold slope) and noise*. All chemical degradation processes, such as *electromigration* are significantly slowed down to a negligible level
- However it has also been reported that device *degradation due to channel hot carriers (electrons in particular) is increased at low temperatures*. The purpose of our study and the test program has been to try to establish with confidence some lifetime estimates for the CMOS circuits to be operated in LAr. In this study we have been following the basics established already starting in 1985, e.g., Hu et al. [1], and the practices adopted more recently by Cressler et al. [2], as well as by industry
- It has also been noted that hot carrier effects, if any, are more pronounced in NMOS than in PMOS. In this discussion we refer to hot electrons rather than holes, and the measurement results presented here have been obtained on NMOS transistors
- Reference

1. C. Hu, S. C. Tam, F.-C. Hsu, P.-K. Ko, T.-Y. Chan, and K. W. Terrill, "Hot-electron-induced MOSFET degradation-model, monitor, and improvement", *IEEE Journal of Solid-State Circuits*, vol. sc-20, no. 1, pp. 295-305, Feb. 1985.
2. T. Chen, C. Zhu, L. Najafizadeh, B. Jun, A. Ahmed, R. Diestelhorst, G. Espinel, and J. D. Cressler, "CMOS reliability issues for emerging cryogenic Lunar electronics applications," *Solid-State Electronics*, vol. 50, pp. 959-963, 2006.

Overview of Basics on Hot-electron effects (HEC) and NMOS lifetime (1)

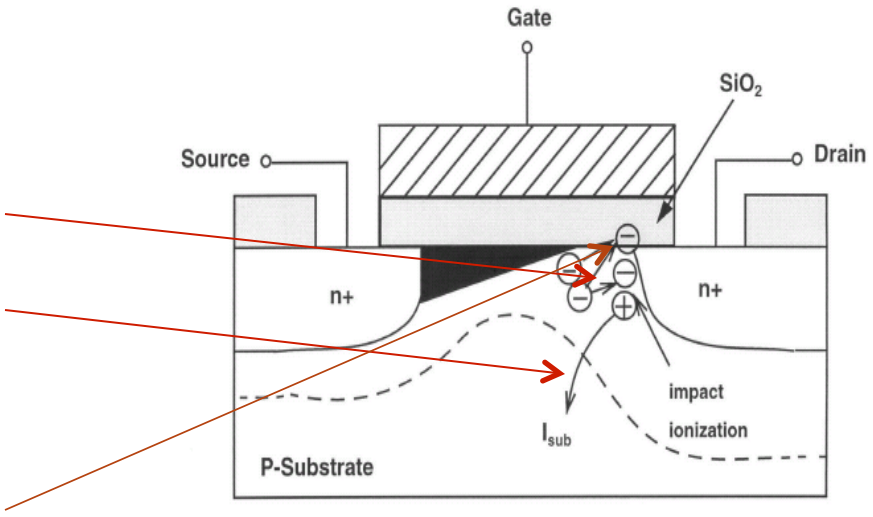
- In deep submicron NMOS (L<0.25μm) electrons can become "hot" at any temperature, by attaining energy $E > kT$.

- Some hot electrons exceed the energy required to create an electron-hole pair, $\varphi_i \cong 1.3eV$ resulting in *impact ionization*. Electrons proceed to the drain. The *holes* drift to the substrate. The ***substrate current,***

$$I_{sub} = C_1 I_{ds} e^{-\varphi_i / q\lambda E_m} \qquad (1)$$

- A very small fraction of hot electrons exceeds the energy required to create an ***interface state*** (e.g., an acceptor-like trap), in the Si-SiO_2 interface, $\varphi_{it} \geq 3.7eV$ for electrons (~4.6eV for holes). This causes a change in the transistor characteristics (transconductance, threshold, intrinsic gain). The time required to change any important parameter (the changes in different parameters are correlated) by a specified amount (e.g., g_m by -10%) is defined as the ***device lifetime***. It can be calculated as,

$$\tau = C_2 \frac{W}{I_{ds}} e^{\varphi_{it} / q\lambda E_m} \qquad (2)$$



q = electron charge

$\boldsymbol{\lambda}$ = electron mean free path

E_m = *electric field*

I_{ds}= drain-source current

W= channel width

C_1, C_2 - constants

Overview of Basics on Hot-electron effects (HEC) and NMOS lifetime (2)

- **It has been widely recognized in the literature (e.g., [1] and [2]) that I_{sub} is a monitor for all hot-electron effects and it is the best predictor of device lifetime**
- The reason that device lifetime or degradation may be predicted from the substrate current I_{sub} is that both observable hot electron effects (electrical and optical) are driven by a common driving force – the channel electric field, or more specifically the maximum channel electric field E_m , which occurs at the drain end of the channel.
- The *substrate current is connected to the lifetime* (defined by any arbitrary but consistent criterion) by the relation {obtained by cancellation of $q\lambda E_m$ between Eqs, (1) and (2)},

$$\tau = H \frac{1}{\left(I_{ds}/W\right)} \left(\frac{I_{sub}}{I_{ds}} \right)^{-\varphi_{it}/\varphi_i} \qquad (3)$$

- The constant H [As/μm] is a function of the channel length L, the temperature and the device technology (interface quality, details of drain doping, etc.) and the criterion used for definition of the lifetime (e.g., 10% decrease in transconductance, g_m, as used in industry).

Overview of Basics on Hot-electron effects (HEC) and NMOS lifetime (3)
Lifetime τ vs I_{sub}/I_{ds} and I_{ds}/W

- While the proportionality constant *H* will vary from case to case depending on the technology, channel length, temperature, the functional relationship
- in Eq. (3) is most useful in lifetime measurements and predictions,

$$\tau I_{ds} \Big/ W \propto \frac{1}{\left(I_{sub}/I_{ds}\right)^{a}} \qquad (4)$$

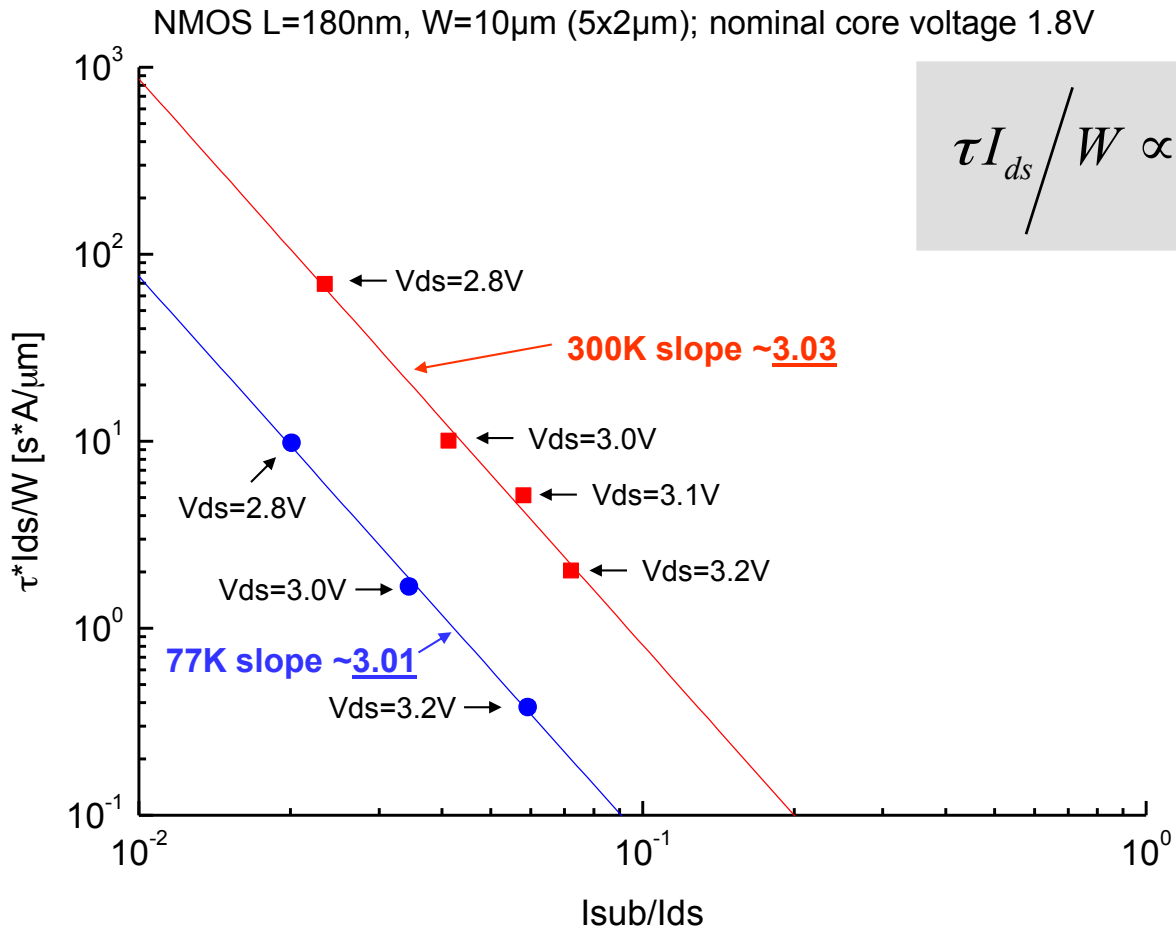
- The exponent ***a*** is defined as the ***ratio*** of the *critical electron energy to generate an interface trap* and *the critical energy to produce an electron-hole pair by impact ionization,*

$$a = \varphi_{it} \Big/ \varphi_{i} \;;\; 2.9 - 3.2$$

$$\varphi_{i} \;;\; 1.3eV ; \varphi_{it} \;;\; 3.7eV - 4.1eV$$

- The ratio of these two critical energies defines the *very steep dependence of the lifetime on the substrate current*. This ratio is largely independent of temperature.

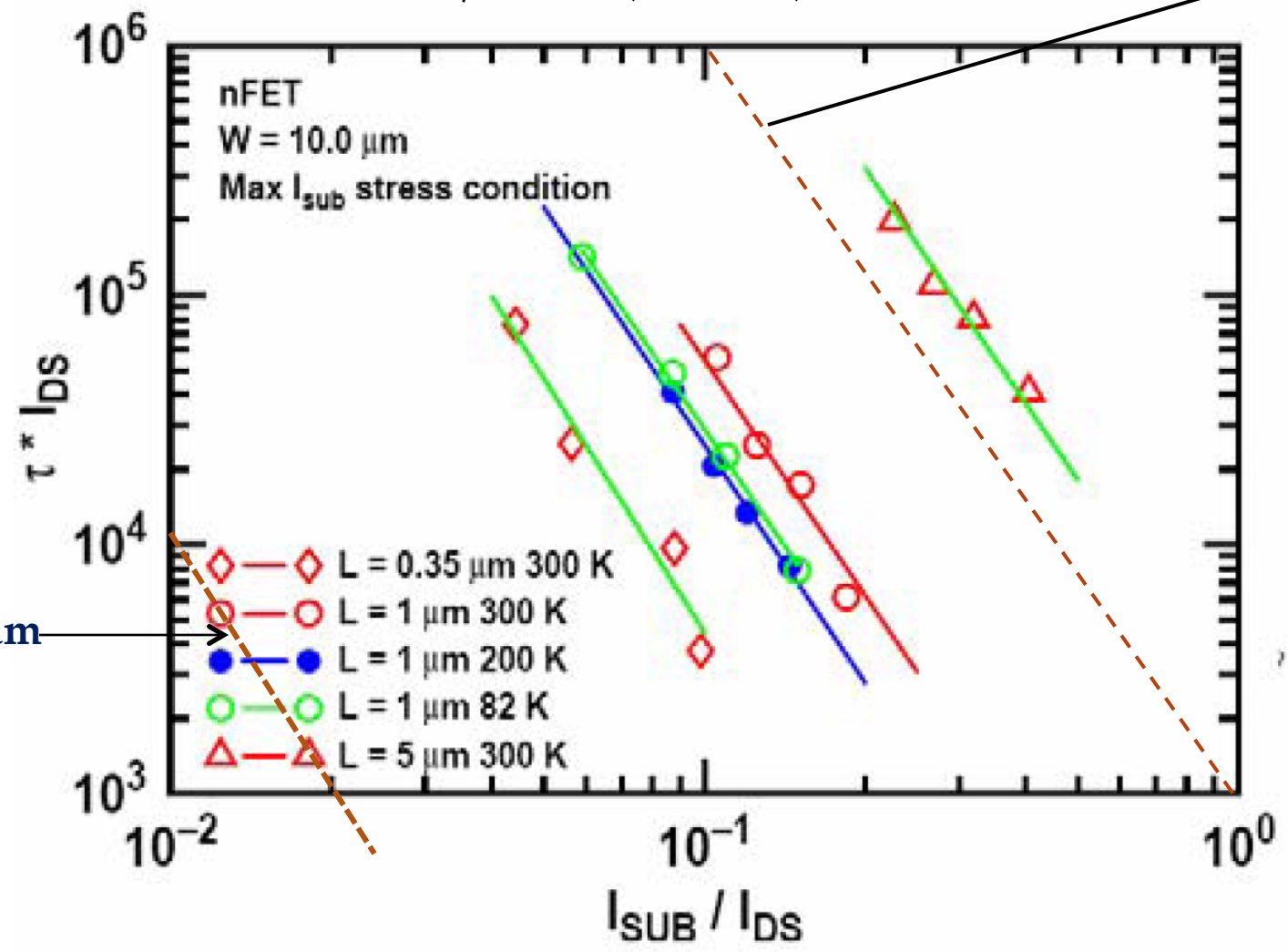
Measurement Type I: "Stress Plot"



- **Fig.1.** This is an ***accelerated lifetime test*** where the transistor is placed under a ***severe stress***, to reduce the lifetime due to hot-electron degradation to a practically observable range, by a drain source voltage considerably higher than the nominal voltage (1.8V for L_{min}=180nm). *The measured points at both 300K and 77K are very close to the characteristic slope for the interface state generation,* ***a≈3***.

Stress plots for IBM SiGe BiCMOS process with different channel lengths. Measurements by J. Cressler, et al. (Georgia Tech) confirming the *slope*:

$$\tau I_{ds} \Big/ W \propto \frac{1}{\left(I_{sub}/I_{ds}\right)^{a}} \rightarrow a \; ; \; 3$$



L=0.18 µm 300K (BNL)

Fig.2.

Lifetime *vs* $1/V_{ds}$ extracted from the stress measurements

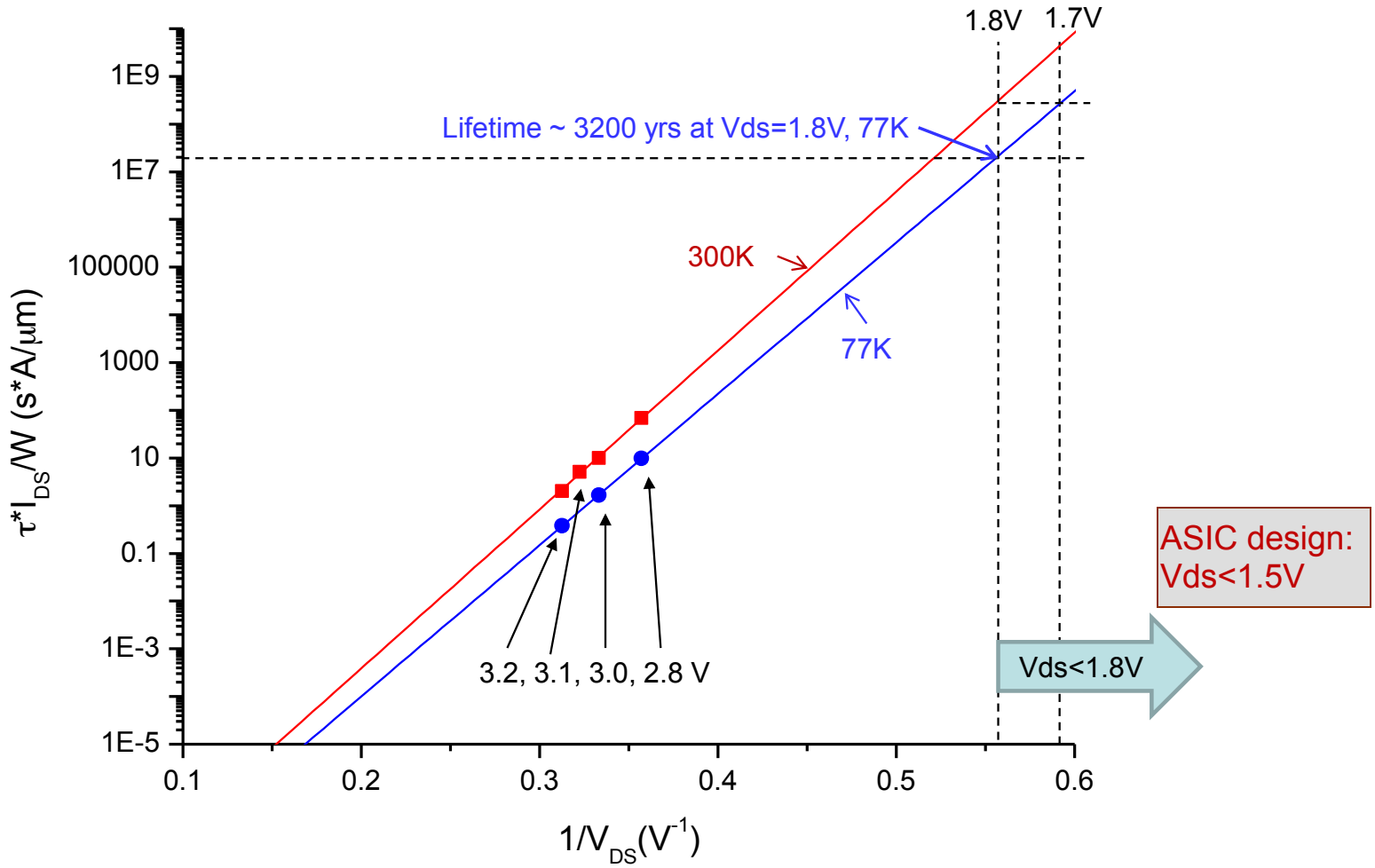
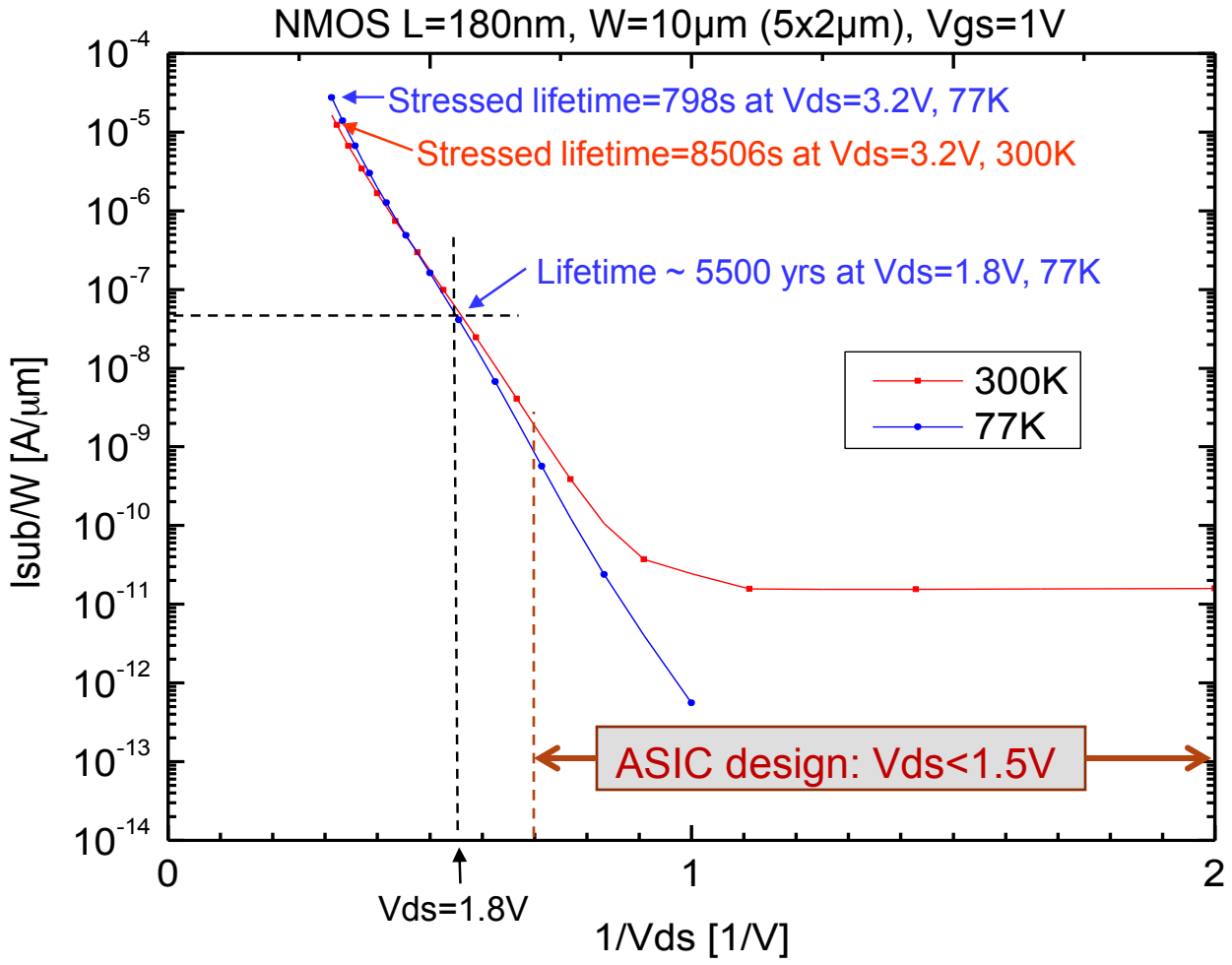


Fig.3. NMOS L=180nm, W=10μm (5x2μm); nominal core voltage 1.8V.
The projected lifetime at 300K is ~ an order of magnitude longer than at 77K.
Reducing V_{ds} at 77K by ~ 6% makes the lifetime equal to that at 300K.

Measurement Type II: Substrate current I_{sub} *vs* $1/V_{ds}$



- *Note that lifetime:*

$$\tau \propto I_{sub}^{-3}$$

Fig.4. *One order of magnitude in substrate current* I_{sub} corresponds to *three orders of magnitude in lifetime*

Analog ASIC for DUNE: I_{sub} and $1/V_{ds}$ distribution for all transistors (TSMC 180nm, 1.8V node)

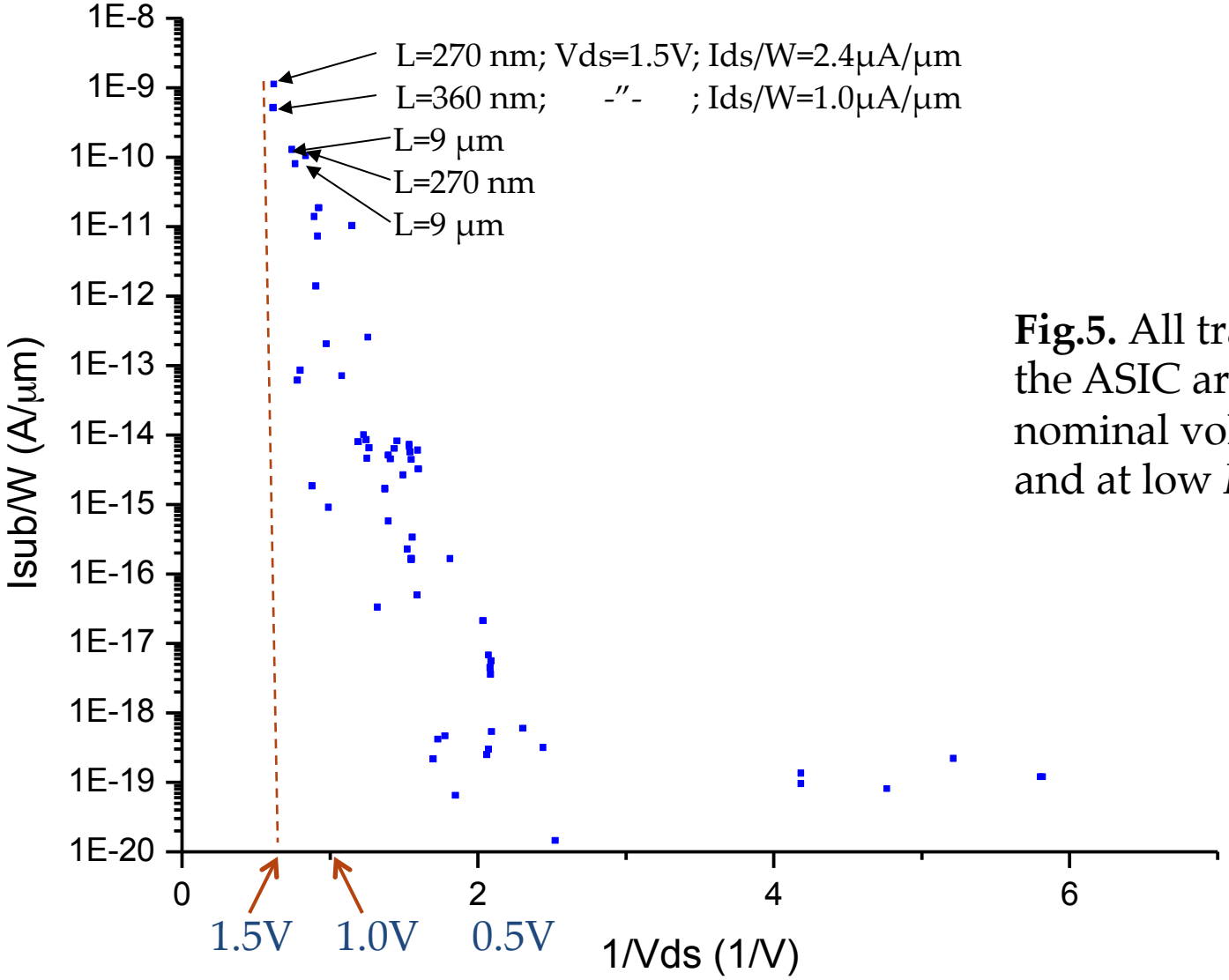


Fig.5. All transistors in the ASIC are well below nominal voltage of 1.8V and at low I_{sub}

Designing CMOS for low power = long lifetime

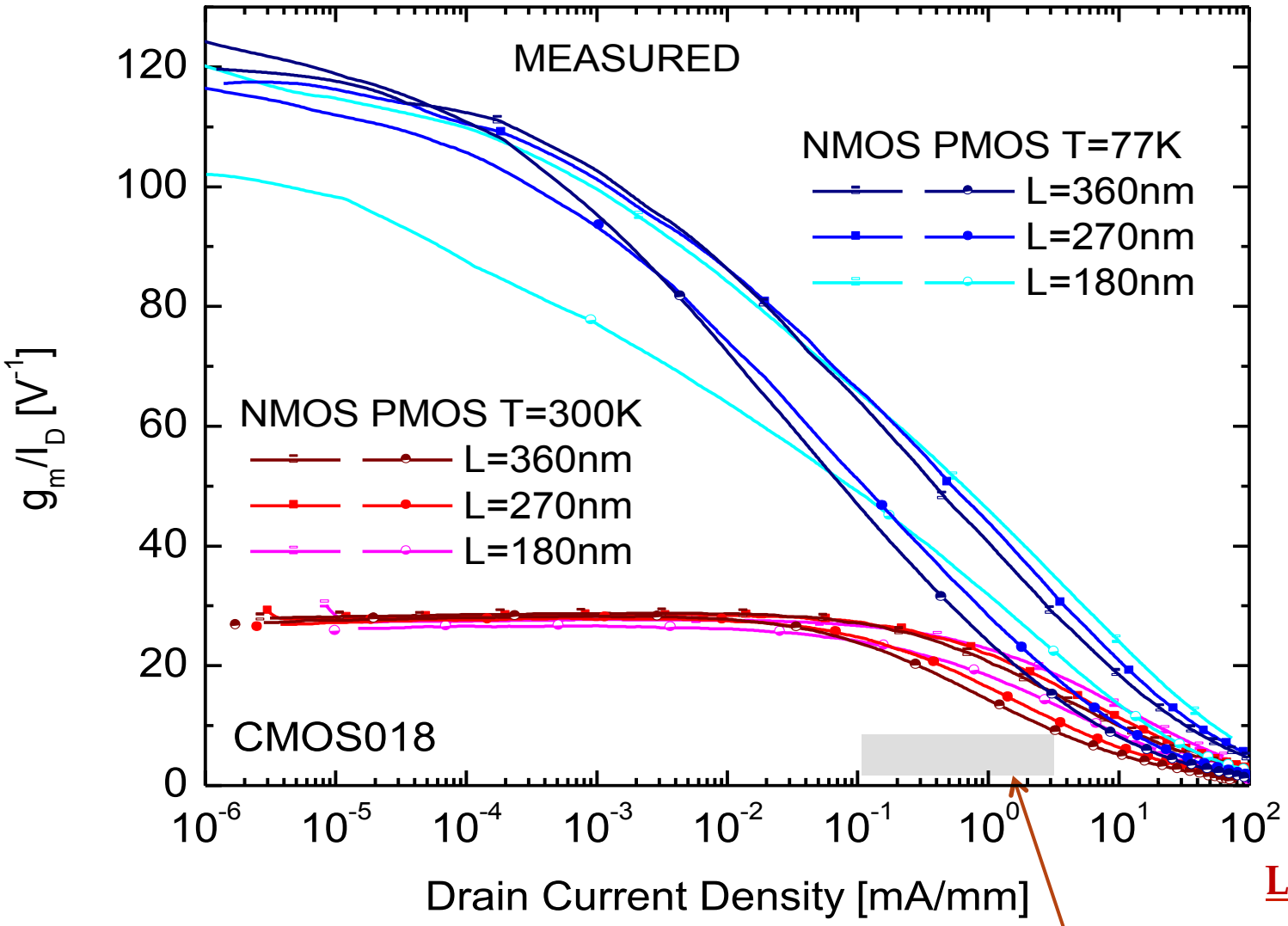


Fig.6.

Design region (approx.) for *low power* and *long lifetime* at 77K (moderate inversion)

Life time testing (stress) region (V_{ds}>1.8V)

NMOS in *dc* operation: Summary (1)

- Stress tests on 180nm TSMC NMOS are in agreement with the literature ***confirming (i) the relation between the lifetime and the substrate current and (ii) that the substrate current can be used as a monitor of hot-electron effects*****.** The dominant effect being interface state generation.

- ***The lifetime at low temperatures is limited by a predictable and a very gradual degradation (aging) mechanism which can be controlled***. Therefore it does not fall under the usual definition of device reliability (failures occurring randomly in time with some probability).

- The criterion for defining the end of a useful device life due to hot-electron effects is arbitrary, given a very gradual ($\Delta g_m \propto t^{1/2}$, *or* $\log t$) degradation process. As long as any chosen criterion for a device parameter change is applied consistently in the stress measurements, the results should follow the basic power law relation, Eqs. (3) or (4). ***The fit of the measurement points to the exponent a≈3 may serve as a consistency check*****.**

- The predicted (extrapolated) lifetime for this particular technology under moderate operating conditions appears to be very long, Fig.3. Given the result of several thousand years at 77K (although shorter than at 300K), even at the nominal core voltage V_{ds}=1.8V, one may question the extrapolation based on a few - what appear closely spaced - stress measurement points.

NMOS in *dc* operation: Summary (2)

- Another way to approach the ***lifetime extrapolation*** is ***by measurement of the substrate current*** as a function of the drain-source voltage V_{ds}. Starting from the highest stress point at V_{ds}=3.2V, I_{sub} is plotted down until it becomes difficult to measure, Fig. 4. (I_{sub} at 300K bottoms out at a thermal component which is negligible at 77K). Since the substrate (impact ionization) current is a measure of hot-electron effects, we can now be confident that we are extending the lifetime by reducing V_{ds}. With the knowledge of the substrate current over the whole V_{ds} range, the lifetime extrapolated to V_{ds}=1.8V in this way would be ~5500 years, in the same ballpark as in Fig. 3.

- It appears that, at least for this technology, the deep submicron region is not as forbidding at 77K as feared. From the literature [2] and from our results two opposite impressions can be formed: a) the lifetime at 77K is an order of magnitude shorter than at 300K – this may be of great concern; b) *the lifetime at 77K equal to that at 300K is achieved by reducing V_{ds} by less than 10%.*

- The latter is equivalent to recognizing that as the device properties are significantly improved at 77K, in part due to increased electron mean free path (MFP) and mobility, the nominal *drain-source voltage has to be scaled down*, to keep the product of MFP and the electric field constant.

NMOS in *dc* operation: Summary (3)

- A detailed picture of the interaction between hot-electrons and the gate-drain region under any potential stress conditions (high V_{ds} *combined with high* I_{ds} *and* L_{min}) is more involved than presented here. However, it is clear from the basics presented and the measurement results that ***the best approach for electronics to be operated in LAr is to stay away from the impact ionization region as much as possible*****,** which appears straightforward for this technology node (180nm).

- The transistors in the analog ASIC are at drain-source voltages well below the nominal 1.8V, in the region of very low substrate current, which is the best assurance of a very long lifetime. In addition, they operate at reduced drain current density, Figs. 5 and 6, as dictated by the low power design, which further reduces the substrate current. Thus ***the low power design provides an additional margin to an already long projected lifetime.***

- DUNE will be able to rely on four mainstream CMOS or BiCMOS processes (**TSMC 180nm** studied at BNL , with a tested ASIC prototype for MicroBooNE, **IBM** studied at Georgia Tech, and **Global Foundries 130nm and TSMC 65 nm** studied at FNAL)

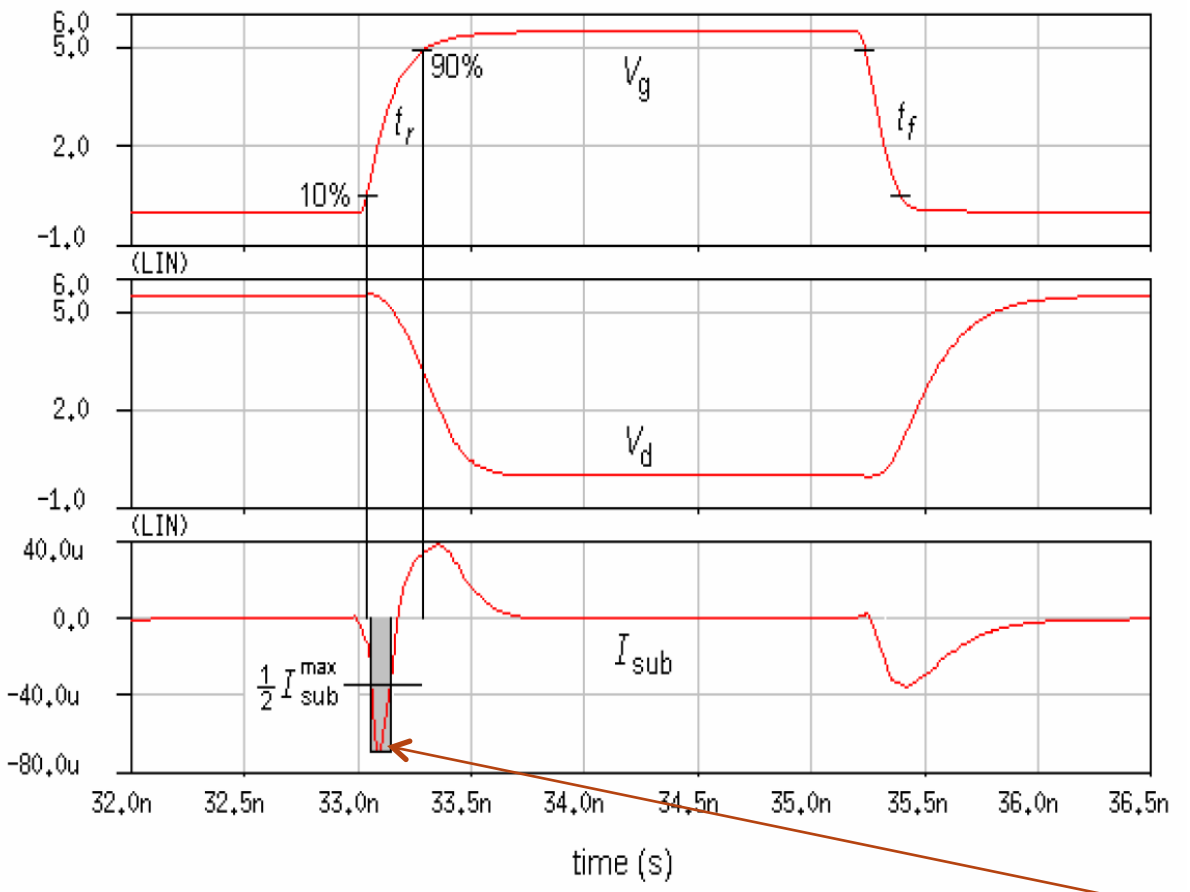
CMOS in AC operation: Logic circuits and FPGAs

- It has been long established (1994) that ***ac*** and ***dc*** hot-carrier induced degradation is the same if the ***effective stress time*** is taken into account. This quasi-static model, confirmed recently (2006) considers the ***ac*** *stress as a series of short* ***dc*** *stresses strung together*

- The lifetime of a logic circuit driven at a clock frequency can be related to the lifetime of the NMOS transistor under continuous ***ac*** operation in terms of the ratio of the effective stress time during a change of state and the clock period. Thus the *Lifetime of digital circuits (**ac** operation) is extended by the inverse duty factor* $4/(f_{clock}t_{rise})$ *compared to **dc** operation.* This factor is large (>100) for deep submicron technology and clock frequencies needed for TPC readout.

- Design guidelines for digital circuits and FPGAs: *Keep the inverse duty factor high*. As an additional conservative measure, reduce V_{ds} by 10%, adding an order of magnitude margin to the lifetime.

Effective Stress Time is a small fraction of the Clock Cycle:



$$\left[\frac{ac\ stress\ time}{dc\ stress\ time}\right] \approx \left(f_{clock} t_{rise}\right)/4$$

Standard method for accelerated stress testing of FPGAs: ***Observe ring oscillator frequency under severe Vds stress.***

(Degradation of Ids leads to increased rise (propagation) time and reduced ring oscillator frequency.)

Hot-carrier induced degradation occurs only when the *substrate current* is high, i.e., nominal Vds and high Ids.

Cold Electronics Development

- Cold electronics installed directly on the detector electrodes is critical to make possible giant LAr TPCs and improve signal to noise ratio
- CMOS at Low Temperature
  - Started from .18um CMOS technology with only 300K models for analog front end; parameters extracted at 77K
  - CMOS found functioning at cryogenic temperature with *increased* gain (g_m/I_{ds}) and *lower* noise
- Development of Readout Electronics for LAr TPC
  - We have accumulated *~3,500 chip•immersions* of analog FE ASIC in LN_2 without any failures due to thermal contraction/expansion
  - ADC characterization test and cold FPGA lifetime study are being conducted
  - Analog FE ASIC + ADC ASIC + Cold FPGA will be used to equip the DUNE 35 Ton and SBND LAr TPC

Cold Electronics Development

- R&D of CMOS cold electronics started in 2008
  - Analog FE ASIC was the first one developed, following by ADC ASIC development, studies of cold regulator and FPGA etc.
  - In parallel, studies of CMOS lifetime and reliability at 77 K have been conducted
    - *"LAr TPC Electronics CMOS Lifetime at 300K and 77K and Reliability under Thermal Cycling," IEEE Trans. on NSci, 60, No: 6, Part: 2, p4737(2013)*
- Cold electronics design is performed jointly with the TPC electrode design for different experiments
  - As a part of our future program, finer segmentation electrodes and readout will be explored (planar anodes instead of wires)

Neutrino Experiments using Cold Electronics

- Projects using, and potentially will be using cold electronics:
  - MicroBooNE
  - ARGONETUBE
  - LArIAT
  - DUNE 35 Ton
  - ICARUS 50l TPC at CERN
  - SBND
  - DUNE Single Phase Test at CERN
  - DUNE Far Detector
- ***R&D on cold electronics started before most of these projects were anticipated or in existence***

Backup Slides

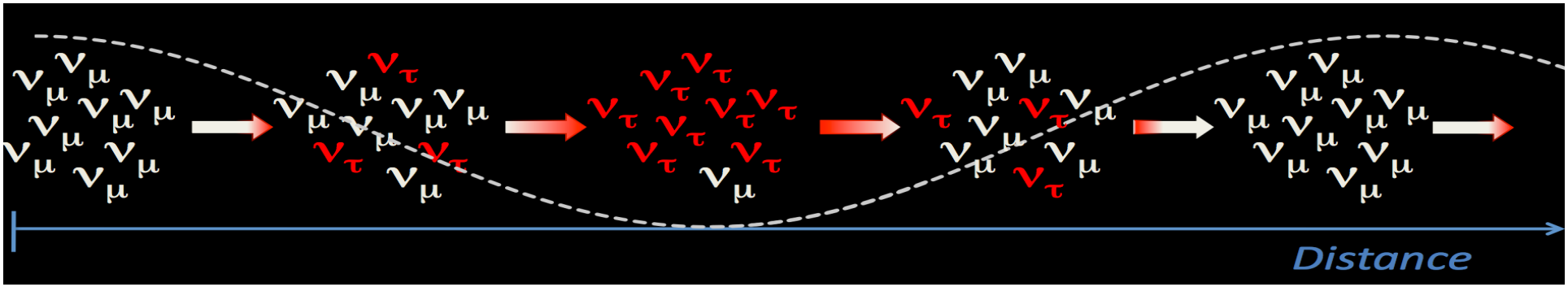
Neutrino Oscillations: Simplified Two Neutrino Case

$$P\left(\nu_\alpha \rightarrow \nu_\beta\right) = \sin^2 2\theta_{ij} * \sin^2\left(1.27\Delta m^2_{ij}\frac{L}{E}\right)$$

The mixing angle, θ, determines the amplitude of the oscillation

Δm^2 determines the shape of the oscillation as a function of L (or E)

- Oscillation between flavors governed by a frequency (Δm^2) and an amplitude ($\sin^2 2\theta$)
- Observed oscillation depends on the initial ν energy (E) and the distance traveled (L)



Three Flavor Mixing

- Generalize two flavor mixing in a similar fashion as CKM
  - Three mixing angles
  - One complex phase
  - Three mass differences

$$\begin{pmatrix} \nu_e \\ \nu_\mu \\ \nu_\tau \end{pmatrix} = \begin{pmatrix} 1 & 0 & 0 \\ 0 & \cos\theta_{23} & \sin\theta_{23} \\ 0 & -\sin\theta_{23} & \cos\theta_{23} \end{pmatrix} \begin{pmatrix} \cos\theta_{13} & 0 & \sin\theta_{13}e^{-i\delta} \\ 0 & 1 & 0 \\ -\sin\theta_{13}e^{i\delta} & 0 & \cos\theta_{13} \end{pmatrix} \begin{pmatrix} \cos\theta_{12} & \sin\theta_{12} & 0 \\ -\sin\theta_{12} & \cos\theta_{12} & 0 \\ 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} \nu_1 \\ \nu_2 \\ \nu_3 \end{pmatrix}$$

Three Flavor Mixing: Experiment

- Mixing experimentally established among three flavors at two L/E scales:

  Atmospheric & Long Baseline Accelerator (L/E ~ 500 km/GeV)

$$\Delta m^2_{atm} = 2.43^{+0.13}_{-0.13} \times 10^{-3}\text{eV}^2$$

  Solar & Long Baseline Reactor Experiments (L/E ~ 15,000 km/GeV)

$$\Delta m^2_{sol} = 7.59^{+0.20}_{-0.21} \times 10^{-5}\text{eV}^2$$

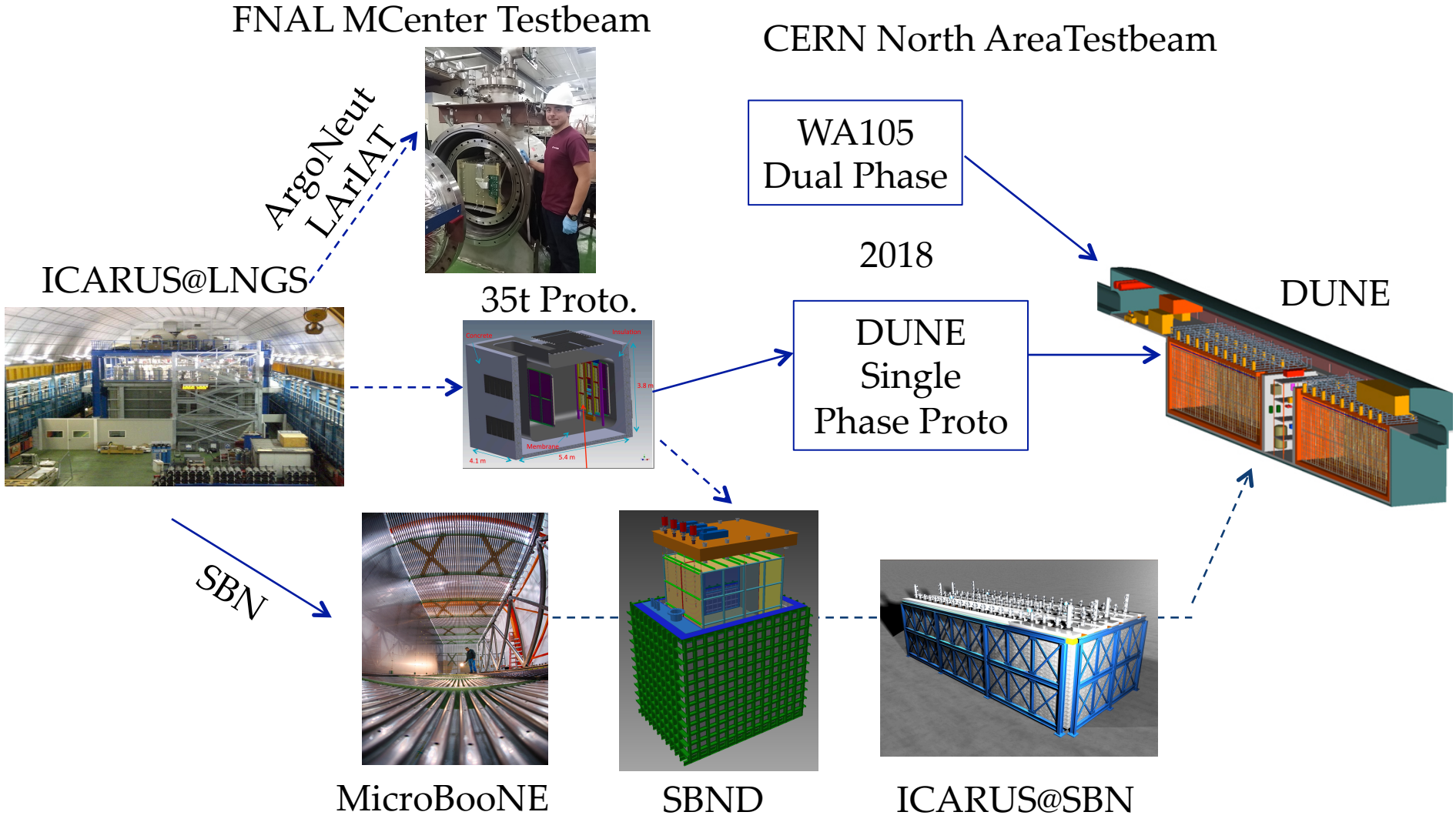
Table 14.1: Sensitivity of different oscillation experiments.

	Source	Type of ν	$\overline{E}$[MeV]	L[km]	min(Δm^2)[eV^2]
	Reactor	$\overline{\nu}_e$	~ 1	1	$\sim 10^{-3}$
Long-baseline	Reactor	$\overline{\nu}_e$	~ 1	100	$\sim 10^{-5}$
	Accelerator	$\nu_\mu, \overline{\nu}_\mu$	$\sim 10^3$	1	~ 1
Long-baseline	Accelerator	$\nu_\mu, \overline{\nu}_\mu$	$\sim 10^3$	1000	$\sim 10^{-3}$
	Atmospheric ν's	$\nu_{\mu,e}, \overline{\nu}_{\mu,e}$	$\sim 10^3$	10^4	$\sim 10^{-4}$
	Sun	ν_e	~ 1	1.5×10^8	$\sim 10^{-11}$

PDG - http://pdg.lbl.gov/2014/reviews/rpp2014-rev-neutrino-mixing.pdf

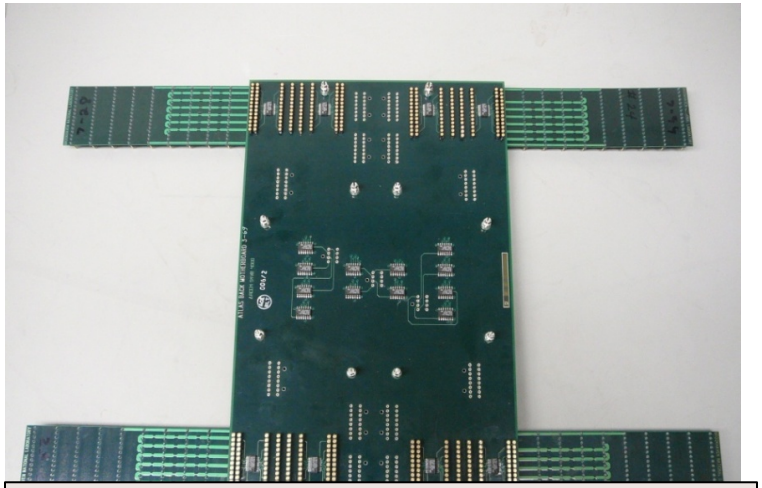
LAr TPC Technology Paths to DUNE

Parallel development: testbeam devices and SBN detectors

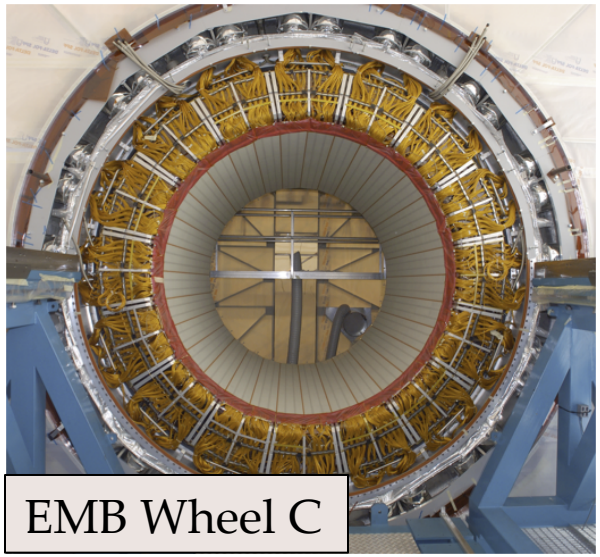


Reliability of Cold Electronics *wrt* *thermal contraction-expansion* PCB and Cold Electronics in ATLAS

- ATLAS LAr Calorimeter
  - 182,468 readout channels
- EM Barrel Mother Board and Summing Board
  - EMB has ~110,000 detector channels read out by 896 128-ch FEBs
  - 960 Mother Boards, 15 different types
  - 7,168 Summing Boards, 4 different types
  - 20,480 resistor network chips on Mother Boards, 5 different types
  - ~110,000 protection diodes on MB/SB assembly
- EM Barrel Calorimeter has been cooled down since 2004
  - Operation: 11 years so far
  - MB/SB will remain in operation without upgrade for HL-LHC
- 'Inoperative' channels <0.5%, as of 2015 (outside the cryostat)
- Dead channels in the cryostat ~0.02% since 2008



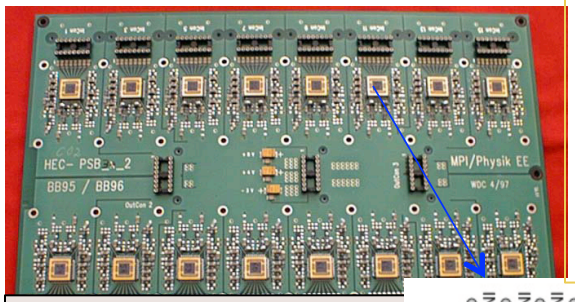
EMB Mid/Back MB+SB Assembly



EMB Wheel C

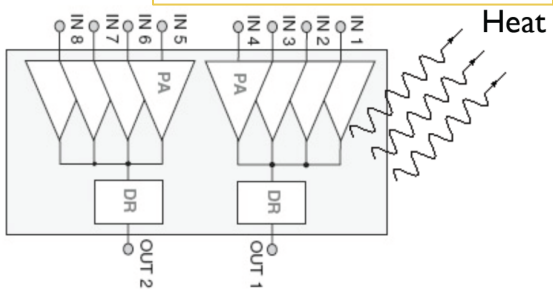
PCB and Cold Electronics in ATLAS

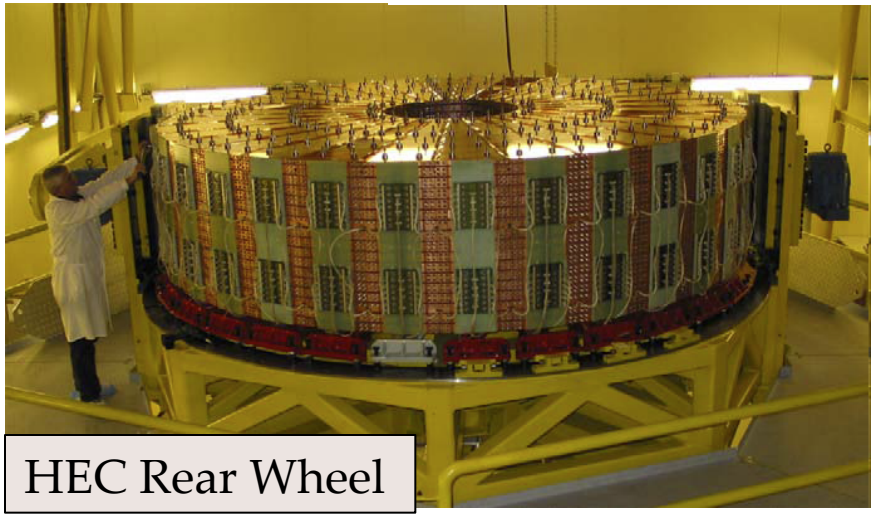
- ATLAS LAr Calorimeter HEC preamplifier ASIC based on GaAs
  - HEC has 5,632 detector channels read out by 48 128-ch FEBs
  - 320 PSBs installed on HEC wheels, 5 different types
  - Total 35,840 cold preamplifier channels, 8,960 summing amp. Each preamplifier ASIC has 8 channels
- HEC Calorimeter has been cooled down since 2005
  - In 2005 first commission in cold: 5 deal channels (< 0.1%). Nome due to preamps. Two due to sum amp (already at warm)
  - In 2015 still 5 dead channels: stable after 10 years of operation
  - HEC cold electronics will remain in operation without upgrade for HL-LHC



HEC Type C PSB

GaAs TriQuint QED-A 1um Stable operation at cryogenic temperatures





HEC Rear Wheel

Comparison of warm and cold Preamps (ARGONTUBE)

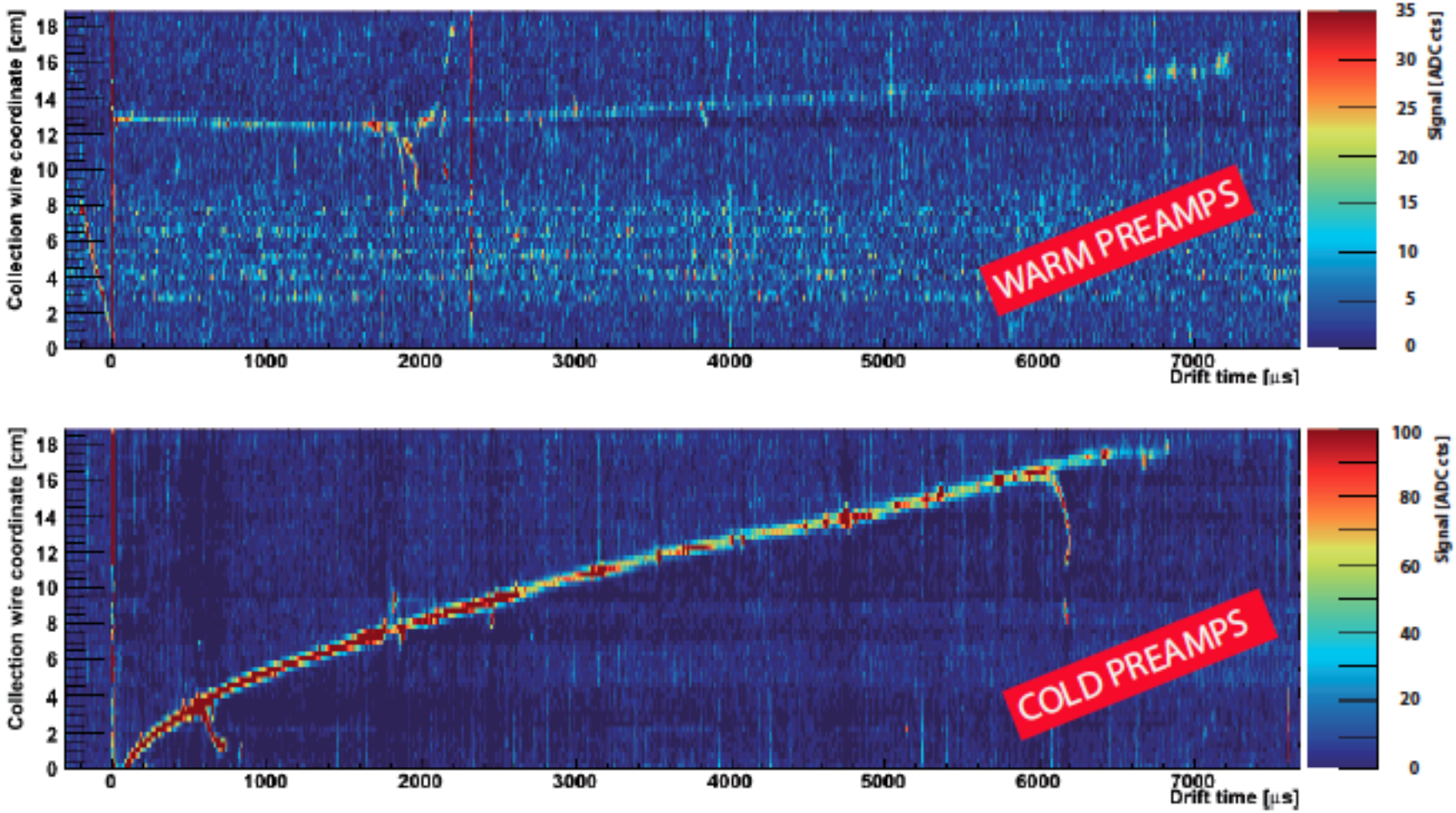


Figure 10: Full length μ track with warm (top) and cold (bottom) preamps.

Comparison of warm and cold Preamps (ARGONTUBE)

- Amount of charge/mm expected from mip

  $\left(\frac{dE}{dX}\right)_{\text{mip}} \approx 0.21\,\text{MeV/mm},\ W_e \approx 23.6\,\text{eV},\ R \approx 0.35 \pm 0.04$ @200V/cm

  $\Rightarrow$ $\mathbf{\frac{\Delta Q}{\Delta x} \approx 8'900\,e/mm}$

- Analyze transversal mip. tracks passing close to the readout plane.
- *RMS noise*

  $N_{\text{warm}} = 1.1 \pm 0.1\,\text{mV},$

  $N_{\text{cold}} = 2.1 \pm 0.1\,\text{mV} \approx 525e^{-}(ENC)$

- *MIP signal*

  $S_{\text{warm}} = 2.8 \pm 0.6\,\text{mV}$

  $S_{\text{cold}} = 33.0 \pm 7.9\,\text{mV} \approx 8'100\,\text{e/mm}$ (corrected for recomb.)

$\Rightarrow$ **Signal to noise ratios**

$S/N_{\text{warm}} = 2.6 \pm 0.6$ $\qquad$ $S/N_{\text{cold}} = 15.7 \pm 3.8$

Stress Test Flow Chart and Layout of test NMOS transistors

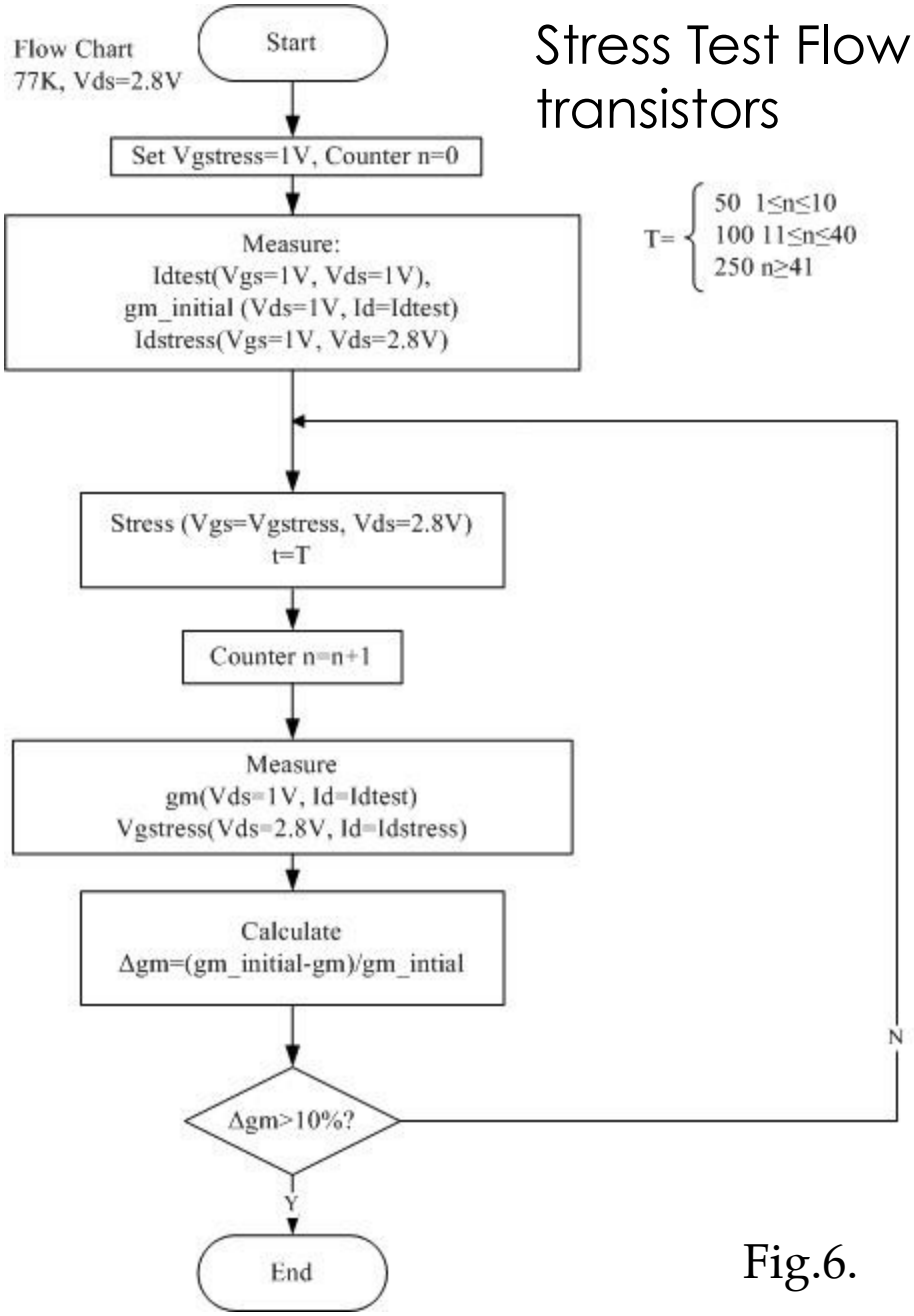
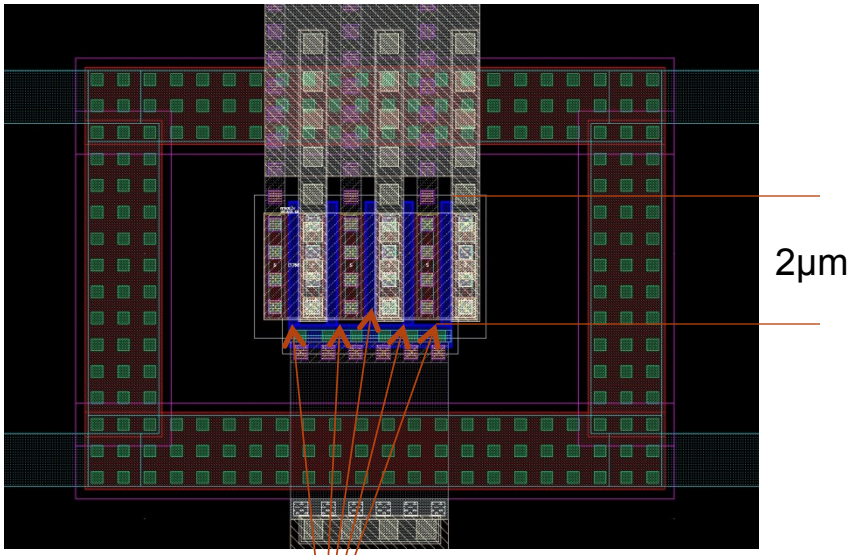


Fig.6.



Test transistors, NMOS L=180nm, W=10μm (5 fingers x 2μm), designed to have negligible IR drop and power dissipation <15mW in stress tests to prevent temperature change due to self-heating.