Instrumentation of Particle Physics Experiments

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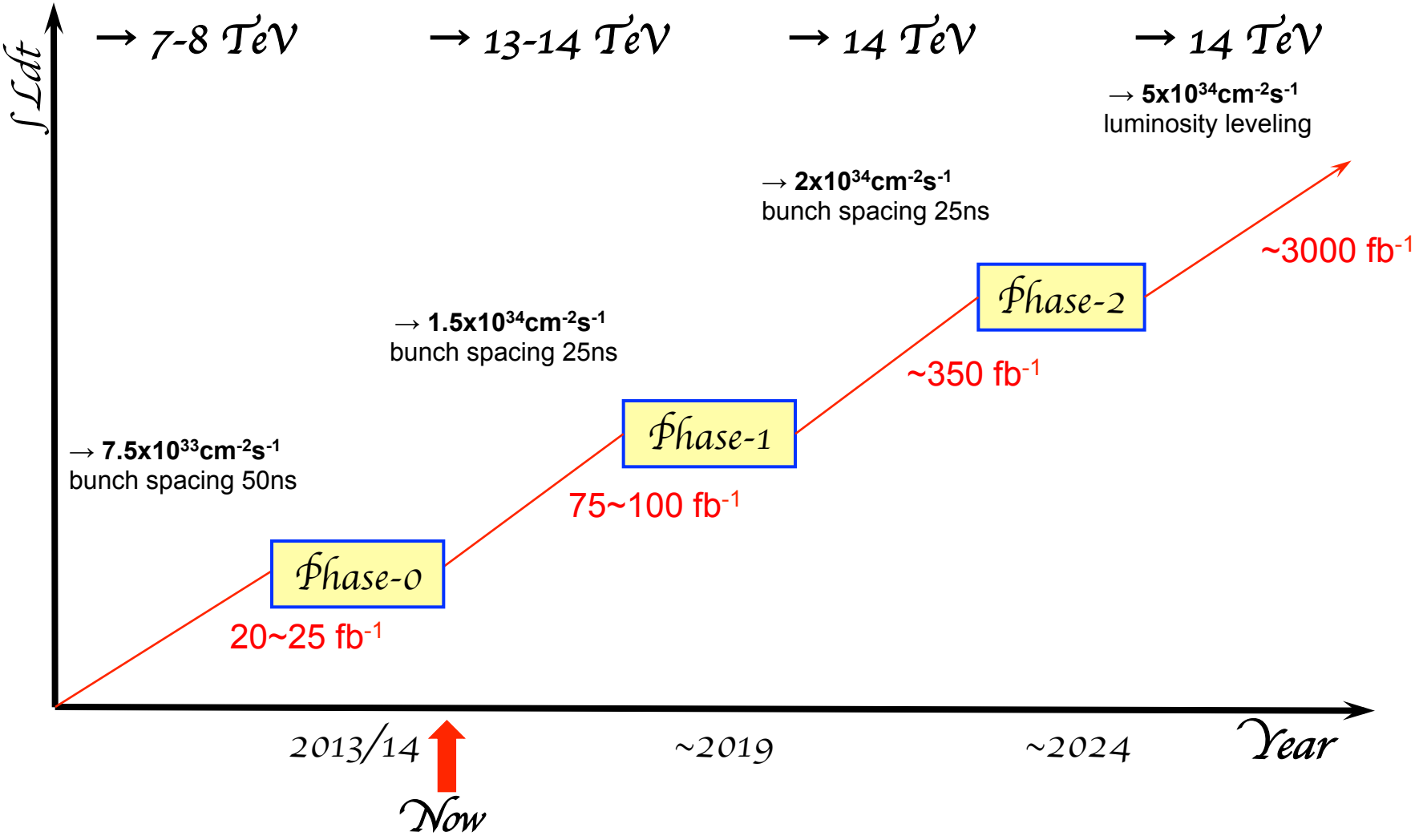
Lecture 3 – LAr Readout Electronics Upgrade

- LHC and ATLAS Upgrade Plan
- Roadmap of LAr Readout Architecture in ATLAS Upgrade
- Electronics Development for Phase-0 Upgrade
- Electronics Development for Phase-I Upgrade
- Electronics R&D for Phase-II Upgrade

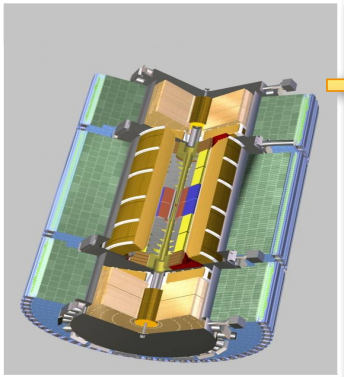
LHC and ATLAS Upgrade Plan

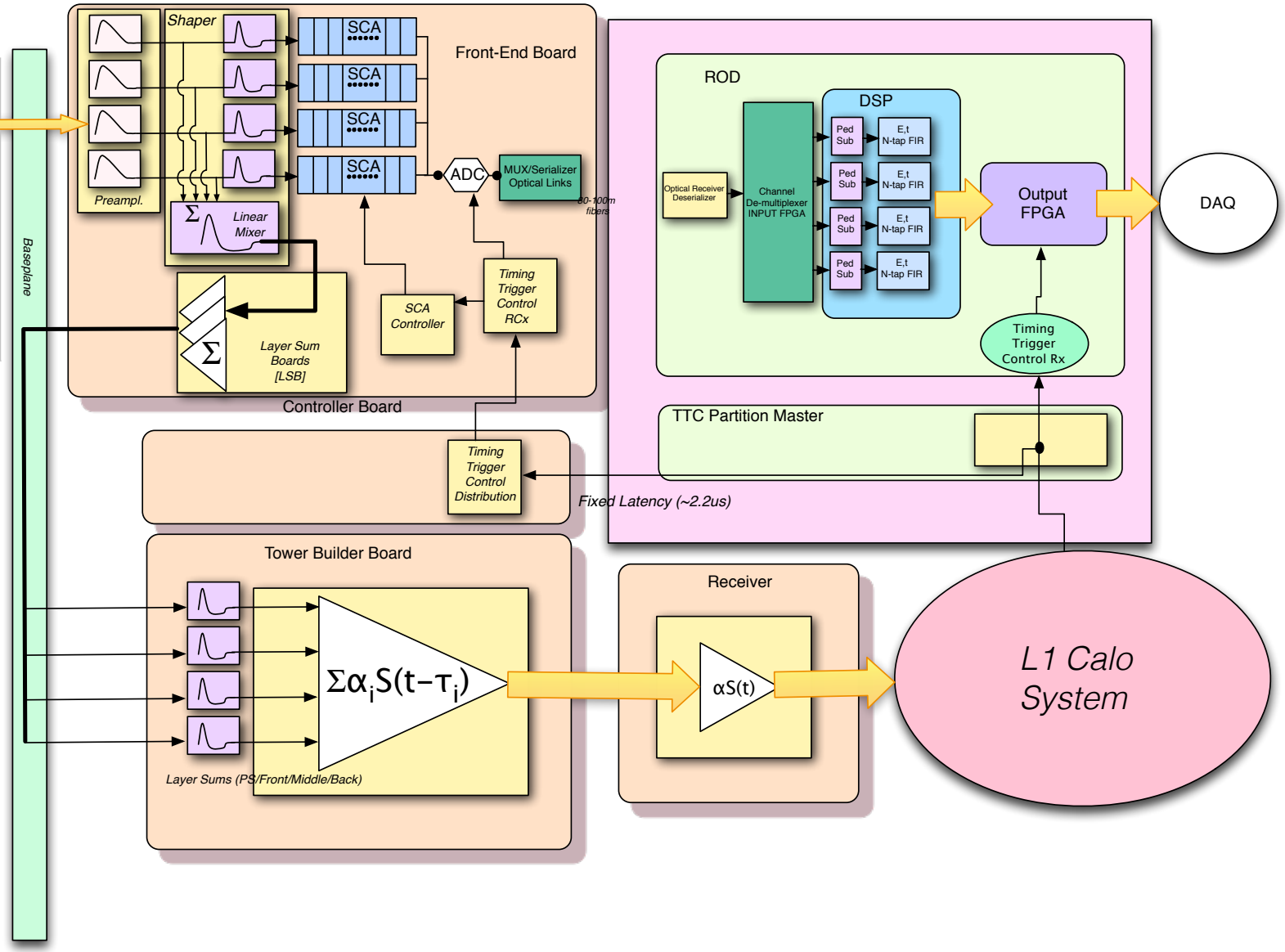


Roadmap of LAr Readout Architecture in ATLAS Upgrade

- Current Readout Architecture
- Readout Architecture in Phase-I Upgrade
- Readout Architecture in Phase-II Upgrade

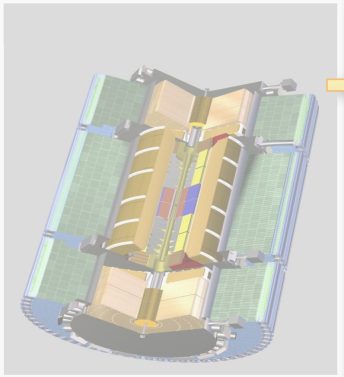
Current LAr Readout Architecture

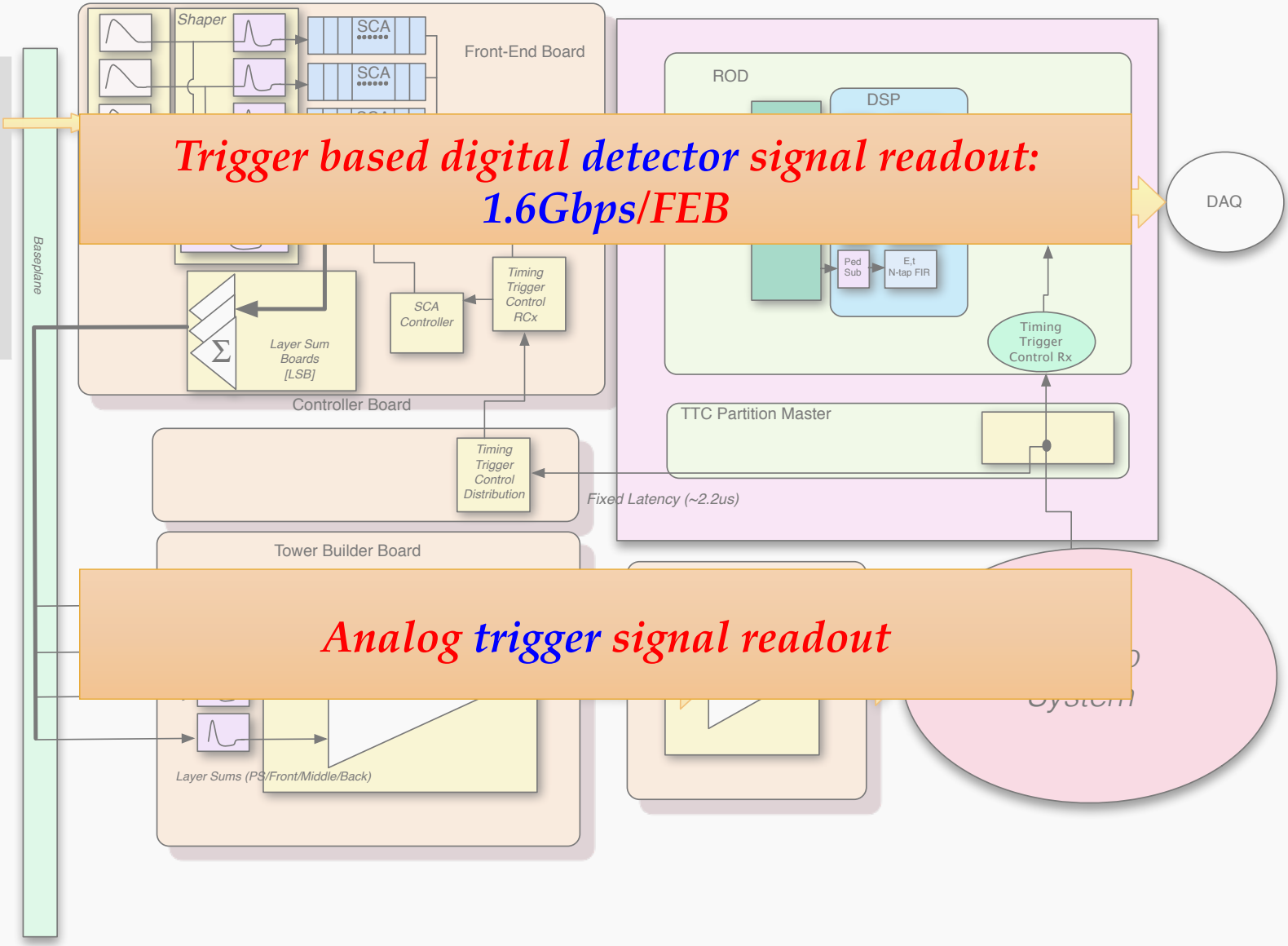


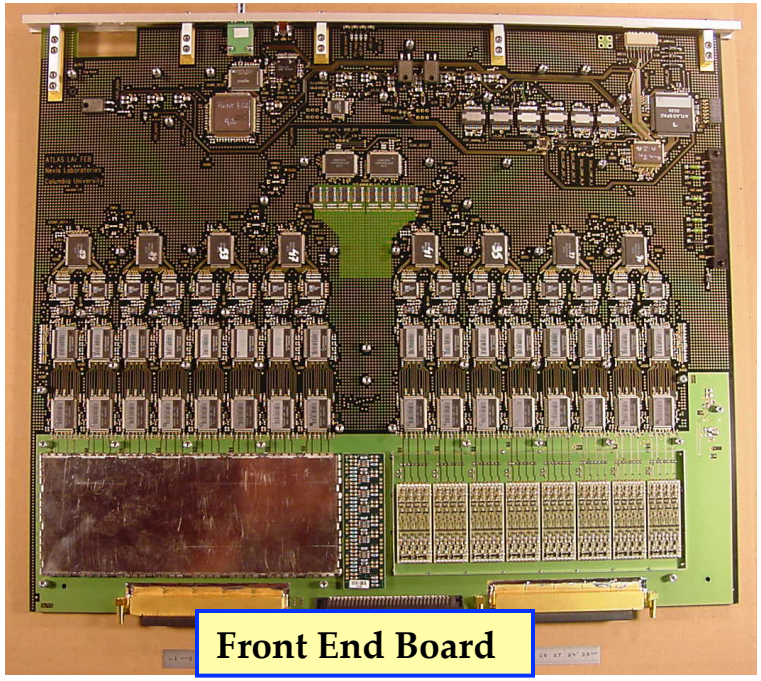


Analog trigger tower signals sent to L1Calo through TBB and Receiver, digitization happens on Pre-processor

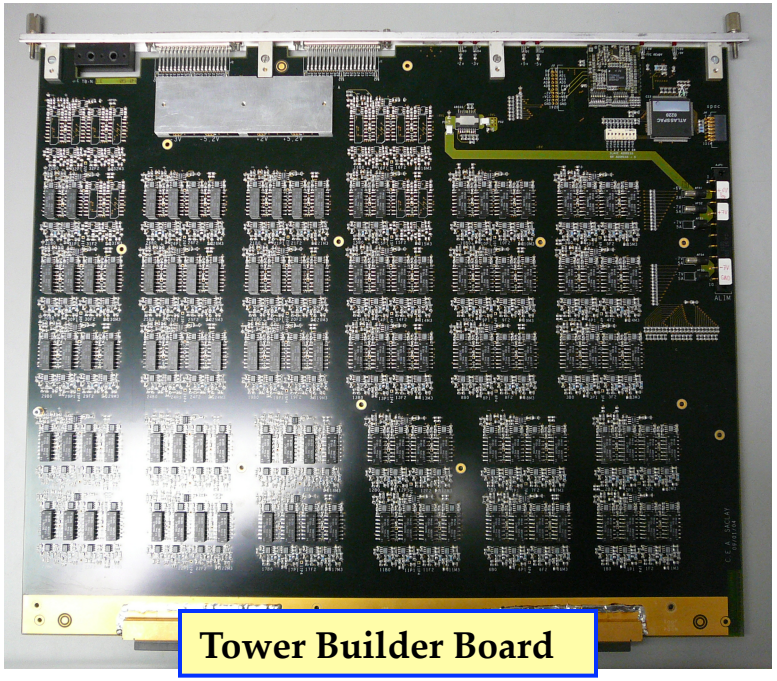
Current LAr Readout Architecture



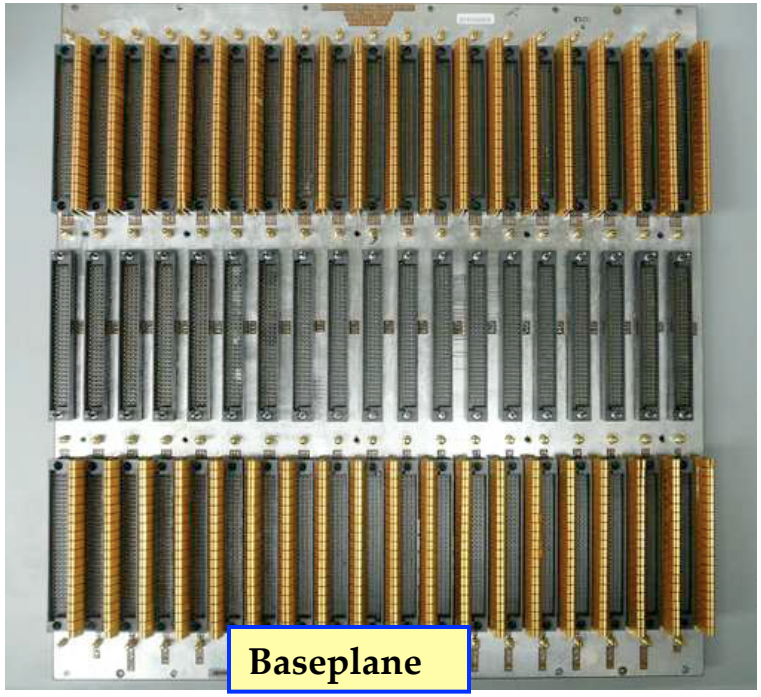




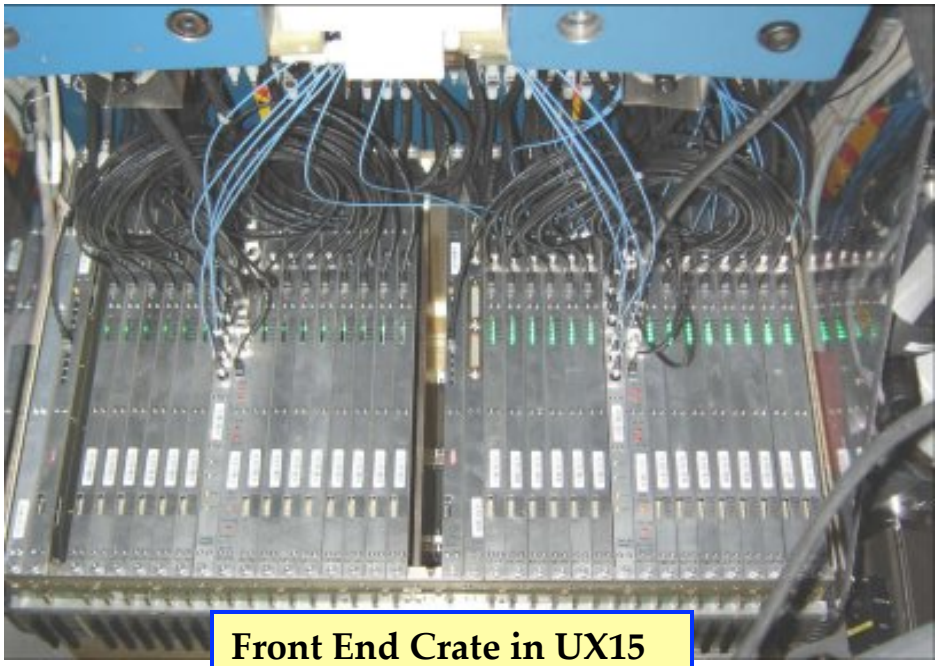
Front End Board



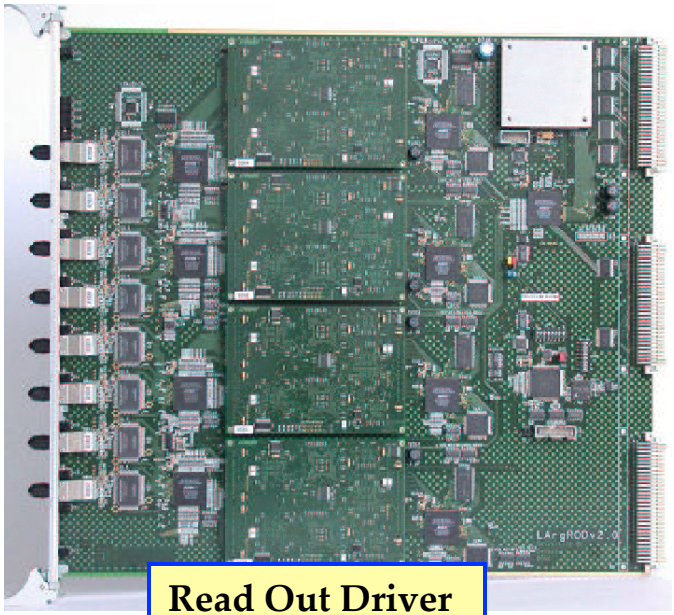
Tower Builder Board



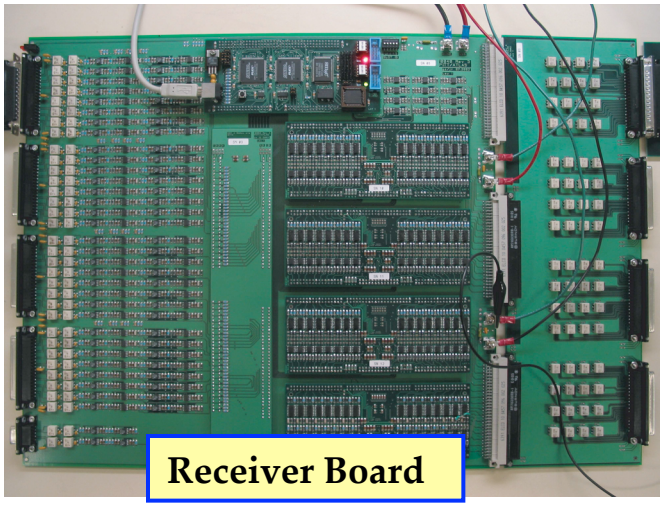
Baseplane



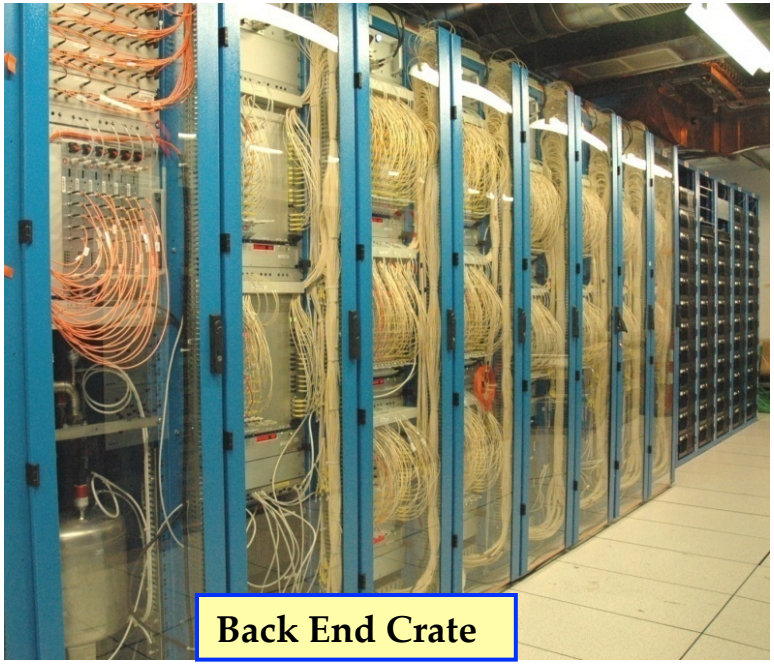
Front End Crate in UX15



Read Out Driver



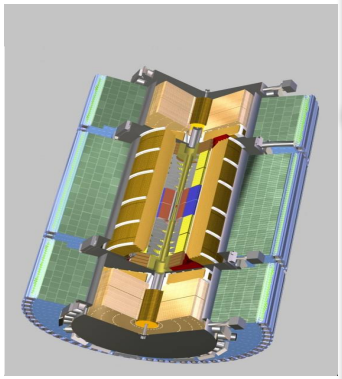
Receiver Board

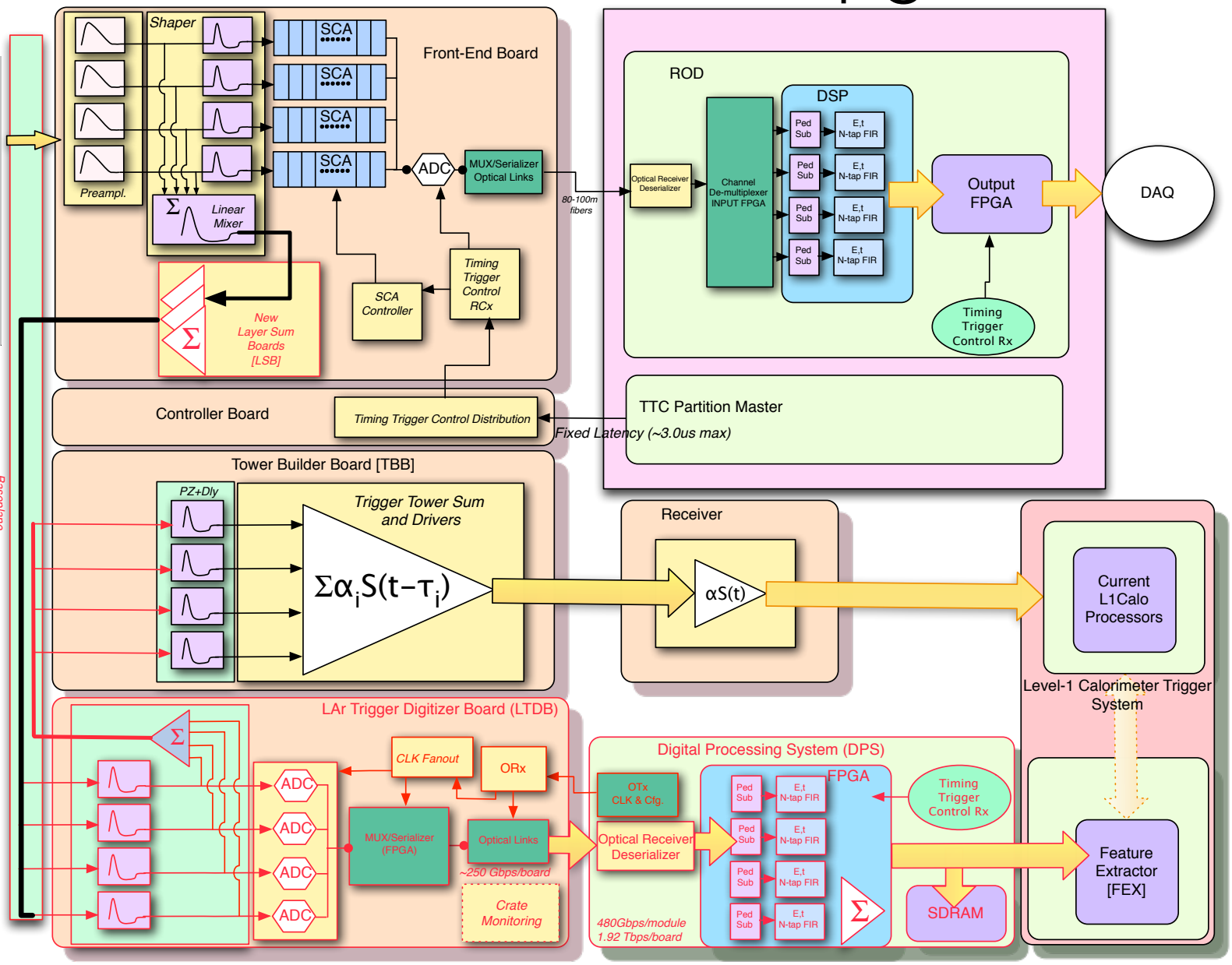


Back End Crate

Cabling from Receiver to L1Calo

Readout Architecture in Phase-I Upgrade



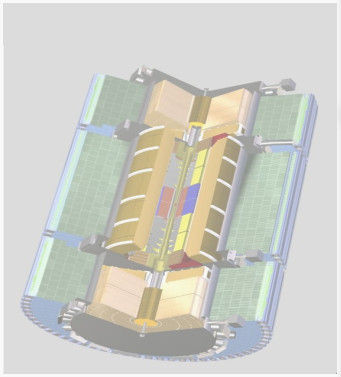


Phase 0: ~0.5k super cells, 1.4x0.4 are on one FEC of the barrel calorimeter

Possible implementation
$\Delta\eta\times\Delta\phi$=0.025x0.1 1st and 2nd layer EM
$\Delta\eta\times\Delta\phi$=0.1x0.1 elsewhere

Phase-1: extend to the full calorimeter trigger readout (~35k channels), L1 trigger using digitized super cells

Readout Architecture in Phase-I Upgrade

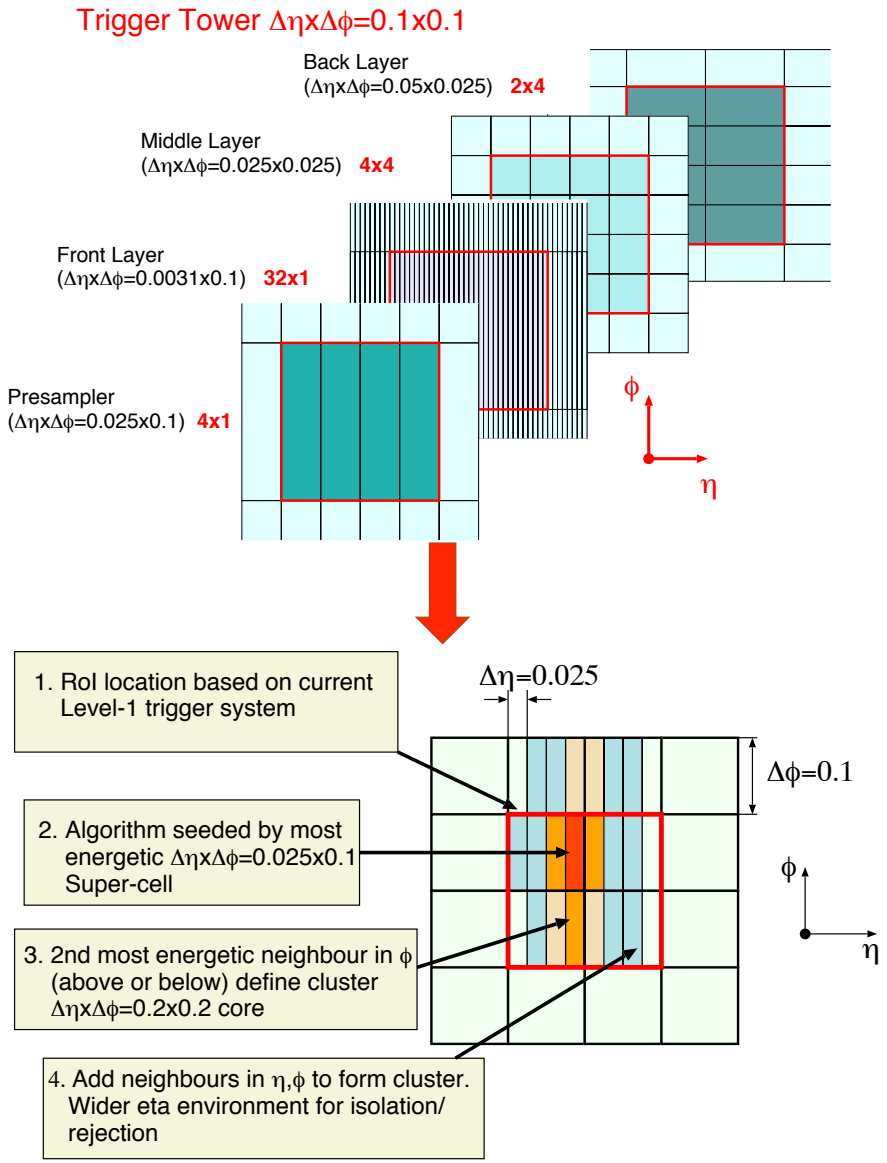


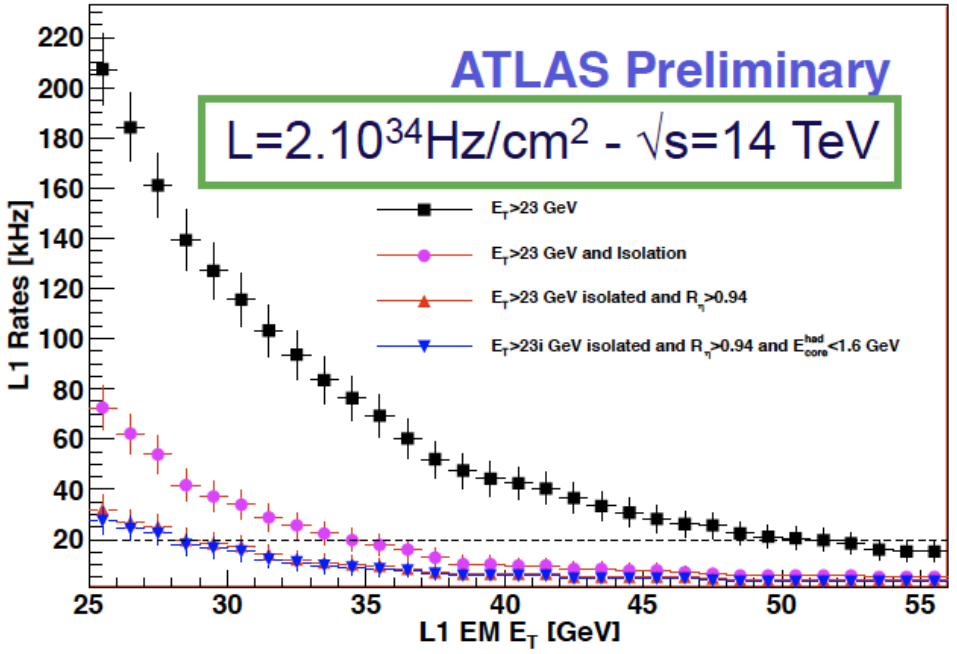
Possible implementation
ΔηxΔφ=0.025x0.1 1st and 2nd layer EM
ΔηxΔφ=0.1x0.1 elsewhere

Trigger based digital detector signal readout: 1.6Gbps/FEB

Analog trigger signal readout & Continuous digital trigger signal readout: ~200Gbps/LTDB

Improvement of L1 Trigger



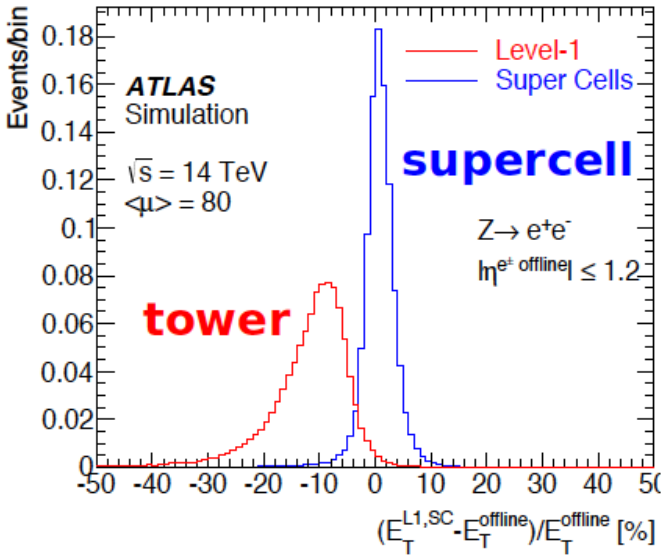


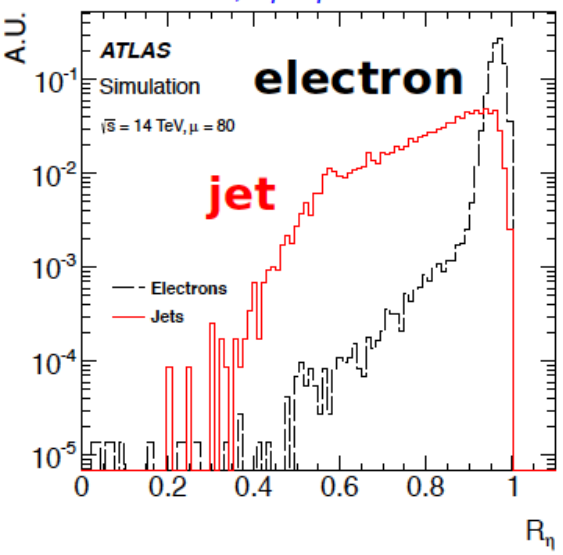
Critical to maintain low threshold for single lepton Level-1 trigger

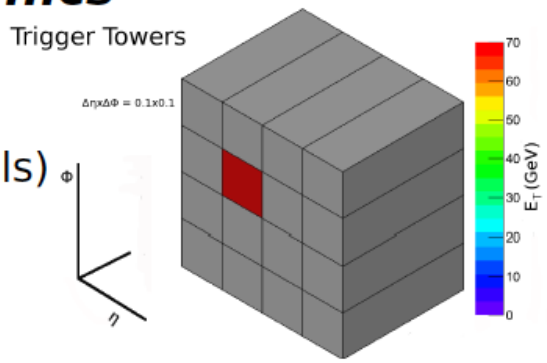
LAr Trigger Segmentation

- ***BNL proposed concept and overall design for Phase-I Upgrade of Liquid Argon calorimeter trigger electronics***
- ***Increased granularity and functionality of LAr calorimeter Level 1 trigger***
  - fine lateral and longitudinal LAr segmentation (supercells)
  - calculate shape information for electrons and taus and improve energy measurement in the trigger readout chain to improve trigger rejection
  - *detailed studies on supercell configuration and electron shower shapes by BNL*

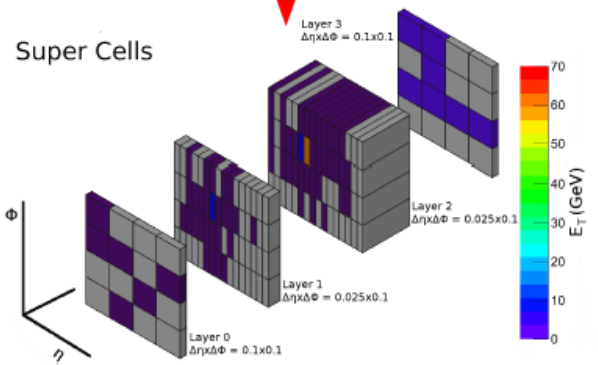
$$R_\eta = \frac{E^{\text{layer 2}}_{T,\Delta\eta\times\Delta\phi=0.075\times0.2}}{E^{\text{layer 2}}_{T,\Delta\eta\times\Delta\phi=0.175\times0.2}}$$



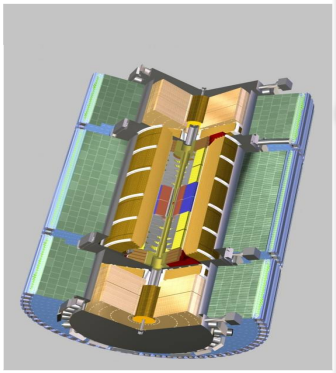




Phase-I Upgrade

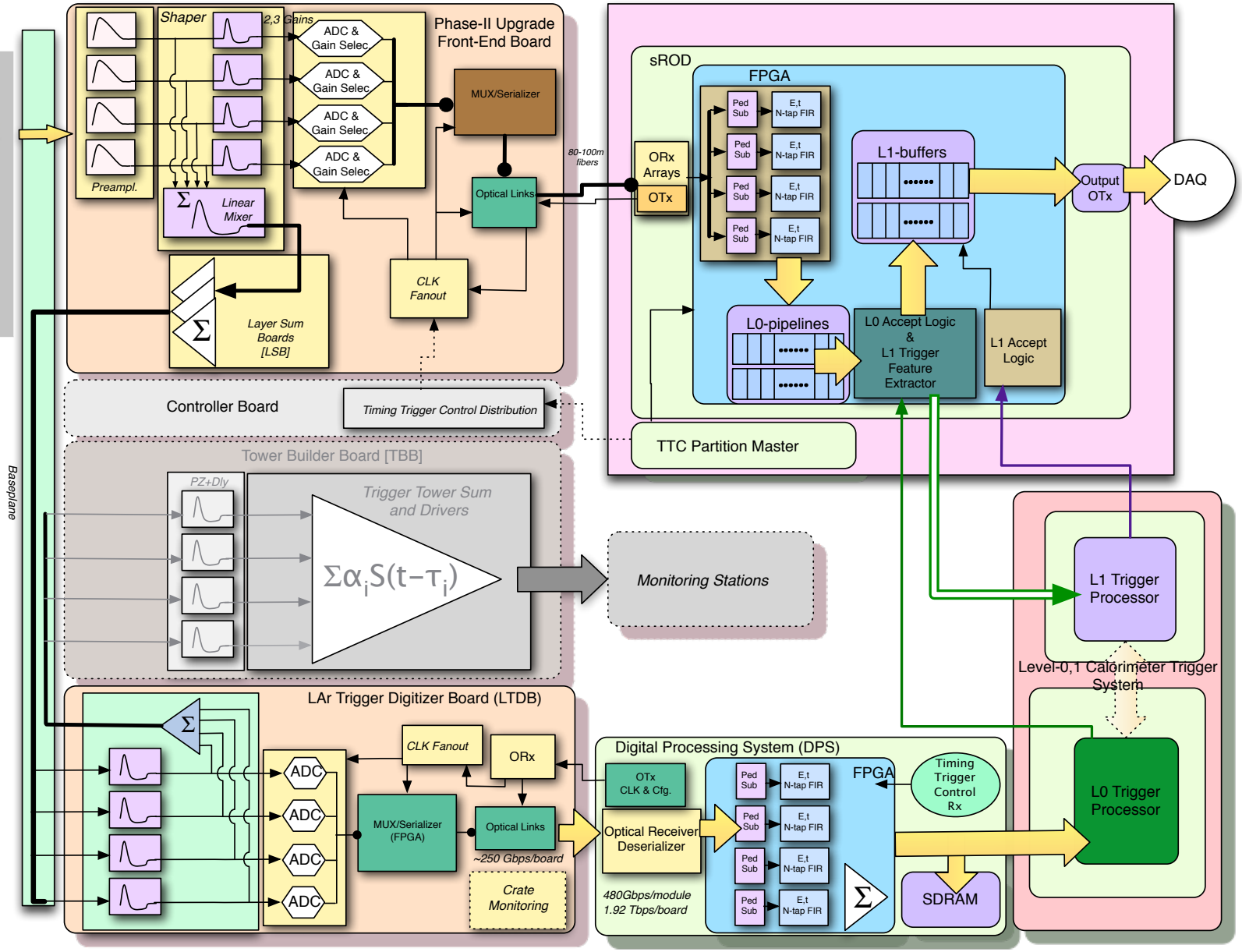


Readout Architecture in Phase-II Upgrade

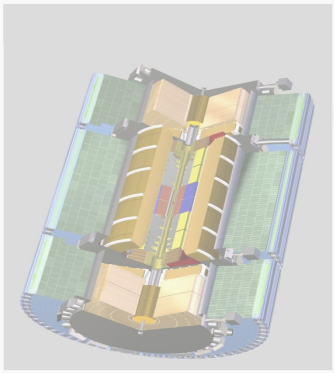


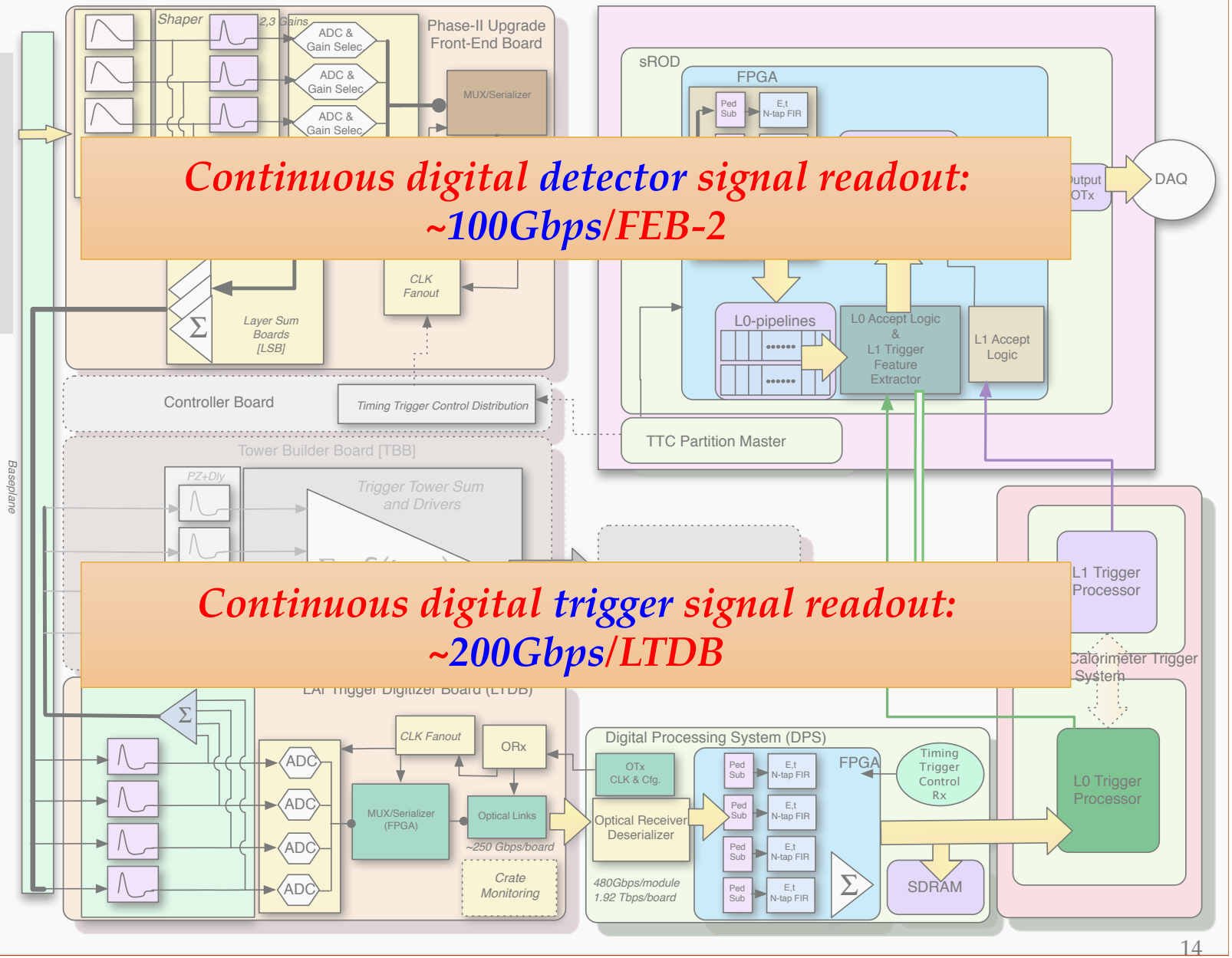
Full calorimeter digital readout (~200k channels)

Calorimeter trigger may evolve into a fast L0 trigger from digitized super cells and a L1 trigger, which uses higher granularity data



Readout Architecture in Phase-II Upgrade





Electronics Development for Phase-0 Upgrade

- LTDB Demonstrator Development
- LDPB Demonstrator Development

Electronics Development for Phase-0 Upgrade

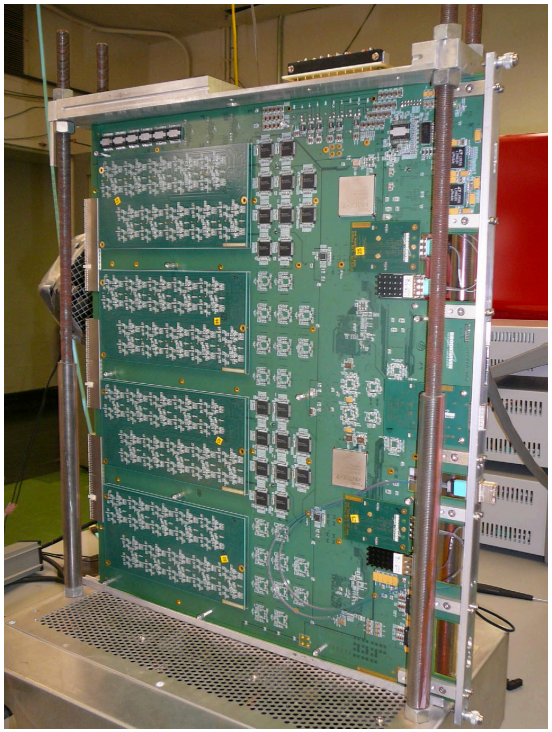
- ATLAS LAr Phase-0 upgrade took place during LHC LS1 (Long Shutdown 1) from 2013 – 2015
- During the LS1, some electronics upgrade has been planned
  - Refurbishing of LV power supplies – ***not to be discussed here***
  - Installation and commissioning in-situ demonstrator
- LAr demonstrator project in Phase-0 upgrade is a pre-cursor of the Phase-I upgrade
  - All demonstrator electronics would be certified with a full lab system tests at the LAr EMF (Electronic Maintenance Facility) at CERN
  - After successful verification, one FEC ($\Delta\eta$ x $\Delta\phi$ = 1.4 x 0.4) with the readout for the increased granularity will be equipped with new demonstrator electronics

Electronics Development for Phase-0 Upgrade

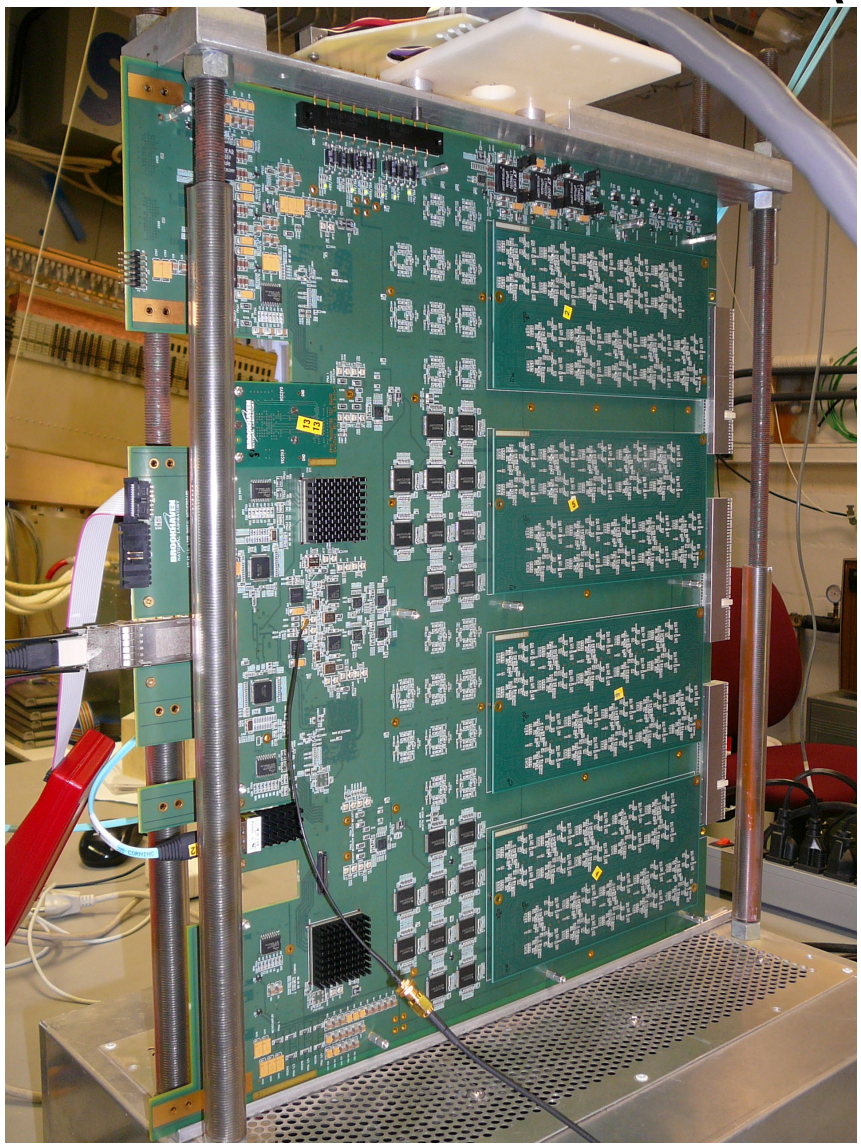
- Motivations of LAr demonstrator project
  - Collect data from the Super Cells and validate energy reconstruction and bunch crossing identification algorithms in FPGAs with the high pileup and saturated pulses occurring in LHC conditions
  - Measure trigger efficiency and jet background rejection using various LDPB filters and selection algorithms deployed in the Feature Extractors
  - Learn about installation and operation of the apparatus in the ATLAS environment, well in advance of LS2, with potential feedback to the final design of the system or its components
  - With the new baseplane and LSBs in place, the LTDB demonstrators can later be replaced by other prototype boards during later winter shutdowns

Electronics Development for Phase-0 Upgrade

- LTDB Demonstrators
  - Two LTDB demonstrators have been developed to study the different architecture of LTDB design
    - Digital mother board with analog mezzanine
    - Analog mother board with digital mezzanine

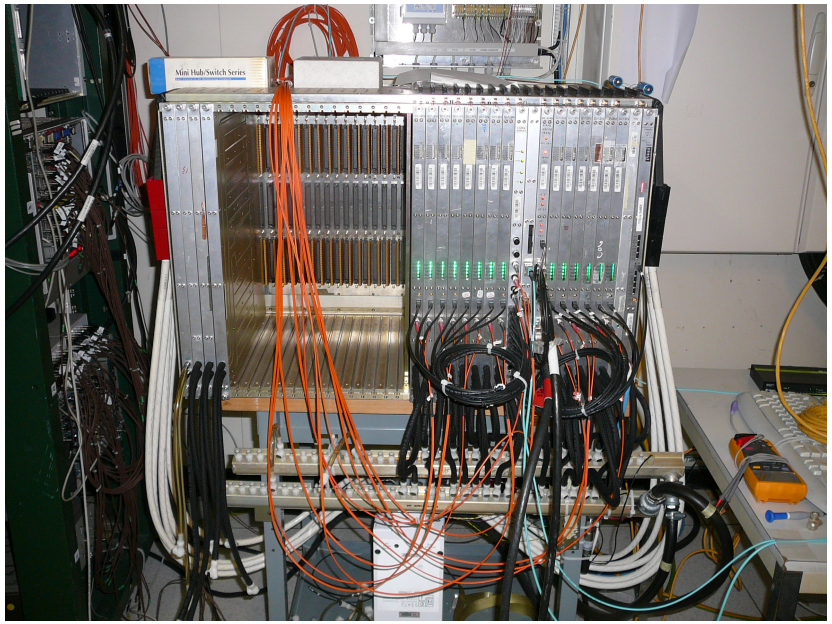


LTDB Demonstrator (1)

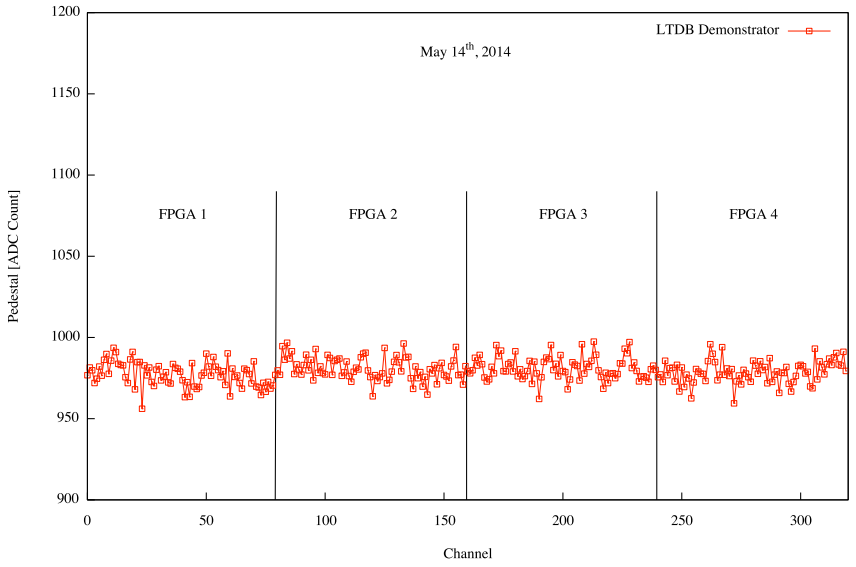


- LTDB is a front-end board to digitize trigger signals on detector
  - High density – 320 super cell signals
  - Board dimension 408.9 mm x 489.0 mm (16.10 in x 19.25 in)
  - High speed digitization – 40 Msps
  - High speed data transmission – 40 optical links running at 5 Gb/s
  - Mixed signal design – analog signal conditioning and digital signal processing
  - Radiation tolerant – radiation qualified components running in ATLAS pit

LTDB Demonstrator (2)

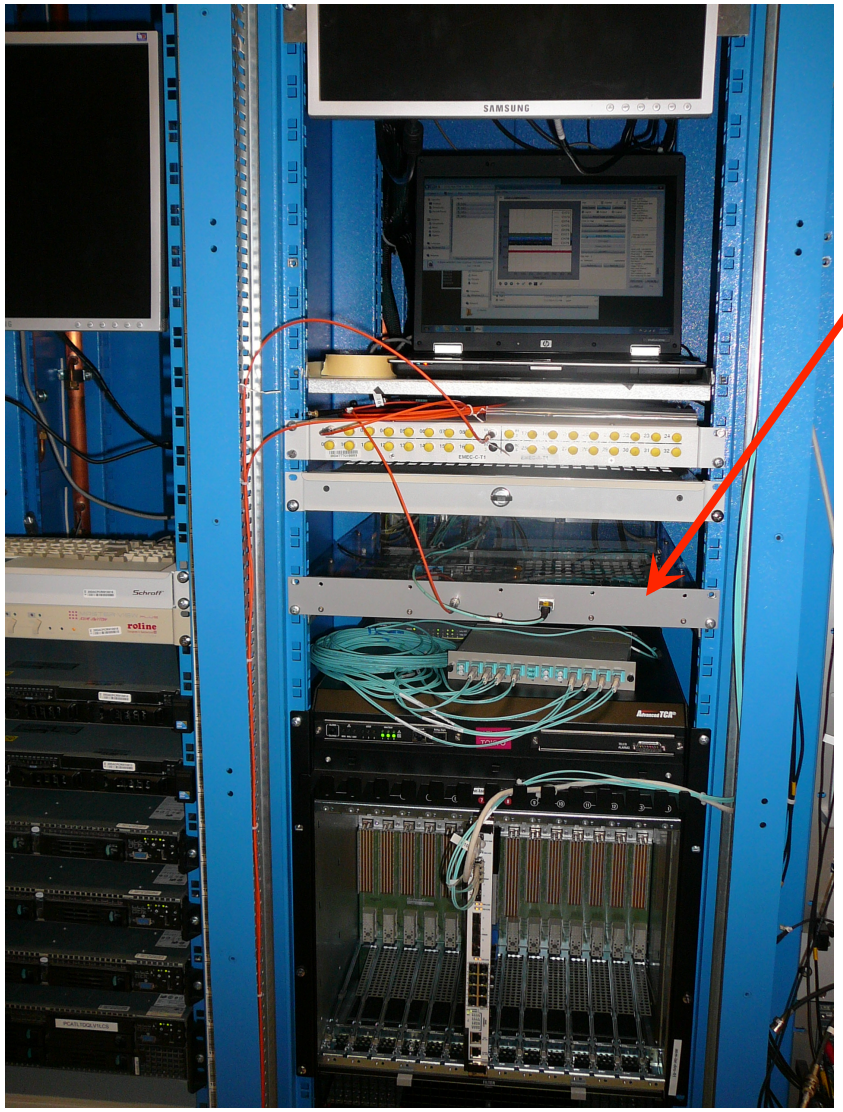


Pedestal Measurement of LTDB Demonstrator at CERN EMF

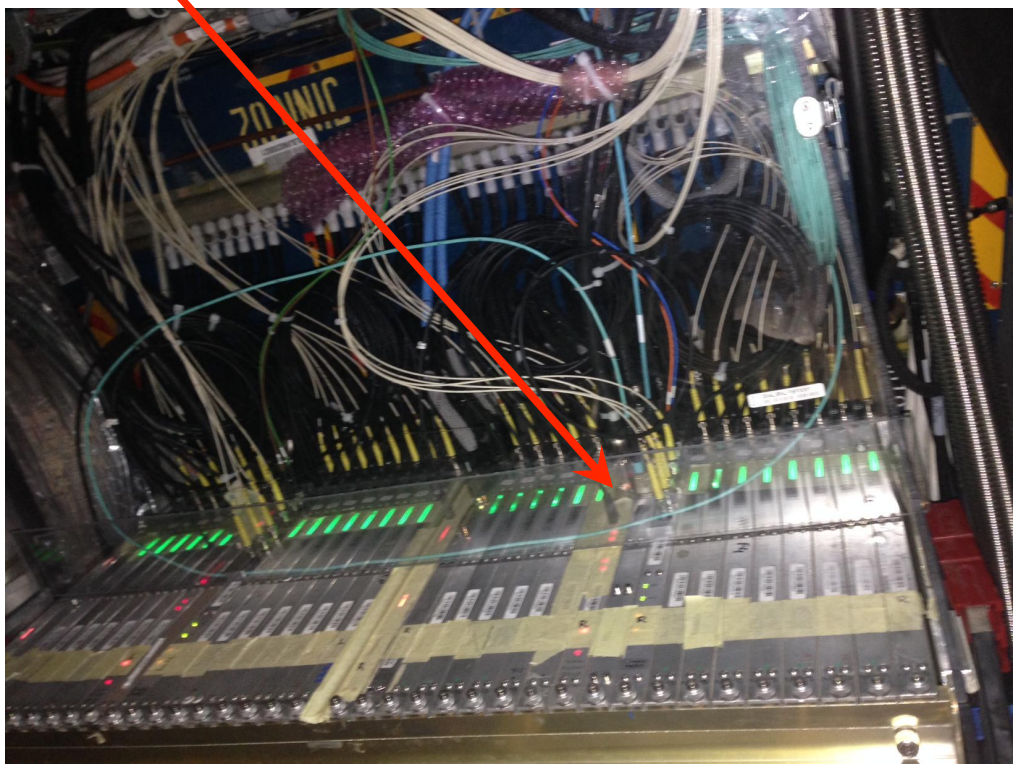


- LTDB Demonstrator
  - Demonstrator program is well documented in LAr TDR
  - Design is based on COTS components with careful qualification tests
  - Successful system integration test at CERN EMF
  - Passed ATLAS review with satisfactory system performance in May 2014
  - Green light to install LTDB demonstrator on detector in July 2014

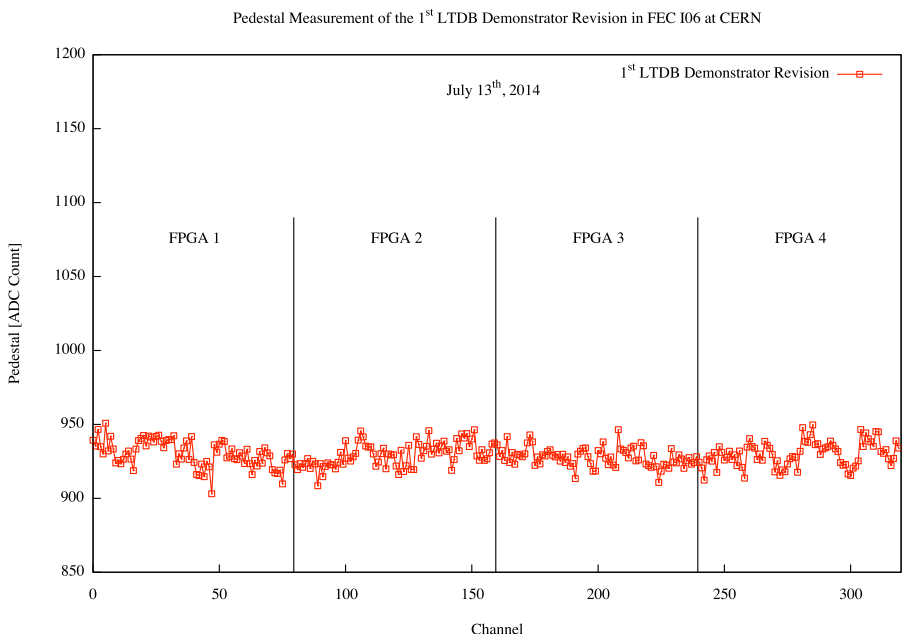
LTDB Demonstrator (3)

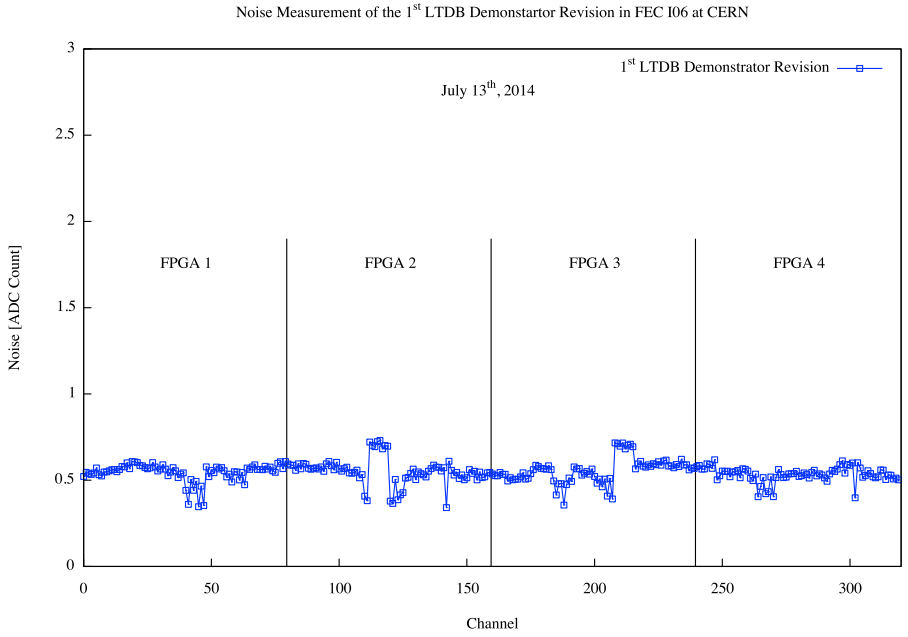


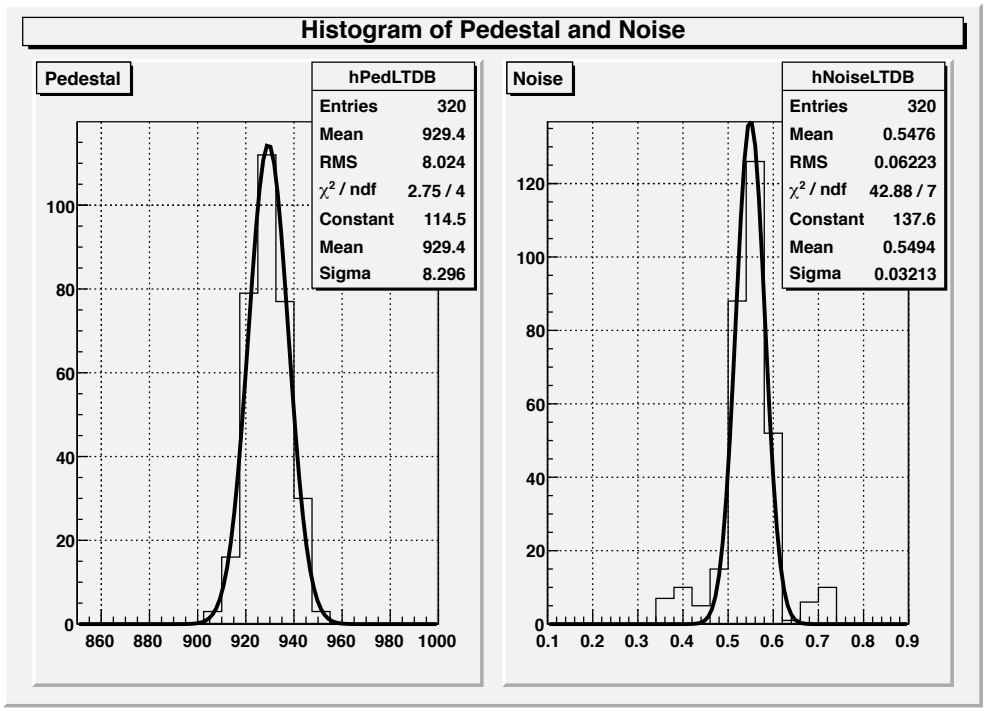
- The GLIB rack box was installed in ATLAS USA15 at CERN on 07/13, 2014
  - GLIB Rack Box
- The LTDB demonstrator was installed in ATLAS UX15 at CERN on 07/02, 2014
  - LTDB in Front End Crate



LTDB Demonstrator (4)

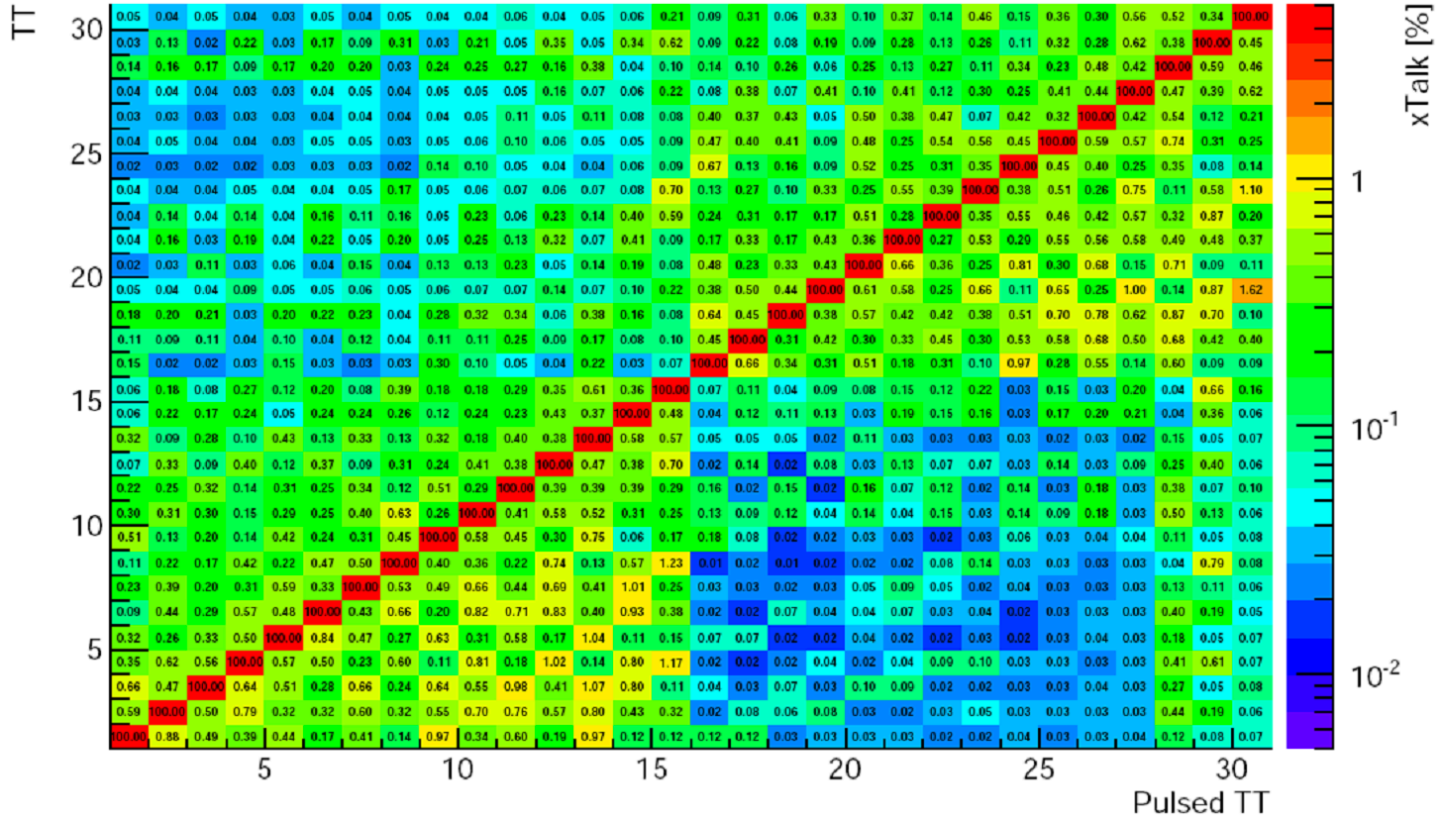






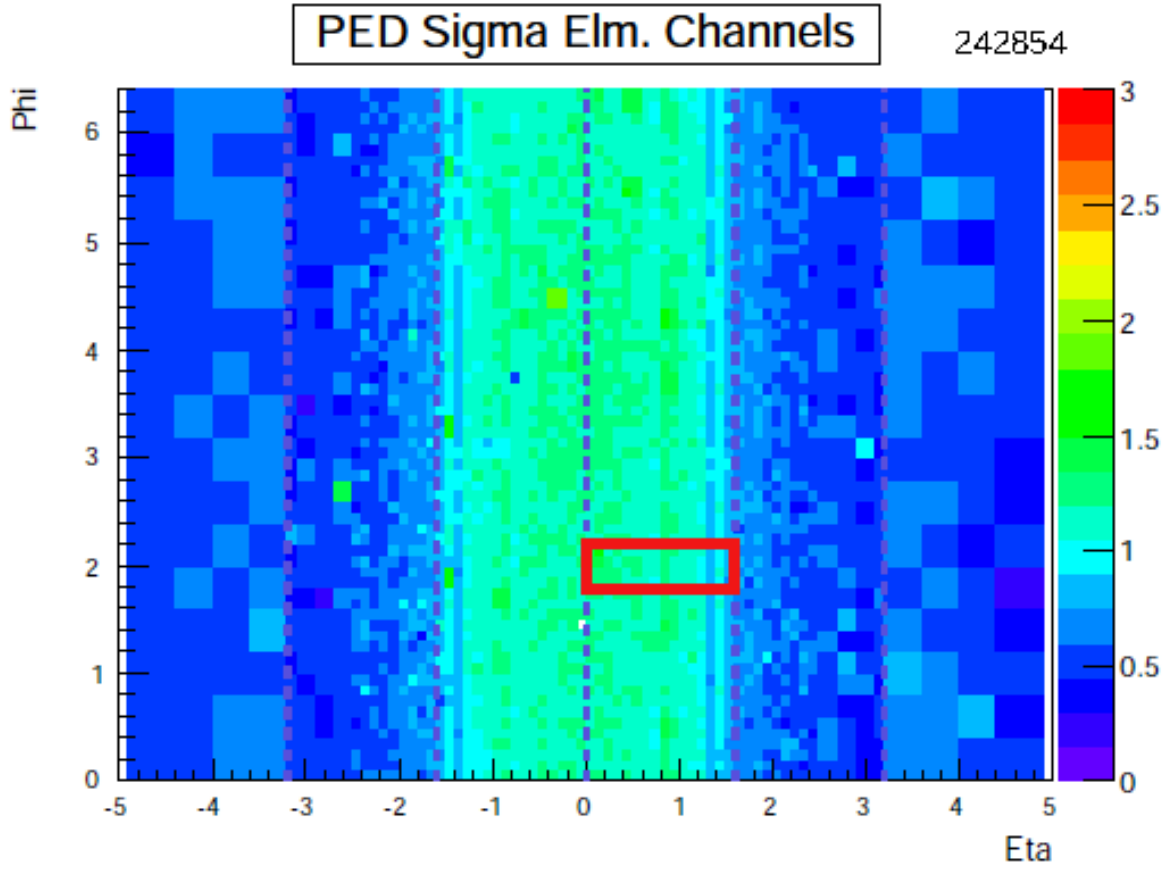
- LTDB Demonstrator
  - LTDB demonstrator has been successfully installed on detector in July, 2014
  - Data taken in I06 FEC shows satisfactory performance

LTDB Demonstrator (5)



- Crosstalk study of LTDB demonstrator and new baseplane in the FEC
  - The LTDB has no obvious influence to the FEB outputs and the Trigger Tower signal
  - The crosstalk is smaller than 2% for all the trigger towers, dominated by detector

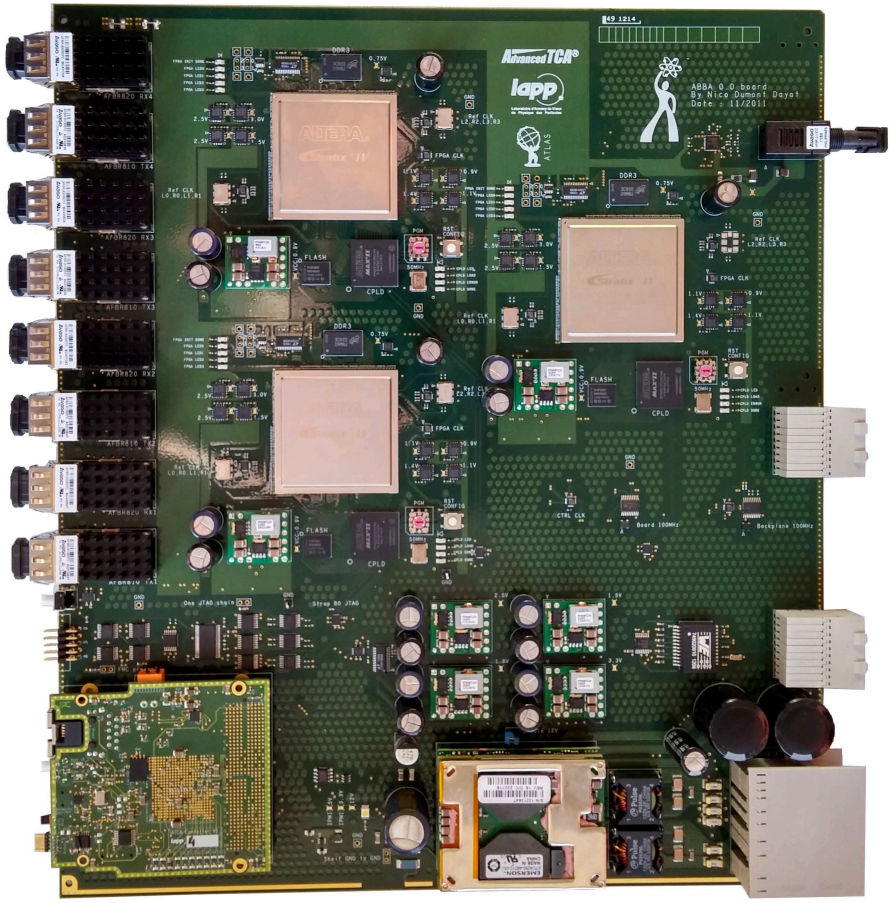
LTDB Demonstrator (6)



- Noise study of LTDB demonstrators installed on detector
  - Position of the crate with the installed demonstrator is ($\Delta\eta$ = 0-1.4, $\Delta\phi$ = 1.8-2.2)
  - Total noise when with all shaper switches on is measured, which is the same for this demonstrator crate and other crates.

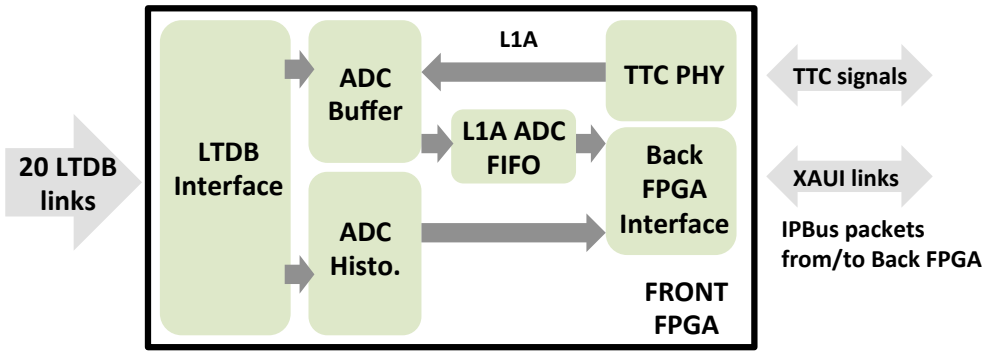
LDPB Demonstrator (1)

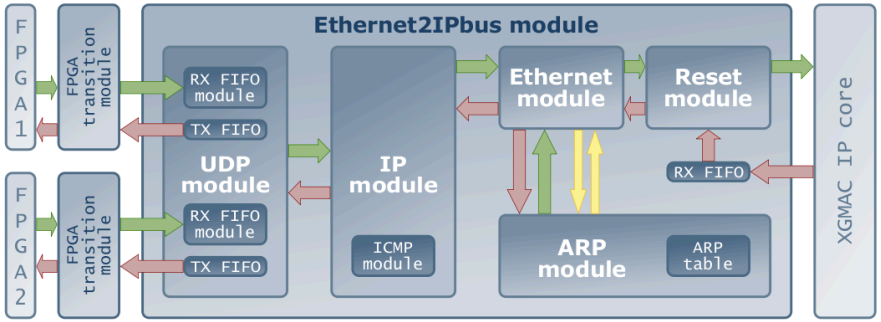
- LDPB demonstrator is realized by an ATCA based ABBA board
  - Three ATLERA Stratix IV GX FPGAs for data processing
  - 8 Avago PPOD transceivers to handle 48 input and 48 output links
- A customized protocol interface is used between the LTDB demonstrator and ABBA board
  - Same data format for two different LTDB demonstrators
- The PC is used to control and configure the ABBA boards using TDAQ (Trigger and Data Acquisition System) and LAr Online System
  - The interface between them is the 10Gbps Ethernet



LDPB Demonstrator (2)

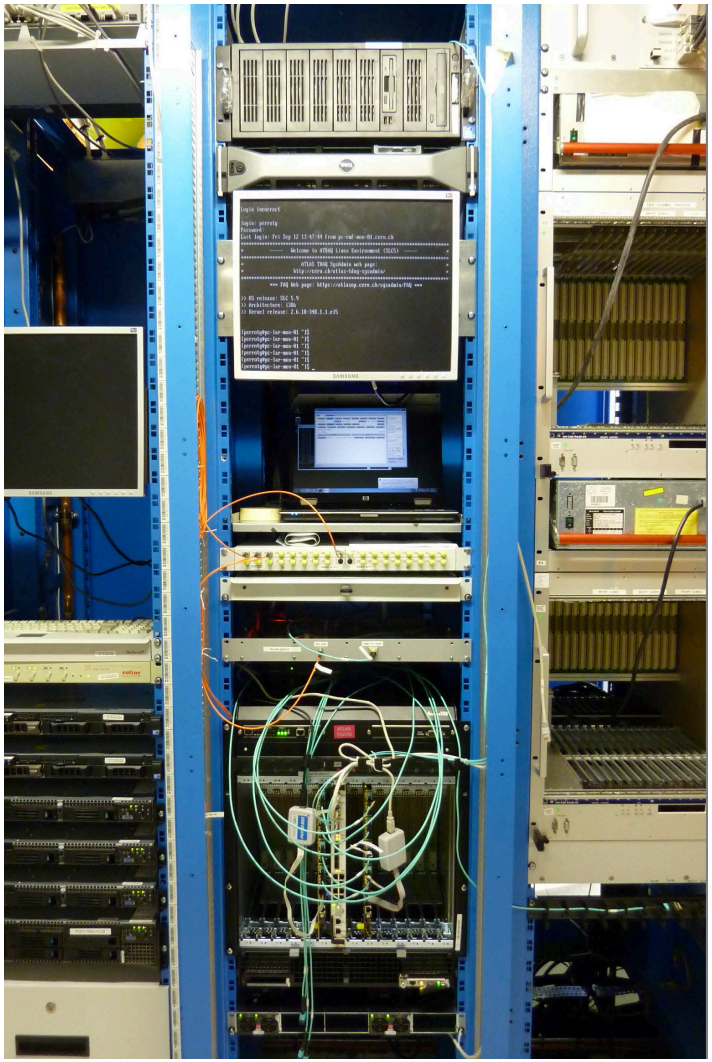
- LDPB demonstrator firmware development includes two main components: Front FPGA and Back FPGA
- Front FPGA Firmware
  - LTDB interface: Receive and decode ADC frame from LTDB
  - ADC buffer: Circular buffer to store ADC values
  - ADC histo: ADC histogram
  - TTC PHY: TTC signals decoding (L1A, BCR…), TTC clock
  - L1A ADC FIFO: ADC samples stored each L1A
  - Back FPGA interface : XAUI and IPBus interface with Back FPGA in order to read/ write internal registers/RAM/FIFO
- Back FPGA Firmware
  - Front FPGA interface: XAUI and IPBus interface
  - DAQ system interface: 10 Gigabit Ethernet (XGbE) to ATCA system switch





LDPB Demonstrator (3)

- The ABBA board, and the PC controller are installed in an ATCA chassis in the ATLAS USA15
  - 100 meters 48-link fibers are used to connect LTDB demonstrator from UX15 to ABBA board
- A GLIB Rack Box is assembled in the USA15 for the LTDB slow control, and the FPGA reconfiguration
  - It shares the same rack for ABBA board installed ATCA chassis
  - 100 meters 12-link fibers are used to connect LTDB demonstrator from UX15 to GLIB box



Electronics Development for Phase-I Upgrade

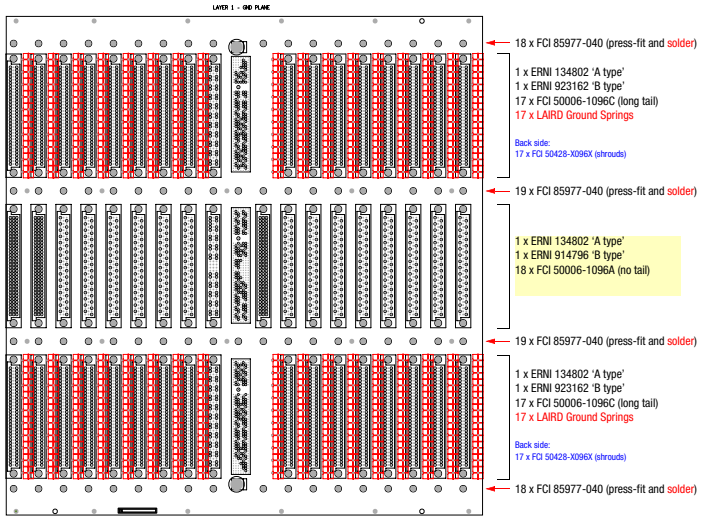
- LTDB Development
- LDPS Development

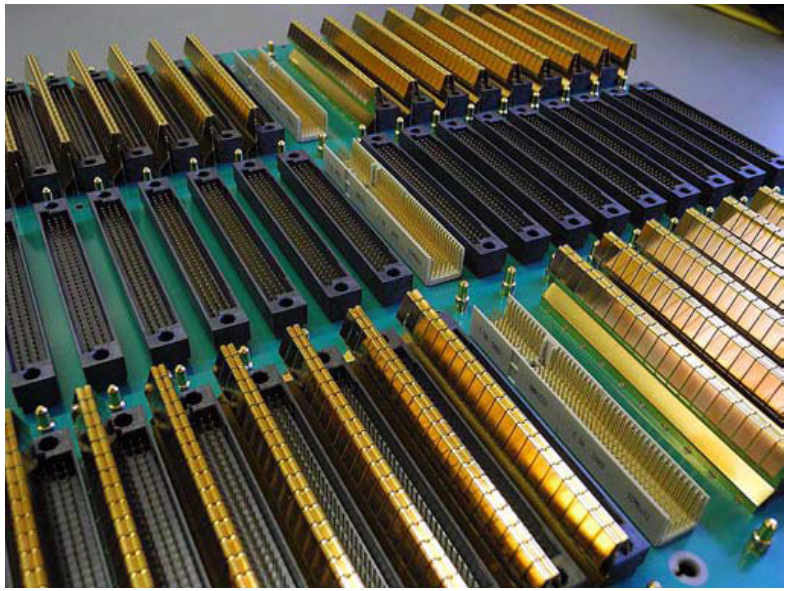
Electronics Development for Phase-I Upgrade

- New Layer Sum Board (LSB)
  - Personality card on FEB
  - Provide finer granularity super cell signals
  - $\Delta\eta$ x $\Delta\Phi$= 0.025 x 0.1 on front layer and middle layer
- New Baseplane
  - New slot added for LTDB, TBB is kept as is
  - Higher density super cell signals transmission on baseplane
- Liquid Argon Trigger Digitizer Board (LTDB)
  - Sum super cell signals and provide $\Delta\eta$ x $\Delta\Phi$= 0.1 x 0.1 layer sum signals to TBB
  - Digitize super cell signals and transmit off detector over parallel fiber optical link
- Liquid Argon Digital Processing System (LDPS)
  - Reconstruct energy and timing from digital super cell signals
  - Interface to Feature Extractor (FEX) of L1Calo system

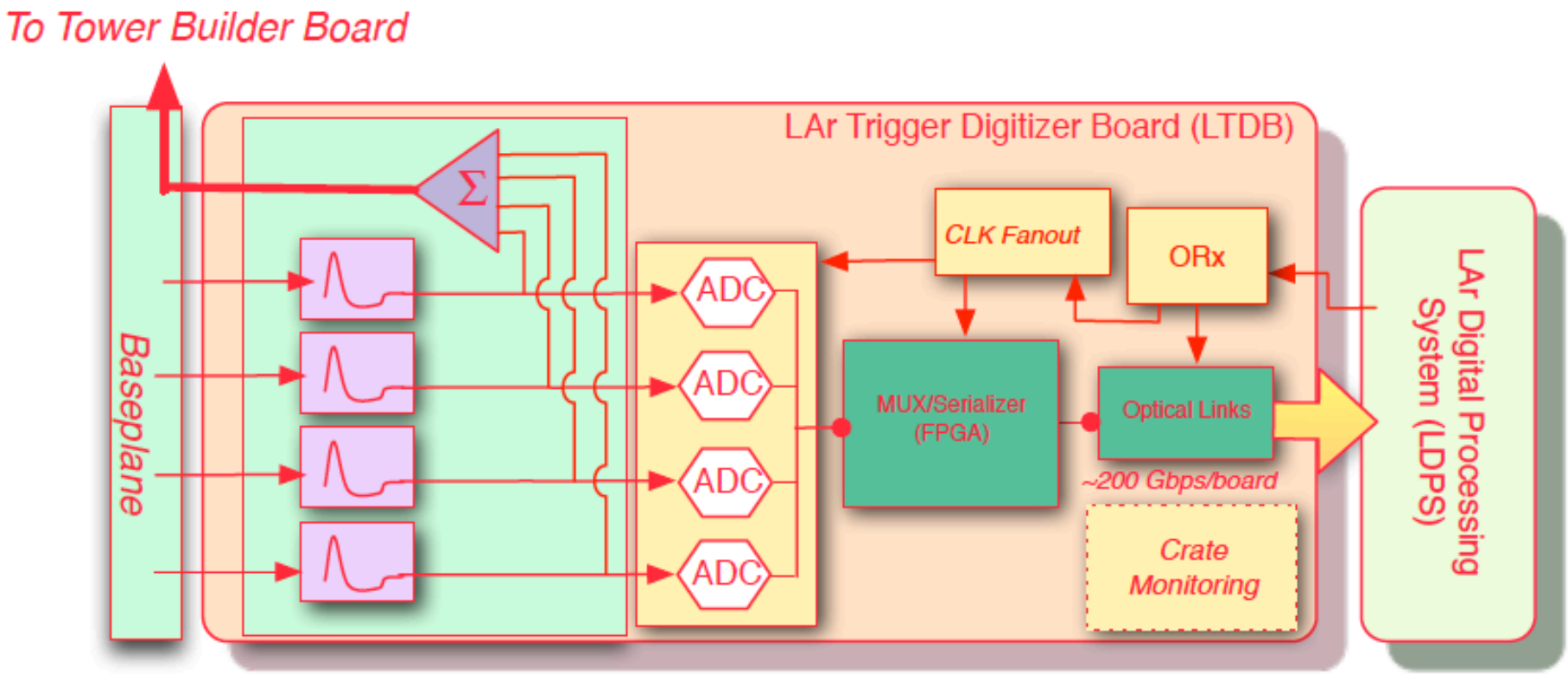
Baseplane Development

- Five different types of baseplane
  - EM Barrel
  - EM Endcap Standard
  - EM Endcap Special
  - HEC
  - FCAL
- EM barrel baseplane has been designed and prototyped
  - One prototype EMB baseplane has been installed on detector for demonstrator project in June 2014
- Design and assembly of baseplane are very challenging
  - High density layout
  - Custom parts and obsolete parts – ***a typical upgrade issue***
  - Complex assembly fixture





LTDB Development



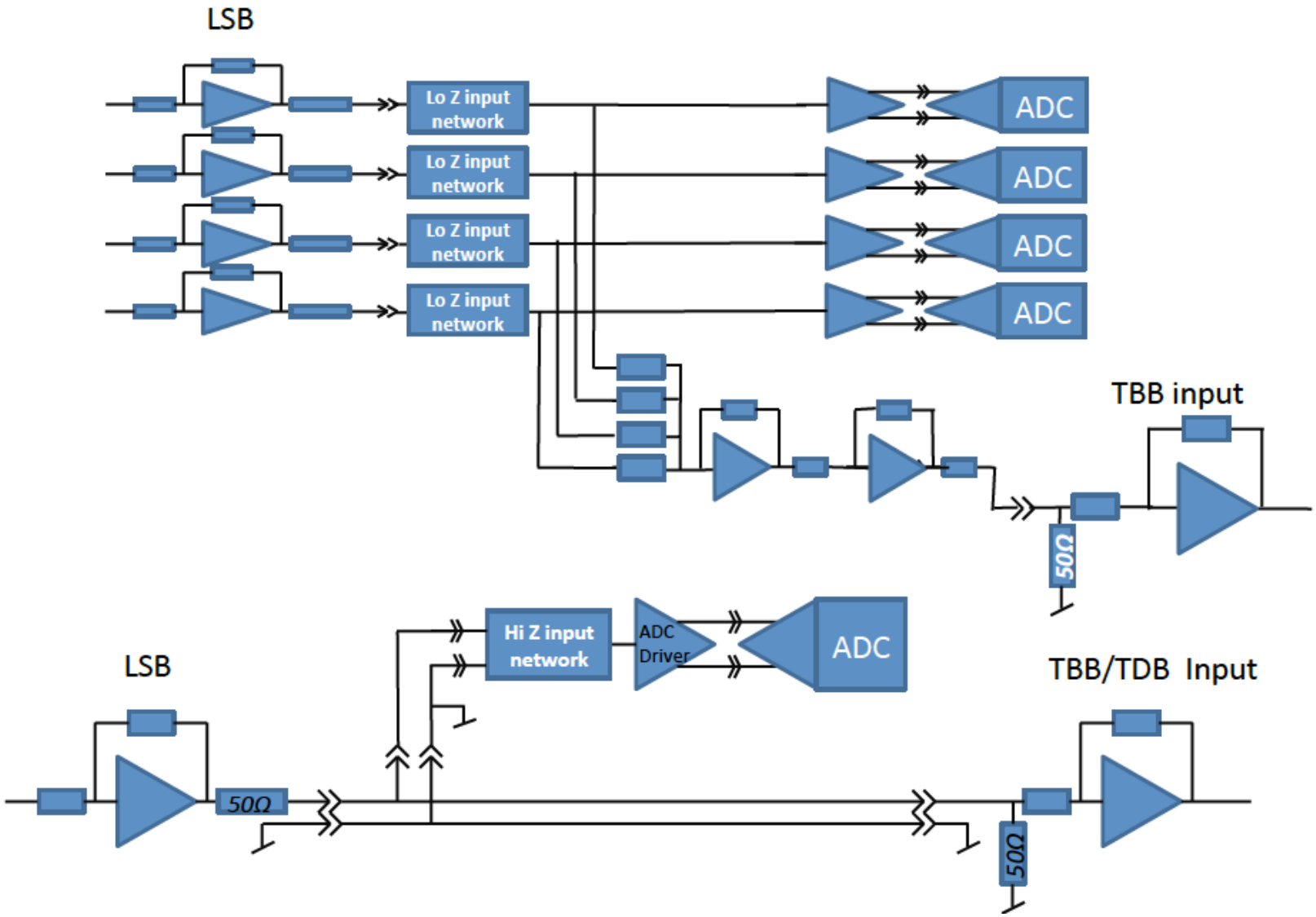
LTDB Development

- Analog Signal Conditioning
  - Sum of super cell signals
  - ADC driver
- Digitization of Super Cell Signal
  - Key component: ADC
- Optical Transmission
  - Data aggregation: MUX and serializer
  - Optical transceiver
- Auxiliary
  - TTC interface
  - Power interface
  - Cooling management

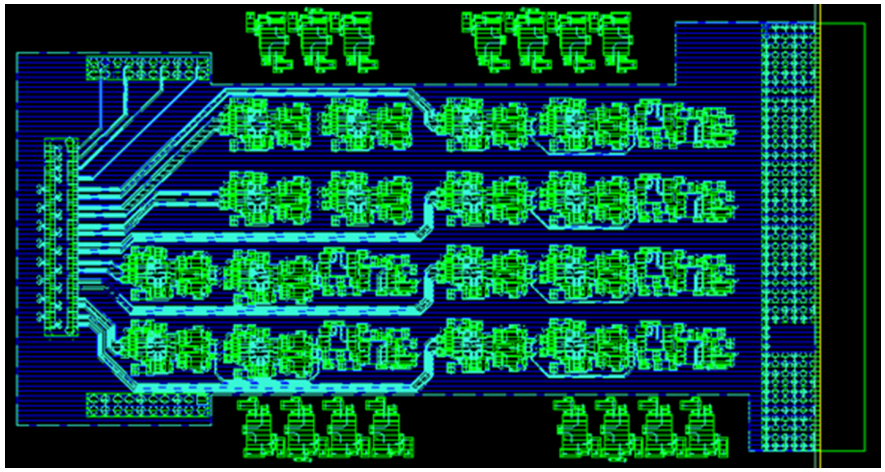
LTDB Analog Signal Conditioning

- Components Selection
  - Bandwidth
  - Low power consumption
  - Radiation tolerant
- Spice Simulation
  - Complete simulation package of full readout chain from preamplifier all the way to TBB
  - Study signal saturation along the readout chain
  - Determine optimum gain setting and utilization of ADC dynamic range

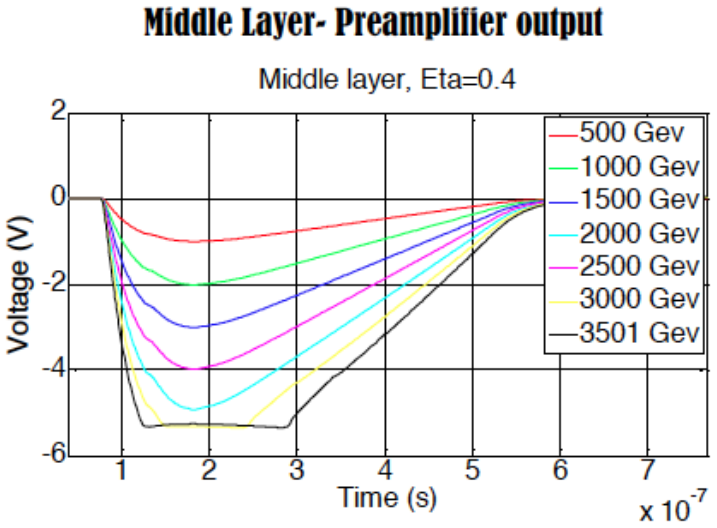
LTDB Analog Signal Conditioning

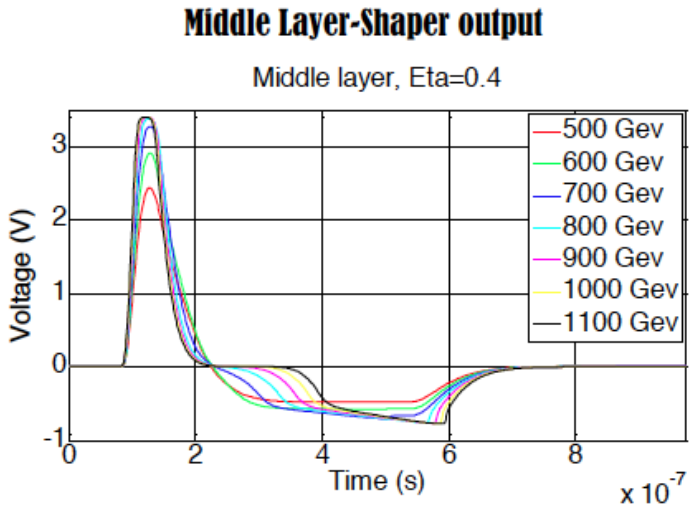


LTDB Analog Signal Conditioning

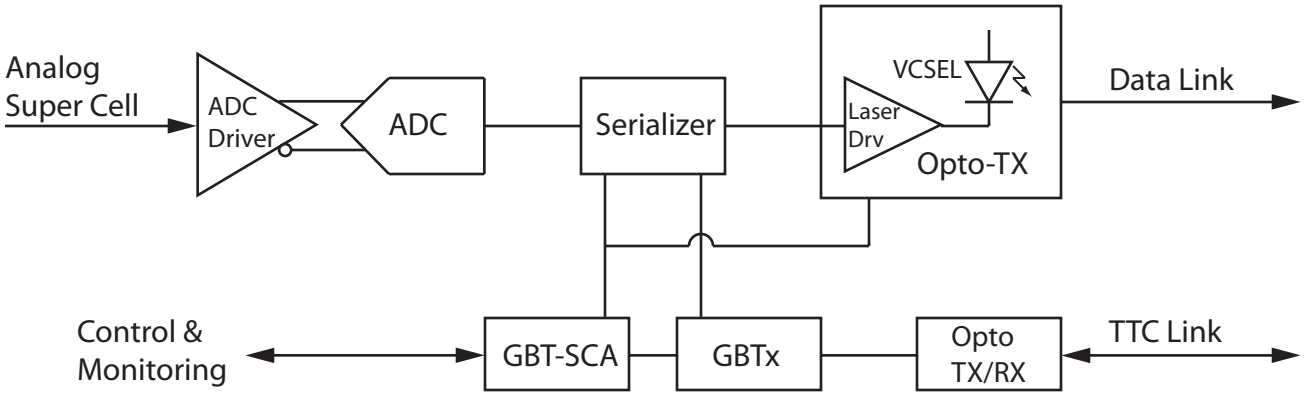


- View of one face (representing 32 channels) of a 64 channel section motherboard prototype
- Design has been implemented on the LTDB demonstrator
- Gain selection of analog section is being studied and to be determined
  - Variable gain to keep same E_T/ADC
  - Constant gain to make use of the full ADC dynamic range





LTDB Digital Section



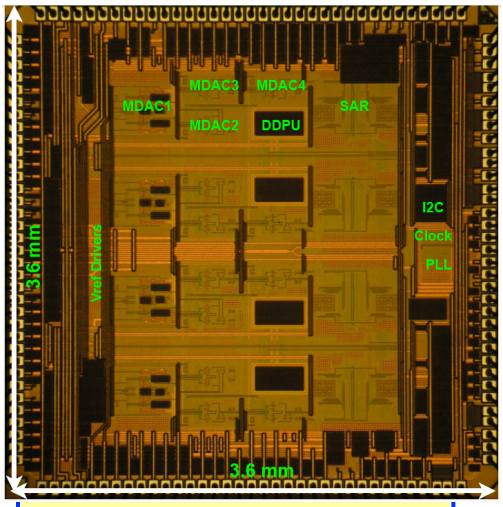
- The LTDB digital section includes two signal flow paths: the data link and the control (TTC) link
- Super Cell signals are digitized by the ADC, reorganized and serialized by LOCx2, and transmitted via the MTx over fiber optical links
- The TTC link is responsible for clock distribution, slow control and monitoring
  - It is composed of the GBTx, GBT-SCA and MTRx
  - The GBTx is used to interface to the back end of the TTC system via MTRx over duplex fiber optical links
  - The GBTx and GBT-SCA chipset is used to provide clock distribution, slow control and monitoring on the LTDB.

LTDB Signal Digitization: ADC

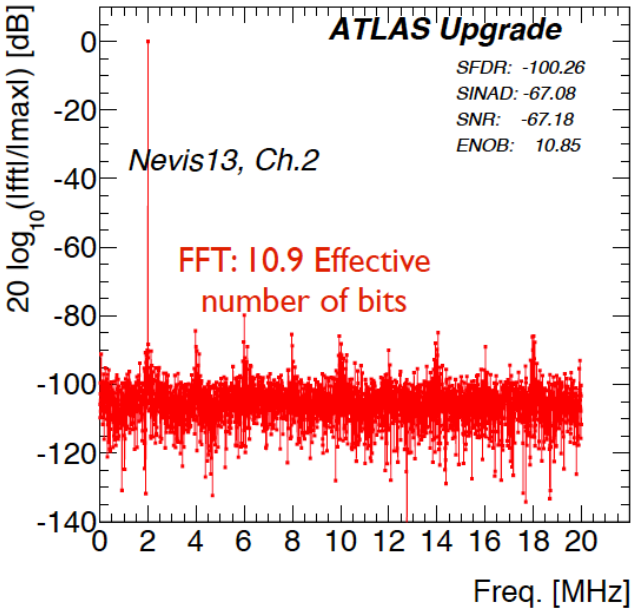
- ADC is the most technologically challenging component in both Phase-I and Phase-II upgrade
  - 16-bit dynamic range – 12-bit resolution – 40Msps
  - Low latency – few (~5) bunching crossings – minimize Level 1 trigger latency
  - Radiation tolerant and SEE immune
- Strategies being followed
  - Development of custom ADC
    - IBM 0.13μm 8RF CMOS technology, lots of CERN based experience
    - Already shown to be radiation hard, lower cost compared to SiGe
  - Evaluation of COTS ADC
    - High density, high speed, large dynamic range and low power ADC are available from industrial in past few years
    - Find a magic bullet with commercial parts
    - Irradiation tests (TID, SEE) are being performed on COTS ADC

ADC ASIC Development

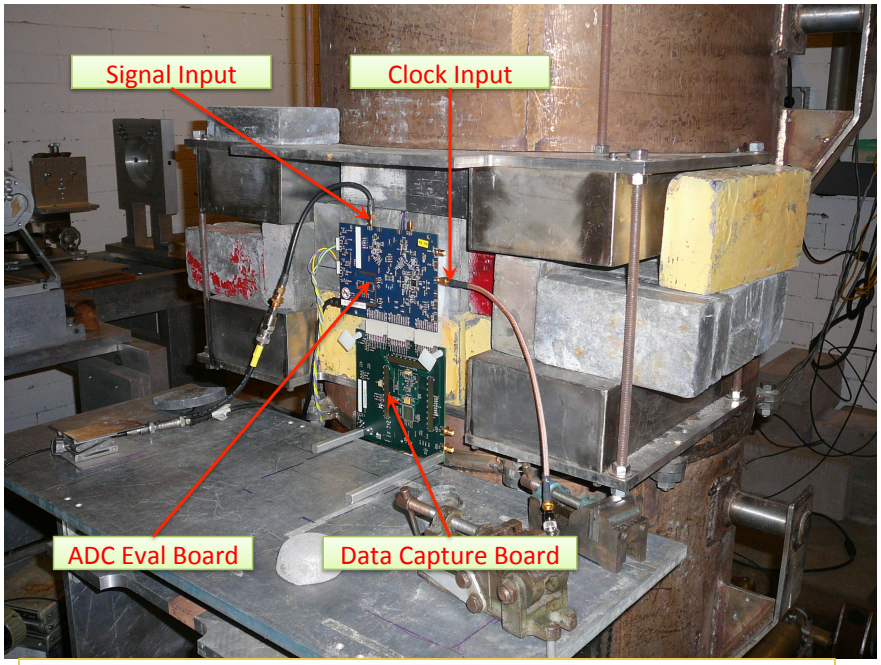
- Nevis10 chip
  - Two 4-stage ADC pipelines, 1.5bits/stage with S/H
  - Gain selector structures for each pipeline
  - Support structures
  - Analog performance is equivalent to COTS 12-bit ADC
  - Radiation tolerant > 10MRad, $2x10^{14}$ p/cm^2
- Nevis12 chip
  - Dual channel 12-bit ADC: 4-bit pipeline + 8-bit SAR
  - ENOB ~11.5 bit, power ~50mW/ch, latency ~76.5 ns
- Nevis13/14 chip
  - Quad channel 12-bit ADC: 4-bit pipeline + 8-bit SAR
  - Built-in PLL to avoid on board fast clock distribution
  - ENOB ~ 10.9 bit



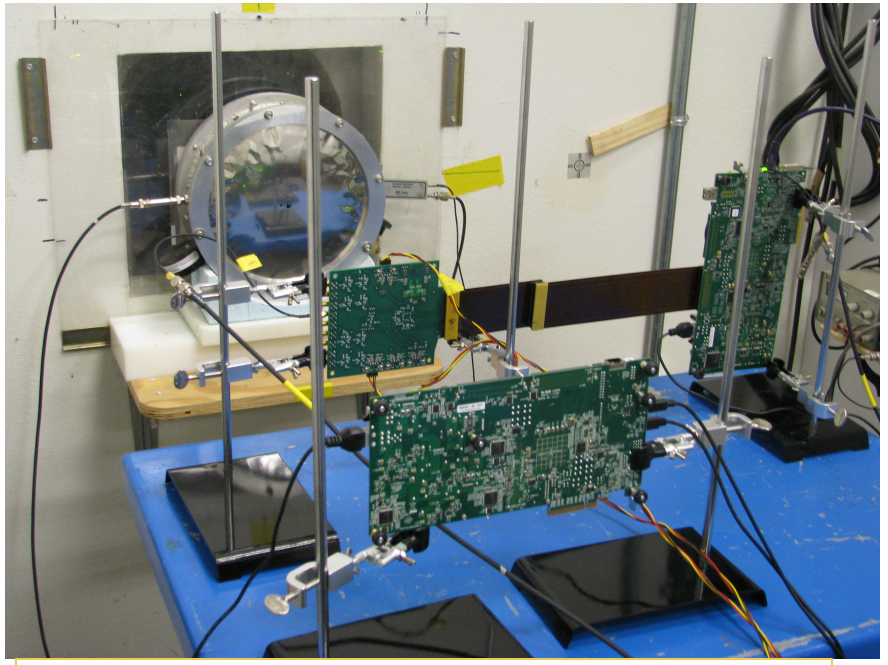
Layout of Nevis13 chip



COTS ADC Evaluation Test



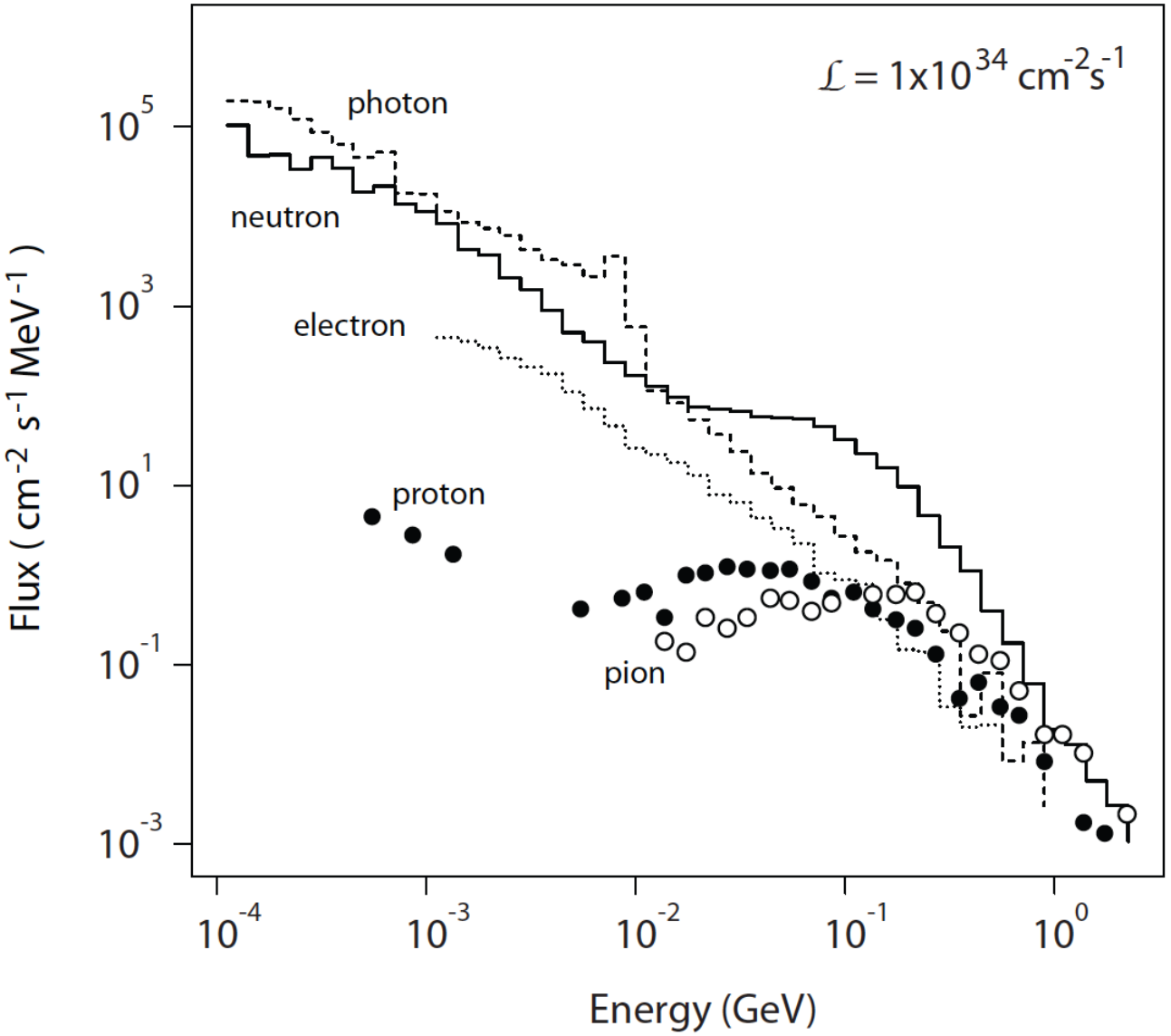
TID Irradiation Test with ^{60}Co γ Source at BNL



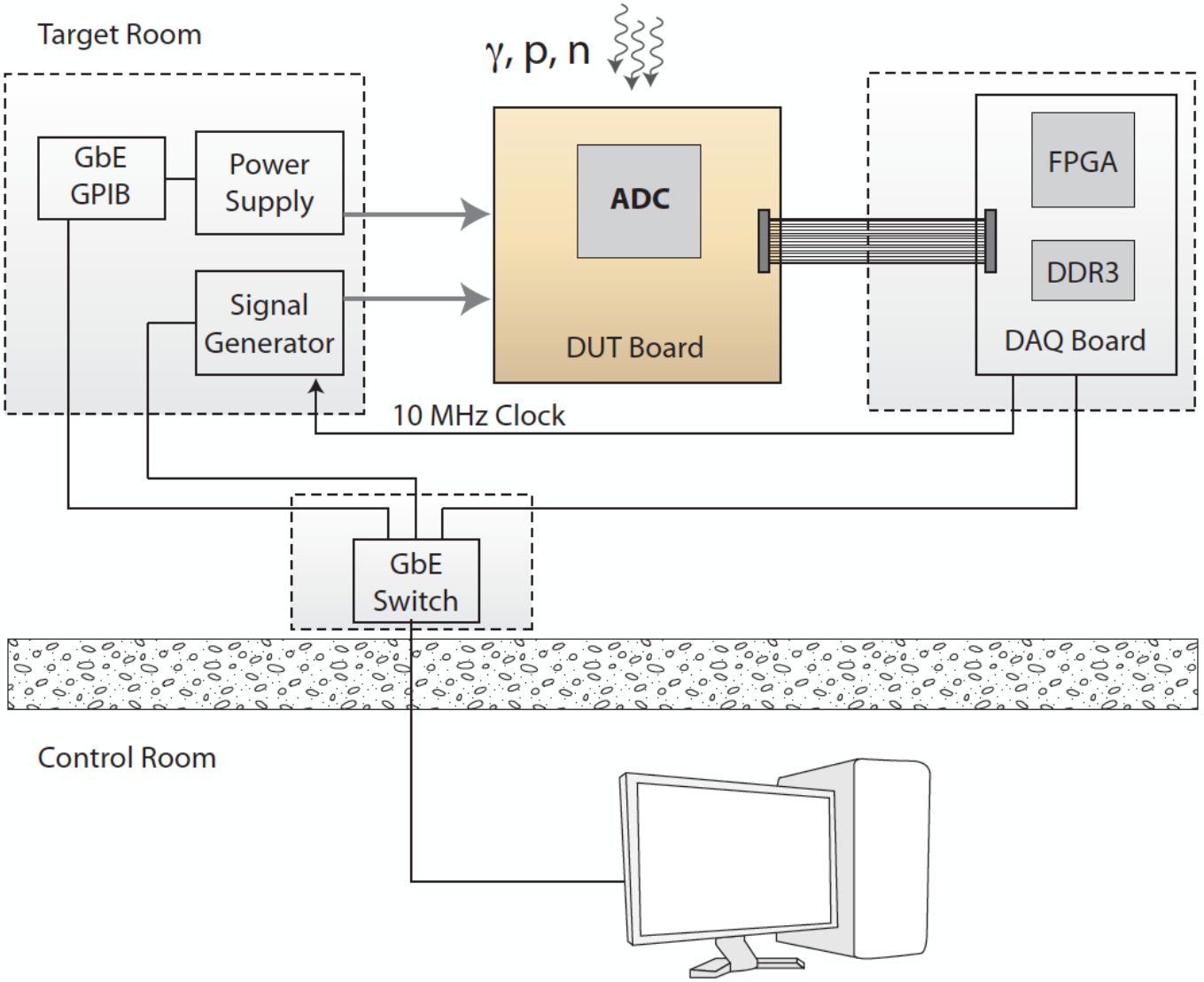
ADS5272 SEE Test Setup at LANSCE

- COTS ADC evaluation test will have to study the radiation tolerance
  - TID irradiation test was performed with ^{60}Co γ Source at BNL
  - SEE irradiation test was performed with proton beam at MGH and IUCF, and neutron beam at LANSCE
- TI ADS5272 has been identified as a candidate of LTDB design in Phase-I upgrade

The Radiation Field at LAr Barrel Crates



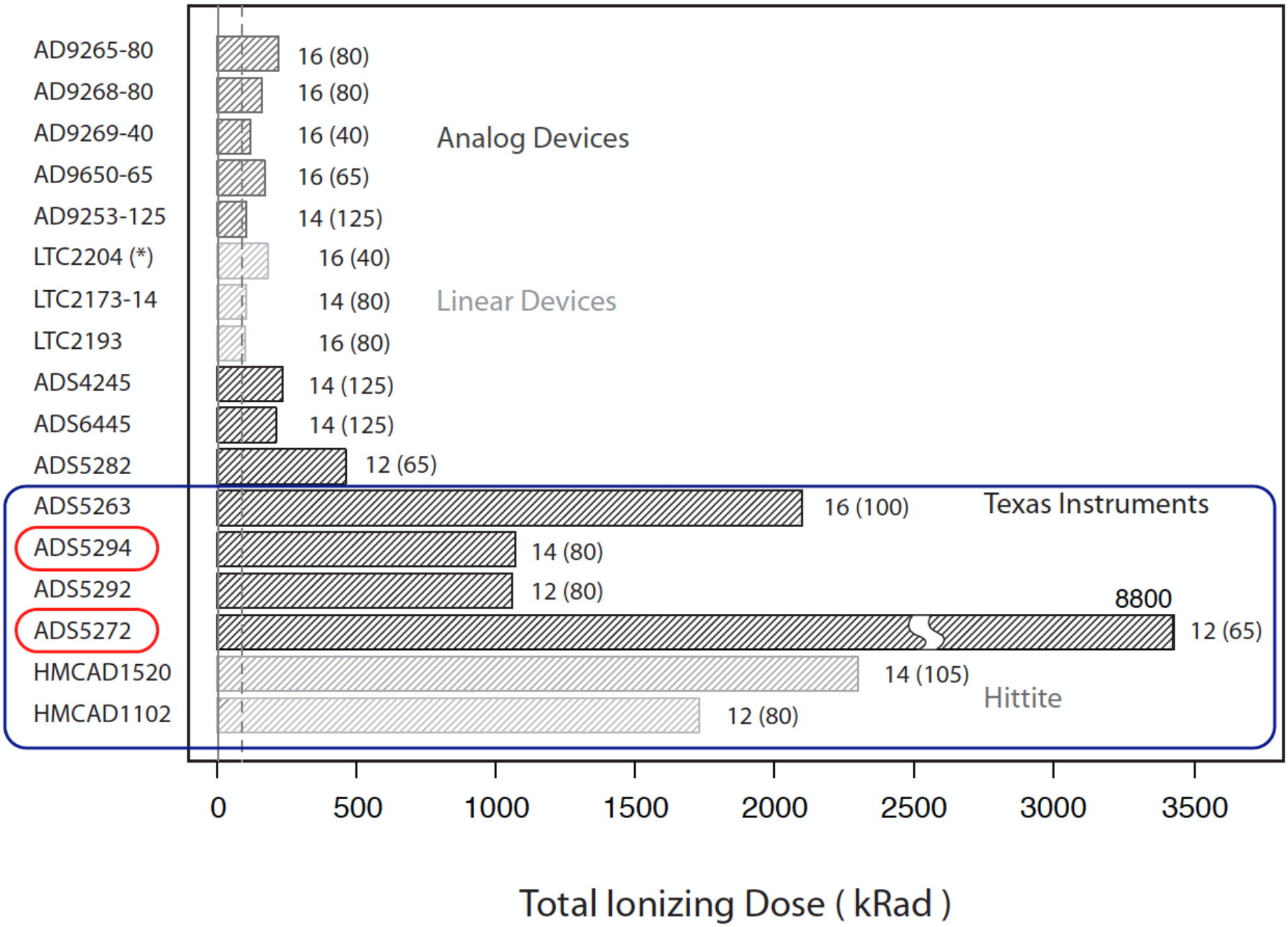
Experimental Setup



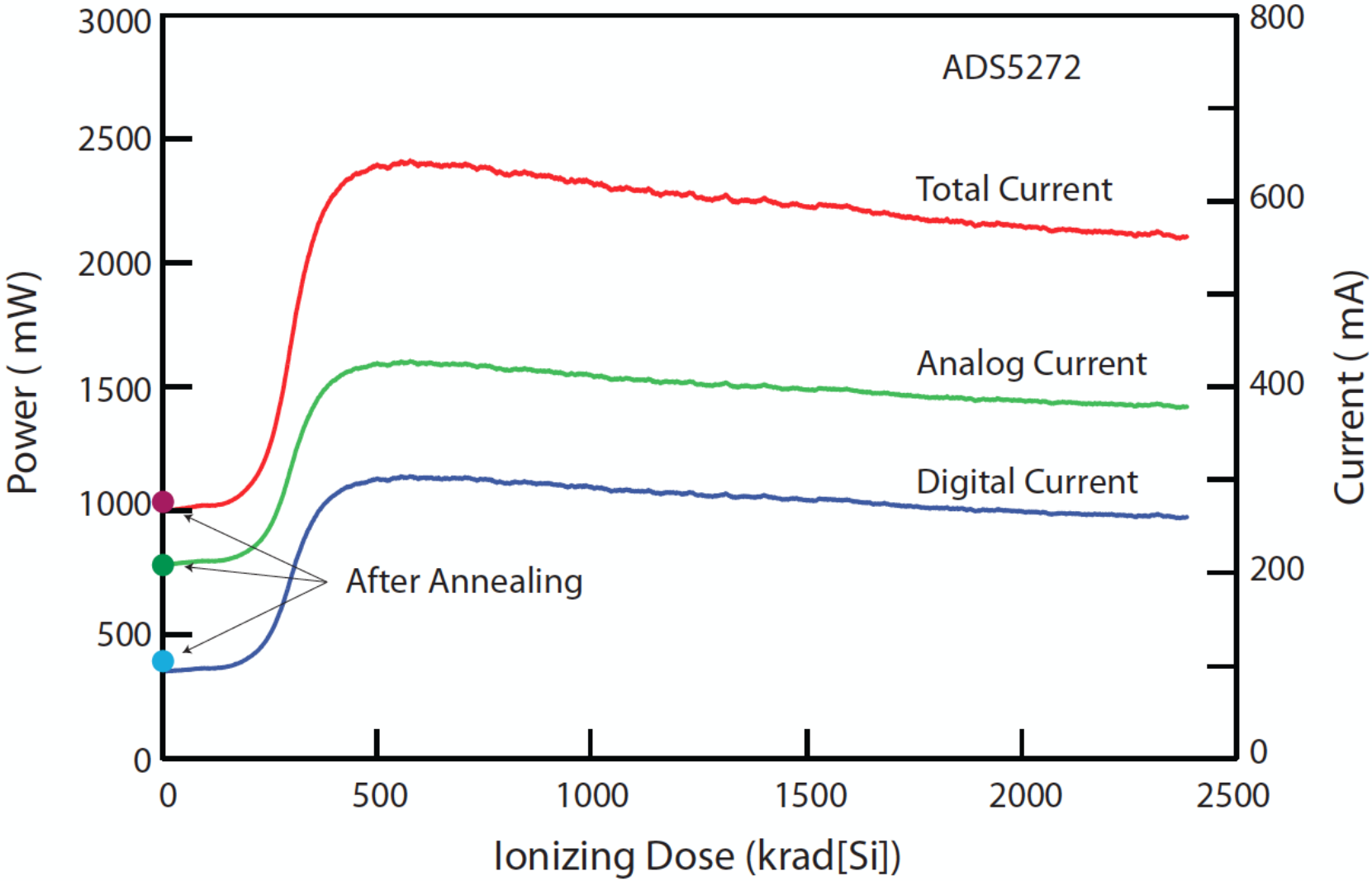
Total Ionizing Dose Results from ^{60}Co Irradiation

ADC	Dynamic Range [bit]	F [MHz]	Analog Input Span [V_{p-p}]	Channels per Chip	P_{total} per Channel [mW]	Feature Size (nm)	Vendor	TID [$kRad(Si)$]
AD9265-80	16	80	2	1	210	180	ADI	~220
AD9268-80	16	80	2	2	190	180	ADI	~160
AD9269-40	16	40	2	2	61	180	ADI	~120
AD9650-65	16	65	2.7	2	175	180	ADI	~170
AD9253-125	14	125	2	4	110	180	ADI	~105
LTC2204	16	40	2.25	1	480	350	Linear	~180
LTC2173-14	14	80	2	4	94	180	Linear	~105
LTC2193	16	80	2	2	125	180	Linear	~100
ADS4245	14	125	2	2	140	180	TI	~235
ADS6445	14	125	2	4	320	180	TI	~210
ADS5282	12	65	2	8	77	180	TI	~460
ADS5263	16	100	4	4	280	180	TI	~2100
ADS5294	14	80	2	8	77	180	TI	~1070
ADS5292	12	80	2	8	66	180	TI	~1060
ADS5272	12	65	2.03	8	125	180	TI	~8800
HMCAD1520	14	105	2	4	133	180	Hittite	~2300
HMCAD1102	12	80	2	8	59	180	Hittite	~1730

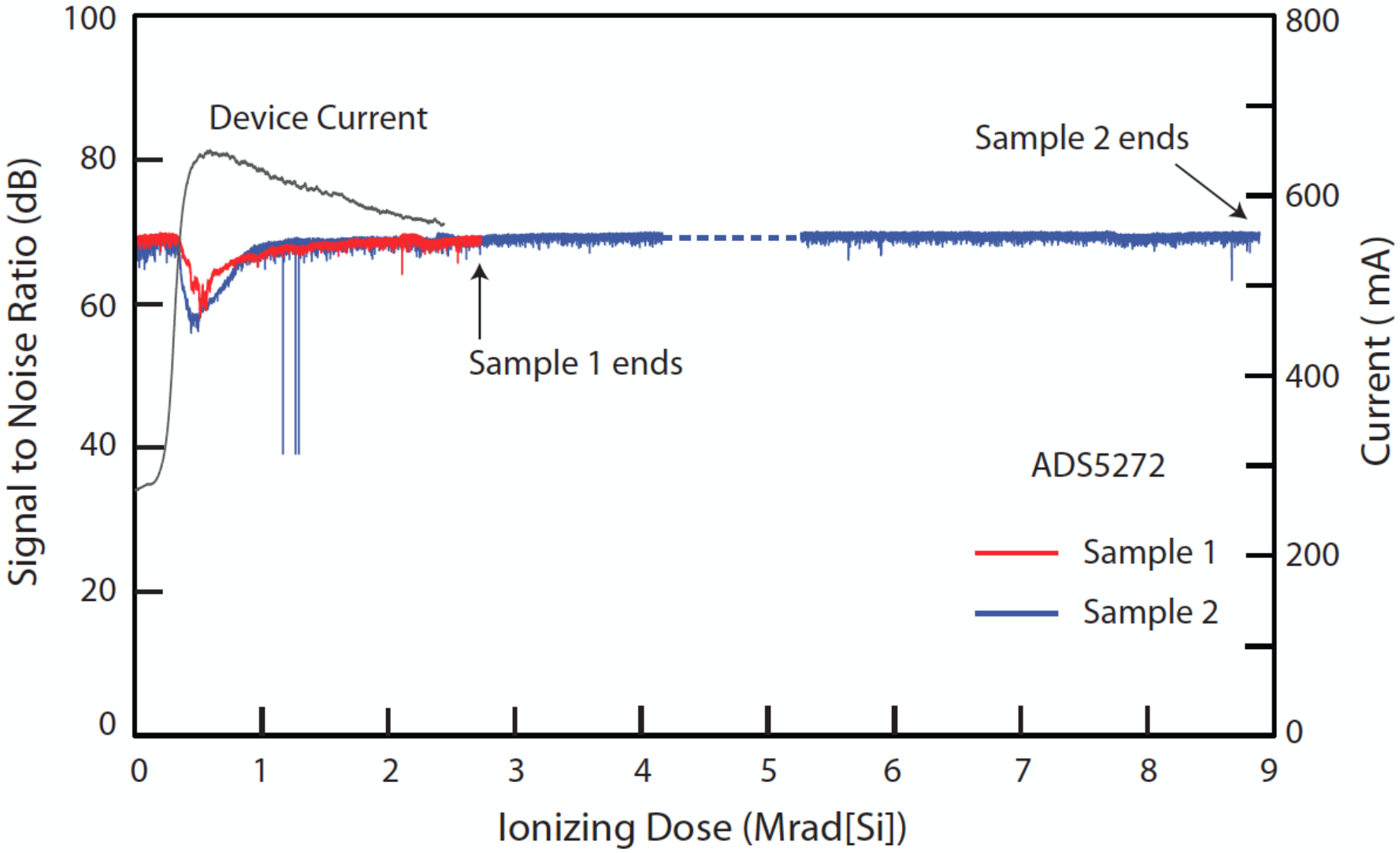
- Dose rate used is 14 krad/h


AD9265-80
AD9268-80
AD9269-40
AD9650-65
AD9253-125
LTC2204 (*)
LTC2173-14
LTC2193
ADS4245
ADS6445
ADS5282
ADS5263
ADS5294
ADS5292
ADS5272
HMCAD1520
HMCAD1102
16 (80)
16 (80)
16 (40)
16 (65)
14 (125)
16 (40)
14 (80)
16 (80)
14 (125)
14 (125)
12 (65)
16 (100)
14 (80)
12 (80)
8800
12 (65)
14 (105)
12 (80)
Analog Devices
Linear Devices
Texas Instruments
Hittite
0
500
1000
1500
2000
2500
3000
3500
Total Ionizing Dose (kRad)

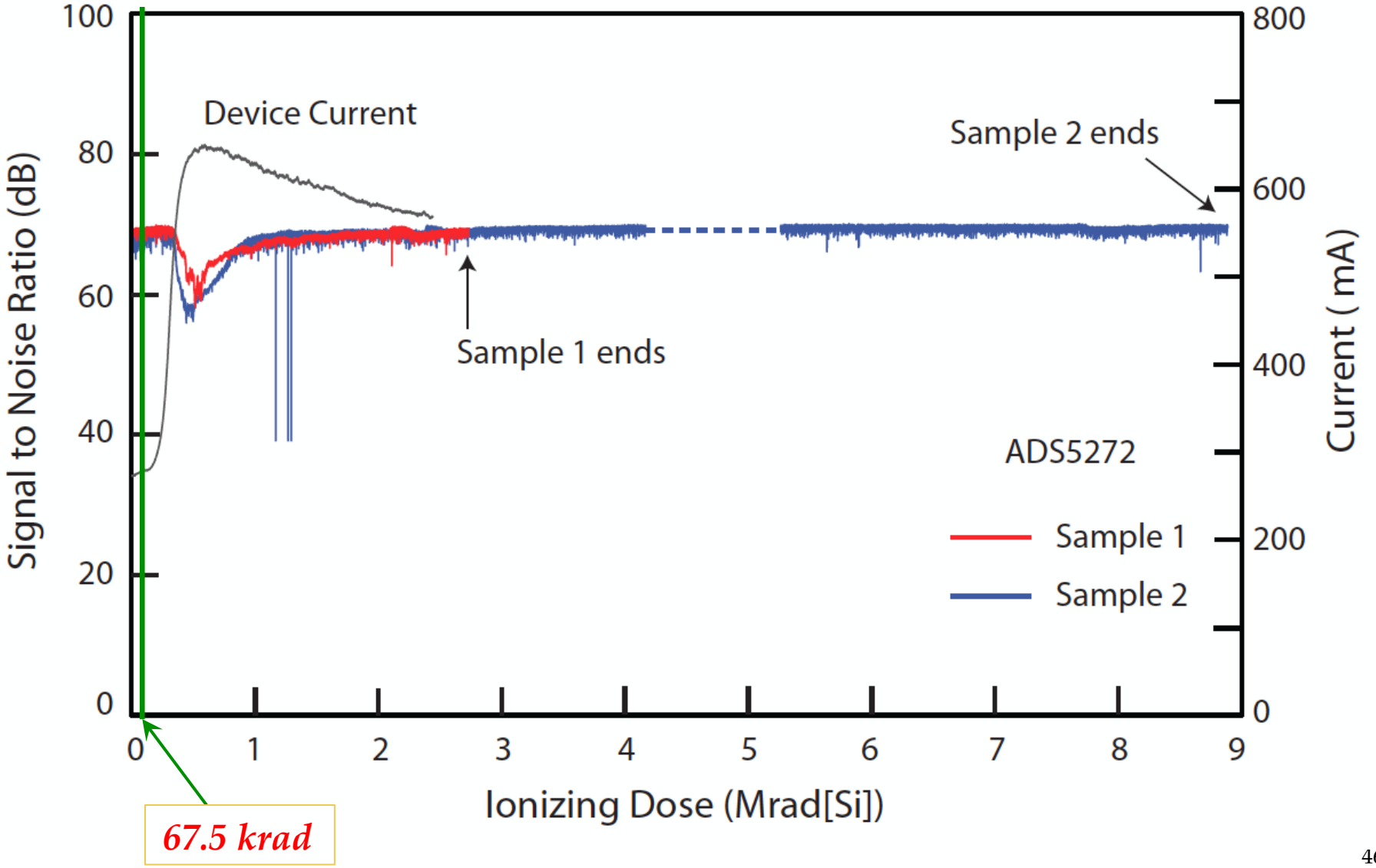
Response of ADS5272 to Ionizing Dose



Signal to Noise Ratio for ADS5272 as Function of Dose



Signal to Noise Ratio for ADS5272 as Function of Dose



Summary of Ionization Dose Tests

- All ADC tested perform well up to 100 krad. Six are resilient to doses larger than 1 Mrad
- ADS5272 has good recovery after an annealing period at high temperature and room temperature. Controlled annealing testes were performed with 20 samples. They all return to within 0.5% of the pre-irradiation values
  - ***For ADS5272, RTC_{tid} calculation can use SF_{ldr} = 1 (instead of 5)***
- Gain change due to dose was measured for ADS5272 (-0.015% per krad) and for ADS5294 (-0.007% per krad)
- ADS5272 continues to work even at much higher integrated doses with a higher current

Summary for SEE Irradiations

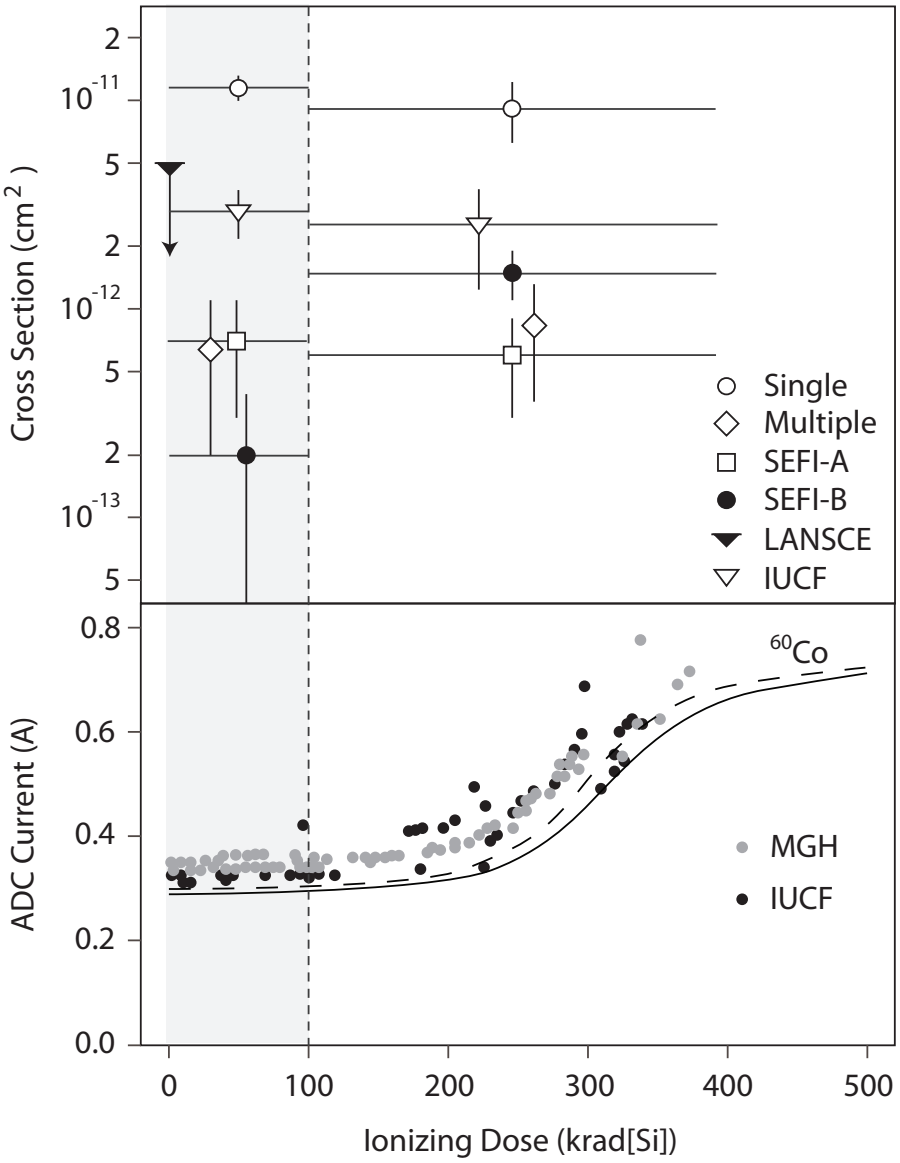
Component	Facility	Energy (MeV)	Total Fluence cm^{-2}	Total Dose krad	NIEL cm^{-2}	Channels Read
ADS5272	IUCF	205	5.67×10^{12}	338	5.50×10^{12}	1
	IUCF	205	5.43×10^{12}	324	5.27×10^{12}	1
	IUCF	205	3.90×10^{12}	232	3.78×10^{12}	1
ADS5272	MGH	216	6.75×10^{12}	374	6.55×10^{12}	8
	MGH	216	4.08×10^{12}	226	3.96×10^{12}	8
	MGH	216	2.39×10^{12}	132	2.31×10^{12}	8
ADS5272	LANSCE	< 800	1.98×10^{11}	~ 1	$\sim 5 \times 10^{11}$	1
ADS5294	MGH	216	1.55×10^{12}	86	1.50×10^{12}	8
	MGH	216	3.92×10^{12}	217	3.80×10^{12}	8

- NIEL calculated as: $\phi_{eq} = \frac{1}{F(1\ MeV)} \int \phi(E) F_h(E) dE$
- With damage functions obtained from literature

SEU Classification

- We detected three types of SEU
- The first type is the most common upset, that we call a bit flip. In these cases a bit is modified for the duration of one clock cycle
- The second type is a functional interrupt, where the ADC stops performing requiring that registers are reprogrammed to resume operations. We call these events SEFI-A
- The third type is also a functional interrupt that needs a power cycle to resume. We call these events SEFI-B

SEE Cross Sections for ADS5272



- SEFI – Single Event Functional Interrupt
- SEFI-A: Reset by reconfiguration of registers. Device recovers in 1.6 µs
- SEFI-B: Requires a power cycle
- *Quoted values are per device. Each ADC digitizes 8 channels*

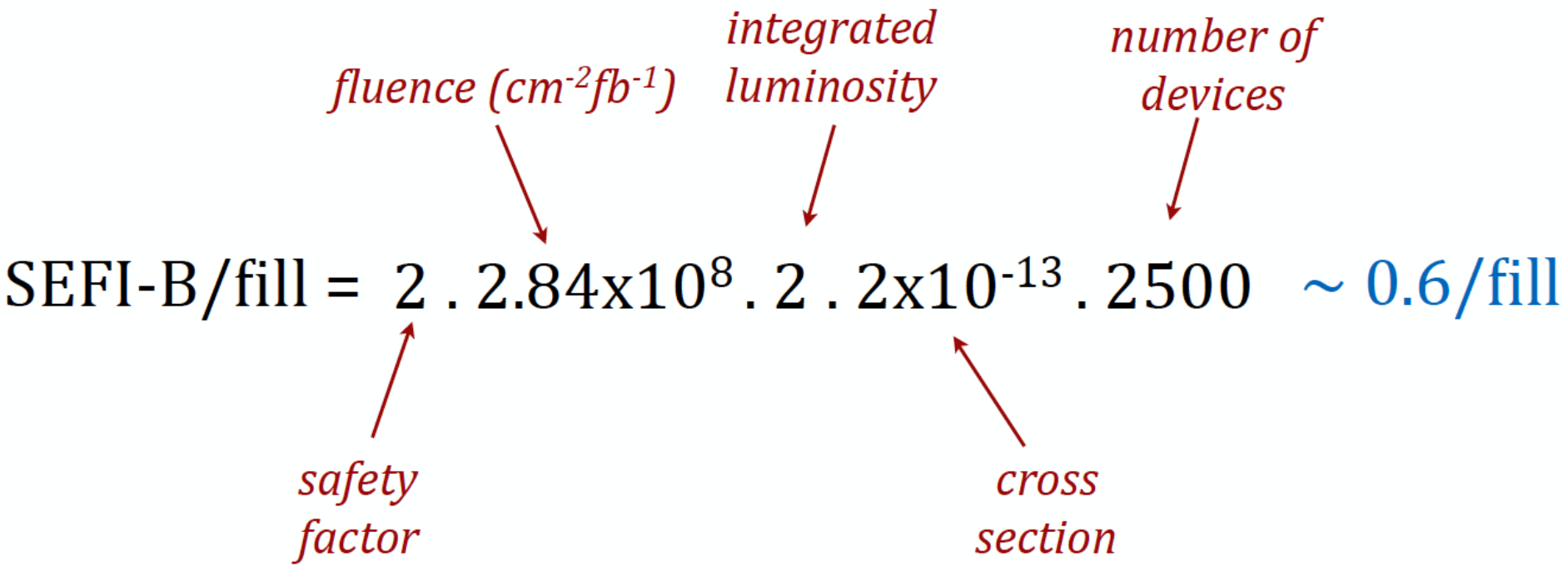
Summary for ADS5272 and ADS5294

SEE Measurement	ADS5272 (<100 krad)	ADS5272 (>100 krad)	ADS5294 (<100 krad)	ADS5294 (>100 krad)
SEU S (cm^{-2})	$(1.2 \pm 0.2) \times 10^{-11}$	$(0.9 \pm 0.3) \times 10^{-11}$	$(7.2 \pm 0.6) \times 10^{-11}$	$(6.7 \pm 1.2) \times 10^{-11}$
SEU M (cm^{-2})	$(6.5 \pm 4.5) \times 10^{-13}$	$(8.5 \pm 4.9) \times 10^{-13}$	$(3.2 \pm 0.5) \times 10^{-11}$	$(2.2 \pm 1.0) \times 10^{-11}$
SEFI A (cm^{-2})	$(0.7 \pm 0.4) \times 10^{-12}$	$(0.6 \pm 0.3) \times 10^{-12}$	$(7.1 \pm 1.5) \times 10^{-12}$	$(7.8 \pm 2.1) \times 10^{-12}$
SEFI B (cm^{-2})	$(0.2 \pm 0.2) \times 10^{-12}$	$(1.5 \pm 0.4) \times 10^{-12}$	–	–

- *Quoted values are per device. Each ADC digitizes 8 channels*
- ADS5272 – Identified SEU, and two types of SEFI. One that is recoverable via registers reprogramming (1.6 µs) and a second that requires a power cycle
- ADS5294 – There is no dependence on total dose for SEFI. SEFI requires reprogramming of three registers, that takes approximately 5 µs

Rates and Mitigation

- For LAr barrel trigger boards in ***Phase-II***, the **SEFI-B rate** is:

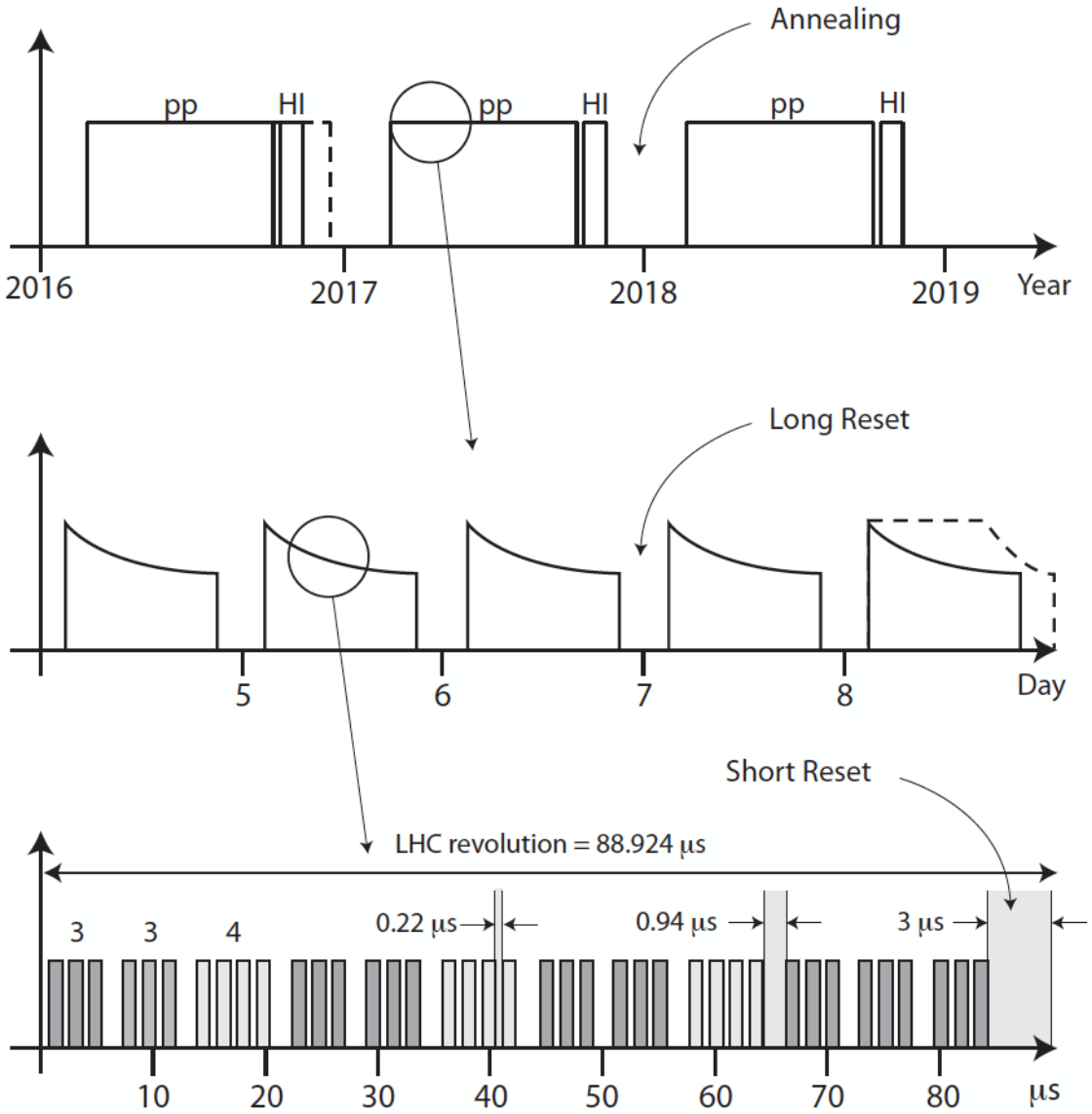


Expected Number of Upsets in LAr Barrel

SEE Type	ADS5272	Recovery time	ADS5294	Recovery time
Upset in a single channel	34	25 ns	204	25 ns*
Upset in multiple channels	2	25 ns	91	25 ns*
SEFI A	2.0	1.6 μs	20	5 μs
SEFI B	0.6	on/off	—	—

- * in 15% of cases the recovery time is ~ 100 – 125 ns
- Based on 2500 ADCs, 2 fb^{-1} integrated luminosity in one fill. A safety factor of 2 was applied

The LHC Periodicities



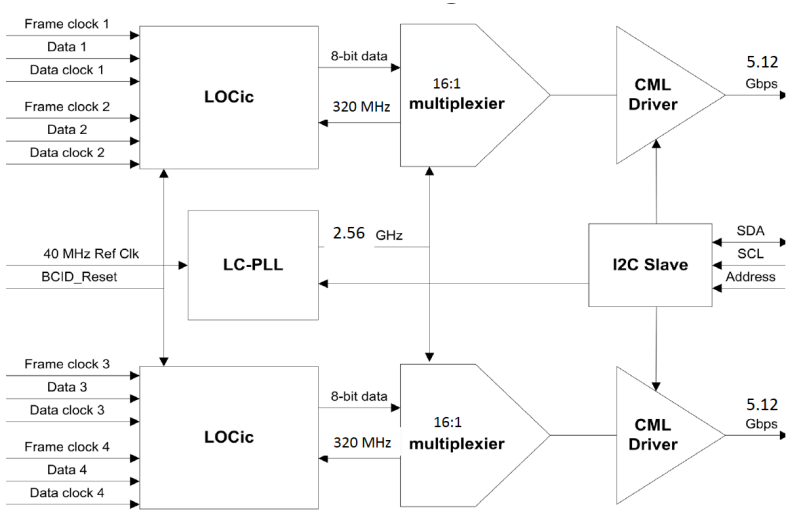
Can We Eliminate SEFI-B?

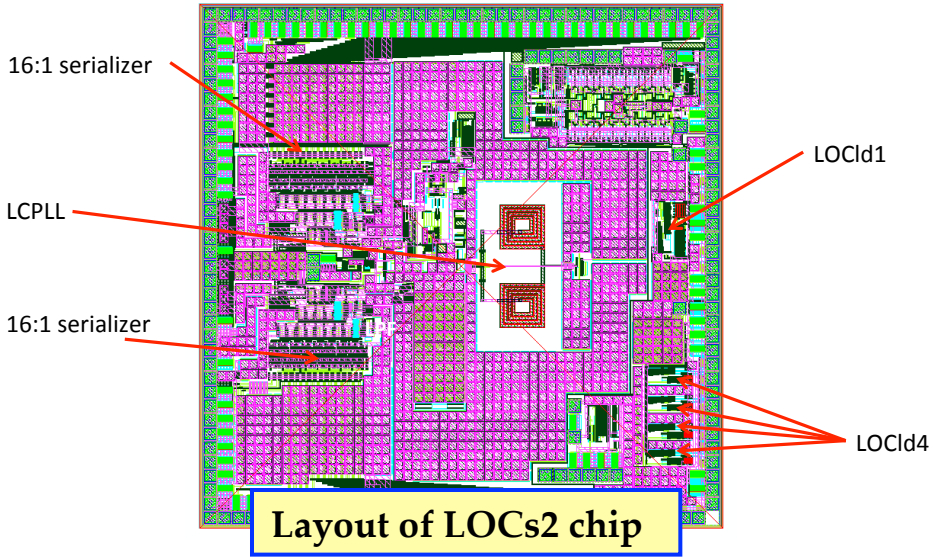
Can We Eliminate SEFI-B?

SEE Measurement	XADS5272	ADS5272(<100kRad)	ADS5272(>100kRad)
SEU(cm^2)	1.5×10^{-11}	1.2×10^{-11}	0.9×10^{-11}
SEFI-A(cm^2)	0.9×10^{-12}	0.7×10^{-12}	0.6×10^{-12}
SEFI-B(cm^2)	-	0.2×10^{-12}	1.5×10^{-12}

- XADS5272 is a new version of ADS5272 which has been specially designed to mitigate the micro-latchup according to the previous test results
  - SEE irradiation test of XADS5272 was performed at MGH, Boston
  - 3 samples were tested, 100K unit* protons (~300kRad) for each sample
  - Two kinds of SEU were observed: Single sample upset and multiple samples upset
  - No SEFI-B was observed
- XADS5272, ***hardened by TI***, has eliminated SEFI-B

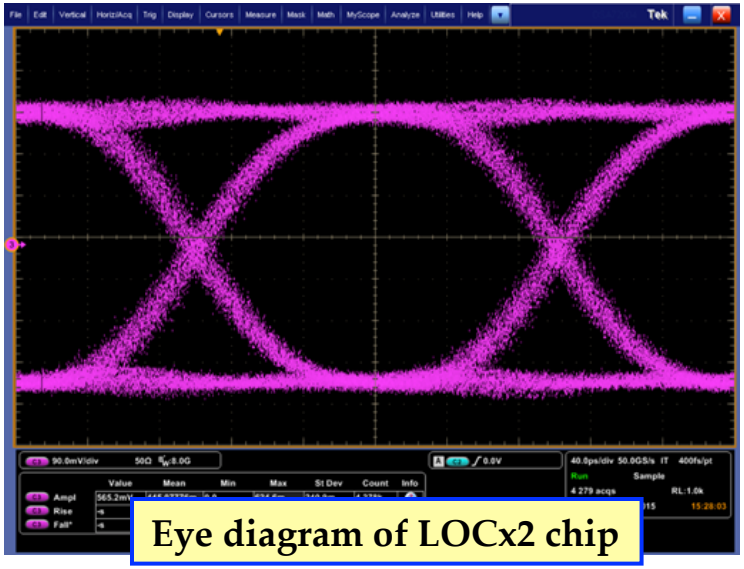
LTDB Optical Transmission





Layout of LOCs2 chip

- LOCs1: 1-ch 5Gbps 16:1 serializer has been designed, tested and radiation qualified
- LOCs2: 2-ch 8Gbps 16:1 serializer has been designed and tested
- LOCx2: an interface chip between ADC and optical transmitter has been designed. Preliminary evaluation test shows good performance

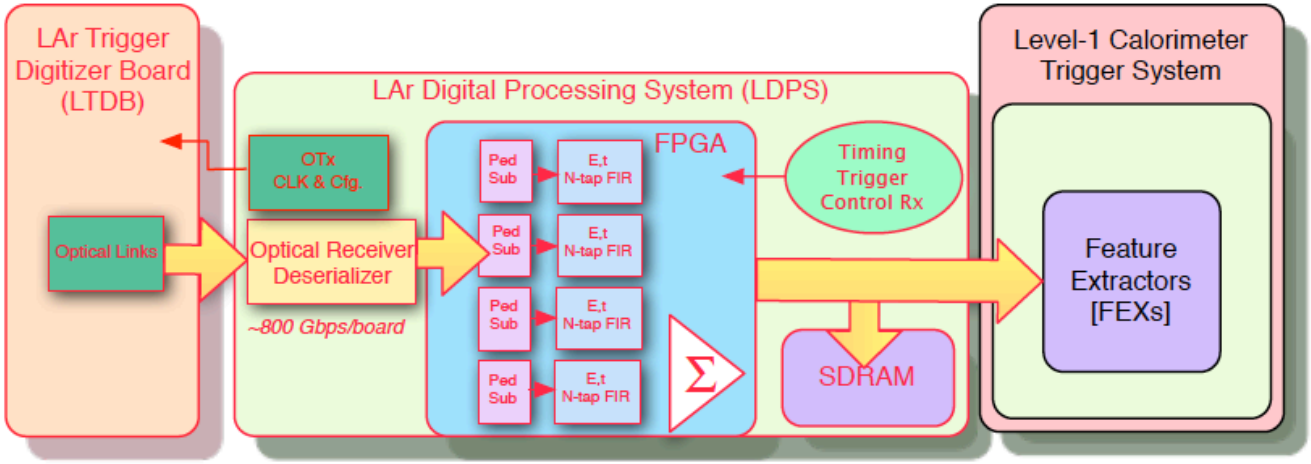


Eye diagram of LOCx2 chip

LTDB Power and Cooling Management

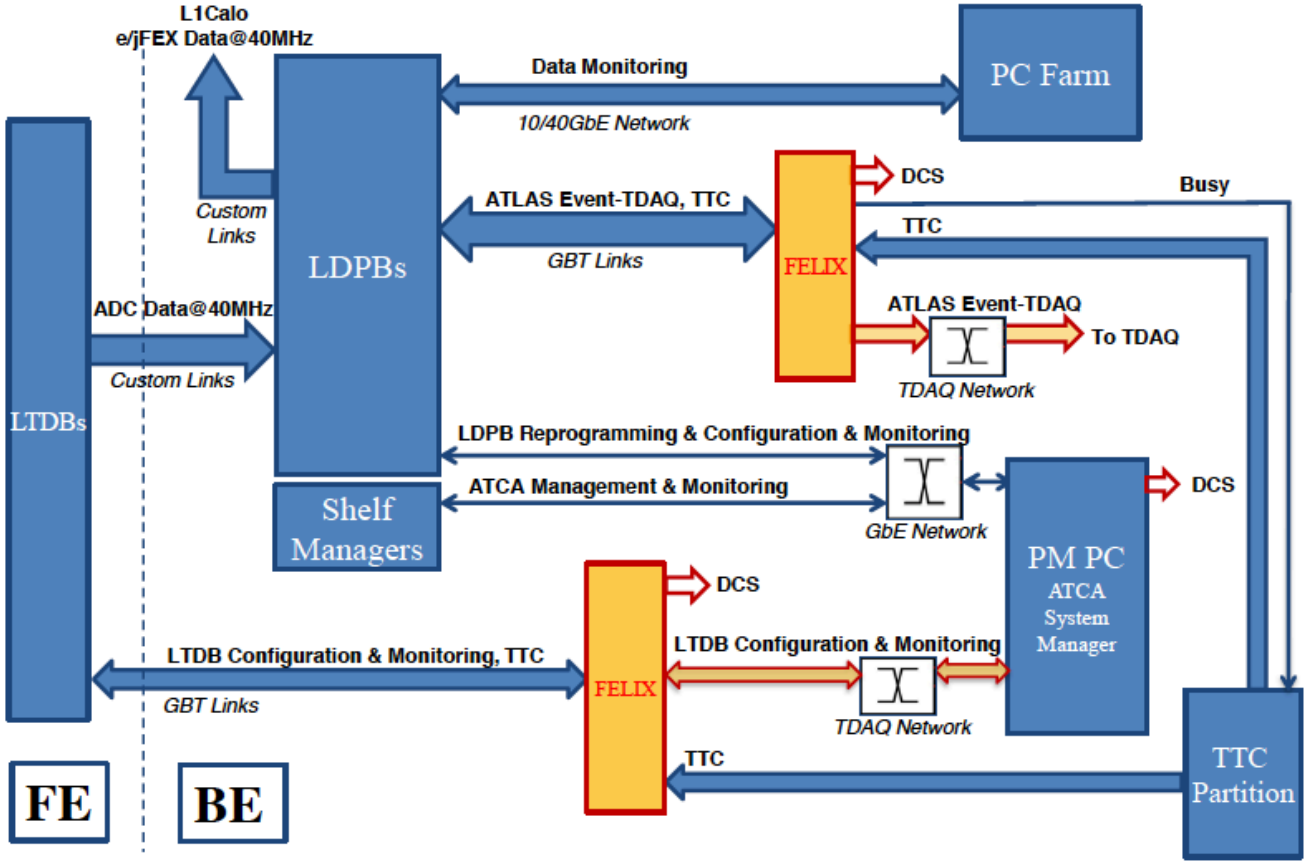
- Power Management
  - LTDB will have to survive Phase-II upgrade
  - Modular design to provide forward compatibility
  - POL and regulator
  - Following up CERN, APOLLO development in Italy and COTS
- Cooling Management
  - Spec cooling for 150W generated on LTDB
  - Design new cooling plates with 2x cooling channels
  - Fixed envelope (20mm pitch) puts many constraints on thermal management
  - Full thermal analysis will be conducted on LTDB model to guide the cooling plate design

LDPS Development



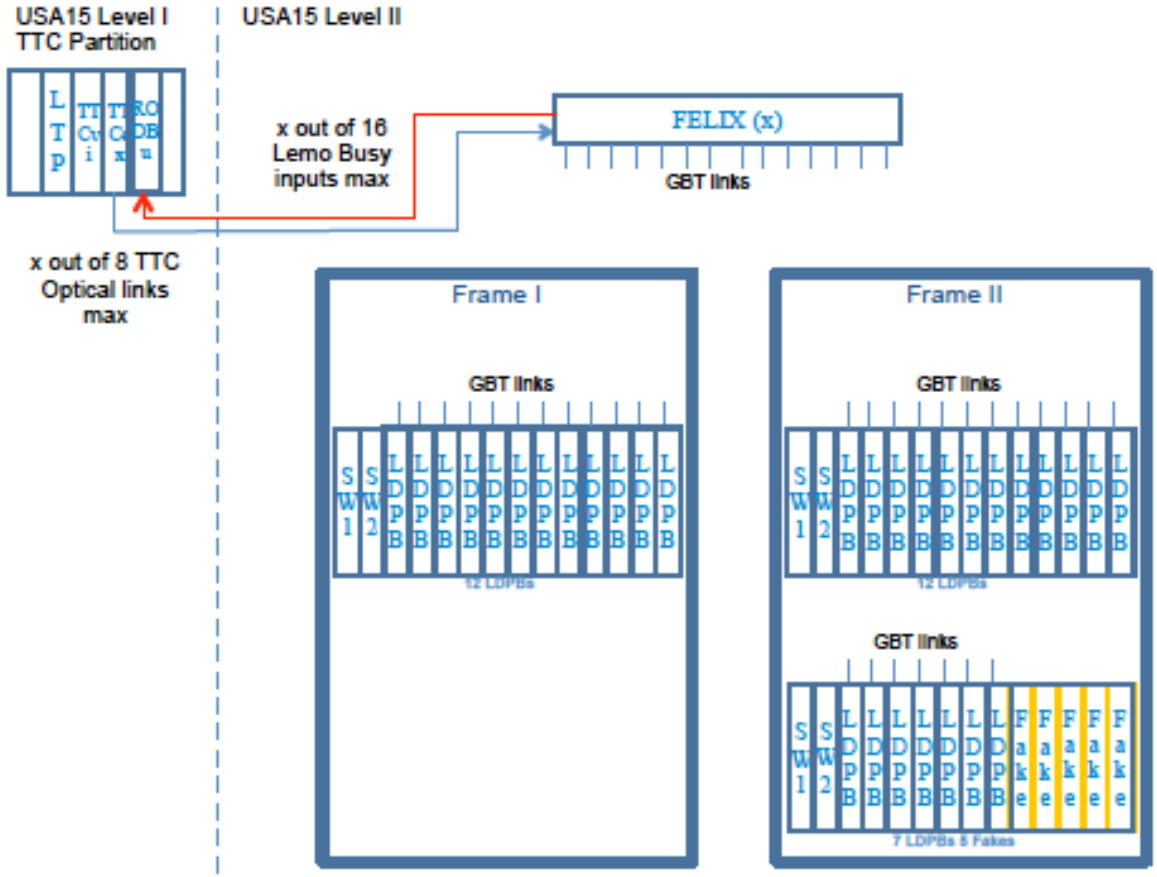
- LDPS is the bridge between the front end LTDB and L1Calo FEX
  - Receive high granularity super cell information from LTDB through optical links
  - Reconstruct energy and timing information by optimum filtering
  - Send calibrated energy information to FEX through optical links
- LDPS Development
  - LDPB: Liquid Argon Digital Processing Blade
  - LDPB is an ATCA carrier board with four AMC format sPUs (super Processing Unit), bandwidth is ~800Gbps
  - High speed parallel optical data transmission
  - FPGA embedded high speed transceiver for optical interface
  - FPGA embedded DSP for high speed parallel data processing

LDPS Development



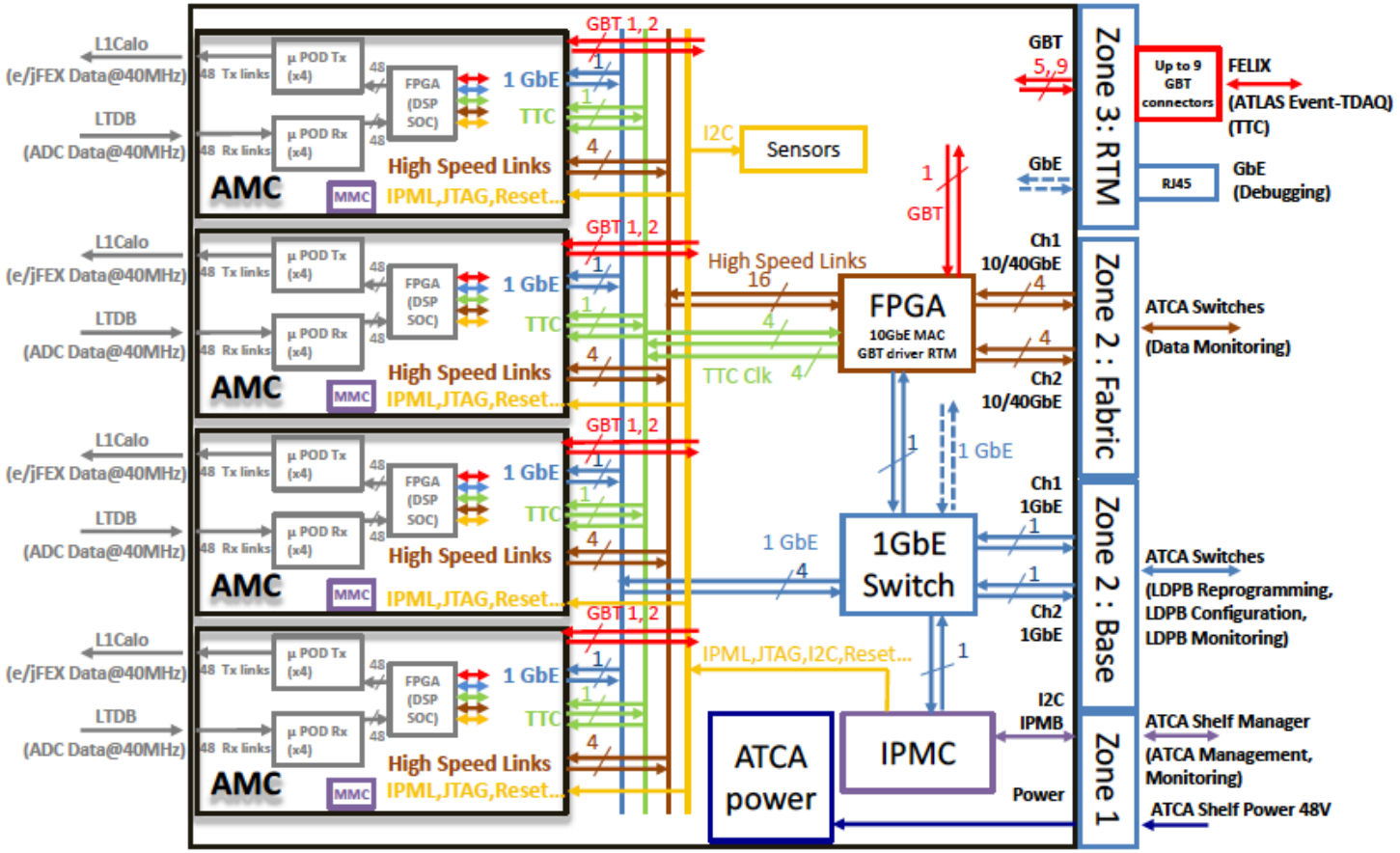
- Blue boxes: LDPB, Shelf manager, Partition Master (PM), TTC partition, PC farm are main components of LDPS
- Yellow boxes: FELIX, which is under TDAQ responsibility

LDPS Development



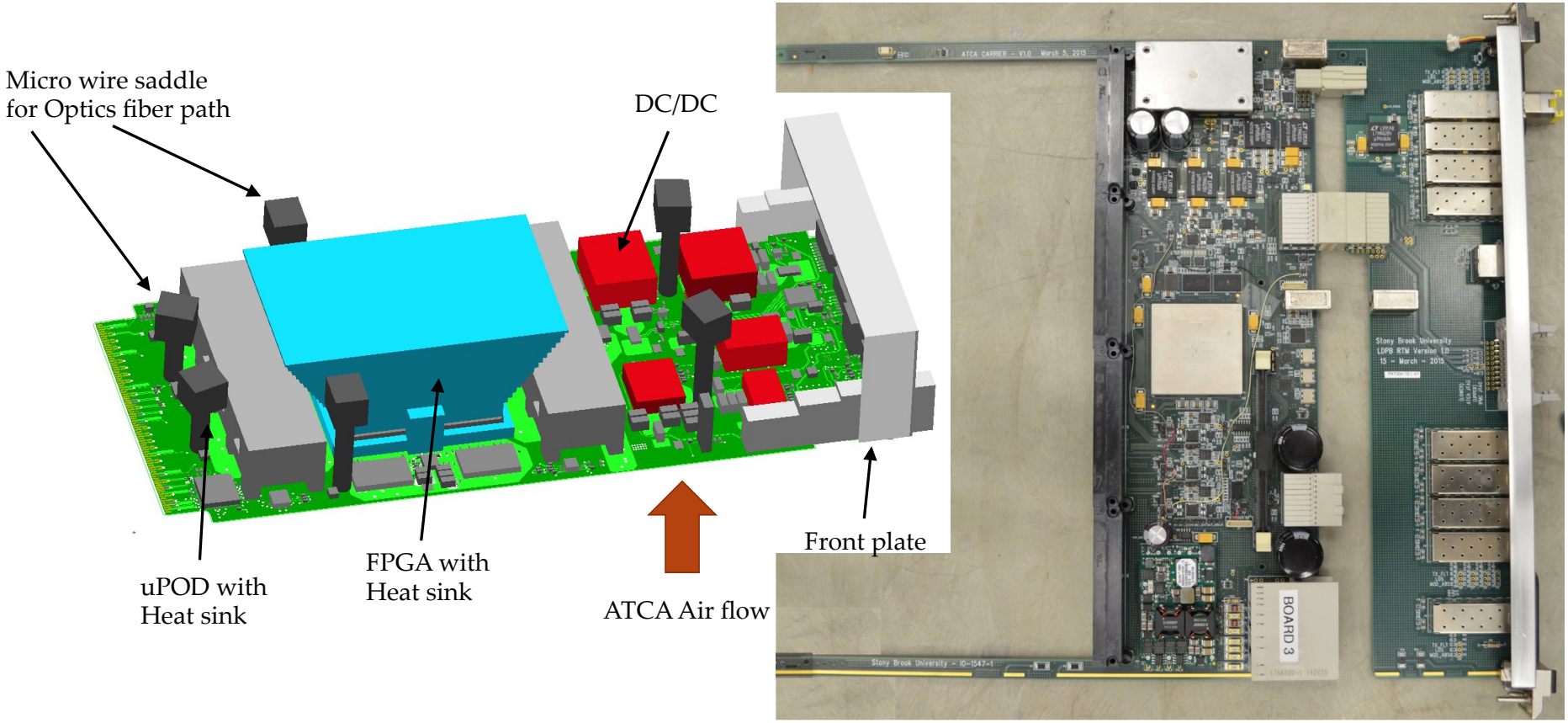
- The LAr Digital Processing System (LDPS) in two frames (racks) and three shelves (crates), along with the TTC and Busy signal treatment for Phase I
- The evolution for Phase II should be transparently handled by the FELIX interface

LDPS Development



- LDPB has two components
  - ATCA Carrier Board and AMC Mezzanine

LDPS Prototype Design



- Each ATCA carrier board will house 4 AMC mezzanines
- The first prototype LDPB carrier board has been built and being tested
- The first prototype AMC mezzanine has been designed and is being fabricated

MicroPOD on AMC Development

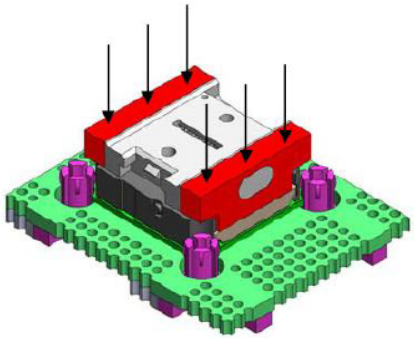
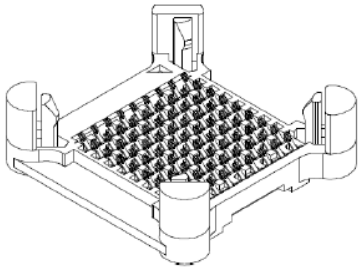
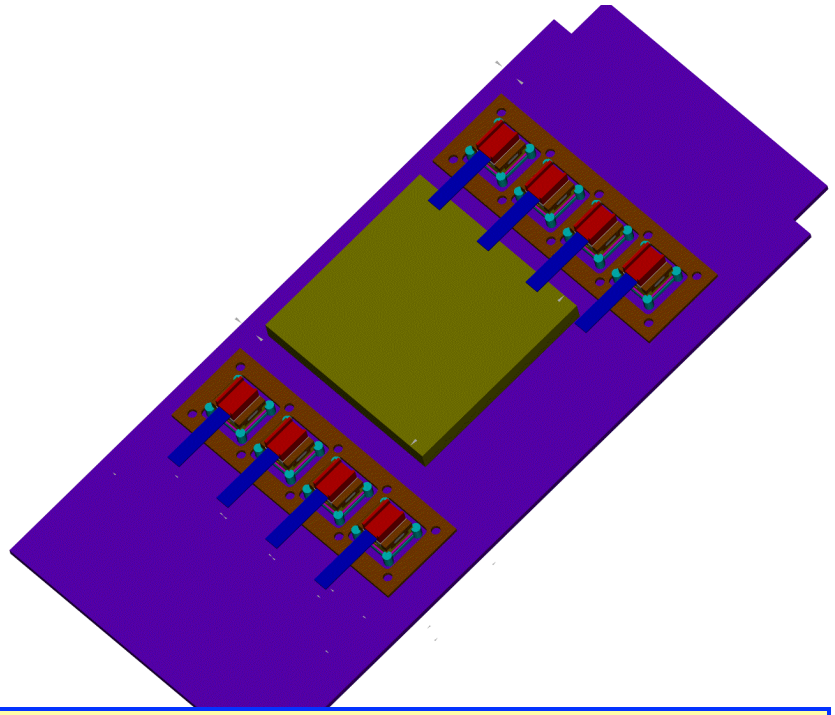


Illustration of force applied to MicroPOD in LGA socket

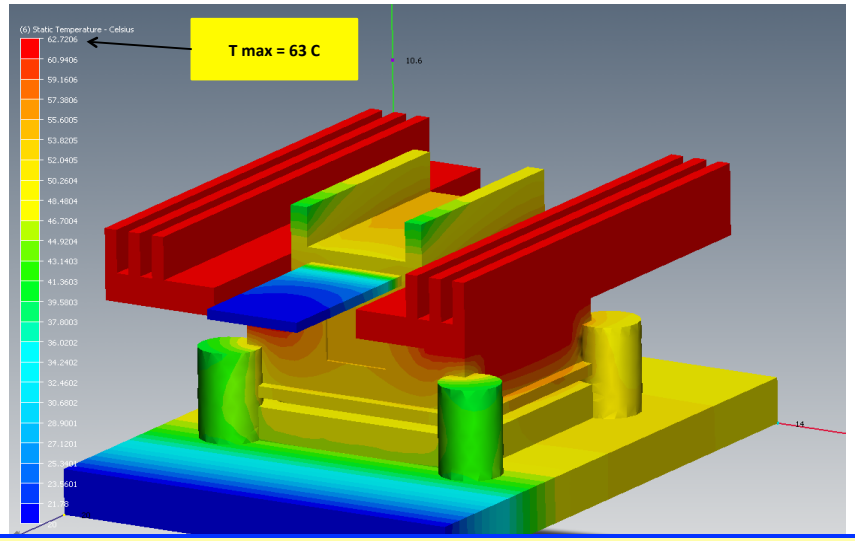


Example of μLGA interposer



Proposed layout of sPU with *eight* MicroPODs

TOTAL POWER GENERATED = 0.8 W, AIR FLOW = 200mm/sec



Thermal analysis of MicroPOD cooling assembly

- MicroPOD has been used by other customers successfully (IBM etc.)
- MicroPOD is a nice choice of AMC sPU module
  - Large volume of data transmission with very small footprint
- *However*
  - Very challenging in both mechanical and electrical designs
  - Cooling assembly needs to be developed

Electronics R&D for Phase-II Upgrade

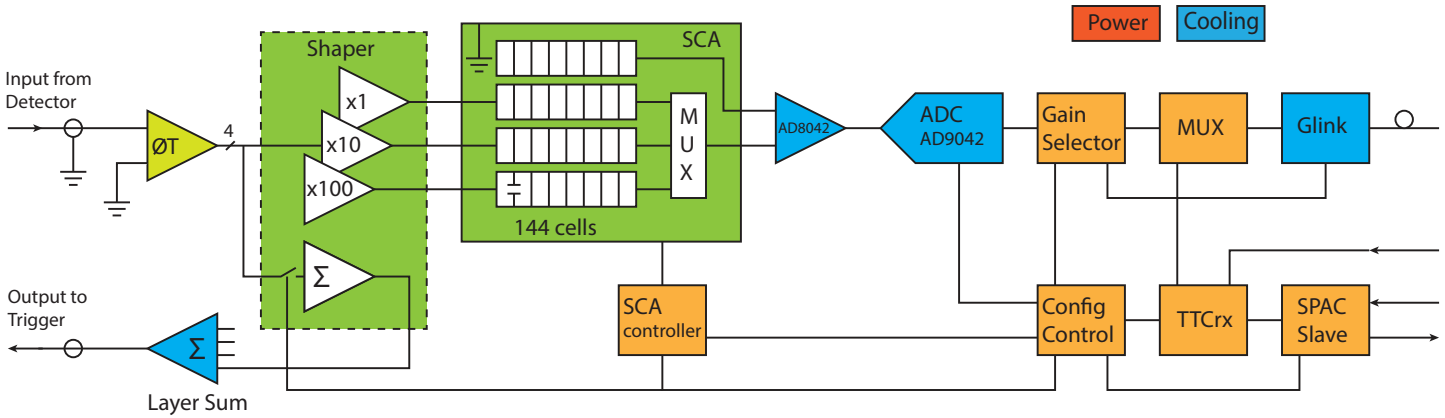
- FEB-2 Development
- ROD-2 Development

Electronics R&D for Phase-II Upgrade

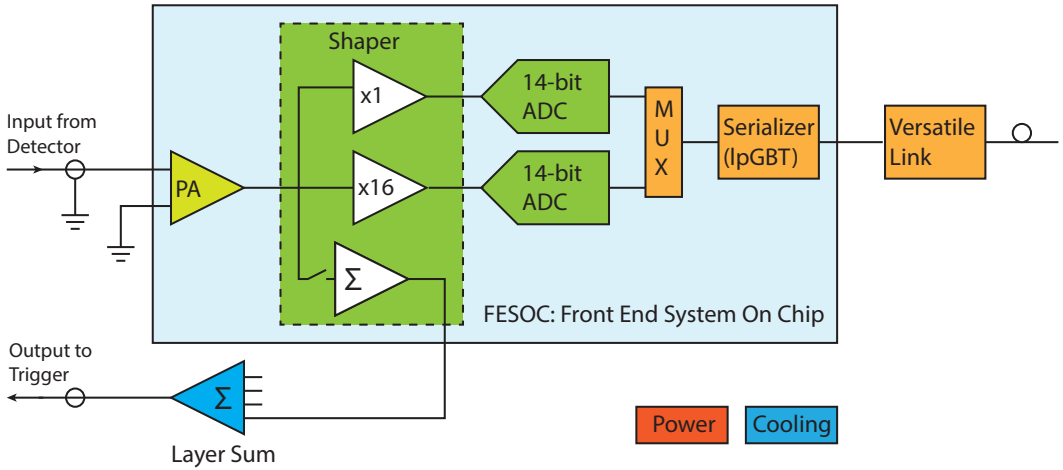
- New Front End Board (FEB-2 or LFEB)
  - Detector signal will be digitized and streamed off detector continuously
  - Full granularity of calorimeter information is available to L1Calo
- New Read Out Driver (ROD-2 or LPPR)
  - ROD-2 is the bridge between FEB-2 and TDAQ
  - ROD-2 provides L0 and L1 buffer, and interface to L1Calo
- Common development between Phase-I and Phase-II
  - Front end: cooling, power, radiation tolerance, digitization and optical transmission etc.
  - Back end: ATCA and AMC platform, large volume data transmission over fiber optical link and high speed DSP in FPGA etc.

Can We do Better in Phase-II Upgrade

- From



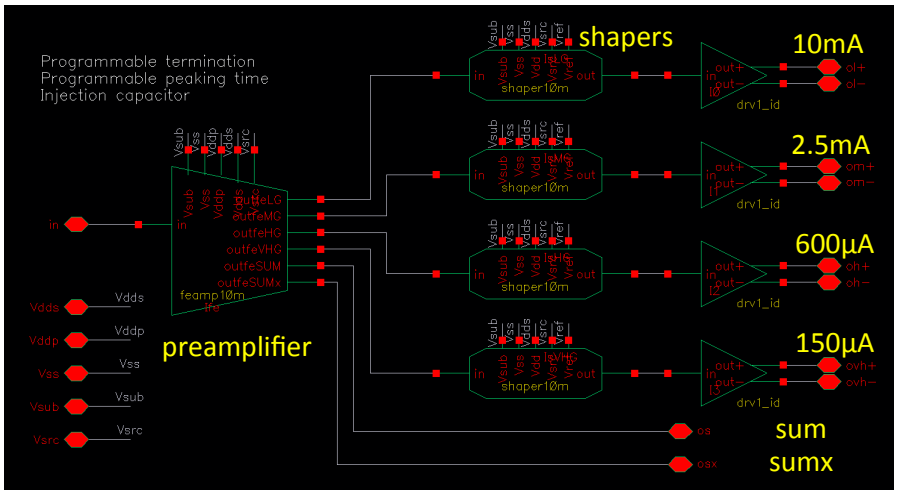
- To

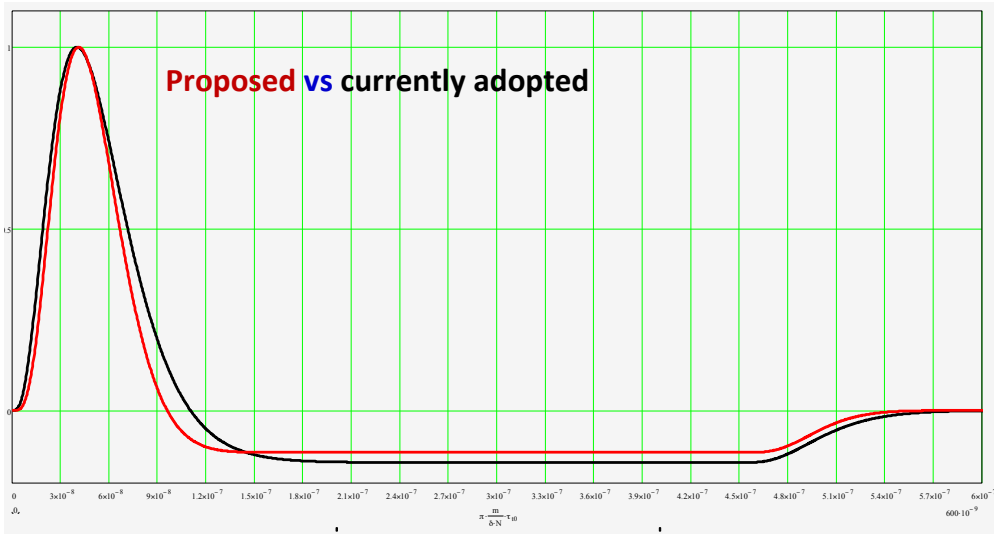


FESOC – Front End System On Chip

- FESOC will greatly simplify the design of FEB-2
  - Evaluation of FESOC will serve the purpose of prototype development of FEB-2
  - Full solution of FEB-2 will be gradually developed along FESOC development, from board design, power and cooling design, system integration to final production and installation
  - Limited R&D in early years is required for FEB-2 design and integration
- The main FEB-2 development will focus on chip level integration instead of board level integration
- FESOC will reduce the power consumption significantly
  - Will ease the system design, including LVPS and cooling
- 65nm CMOS is a potentially viable solution for FESOC
  - Need to demonstrate analog front-end with satisfactory performance
  - A few on-going developments for ADC
  - lpGBTx is being developed in 65nm CMOS at CERN

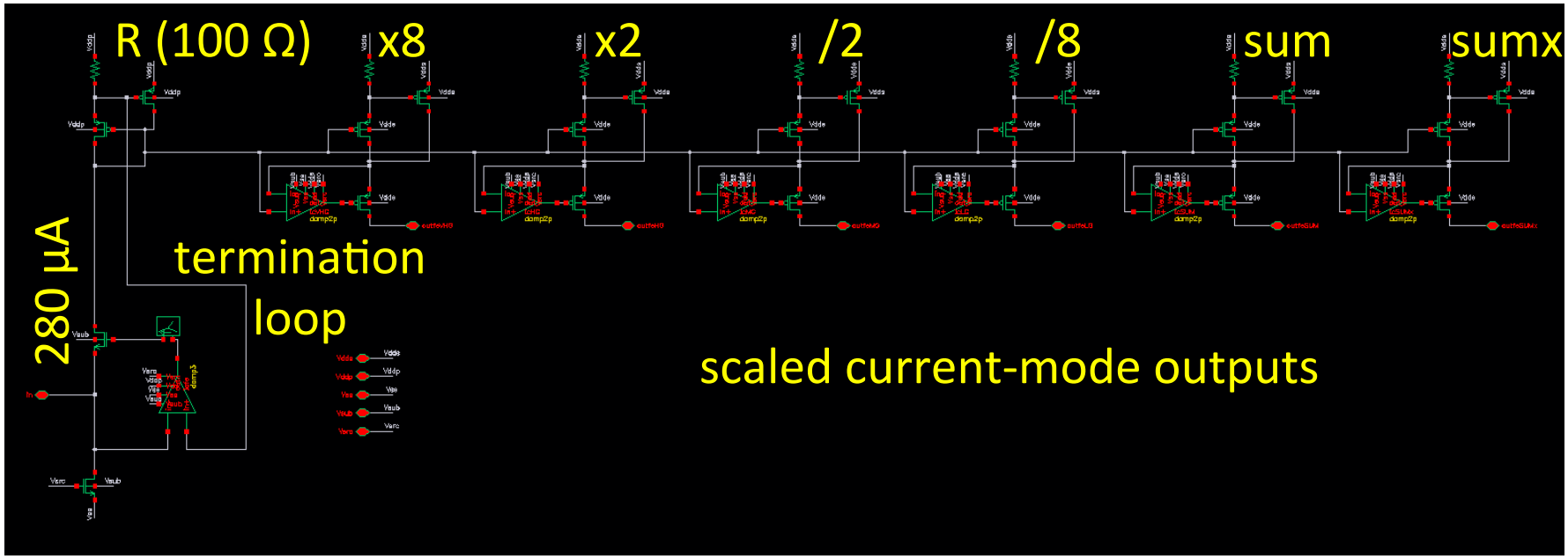
Preliminary design of analog frontend





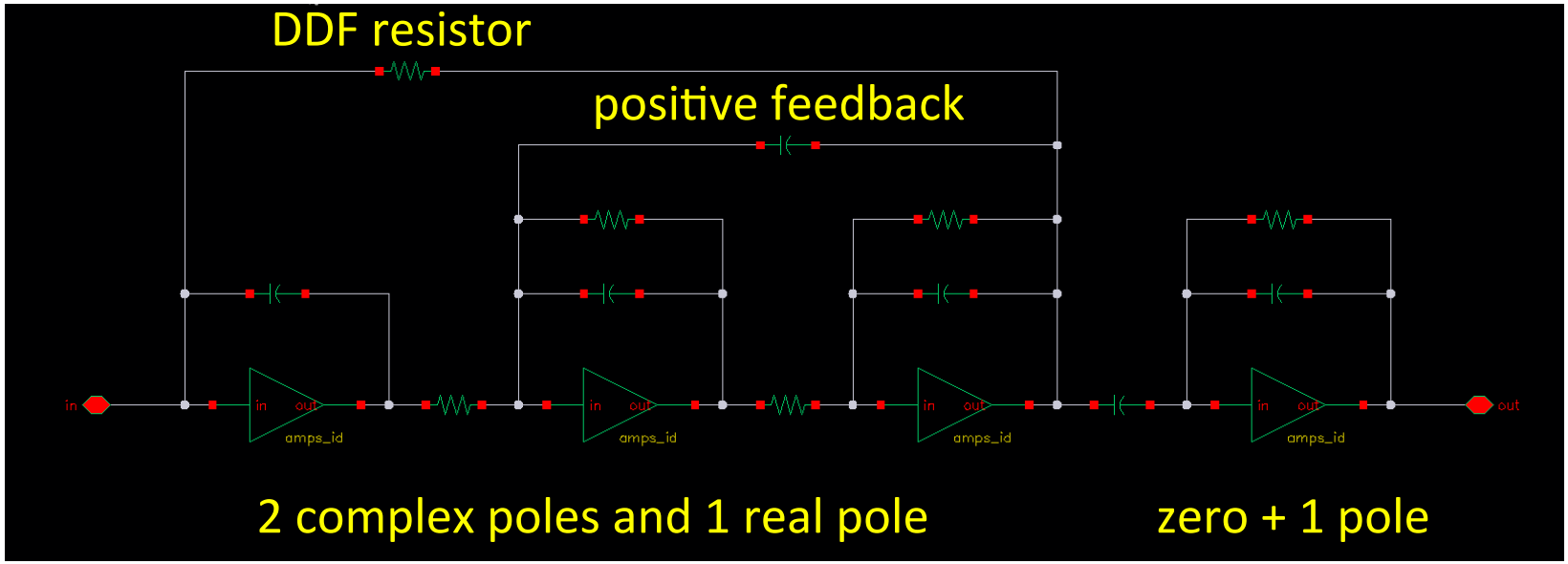
- Consider the middle layer of LAr EM barrel
- Preamplifier power dissipation ~48 mW with single 1.2 V supply
- Pseudo-differential unbalanced amplifier with in-line termination
- Four current-mode outputs to third order shapers with two complex-conjugate poles
- At equal peaking time offers smaller tail and faster return to baseline, thus lower the pile-up

Preamplifier



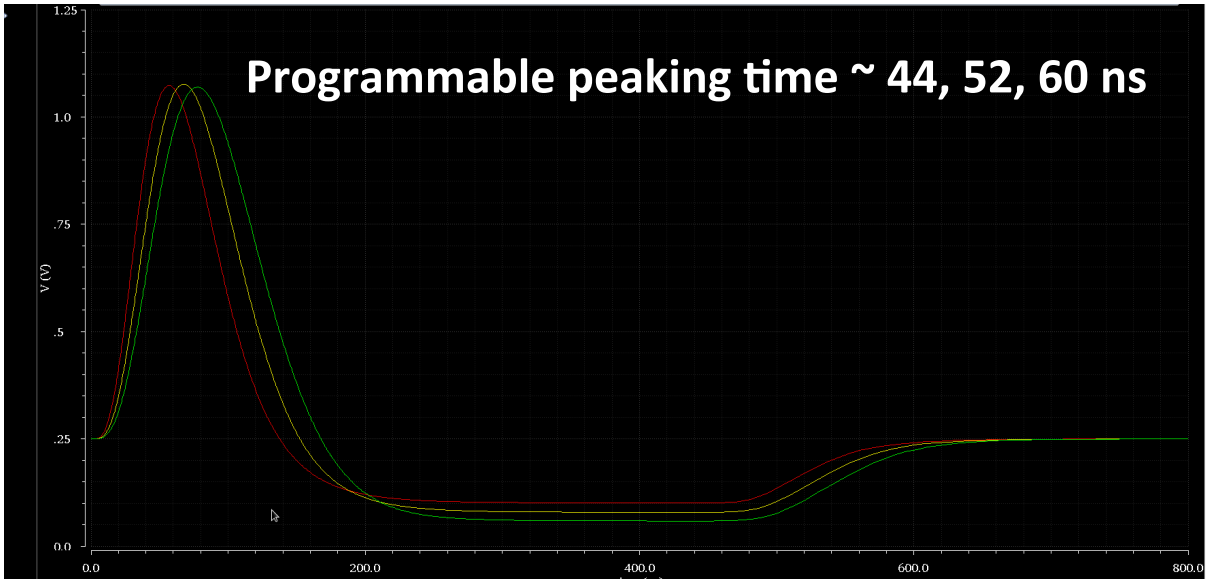
- Pseudo-differential unbalanced amplifier
- AC-coupled in-line termination resistance R
- Scaled mirror amplifiers
- Two sums range: S4 and S8

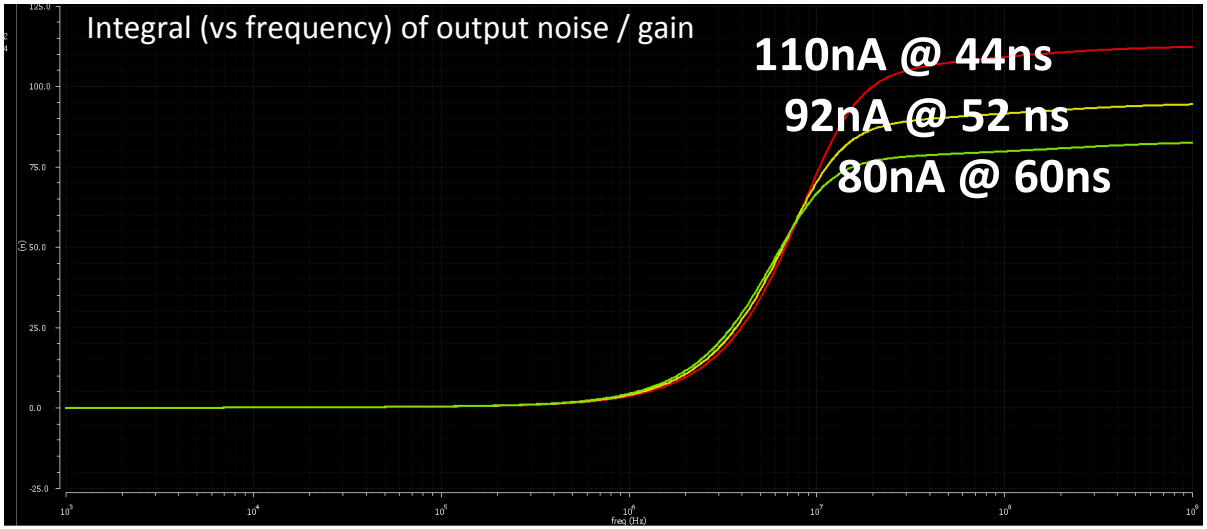
Shaper



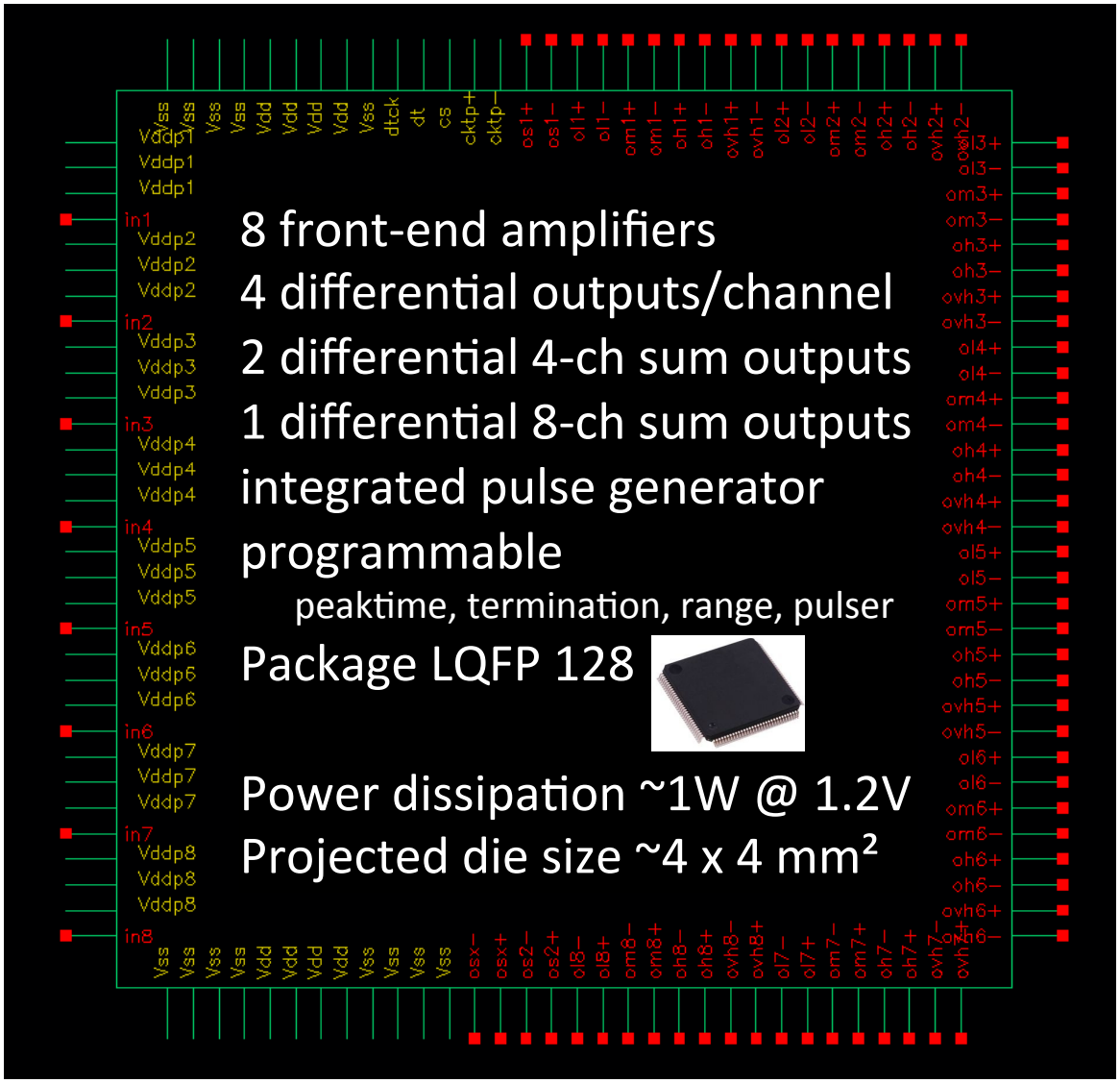
- Delayed dissipative feedback (DDF)
- Third order: 4 poles and 1 zero
- Two complex-conjugate poles
- Programmable
- Actual version will be mirror-based

Preliminary design of analog frontend





Top Level


8 front-end amplifiers
4 differential outputs/channel
2 differential 4-ch sum outputs
1 differential 8-ch sum outputs
integrated pulse generator
programmable
peaktime, termination, range, pulser
Package LQFP 128
Power dissipation ~1W @ 1.2V
Projected die size ~4 x 4 mm²

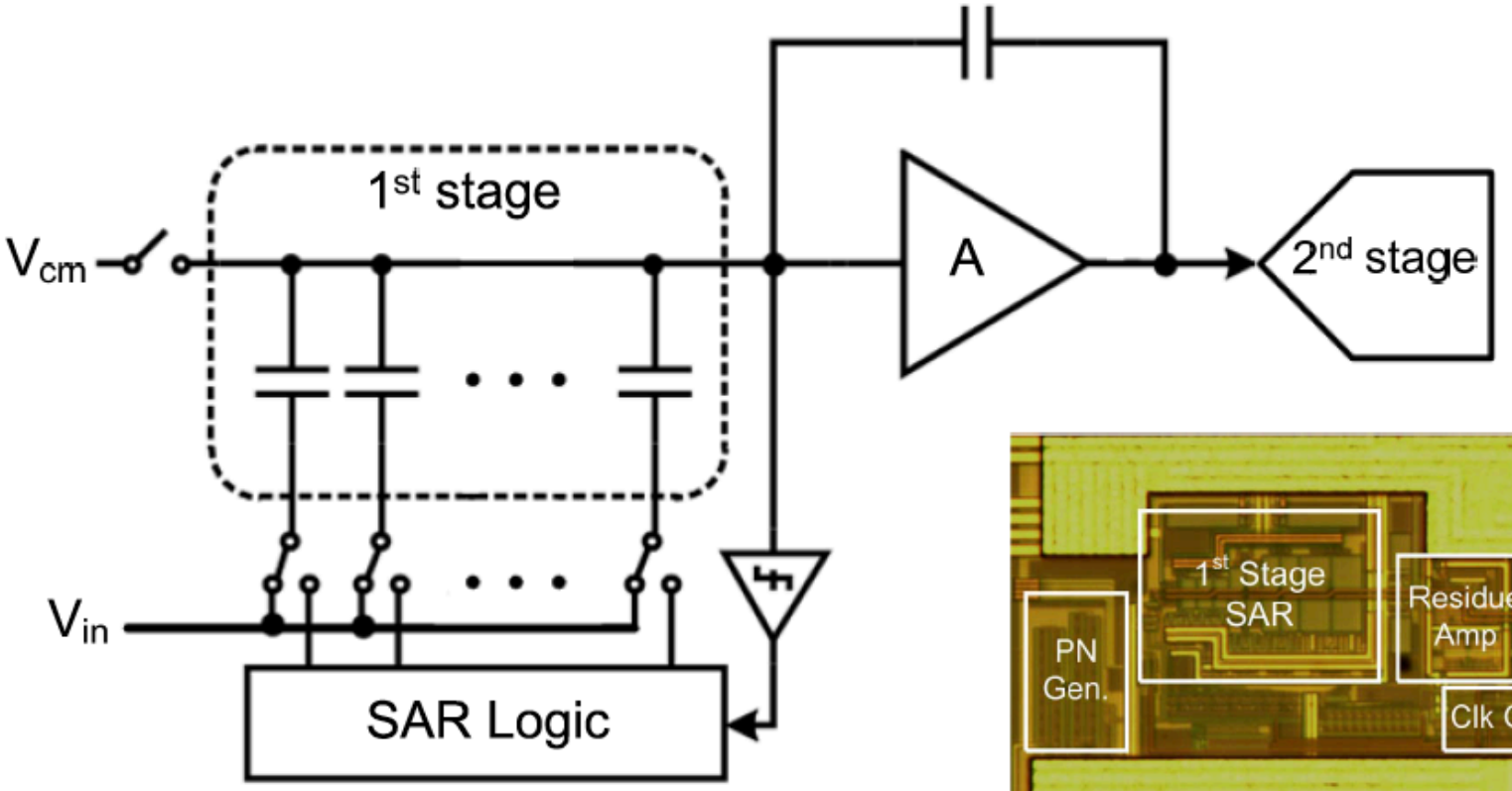
Promising features of the preliminary design

- Detector parameters
  - EMB Middle: 25 Ohm termination, 1.3 nF Cd and 10 mA range
  - EMB Strip: 50 Ohm termination, 250 pF Cd and 1 mA range
- Preliminary study shows very good performance
  - Stable impedance match to cover LAr signal bandwidth
  - Highest gain: ENI < 100 nA, Imax=150 μA (56 GeV), τ_{peak}= 44 ns
    - Current system: HG has Emax=25 GeV, ENI ~ 100 nA w/ OFC
- Electron/Photon performance
  - Simulation study is ongoing to understand noise contributions to the electron/photon resolution with different gain settings and dynamic ranges
  - Front end design will be optimized with inputs from simulation studies
- Investigating options in multiple gains
  - 4-gains with 10 bits ADC: low power, simplified ADC design
  - 2-gain with 12-14 bit ADC: simplified calibration and operation
  - Both can achieve noise performance comparable to the current system

ADC Development

- 12/14 bit, 80 MS/s, 25 mW
- 1.2 V, 65-nm CMOS technology to pave the road for future integration with analog front end
- SAR architecture and digital calibration based on previous designs
  - [1] Y. Zhou, B. Xu, and Y. Chiu, "A 12b 160MS/s synchronous two-step SAR ADC achieving 20.7fJ/step FoM with opportunistic digital background calibration," in IEEE Symp. VLSI Circuits, Dig. Tech. Papers, Jun. 2014, pp. 239–240.
  - [2] W. Liu, P. Huang, and Y. Chiu, "A 12b 22.5/45MS/s 3.0mW 0.059mm^2 CMOS SAR ADC achieving over 90 dB SFDR," in IEEE ISSCC, Dig. Tech. Papers, Feb. 2010, pp. 380–381.
- TID of the existing design verified
- SEE will be addressed in the current design

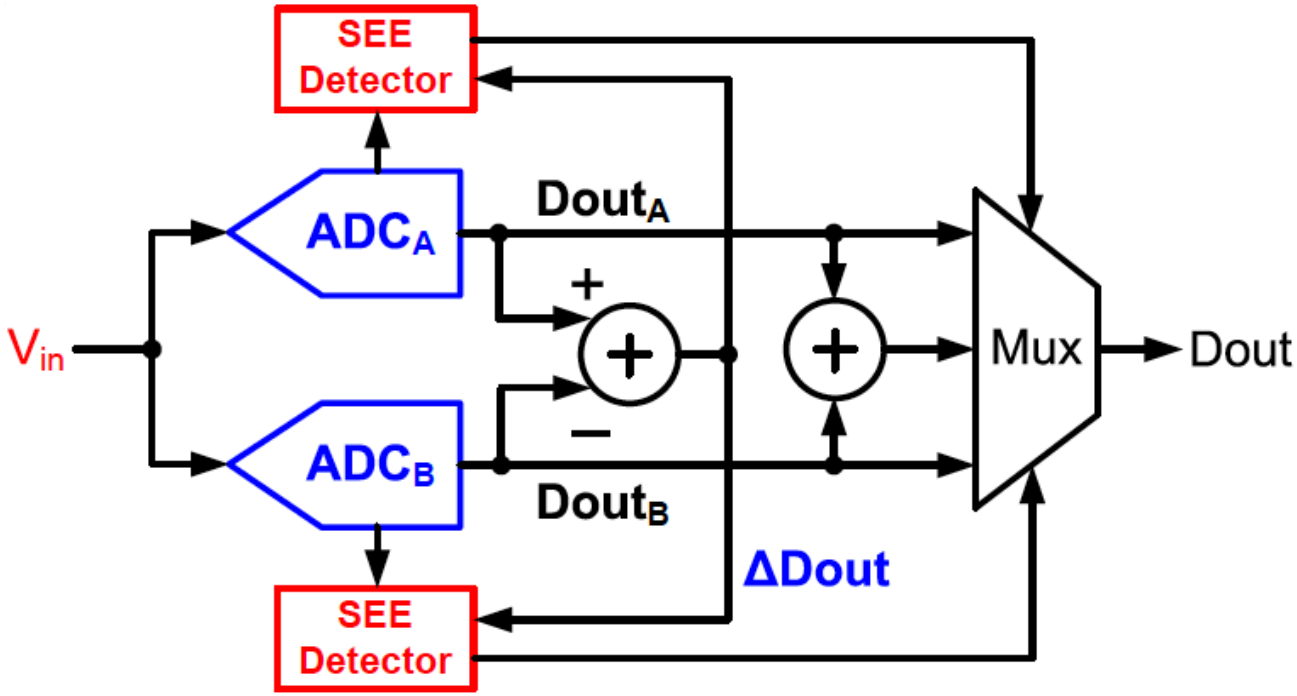
Architecture – Pipelined SAR



[1]

- Fewer number of bits in first stage
- Amplifier removed from SAR Loop
- Easier to get fast conversion

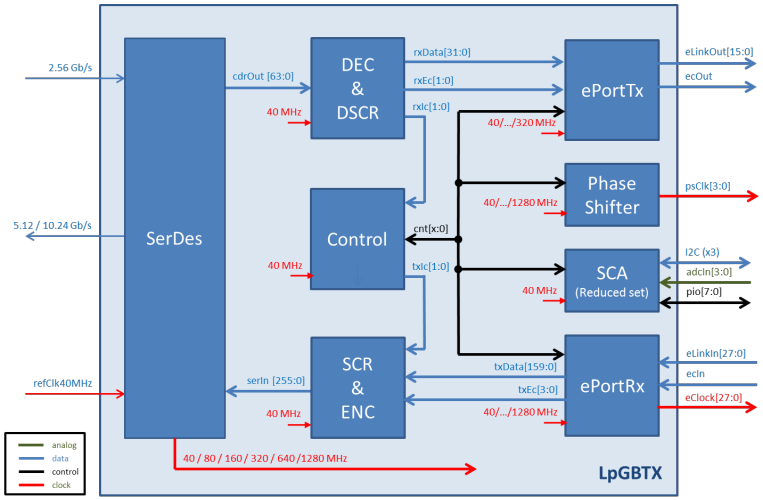
SEE – Split-ADC Redundancy



- 3-dB SNR gain under normal condition (no SEE)
- If ΔDout is large, chose the output of the ADC that is not hit
- Split-ADC also enables digital background calibration

lpGBT Development

- lpGBTx development at CERN
- Bandwidth
  - Low-Power mode
    - 2.56 Gb/s for the optical down link
    - 5.12 Gb/s for the optical up link
  - High-Speed mode
    - 2.56 Gb/s for the optical down link
    - 10.24 Gb/s for the optical up link
- Downlink is using FEC-12 for reliable transmission
- 65nm CMOS technology, IP will be available to be integrated into the LAr FESOC



Option	37
Frame (bits)	**64**
Header (bits)	**4**
Coded header	**Yes**
User field (bits)	**36**
Code (bits)	24
8-bit multiplicity	4.5
User Bandwidth (GHz)	1.44
# eLinks groups (8 bit)	4
eLinks bandwidth (MHz)	80/160/320
#eLinks	16/8/4
EC bandwidth (MHz)	80
IC bandwidth (MHz)	80
Corrected (bits)	**12**
Efficiency	**56%**

lpGBT Development

Bit rate	5.12 Gb/s	10.24 Gb/s
Option	7	7
Frame (bits)	128	2 x 128
Header (bits)	4	4
Coded header	Yes	Yes
User field (bits)	114	228
Code (bits)	10	20
16-bit multiplicity	7.125	14.25
User Bandwidth (GHz)	4.56	9.13
# eLinks groups (16 bit)	7	7
eLinks bandwidth (MHz)	160/320/640	320/640/1280
#eLinks	28/14/7	28/14/7
EC bandwidth (MHz)	0	80
IC bandwidth (MHz)	80	80
Corrected (bits)	5	2 x 5
Efficiency	89%	89%

FEC-5

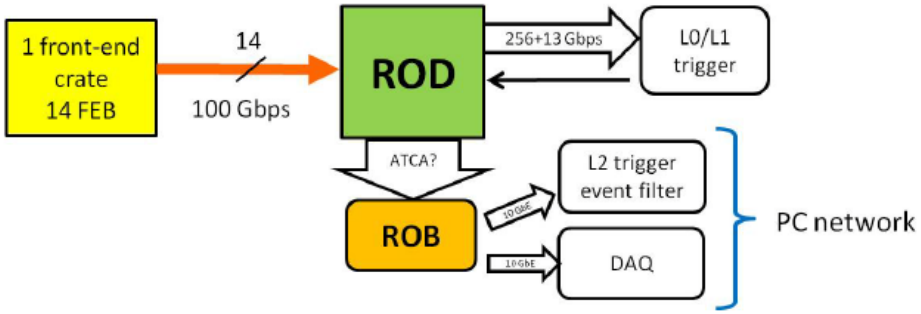
Bit rate	5.12 Gb/s	10.24 Gb/s
Option	28	28
Frame (bits)	128	2 x 128
Header (bits)	4	4
Coded header	Yes	Yes
User field (bits)	100	200
Code (bits)	24	48
16-bit multiplicity	6.25	12.5
User Bandwidth (GHz)	4	8
# eLinks groups (16 bit)	6	6
eLinks bandwidth (MHz)	160/320/640	320/640/1280
#eLinks	24/12/6	24/12/6
EC bandwidth (MHz)	80	80/160
IC bandwidth (MHz)	80	80/160
Corrected (bits)	12	2 x 12
Efficiency	78%	78%

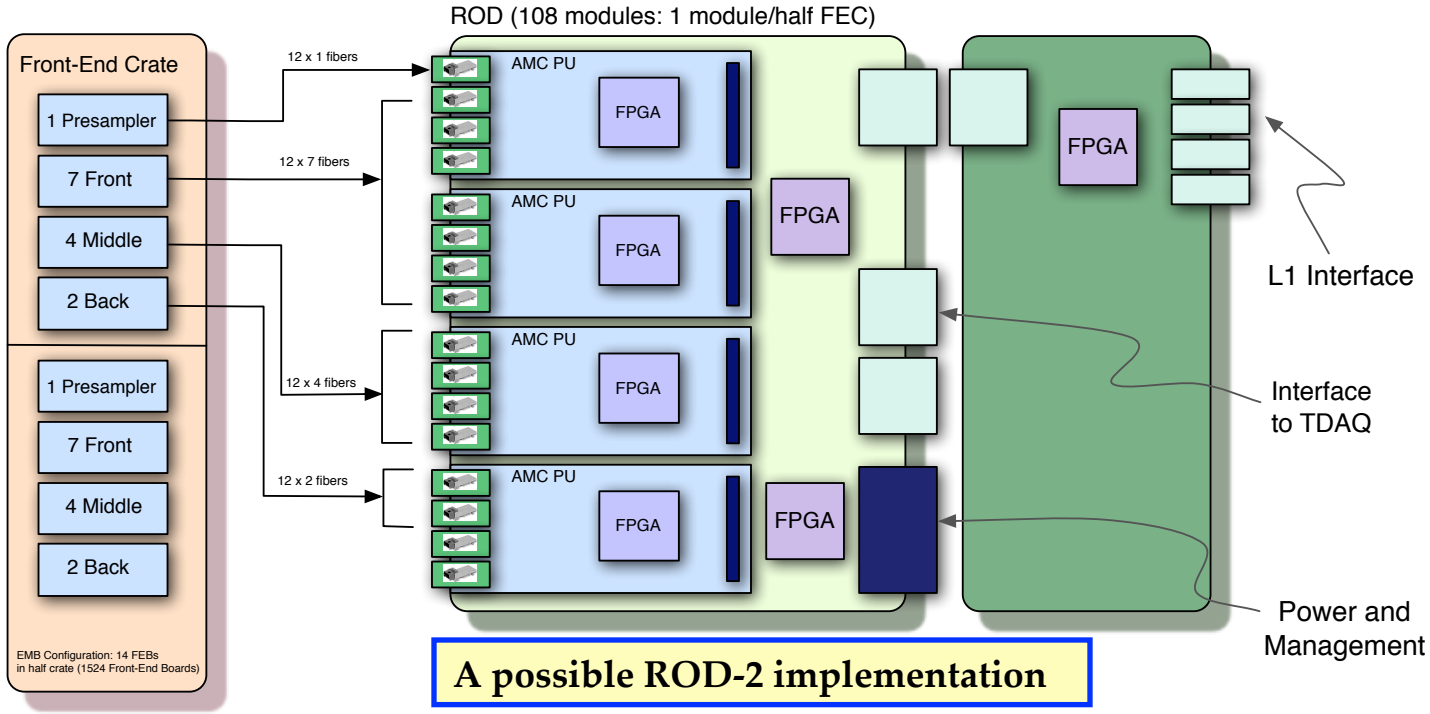
FEC-12

- Uplink is using either FEC-5 or FEC-12 depends on the different requirements
  - FEC-5 is targeting to the high bandwidth
  - FEC-12 is targeting to the SEU tolerance

ROD-2 Development

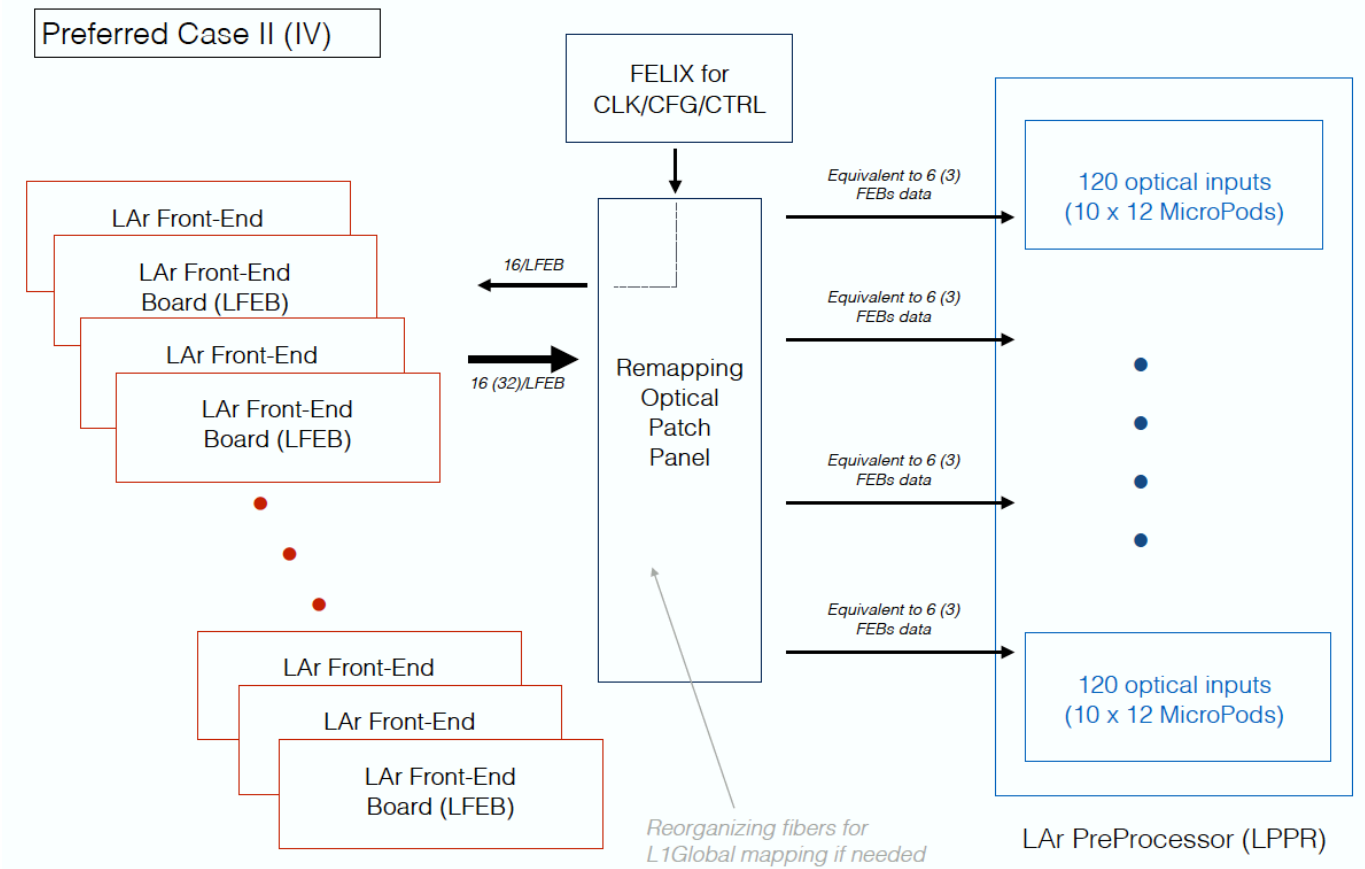
- Data bandwidth of entire LAr w. 1524 FEB-2s > 150Tbps
  - High speed parallel fiber optical transceiver (e.g. 12 fibers @ 10Gbps)
  - Address issues of bandwidth and achievable integration on the ROD-2
  - ROD-2 based on FPGA high speed SERDES and FPGA based DSP to take advantage of parallel data processing
  - Perform L1 trigger sum digitally after E-conversion with flexible and finer granularity within a realistic latency budget





A possible ROD-2 implementation

Phase-II Architecture and Data Flow



- LFEB/FEB-2 sends data to LPPR/ROD-2 over high speed fiber optical links continuously
- LPPR will provide ***full granularity*** of calorimeter information to L1Calo trigger system based on L0Calo trigger decision

Summary

- Radiation tolerance, natural aging of the electronics and higher selectivity of the L1 calorimeter trigger to keep L1 rate below 100kHz are the driving motivations for an upgrade of the front-end electronics
- Phase-I Upgrade ~2019
  - Upgrade of calorimeter trigger electronics
  - Front end LTDB
  - Back end LDPS
- Phase-II Upgrade ~2024
  - Full upgrade of readout electronics
  - Front end FEB-2
  - Back end ROD-2
- Readout architectures are well defined, many challenges need to be overcome
  - Modern technology requires lower voltages, difficult to maintain the required large dynamic range and stringent noise performance
  - Critical radiation hard components (analog front-end, ADC, optical link and power supply)
  - Extremely large bandwidth off-detector readout
  - High performance data handling with very strict latency budget

Backup Slides

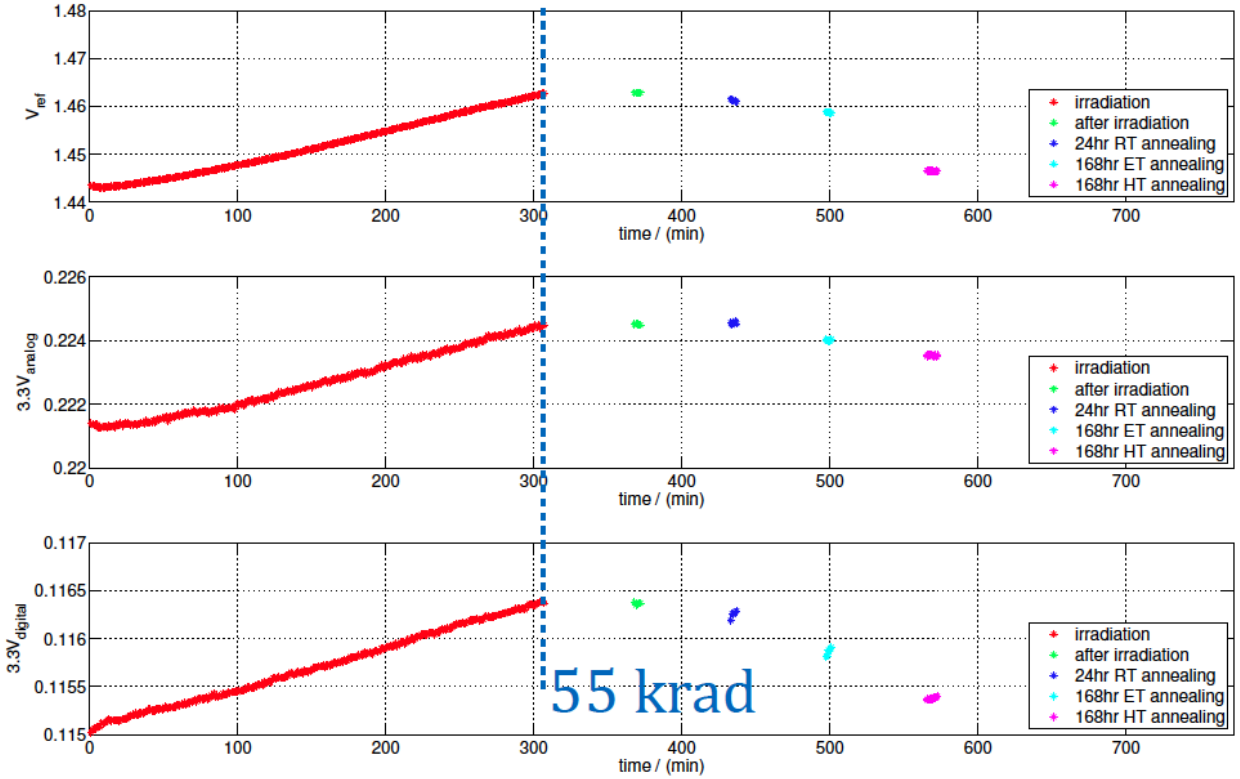
The Radiation Background

	Simulation (per fb^{-1})	Safety Factor	Test Target (for 3000 fb^{-1})
Ionizing Dose	3.0 rad	7.5	67.5 krad
1 MeV eq. neutron	2.0×10^{9}	2	1.2×10^{13}
Hadrons (> 20 MeV)	2.84×10^{8}	2	1.7×10^{12}

- ***We assume single lot purchase, simulation SF 1.5 and low dose rate SF = 5 for TID***
- The radiation background in the LAr Barrel electronics crates is composed of hadron, electrons and photons produced in the last stages of the particle shower in the calorimeters

Annealing Test of ADS5272

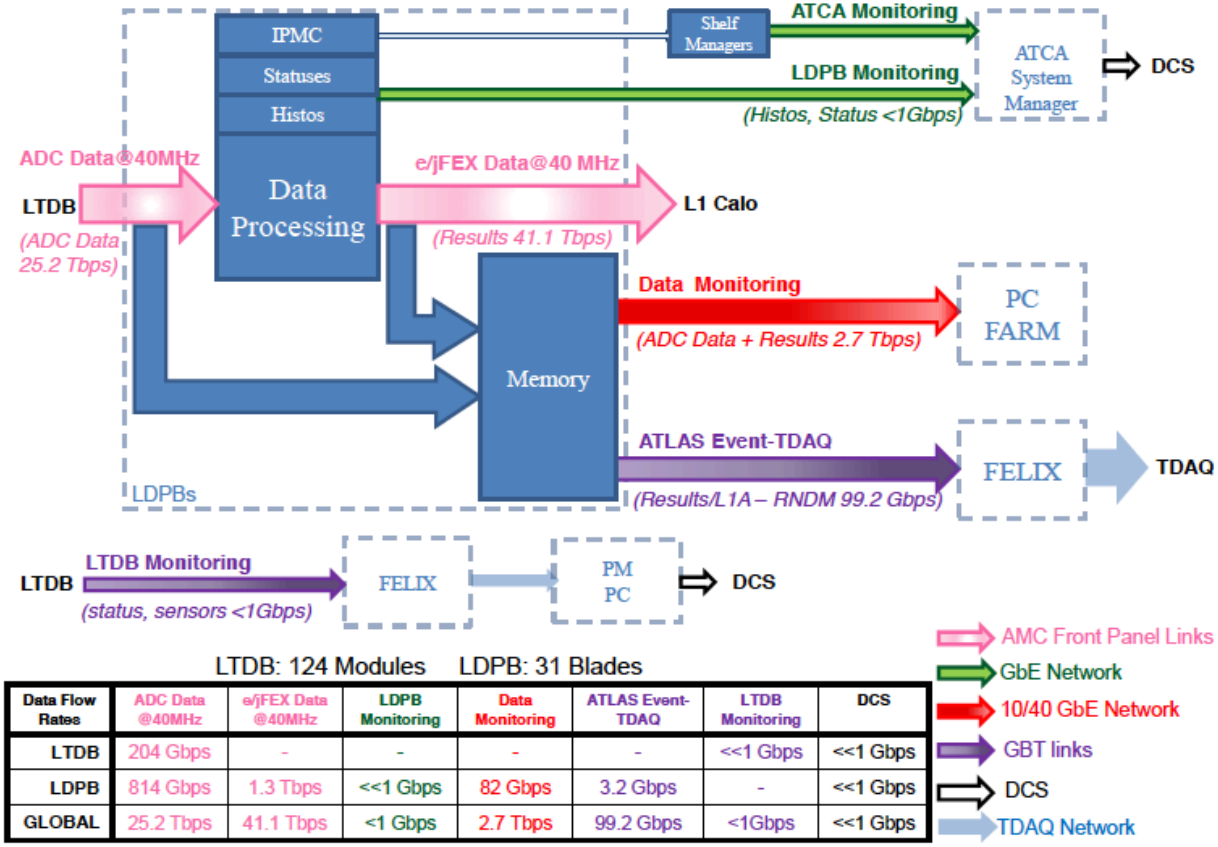
- We follow the **ATLAS Policy on Radiation Tolerant Electronics** that states:
- Annealing test should be performed on 20 samples for pre-selection
- Total dose should be 54 krad from the estimate below
- RTC_{TID} = 3 rad/fb^{-1} * 3000 fb^{-1} * 1.5 (Sim SF) * 4 (Lot SF)
- 168-hour annealing under room temperature
- 168-hour annealing under 100 °C



time points	IRR. start	IRR. stop	0-hr RT	24-hr RT	168-hr RT	168-hr HT
REF Vol.(V)	1.4431	1.4627	1.4629	1.4610	1.4586	1.4465
+3.3VA (mA)	221.3	224.5	224.5	224.5	224.0	223.5
+3.3VD (mA)	115.1	116.4	116.4	116.3	115.9	115.4

- Controlled annealing test of 20 ADS5272 samples
- 20 samples were tested ***ALL*** with similar response.

LDPS Development



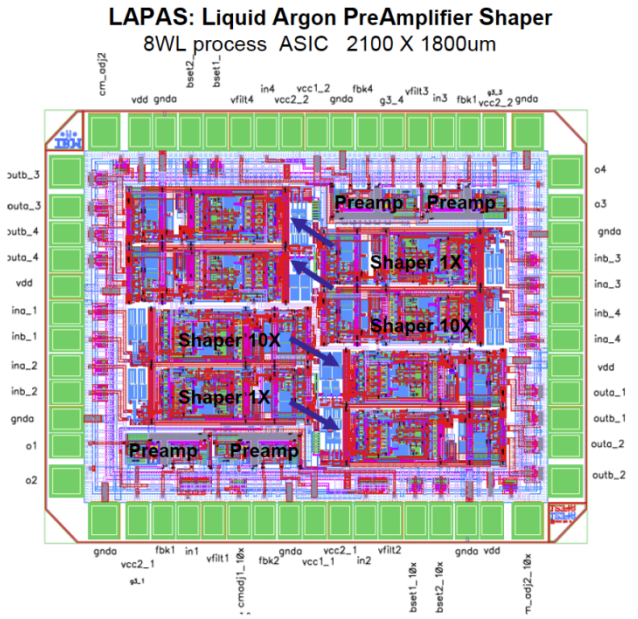
LTDB: 124 Modules LDPB: 31 Blades

Data Flow Rates	ADC Data @40MHz	e/jFEX Data @40MHz	LDPB Monitoring	Data Monitoring	ATLAS Event-TDAQ	LTDB Monitoring	DCS
LTDB	204 Gbps	-	-	-	-	<<1 Gbps	<<1 Gbps
LDPB	814 Gbps	1.3 Tbps	<<1 Gbps	82 Gbps	3.2 Gbps	-	<<1 Gbps
GLOBAL	25.2 Tbps	41.1 Tbps	<1 Gbps	2.7 Tbps	99.2 Gbps	<1Gbps	<<1 Gbps

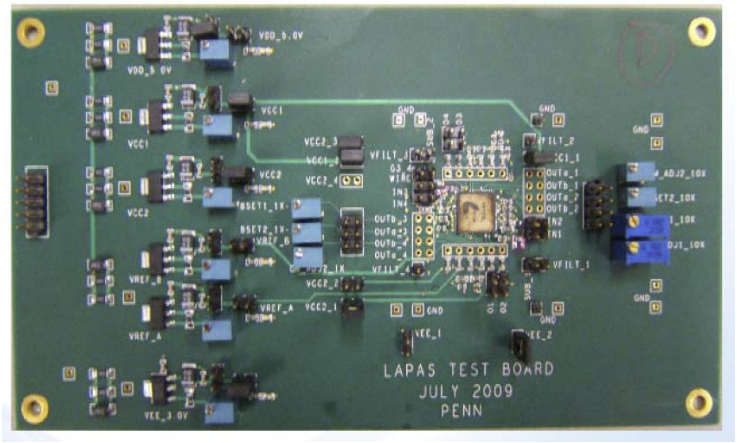
- Data flow of LDPS
  - L1Calo path, TDAQ path, DCS path and Monitoring path

FEB-2 Development: Analog Front-End

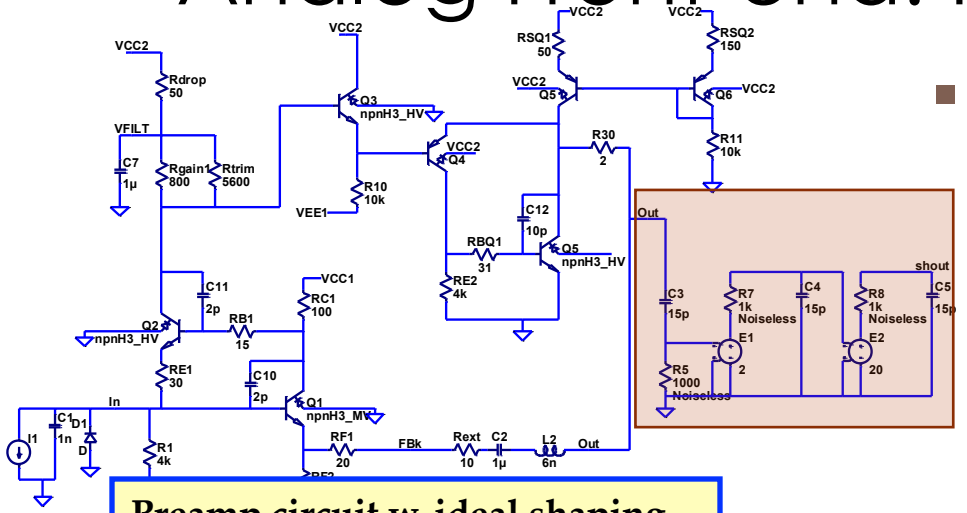
- LAPAS ASIC
  - Quad preamplifier & shaper ASIC in IBM 0.13µm SiGe 8WL
- Preamplifier
  - Based on low noise line-terminating preamplifier circuit topology used presently
  - High breakdown devices allow for higher swing to accommodate full 16-bit dynamic range
  - e_n ~ 0.26nV/√Hz
  - ENI ~ 73nA RMS (included 2nd stage and for C_d = 1nF)
  - P_{tot} ~ 42mW
- Shaper
  - 16-bit dynamic range with two gain settings
  - e_n ~ 2.4nV/√Hz
  - ENI ~ 34nA RMS
  - P_{tot} ~ 130mW (combined 1X, 10X channels)
  - Uniformity: better than 5% across 17 tested ASICs
  - INL: < 0.1% over full scale of 1X and 10X channels
- Test Results
  - All measurements as expected
  - DC results very close to simulations, shaper peaking time is 37ns as predicted
  - Preamp and shaper transient response is good, no shaper control tuning required
  - Common mode auto-tracking is excellent
  - No significant concerns about first TID results



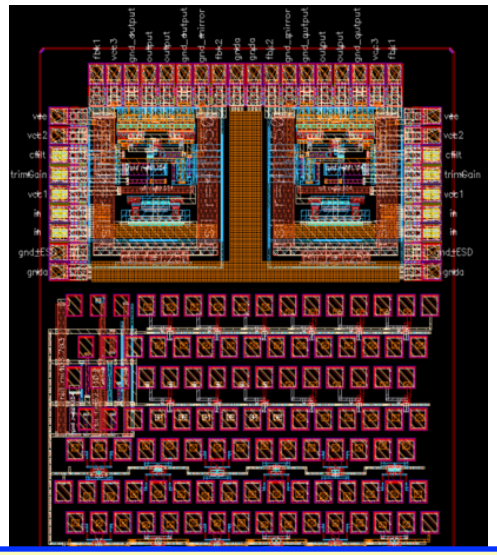
Test Printed-Circuit Board



Analog Front-end: Preamp & Shaper



Preamp circuit w. ideal shaping elements, P_{tot} ~ 45mW



Layout of preamp & shaper and test structures

- Second design based on IHP 0.25µm SiGe SG25H3P BiCMOS process
  - Cheaper and yet better technology due to PNP transistors
  - Preamp/shaper chip including tapped delay and test structures
  - 2-ch preamplifier
  - 1x and 10x gain shaper
- Measurement on test board shows good performance