

中国科学院粒子物理前沿卓越创新中心

大型物理试验读出电子学中 若干技术的研究进展

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核探测与核电子学国家重点实验室

2015年11月22日

个人简历

教育简历

- 2000/09—2004/07, 中国科学技术大学 少年班系
获应用物理学学士学位
- 2004/09—2009/06, 中国科学技术大学 近代物理系
获物理电子学博士学位

工作经历

- 2009/06—2011/08, 中国科学技术大学（博士后）
2009/10—2010/04, 法国CPPM (Marseille Centre for Particle Physics)研究所和CERN, 参与ATLAS Pixel Detector升级
- 2011/09—至今, 中国科学技术大学（副教授）
- 2014年获“粒子物理前沿卓越创新中心”青年拔尖人才奖。

科研方向

- ▶ 研究领域：核电子学

- ▶ 主要研究方向

- 物理实验读出电子学芯片电路研究

- 1) ASIC（专用集成电路）设计研究

- 2) FPGA TDC（时间数字变换器）研究

- 大型物理实验读出电子学工程项目上的工作

- 1) LHAASO WCDA读出电子学

- 2) 兰州重离子加速器CSR外靶实验读出电子学

- 高速高精度模拟-数字变换研究

- 1) 波形数字化技术研究

- 2) 基于高速高精度模-数变换的全数字化束流测量研究

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1. 科研工作

◆ 物理实验读出电子学芯片电路研究

- ◇ 1.1 ASIC研究

- ◇ 1.2 FPGA TDC研究

◆ 大型物理实验读出电子学工程项目上的工作

- ◇ 1.3 LHAASO WCDA读出电子学

- ◇ 1.4 兰州重离子加速器CSR外靶实验读出电子学

◆ 高速高精度模拟-数字变换研究

- ◇ 1.5 波形数字化研究

- ◇ 1.6 数字化束流测量研究

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◆ 高速高精度模拟-数字变换研究

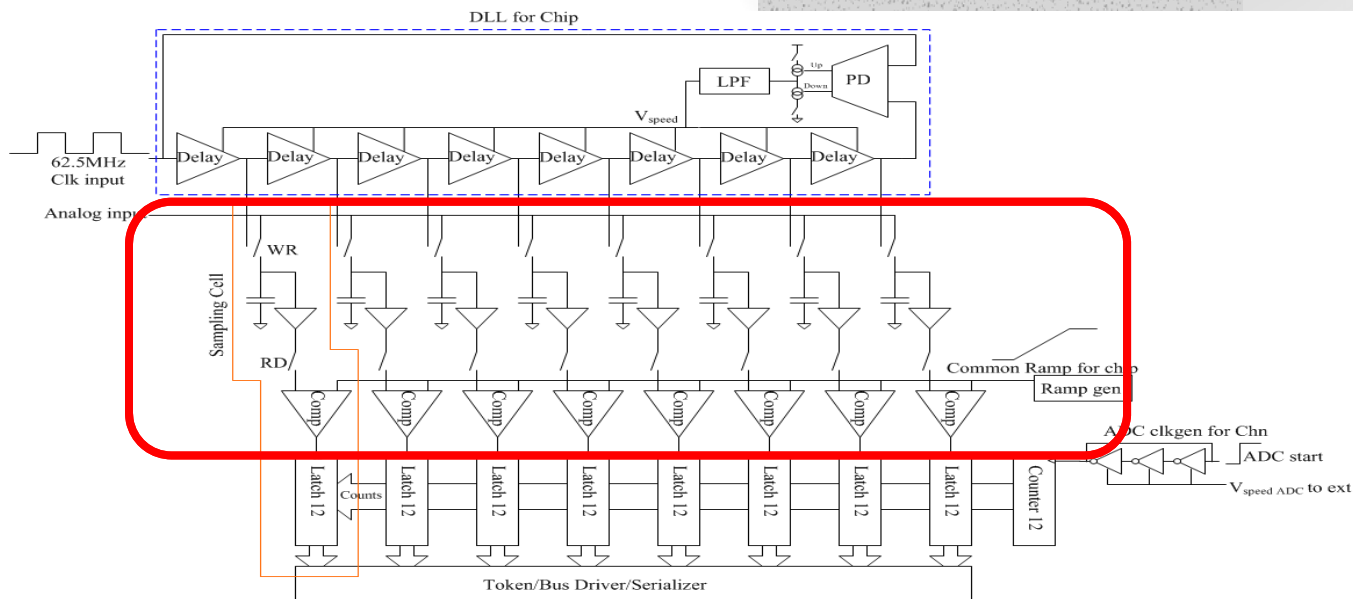
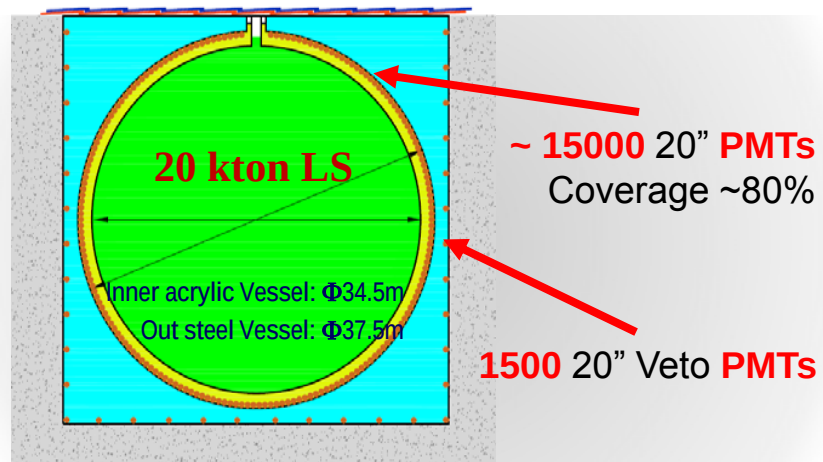
- ◇ 1.5 波形数字化研究

- ◇ 1.6 数字化束流测量研究

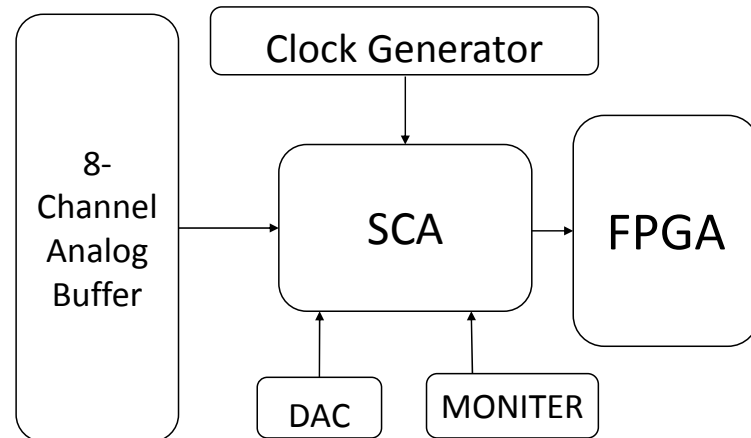
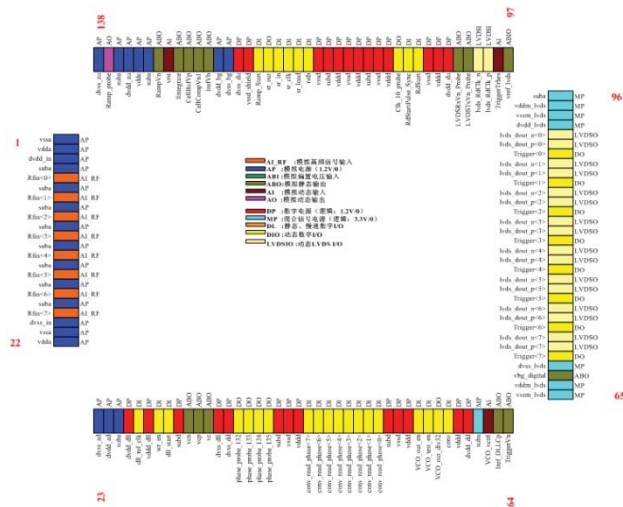
1.1 核电子学ASIC研究

江门地下中微子实验(JUNO)PMT读出ASIC

- ▶ 中科院高能所、清华大学、中科大三家首次合作进行ASIC设计，完成实现波形数字化的SCA芯片
- ▶ 1 Gsps采样，可覆盖0.5 Gsps~2 Gsps采样率
- ▶ 8+1 Chan, 256 cell/Chn
- ▶ Wilkinson ADC for each cell, 数字读出
- ▶ 负责其中核心采样单元的关键电路设计

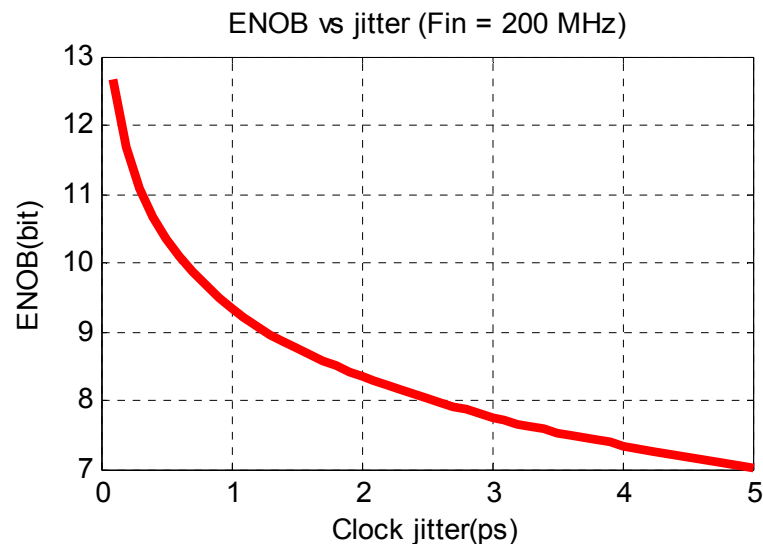


SCA测试系统设计



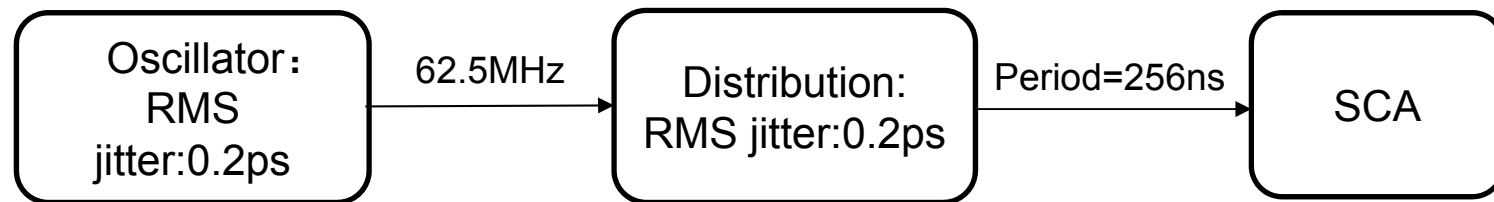
测试系统主要由5个部分构成：

- 1) 模拟信号输入缓冲单元 (DC~ 200 MHz)
- 2) SCA芯片外围电路
- 3) FPGA
- 4) 时钟产生电路
- 5) 状态监控单元

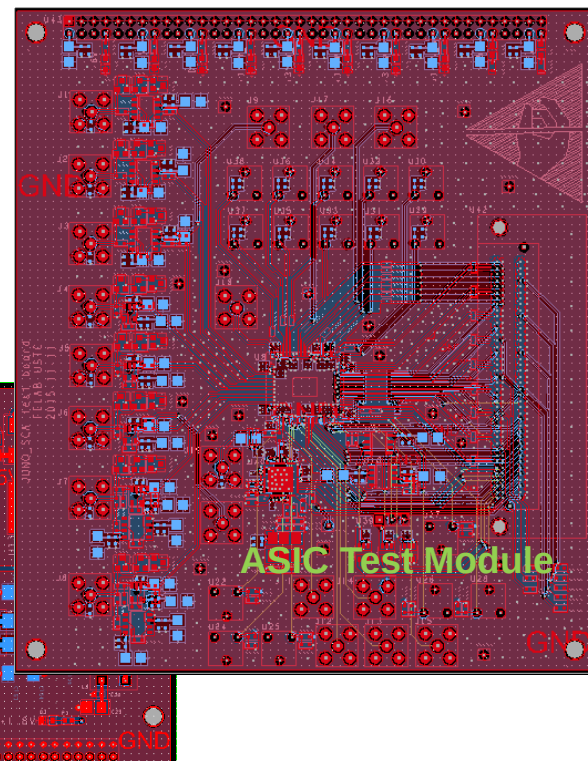
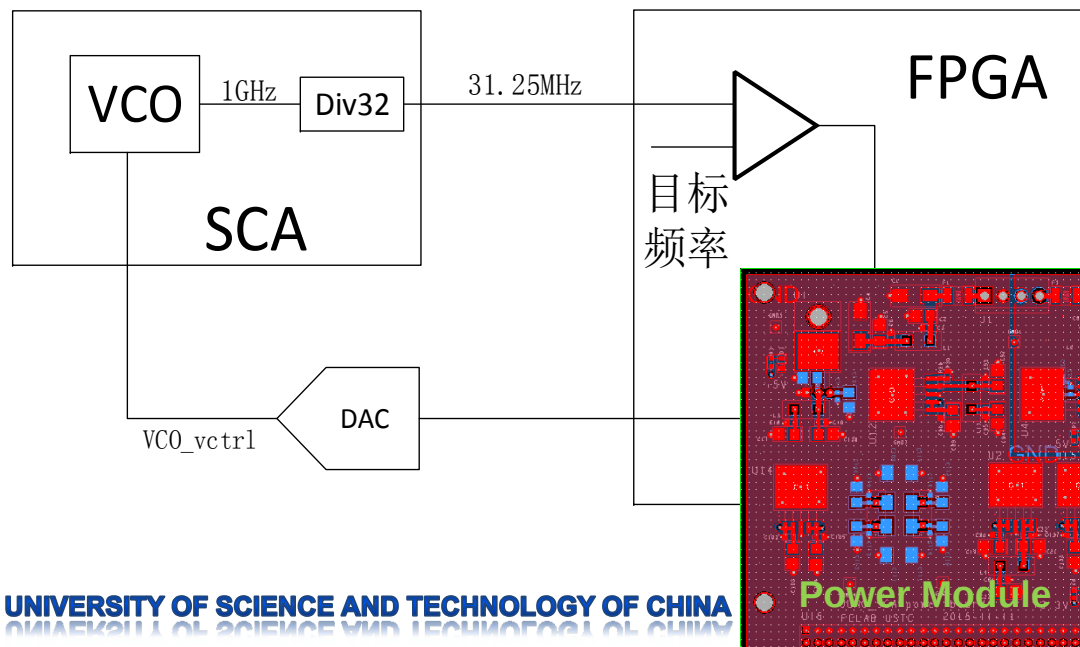


SCA测试系统设计

- SCA采样基准时钟产生电路： RMS jitter ~ 280 fs



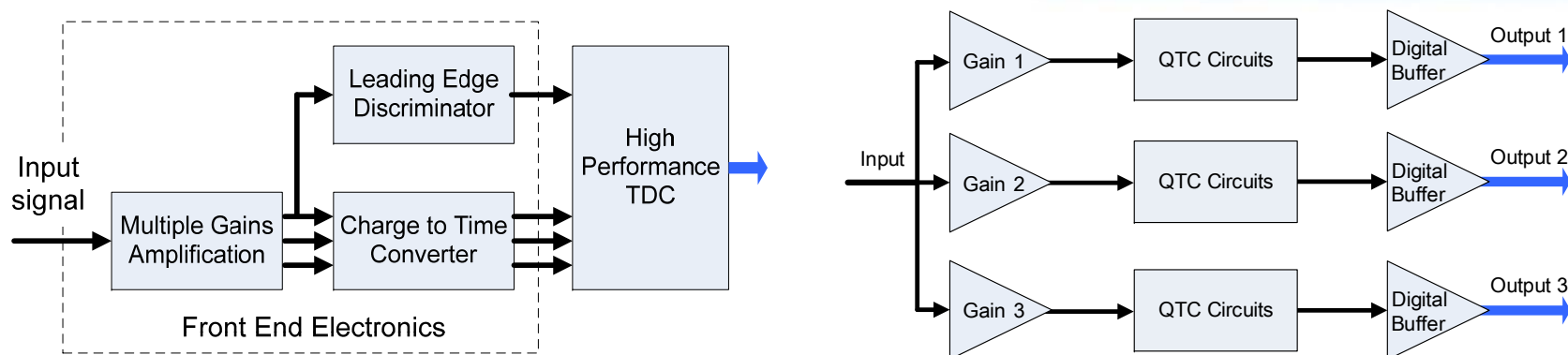
- SCA量化电路Wilkinson ADC时钟控制电路：



1.1 核电子学ASIC研究

PMT读出ASIC芯片设计

- ▶ 用于PMT（光电倍增管）的读出
- ▶ 针对大动态范围信号（4000倍）读出展开研究
- ▶ 基于TOT技术同时实现时间和电荷的数字化



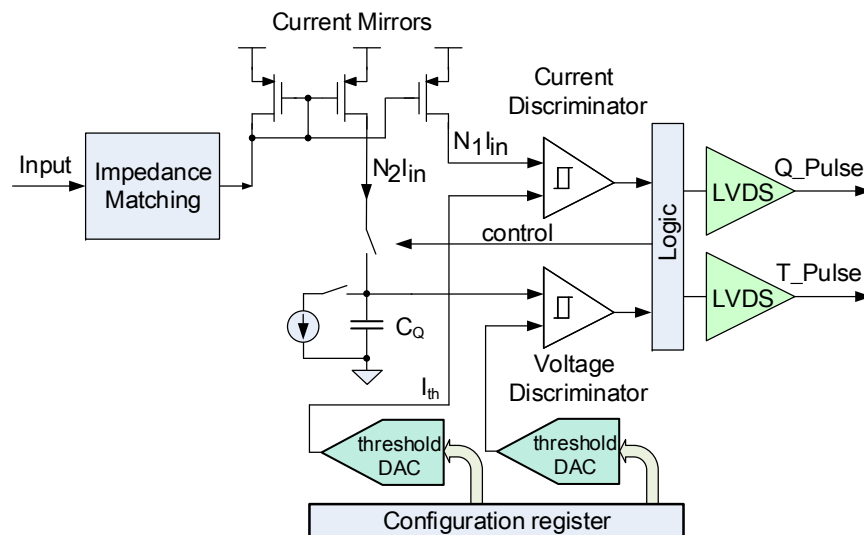
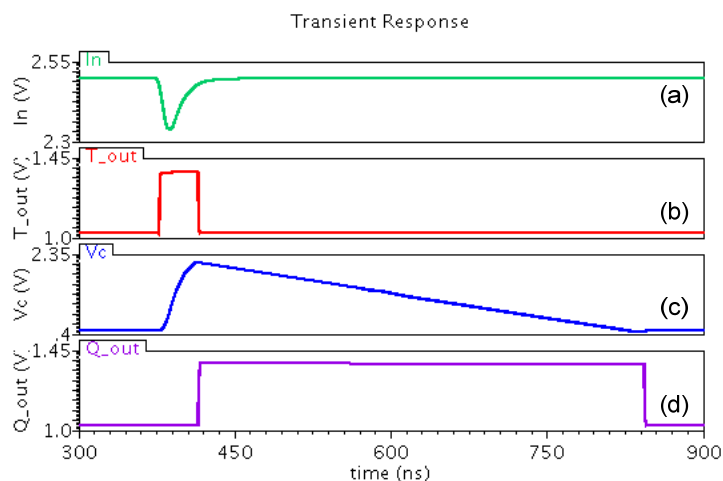
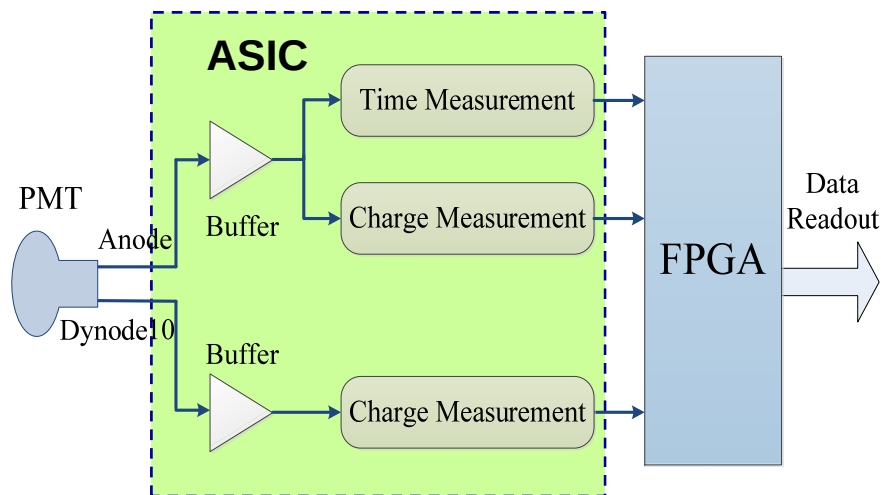
- ▶ 主持两项核探测与核电子学国家重点实验室自主研究课题项目基金
 - 基于TOT方法与电流处理技术的大动态范围信号读出ASIC电路研究
 - 基于放大成形技术的PMT大动态范围信号读出前端ASIC研究
- ▶ 目前一个直接的应用就是在“国家发改委十二五”规划LHAASO的WCDA读出中

PMT读出ASIC芯片设计

- ▶ 关键技术与挑战：
 - ◇ 大动态范围：1~4000倍
 - ◇ 高精度时间及电荷测量
 - ◇ 高精度阻抗匹配

PMT读出ASIC芯片设计

- 基于多增益处理技术实现大动态范围
- 电流型TOT：基于TOT技术，除阻抗匹配外信号处理基于电流模
- 时间测量：电流型前沿定时
 - 响应速度快
 - 阈值由DAC配置提供
 - 交流耦合输入以抑制温漂效应
- 电荷测量：线性放电TOT
 - 时间甄别信号控制电荷测量充电过程

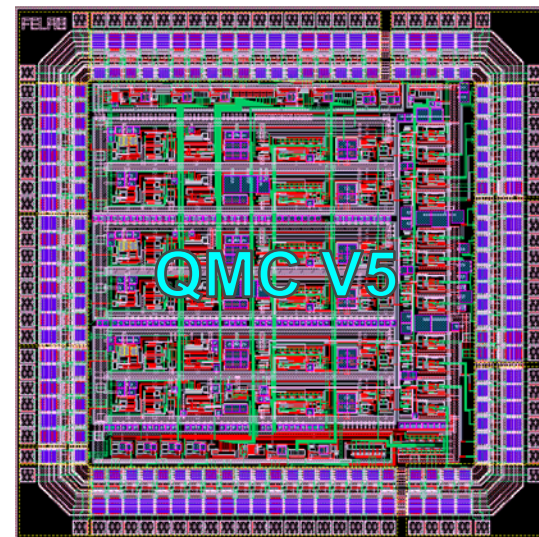
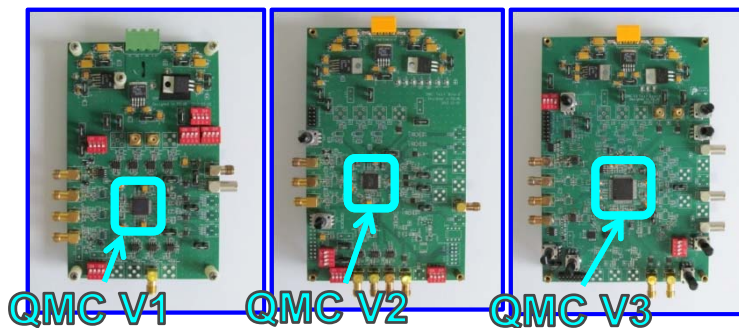


模拟ASIC信号处理：电压模vs电流模

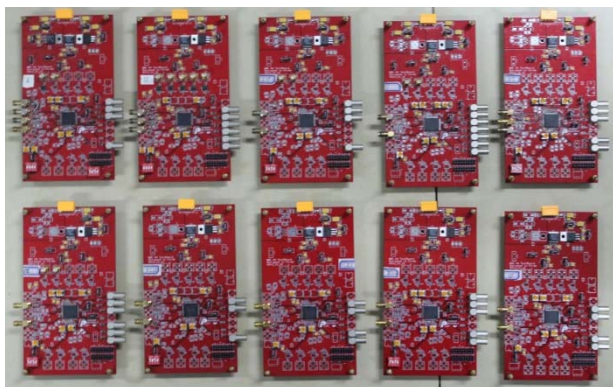
年代	技术	电源电压	信号幅度	集成度
1950	真空电子管	300V	100V	~1
1970	锗, 硅晶体管	10-30V	10V	10
1980	双极型模拟集成电路	15V	10V	100
	双极型数字集成电路	5V	3V	1000
1985	CMOS, LCMOS	15V	10V	1000
1990	FPGA, CPLD, ASIC 2.0 μm	5V, 3.3V	2.5V	1 M
1995	ASIC 0.35 μm	3.3V	$V_{\text{th}}=0.6\text{V}$	10 M
1997-99	ASIC 0.25 μm , 0.18 μm	2.5V, 1.8V;	0.5V	40 M
2001-2004	ASIC 0.13 μm , FPGA 90 nm	1.2V, 1.0V	0.35-0.4V	100 M
2004-2010	CPU FPGA 65 nm, 45 nm	0.7V, 0.6V	0.3-0.25V	1 B

- ▶ 电流模信号处理
 - ◇ 不受电源电压限制, 动态范围大
 - ◇ 模拟信号易于放大
 - ◇ 响应速度快

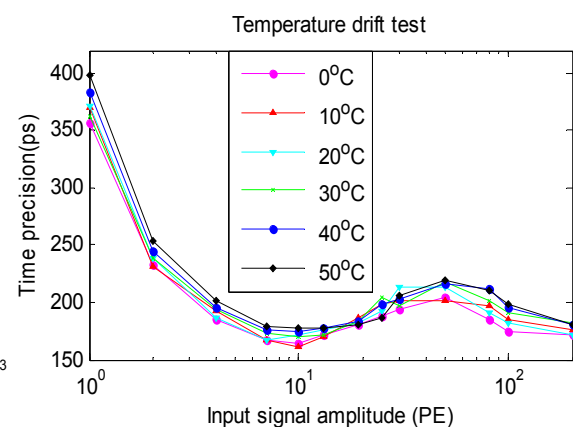
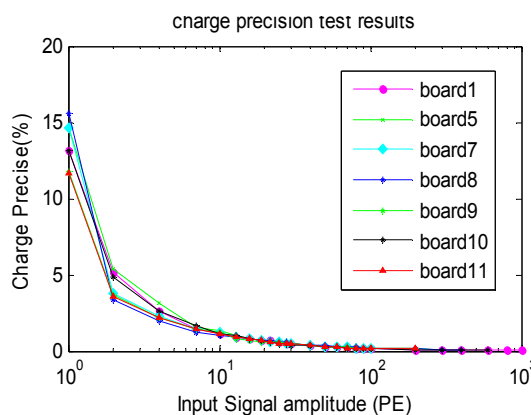
PMT读出ASIC芯片设计



- ▶ 在前三版ASIC电路的设计与测试基础上，完成第4版ASIC的设计，进行了多芯片的系统测试（精度、稳定性、温漂等），电路性能已基本满足应用需求。
- ▶ 基于多通道集成的第五版也已完成设计和测试。

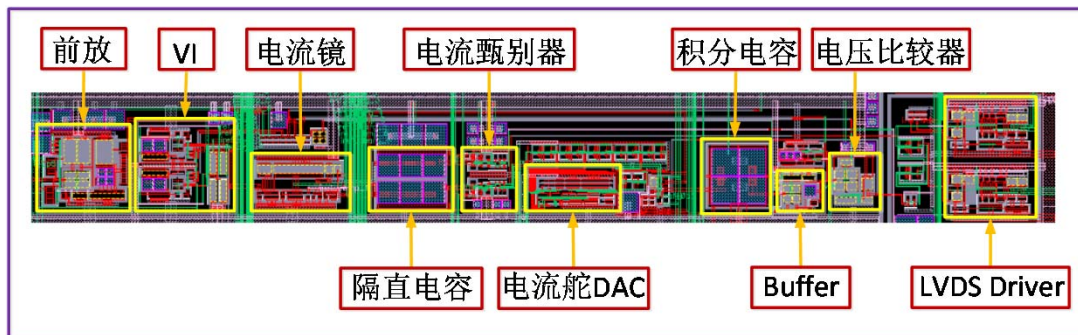


基于TOT技术路线的ASIC测试板



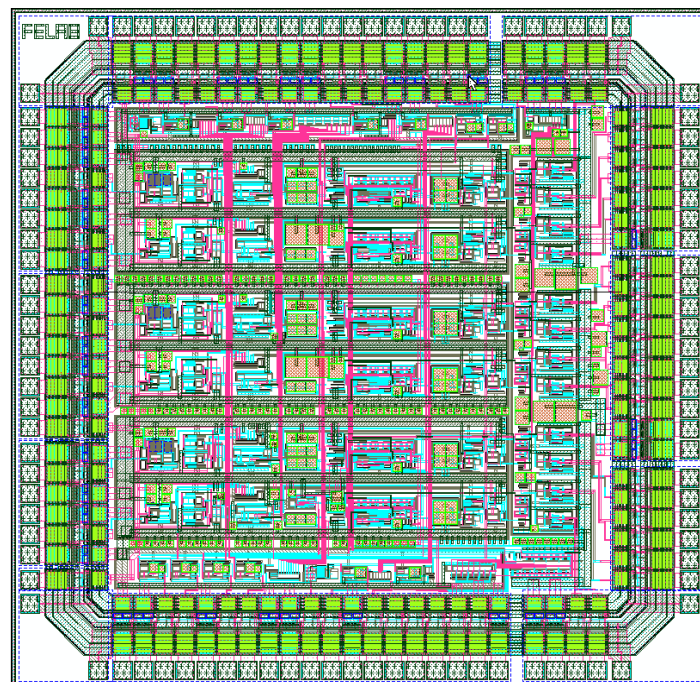
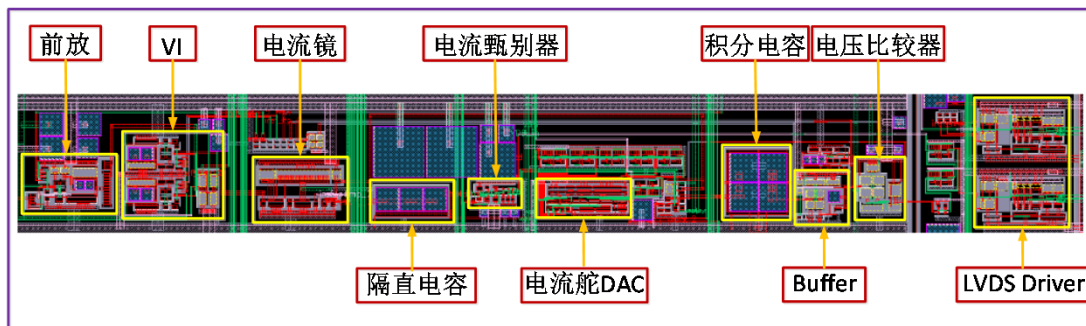
版图设计

阳极通道版图：



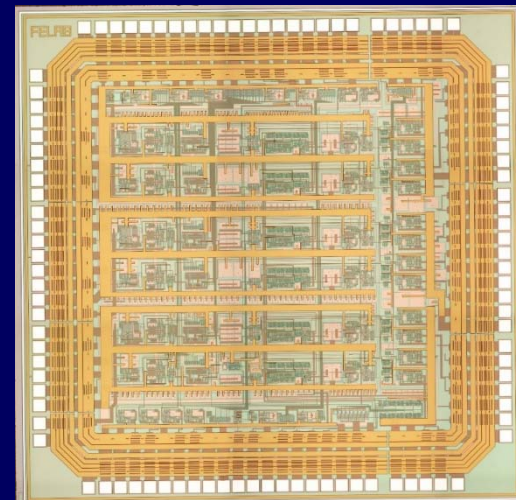
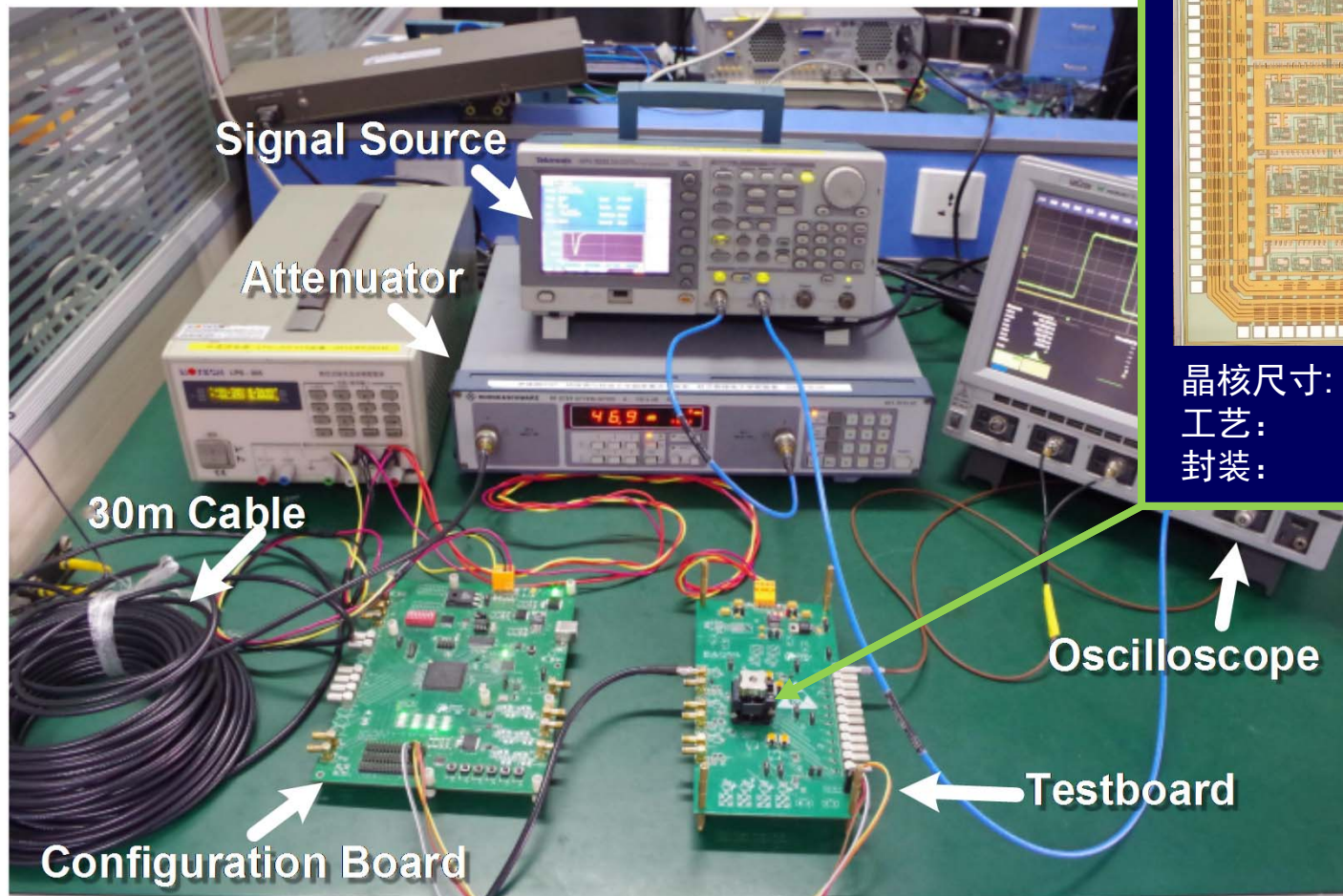
尺寸：2970 μm $\times$ 2970 μm
集成3个PMT读出通道

打拿极通道版图：



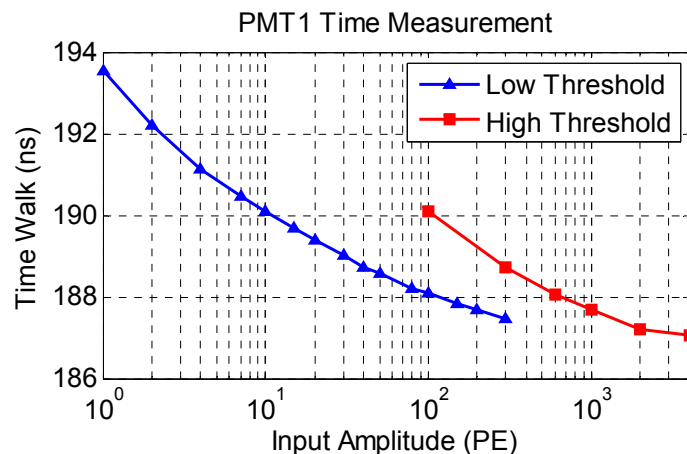
读出ASIC整体版图

PMT读出ASIC芯片设计

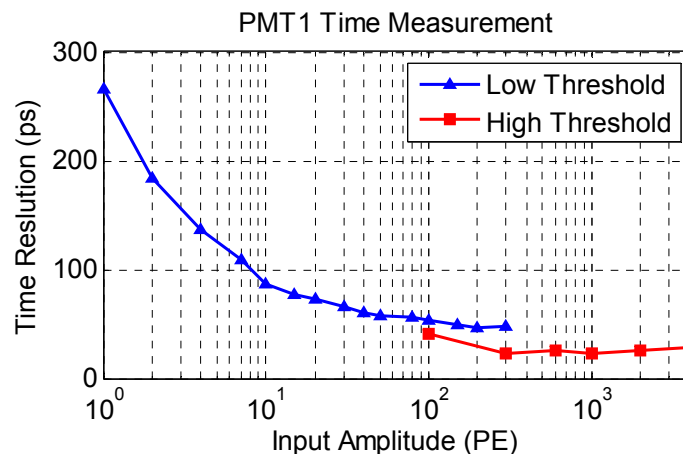


晶核尺寸: 3 mm x 3mm
工艺: GF 0.35 um CMOS
封装: LQFP100

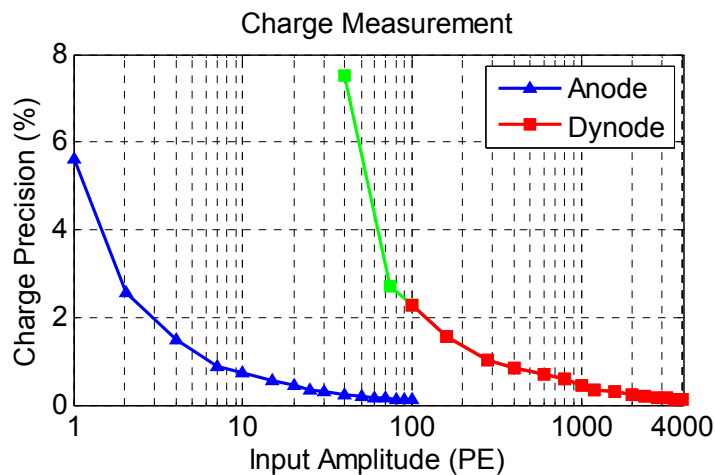
单通道性能测试



time walk



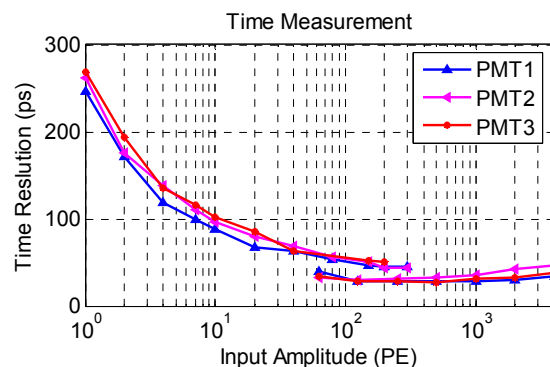
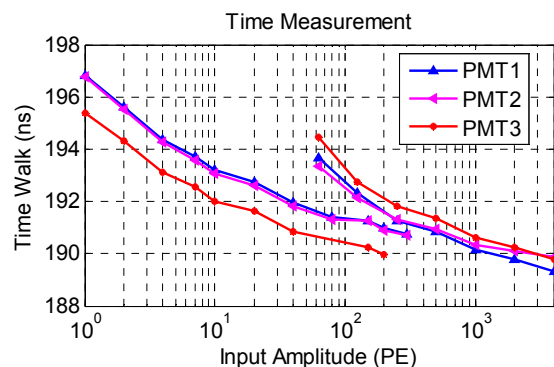
时间精度



电荷精度

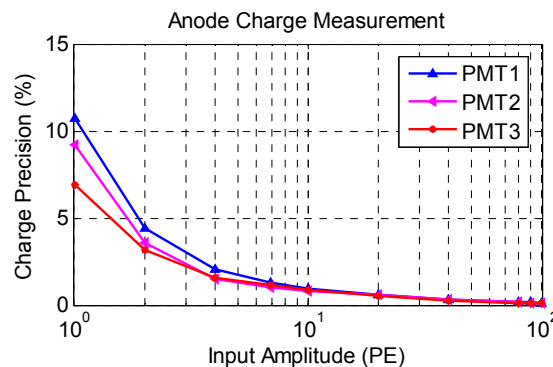
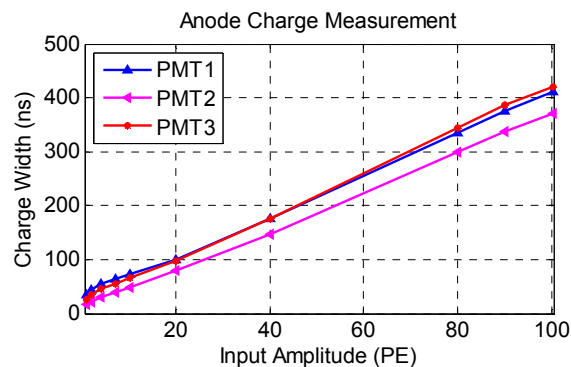
多通道性能测试

时间测量



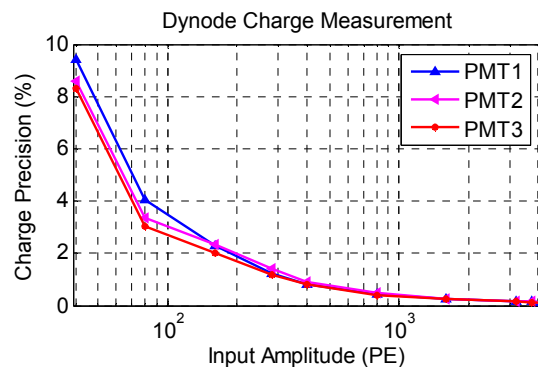
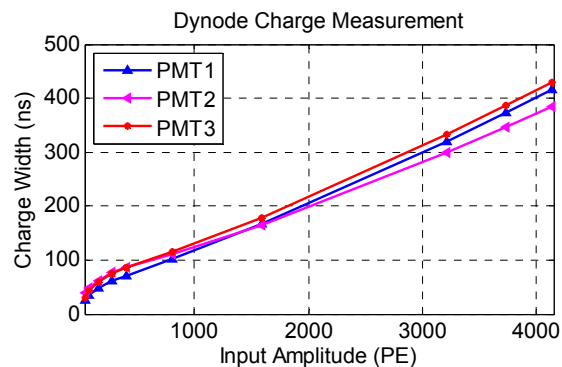
时间测量精度:
 $1 \text{ PE} < 300 \text{ ps}$

阳极电荷



电荷测量精度:
 $1 \text{ PE} < 12\%$
 $4000 \text{ PE} < 1\%$

打拿极电荷

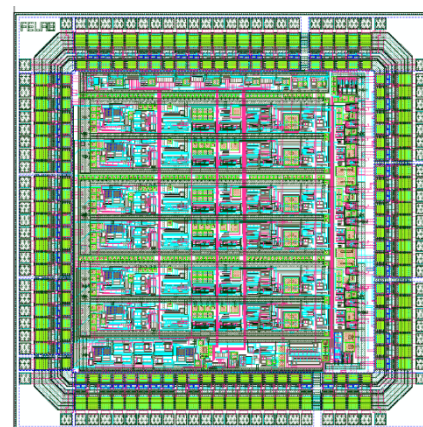


国际上代表性的大动态范围读出ASIC性能

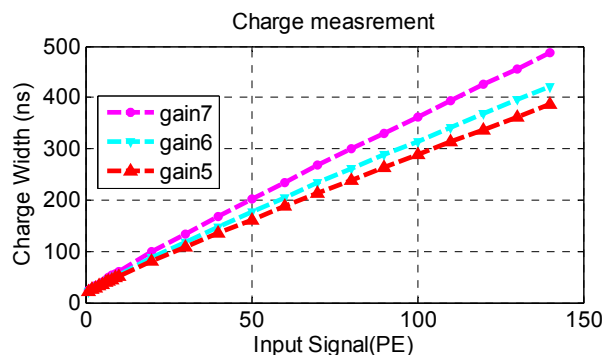
	PARISROC	SPIROC	SCOTT	CLC101	WCDA读出ASIC
技术路线	电压成形+模拟寻峰	电压成形+模拟寻峰	波形数字化（多阈值过阈时间法）	电压甄别+线性放电TOT	电流型TOT
动态范围	600（双增益调节）	2000（双增益通道）	60	2500（三增益通道）	4000
单通道测量范围	70	46	60	50	100
单光电信号电荷量	150 fC	80 fC	8 pC	2 pC	750 fC
单光电子时间测量精度	1 ns	~1.25 ns	~600 ps	~300 ps	<300 ps
单光电子电荷测量精度	——	——	——	10%	15%
死时间	100 us	4 ms	——	900 ns	<600 ns

进一步改进

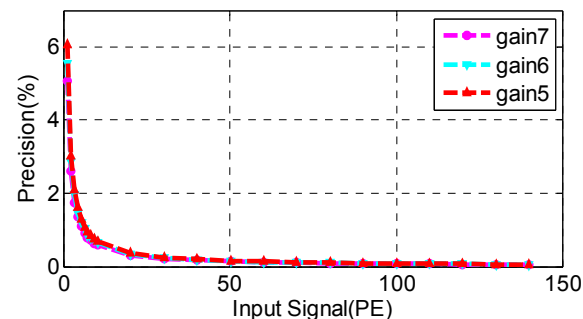
- ▶ 将阳极及打拿极信号处理通道的测量范围从100倍提升至130倍；
- ▶ 提升各通道的一致性；
- ▶ 增益微调功能；
- ▶ 加入calibration电路模块。



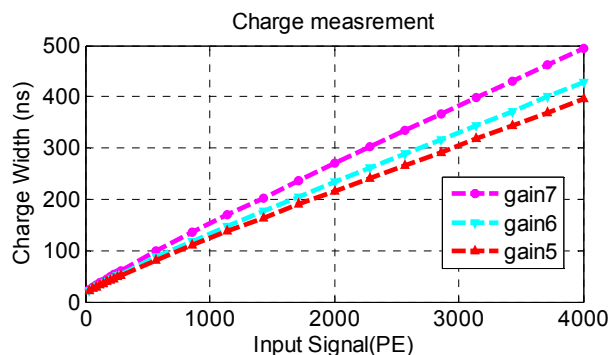
阳极电荷



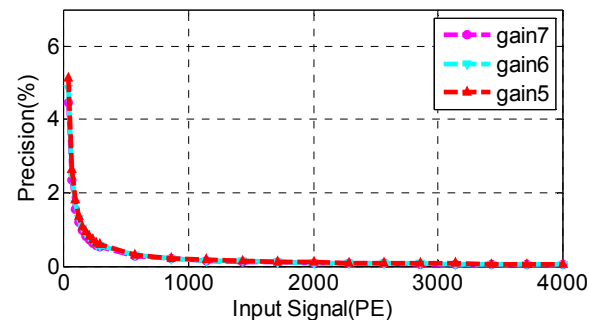
Anode Charge Measurement measurement



打拿极电荷

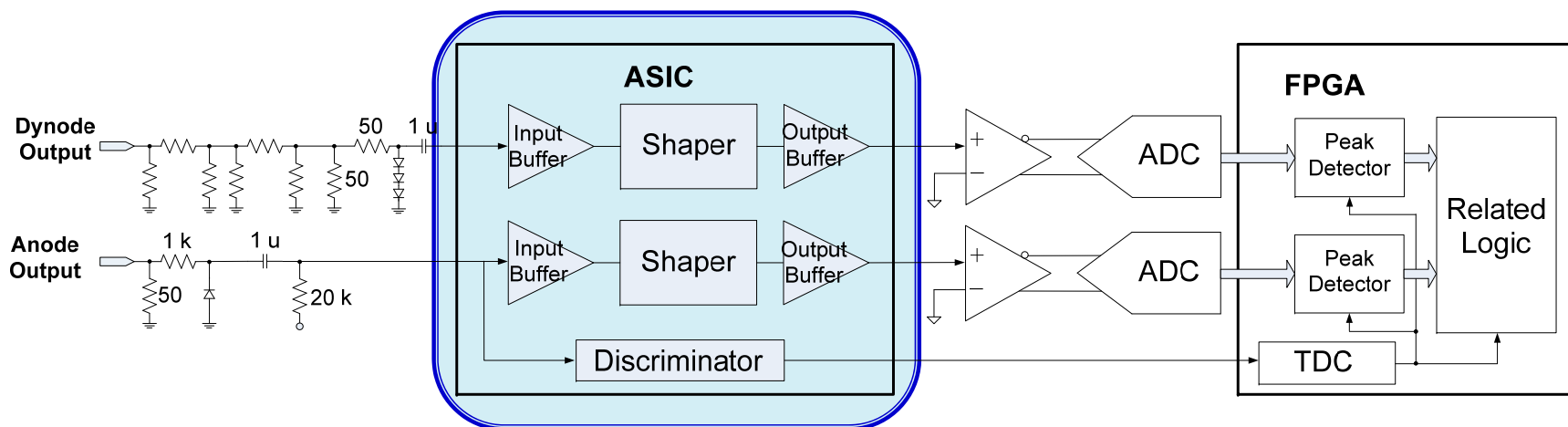


Dynode Charge Measurement measurement



1.1 核电子学ASIC研究

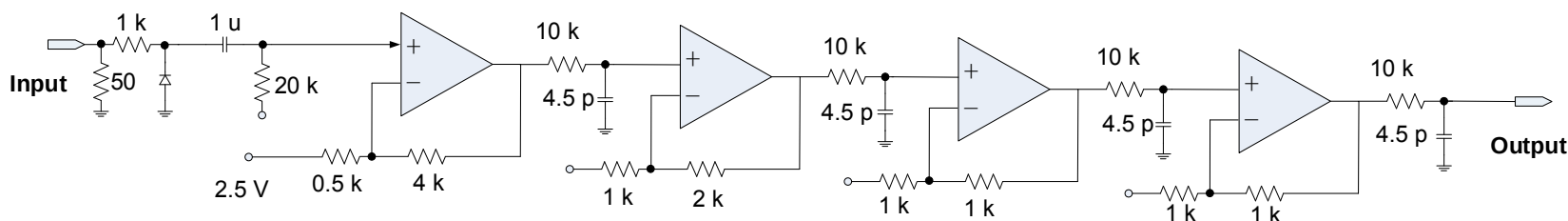
- 同时，展开了另一条技术路线的探索，基于前放+成形+模数变换结合数字寻峰的技术展开研究。



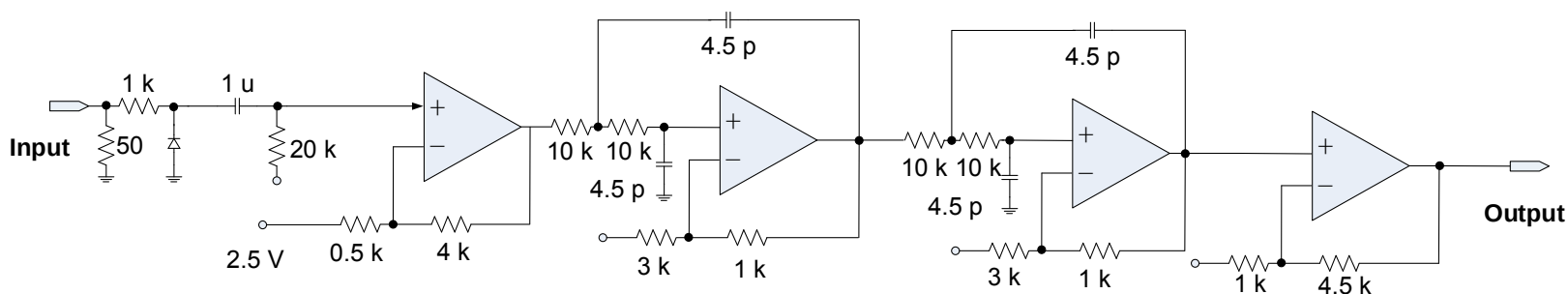
- 基于多增益处理技术实现大动态范围（~4000倍）
- 基于放大成形结合模拟数字变换实现高精度电荷测量
- 基于前沿甄别实现时间测量

成形电路滤波器结构选择

▶ 无源滤波器结构 (RC^n)

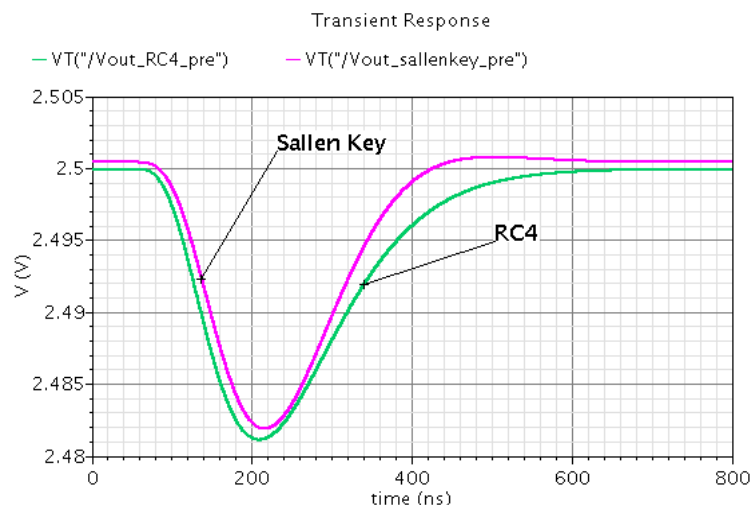


▶ 有源滤波器结构 (Sallen key)



成形电路滤波器结构选择

瞬态仿真和噪声仿真



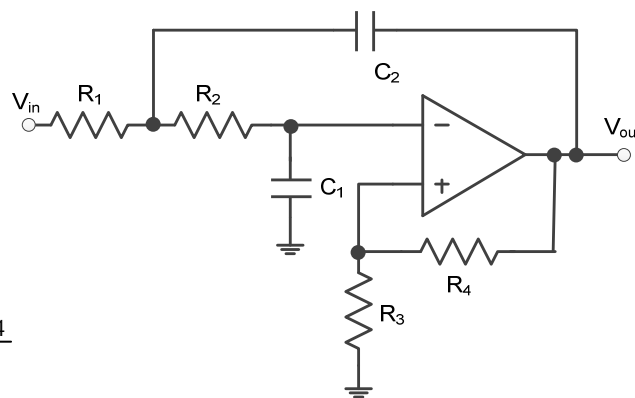
	Sallen key	RC ⁴
积分输出噪声	0.993 mV	0.858 mV
输出幅度 (SPE信号输入)	18.54 mV	18.78 mV
SNR	18.67	21.89
等效精度	5.36%	4.57%

- RC⁴结构SNR略好于Sallen Key结构
- 相对于Sallen Key结构, RCⁿ结构更容易实现更好的稳定性

$$f_c = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$

$$Q = \frac{\sqrt{R_1 R_2 C_1 C_2}}{(R_1 + R_2)C_1 + R_1 C_2(1 - k)}$$

$$k = \frac{R_3 + R_4}{R_3}$$



成形电路滤波器关键参数设计

▶ 测量误差主要来源:

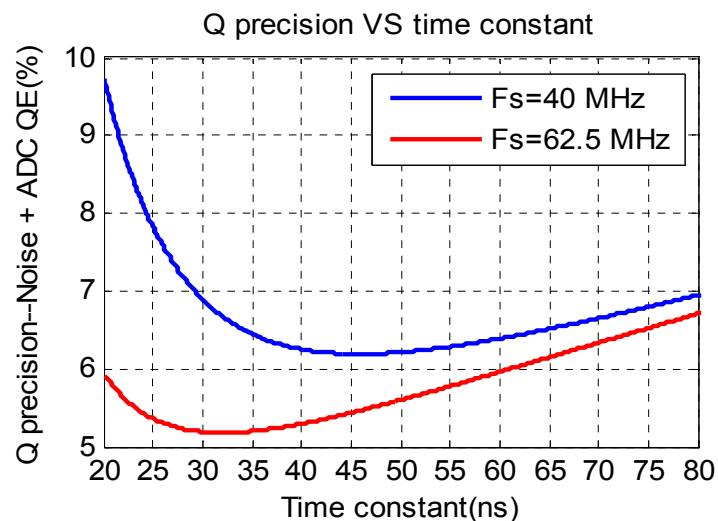
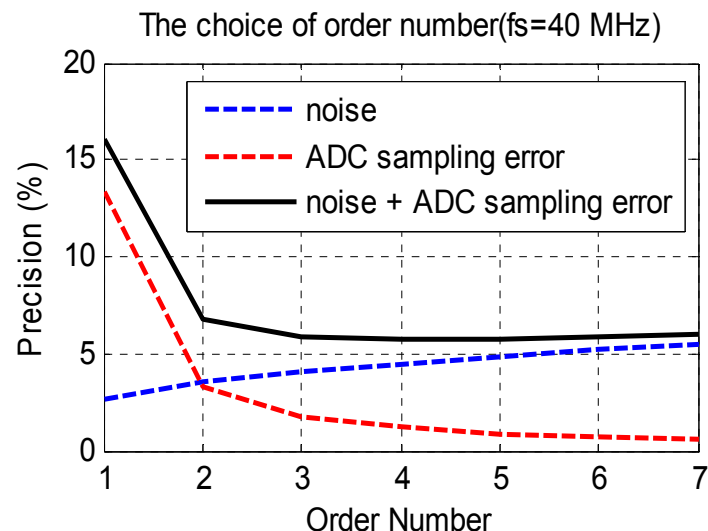
- 1) 模拟前端电路信噪比;
- 2) 寻峰误差;
- 3) ADC量化误差;
- 4) 弹道亏损;

▶ 电路本身噪声 (noise) 所致信噪比随滤波阶数的增加而变差

▶ ADC采样寻峰误差则随滤波阶数的增加而减小

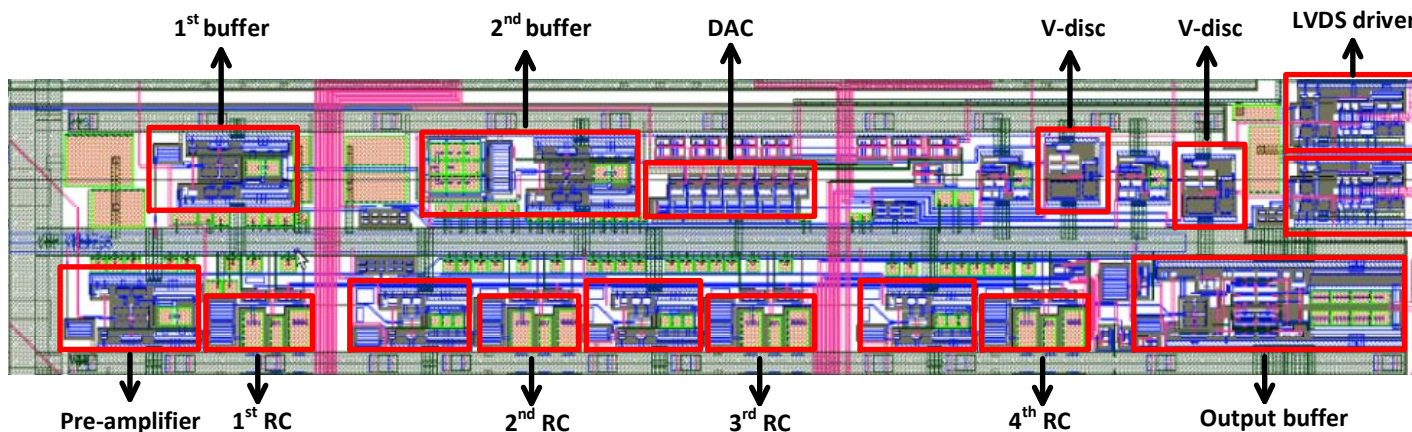
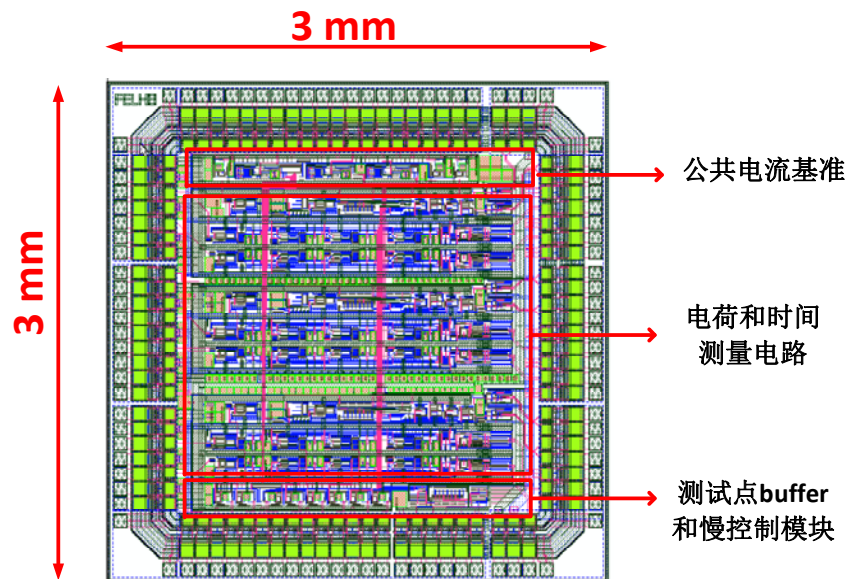
▶ 当滤波阶数大于4阶后, 总体测量精度 (noise + ADC sampling error) 变化不大

▶ 阶数、成形时间的选取最终是各种误差因素的平衡和最优化

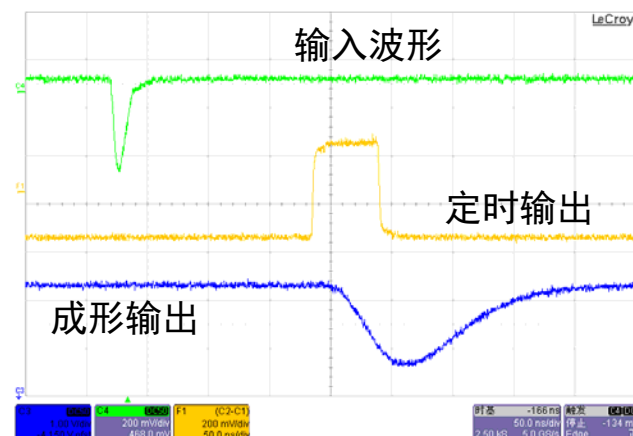
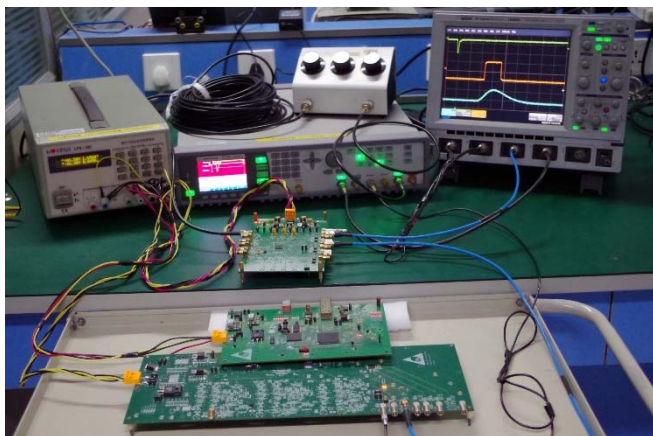


PASC V2版图

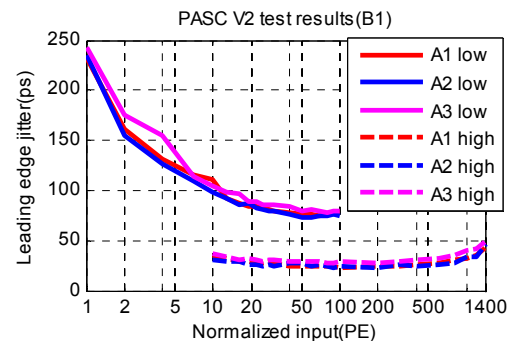
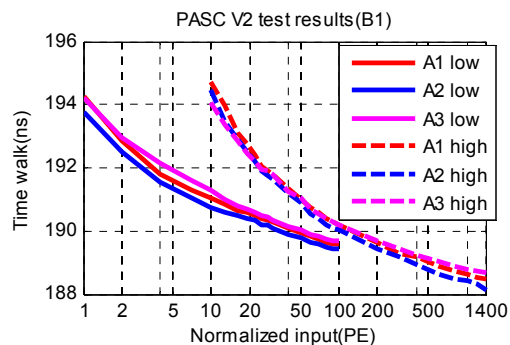
- ▶ 集成6个通道
- ▶ 完成3个PMT读出
- ▶ 电压甄别方案
- ▶ 时间常数可调



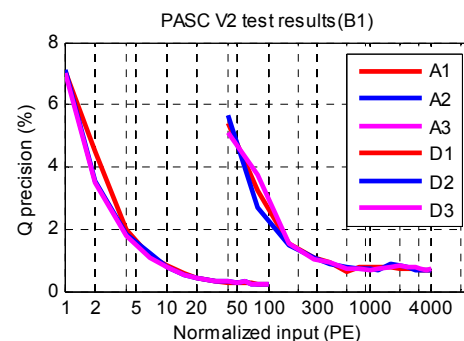
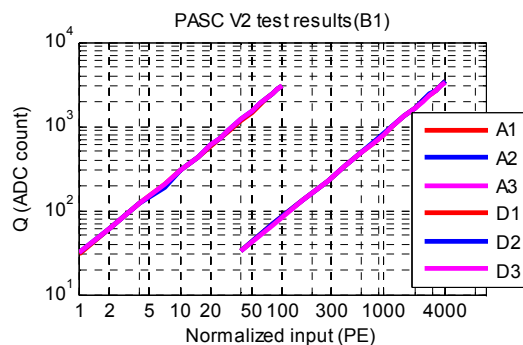
PASC V2测试



时间测量性能



电荷测量性能



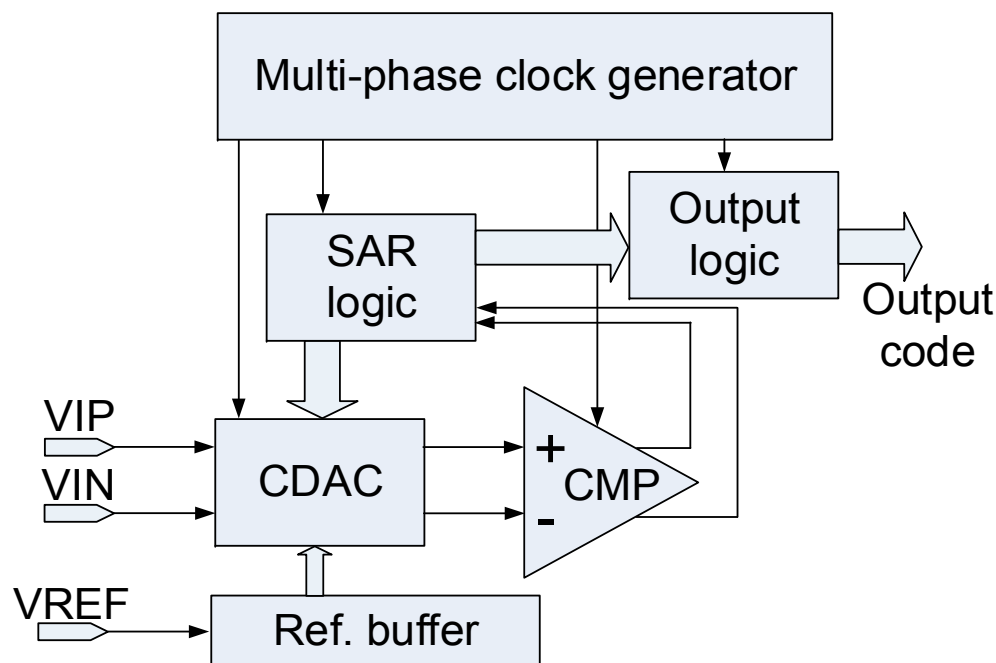
低功耗、中高精度ADC ASIC研究

► 设计目标

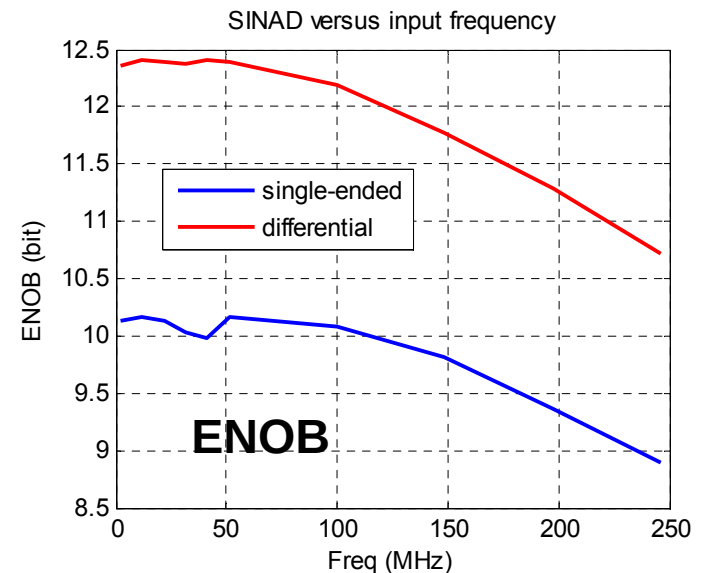
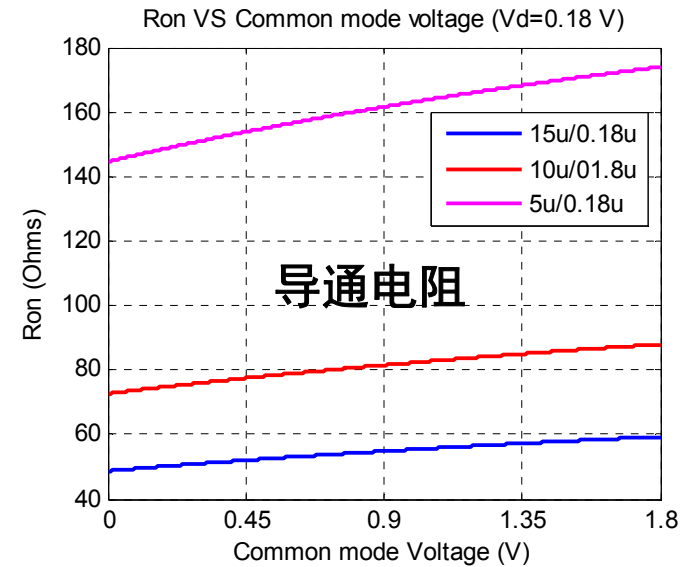
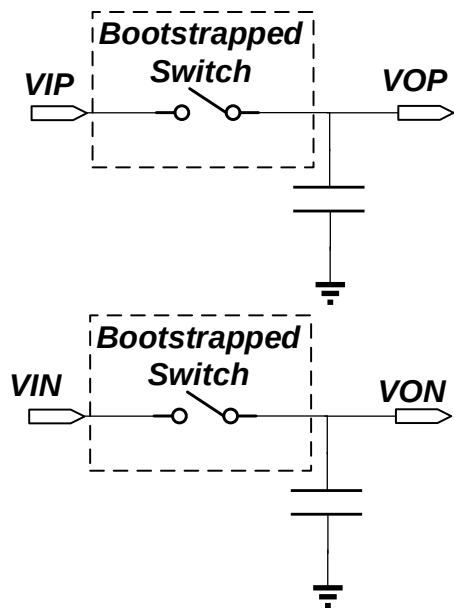
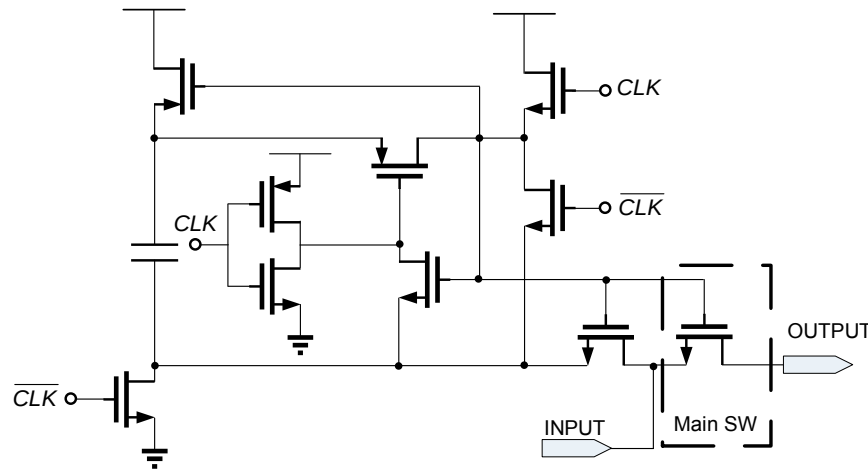
- ◇ 分辨率：12 bit
- ◇ 采样率：40 ~ 50 Msps
- ◇ ENOB > 10 bit

► 主要模块

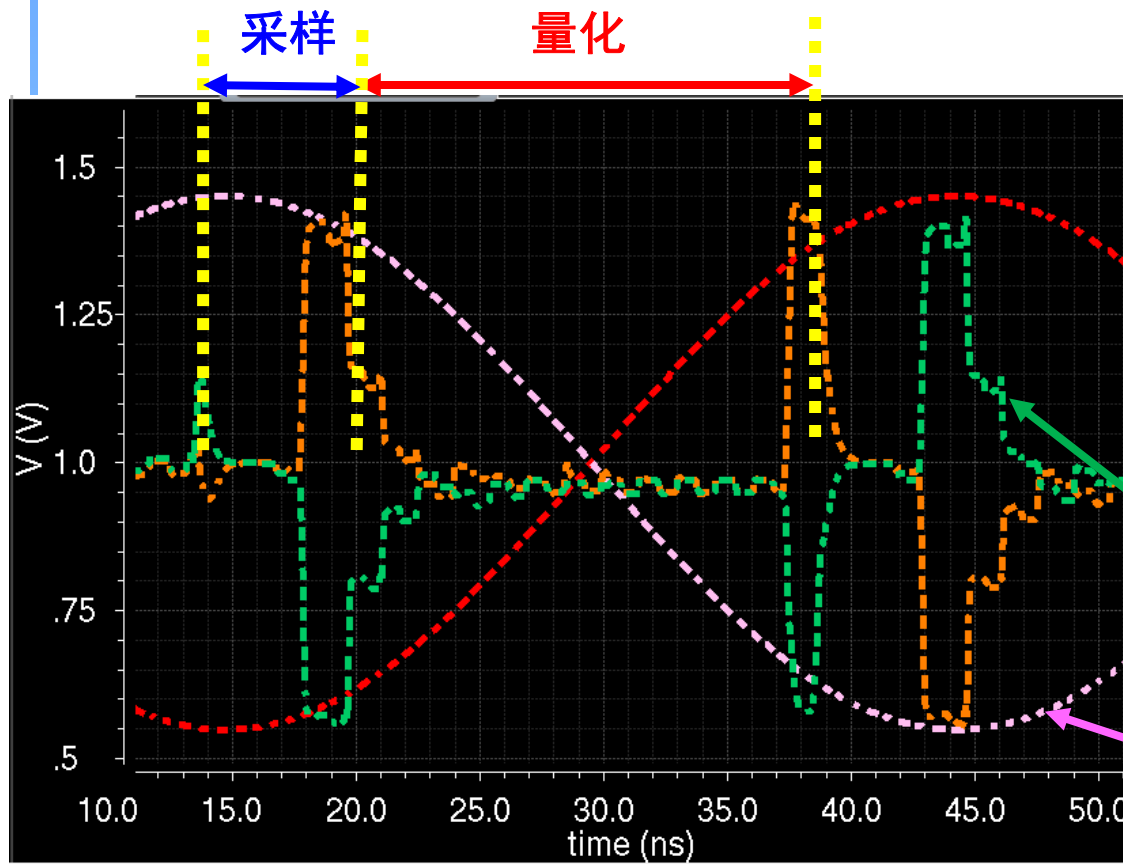
- ◇ 自举开关
- ◇ 电容split DAC
- ◇ 动态比较器
- ◇ 异步时钟和SAR logic
- ◇ Voltage reference buffer



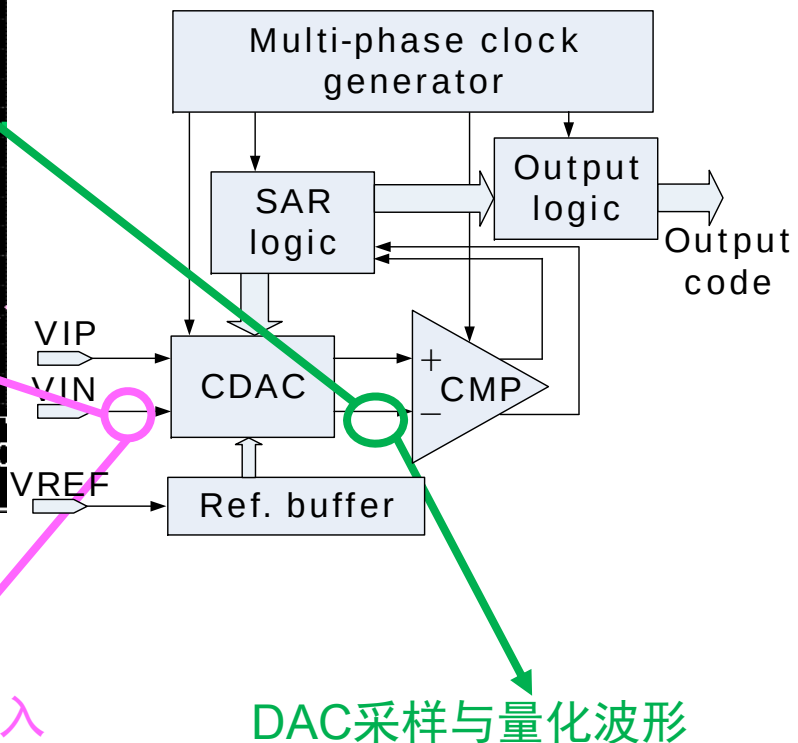
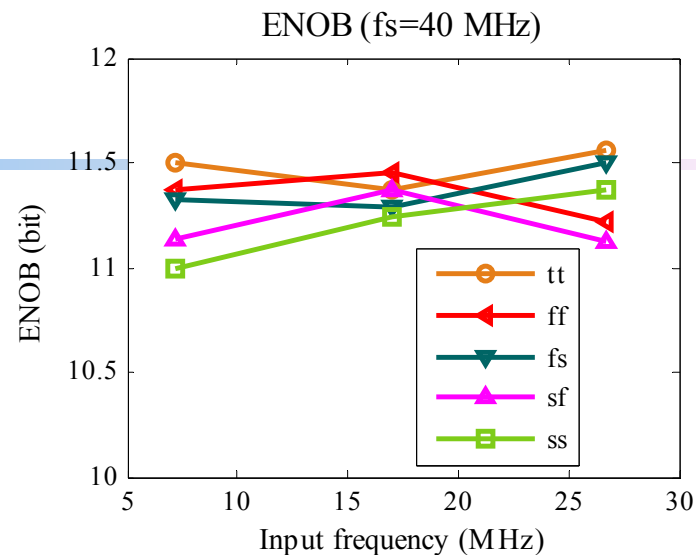
Bootstrapped switch



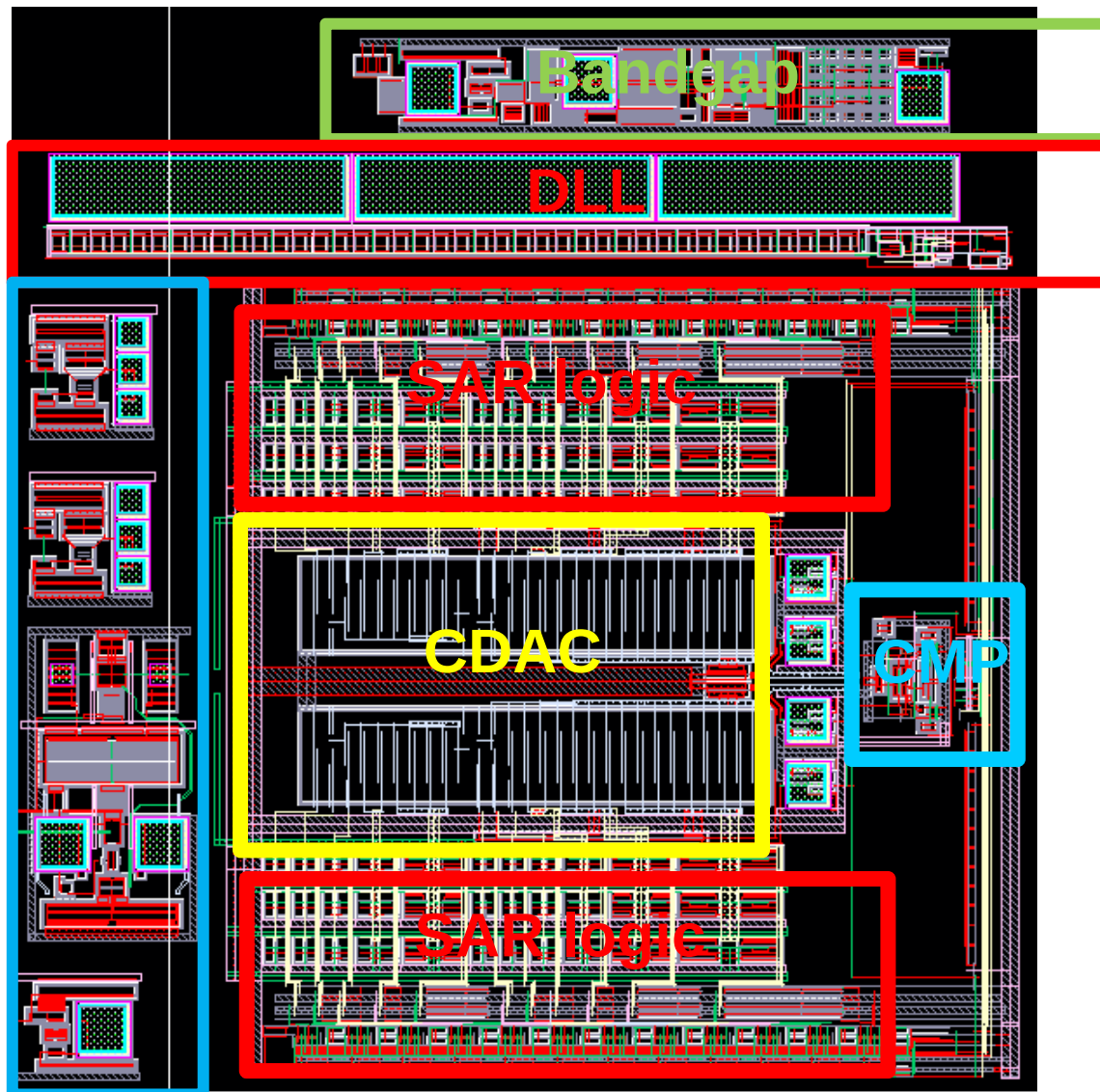
SAR ADC 仿真结果



瞬态仿真结果



SAR ADC 版图



- ▶ GF 0.18 um process
- ▶ Single channel area:
 $700 \times 730 \text{ um}$

1.1 核电子学ASIC研究

Jinst

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Prototype of a front-end readout ASIC for the Water Cherenkov Detector Array in the LHAASO project

L. Zhao,^{a,b} W. Wu,^{a,b} J. Liu,^{a,b} Y. Liang,^{a,b} J. Qin,^{a,b} L. Yu,^{a,b} S. An,^a

^aState Key Laboratory of Particle Detection and Electronics, University of Science and Technology of China, Jinzhai Road, Hefei, 230026, China

^bDepartment of Modern Physics, University of Science and Technology of China, Jinzhai Road, Hefei, 230026, China

E-mail: anqi@ustc.edu.cn

ABSTRACT: The Large High Altitude Air Shower Observatory is in the process of construction. It will be the largest and most sensitive cosmic ray observatory in the world. It will consist of a large array of water Cherenkov detectors (WCDAs) and a large array of particle detectors (PDs). The WCDAs are used to detect the secondary particles of an air shower. The PDs are used to detect the primary particles of an air shower. The WCDAs and PDs are connected by a readout chain. The readout chain consists of a front-end readout ASIC and a data acquisition system (DAQ). The front-end readout ASIC is used to process the signals from the WCDAs and PDs. The DAQ system is used to acquire the data from the front-end readout ASIC.

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INSTRUMENTS & INSTRUMENTATION

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数据来自第 2013 版 Journal Citation Reports®

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-- Nuclear Science and Techniques, accepted
-- 2015 IEEE 12th International Conference on Electronic Measurement & Instruments
-- Chinese Physics C, under 2nd review

Chinese Physics C Vol. 39, No. 12 (2015) 126101

Evaluation of a front-end ASIC for the readout of PMTs over a large dynamic range

WU Wei-Hao(邬维浩) ZHAO Lei(赵雷)¹⁾ LIANG Yu(梁宇) YU Li(于莉)

LIU Jian-Feng(刘建峰) LIU Shu-Bin(刘树彬) AN Qi(安琪)

State Key Laboratory of Particle Detection and Electronics, University of Science and Technology of China, Hefei 230026, China

Abstract: The Large High Altitude Air Shower Observatory (LHAASO) project has been proposed for the survey and study of cosmic rays. In the LHAASO project, the Water Cherenkov Detector Array (WCDA) is one of the major detectors for searching for gamma ray sources. A Charge-to-Time Converter (QTC) ASIC (Application Specification Integrated Circuit), fabricated with Global Foundry 0.35 μm CMOS technology, has been developed for readout of photomultiplier tubes (PMTs) in the WCDA. This ASIC provides both time and charge measurement of PMT signals. The input charge is converted to a pulse width based on the Time-Over-Threshold (TOT) technique and linear discharge method; as for time measurement, leading edge discrimination is employed. This paper focuses on the evaluation of this front-end readout ASIC performance. Test results indicate that the time resolution is better than 400 ps and the charge resolution is better than 1% with large input signals and remains better than 15% @1 photoelectron (P.E.), both beyond the application requirement. Moreover, this ASIC has a weak ambient temperature dependence, low input rate dependence and high channel-to-channel isolation.

Key words: ASIC, time measurement, charge measurement, QTC, LHAASO, WCDA

PACS: 84.30.-r, 07.05.Hd **DOI:** 10.1088/1674-1137/39/12/126101

1 Introduction

The Large High Altitude Air Shower Observatory (LHAASO) project for the study and exploration of particle astrophysics has been proposed, consisting of various kinds of efficient detectors [1, 2]. One of the major components is the Water Cherenkov Detector Array (WCDA), aiming to survey gamma ray origins with its high sensitivity to gamma ray showers above a few hundred GeV [3, 4]. The WCDA is composed of four 150 m $\times$ 150 m water ponds, each with 900 photomultiplier tubes (PMTs) located at the bottom to collect

Cherenkov light produced in the water by the secondary particles of an air shower. A total of 3600 electronics readout channels are required, as shown in Fig. 1. The readout electronics of every 9 adjacent PMTs are combined into one front-end electronics module (FEE), which processes and digitizes the PMT output signals before sending them to the Data Acquisition (DAQ) system [5–8].

Both high precision time and charge measurement is required in the WCDA readout electronics, and the signal dynamic range can vary from 1 P.E. (photoelectron) to 4000 P.E. The resolution of time measurement should

目录

1. 科研工作

◆ 物理实验读出电子学芯片电路研究

◇ 1.1 ASIC研究

◇ 1.2 FPGA TDC研究

◆ 大型物理实验读出电子学工程项目上的工作

◇ 1.3 LHAASO WCDA读出电子学

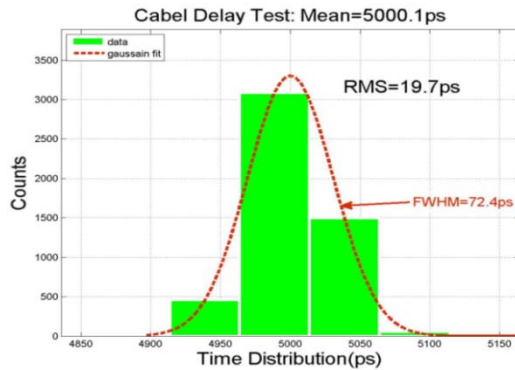
◇ 1.4 兰州重离子加速器CSR外靶实验读出电子学

◆ 高速高精度模拟-数字变换研究

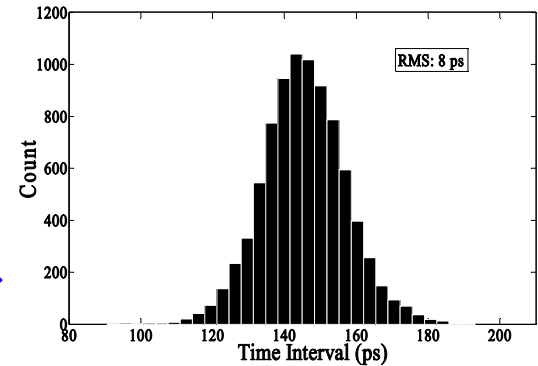
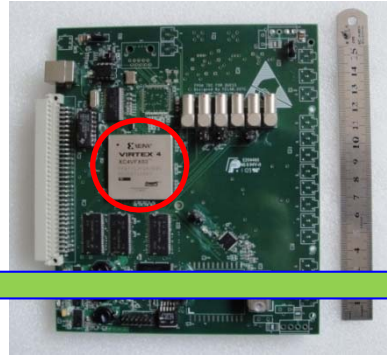
◇ 1.5 波形数字化研究

◇ 1.6 数字化束流测量研究

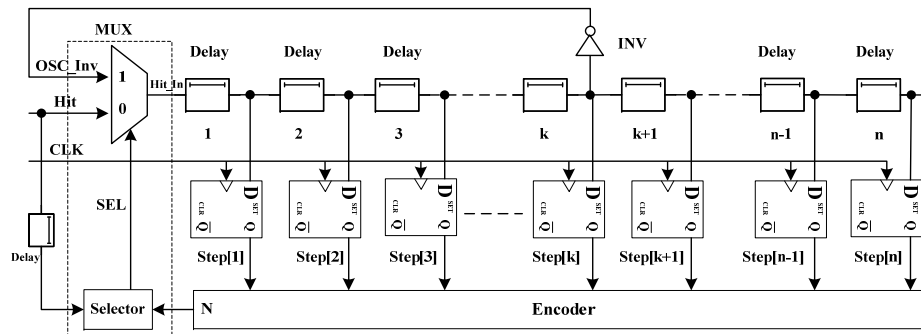
1.2 FPGA TDC研究



RMS ~ 25 ps



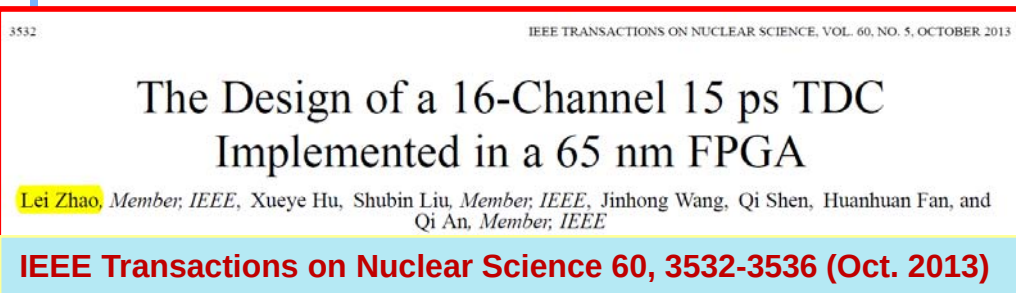
RMS ~ 8 ps



- 不改变任何硬件的基础上进一步提升性能至8 ps测量精度
- 基于原有研究基础，在校青年创新基金、安徽省教育厅、核探测与核电子学重点实验室择优项目等（主持）支持下，深入研究FPGA TDC技术。
- 基于信号序列多次测量技术和非线性修正方法。

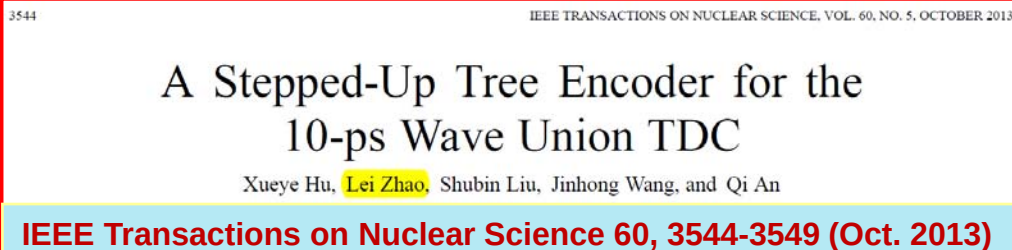
1.2 FPGA TDC研究

- 完善通用FPGA TDC测量模块的功能。
- 改进译码电路的设计，为将其实用化做好准备。

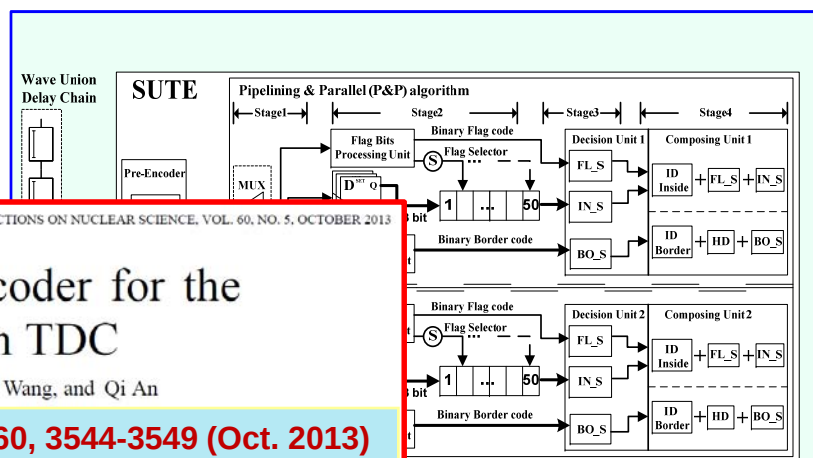


Abstract—We present the implementation of a high-resolution Time-to-Digital Converter (TDC) in a Field Programmable Array (FPGA) from Xilinx Virtex-5 family. The design of the TDC is based on a counter and interpolator method. Dedicated carry chains in CARRY4 blocks of the Virtex-5 FPGA are utilized for interpolation, which realizes the fine time measurement within one system clock period. Simulation results show that the delay from CIN to COUT in CARRY4 block is as large as 104 ps. To subdivide the delay cell into finer taps for a higher resolution considering the inhomogeneous delay cells, multiple strategies are applied to perform the calibration and to enhance the TDC resolution. Meanwhile, we also apply Place and Route (PAR) constraints to fit our TDC requirements. Finally, a total of 16 TDC channels with a timing performance of about 15 ps RMS are implemented in one FPGA.

Index Terms—Compensation, field programmable gate array (FPGAs), time measurement, time-to-digital converter (TDC).



Abstract—A stepped-up tree encoder (SUTE) has been designed to deal with the issue of non-thermometer-to-binary (NTH2B) coding for a 10-ps wave union FPGA TDC. The encoder is composed of two pipeline stages: pre-encoding and parallel encoding. The pre-encoding stage is capable of bubble error correction (BEC) as well. With the NTH2B coding algorithm applied in a Xilinx Virtex-4 FPGA, we achieved a NTH2B conversion rate of up to 100 MHz for more than 2



Chinese Physics C Vol. 37, No. 10 (2013) 106102

A fast improved fat tree encoder for wave union TDC in an FPGA *

SHEN Qi(沈奇)^{1,2} ZHAO Lei(赵雷)^{1,2,1)} LIU Shu-Bin(刘树彬)^{1,2} LIAO Sheng-Kai(廖胜凯)^{2,3}
 QI Bin-Xiang(祁宾祥)^{1,2} HU Xue-Ye(胡雪野)^{1,2} PENG Cheng-Zhi(彭承志)^{2,3} AN Qi(安琪)^{1,2}

¹ State Key Laboratory of Particle Detection and Electronics, University of Science and Technology of China, Hefei 230026, China

² Department of Modern Physics, University of Science and Technology of China, Hefei 230026, China

³ Hefei National Laboratory for Physical Sciences at Microscale, Hefei 230026, China

Chinese Physics C, 37, pp. 116102-1 - 116102-9 (Oct. 2013)

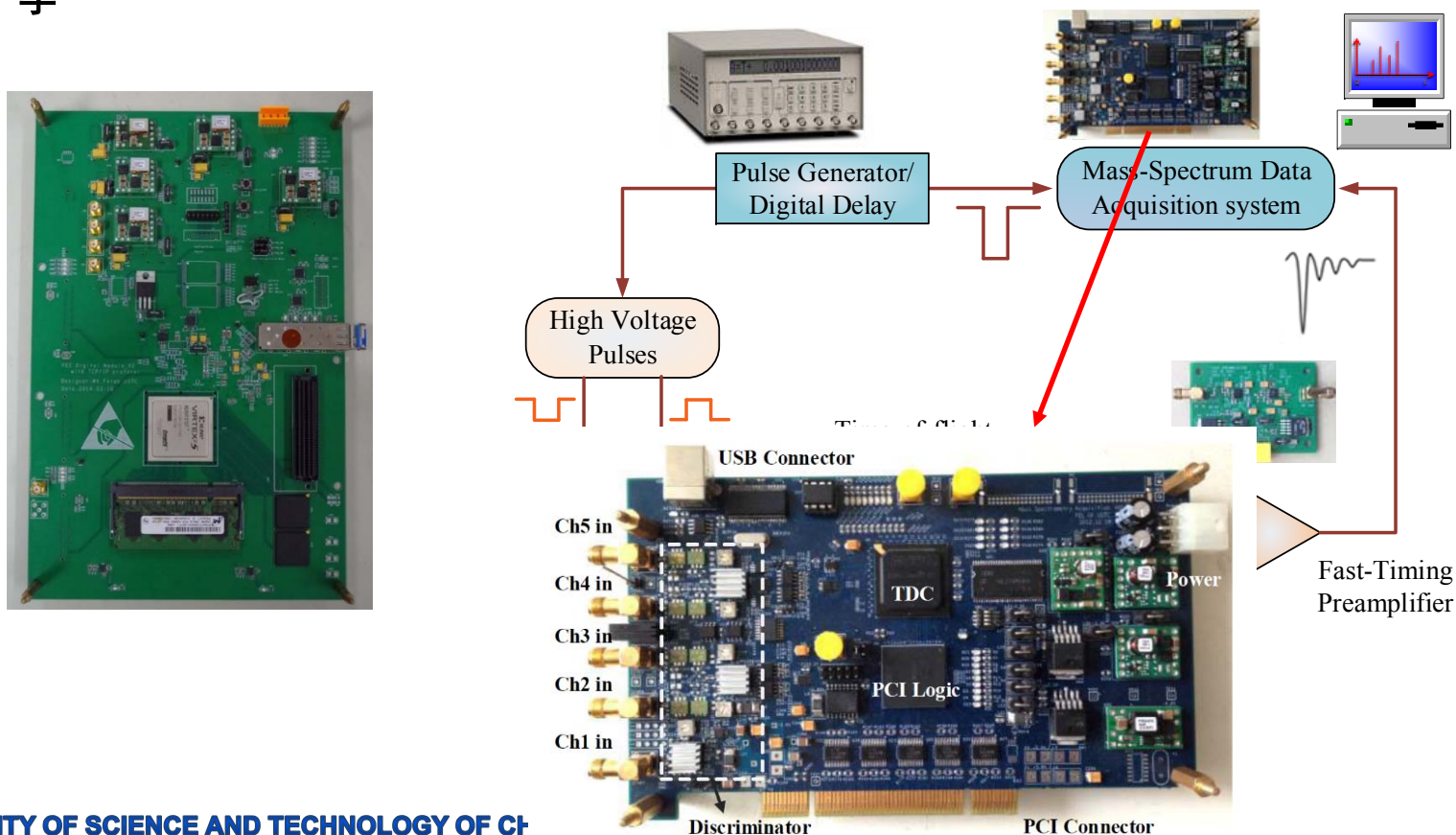
(NTH2B) encoding process should be finished within just one system clock cycle. So the implementation of the NTH2B encoder is quite challenging considering the high speed requirement. Besides, the high resolution wave union TDC also demands that the encoder convert an ultra-wide input code to a binary code. We present a fast improved fat tree encoder (IFTE) to fulfill such requirements, in which bubble error suppression is also integrated. With this encoder scheme, a wave union TDC with 7.7 ps RMS and 3.8 ps effective bin size was implemented in an FPGA

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ENGINEERING, ELECTRICAL & ELECTRONIC	Q2
NUCLEAR SCIENCE & TECHNOLOGY	Q1

1.2 FPGA TDC研究

➤ FPGA TDC的应用研究:

- ▶ 国家发改委十二五规划--大型高海拔空气簇射观测站（LHAASO）水契伦科夫探测器（WCDA）读出电子学
- ▶ 国家同步辐射实验室基于各种燃料的科学实验研究的宽压力层流预混火焰实验平台质谱仪读出电子学



1.2 FPGA TDC研究

REVIEW OF SCIENTIFIC INSTRUMENTS 85, 045115 (2014)



A field-programmable-gate-array based time digitizer for the time-of-flight mass spectrometry

Chunfeng Ye,^{1,2,3} **Lei Zhao**,^{1,2,a} Zhongyue Zhou,⁴ Shubin Liu,^{1,2} and Qi An^{1,2}

¹State Key Laboratory of Particle Detection and Electronics, University of Science and Technology of China, Hefei 230026, China

²Department of Modern Physics, University of Science and Technology of China, Hefei 230026, China

³705 Research Division, Electronic Engineering Institute, Hefei 230037, China

⁴National Synchrotron Radiation Laboratory, University of Science and Technology of China, Hefei 230029, China

-- 19th IEEE Real Time Conference, 2014, Japan
-- 22nd IEEE Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM), 2014, Boston, USA

Review of Scientific Instruments, 85, 045115-1 – 045115-7 (2014)

digital conversion, is one of the important parts in modern TOF mass spectrometry implemented with analog circuitry or application-specific-integrated-circuit (ASIC). However, it is difficult to achieve a high density with the analog approach. Furthermore, long design cycle and the function cannot be easily revised for different applications. We present a highly flexible, accurate, yet low-costing design of time digitizer based on a field-programmable-gate-array (FPGA) and time interpolation method. Test results show that the bin size of this time digitizer is 390 ps with an average standard deviation (σ) of 1.5 ps. The differential nonlinearity is in the range of -0.10 to $+0.05$ LSB (least significant bit). The measurement time range is larger than 107 s. Compared with other techniques, it is simpler and less complex while providing a good flexibility. In addition, this technique can also be used for multiple STOP pulse measurements for each START pulse reference, enabling multiple times-of-flight with a common start trigger. Besides, a time stamp is recorded for each event, rendering this time digitizer versatile in other applications. Moreover, because of the characteristic of a FPGA, more functions can be integrated in the time digitizer.

REVIEW OF SCIENTIFIC INSTRUMENTS

14 AI

(19) 中华人民共和国国家知识产权局



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(71) 申请人 中国科学技术大学

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96 号

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安琪

(74) 专利代理机构 北京科迪生专利代理有限公司 11251

代理人 杨学明

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公开号：CN103472712A、名次1/5

权利要求书1页 说明书8页 附图3页

(54) 发明名称

一种基于 FPGA 的高精度高集成度时间数字
转换器及实现方法

(57) 摘要

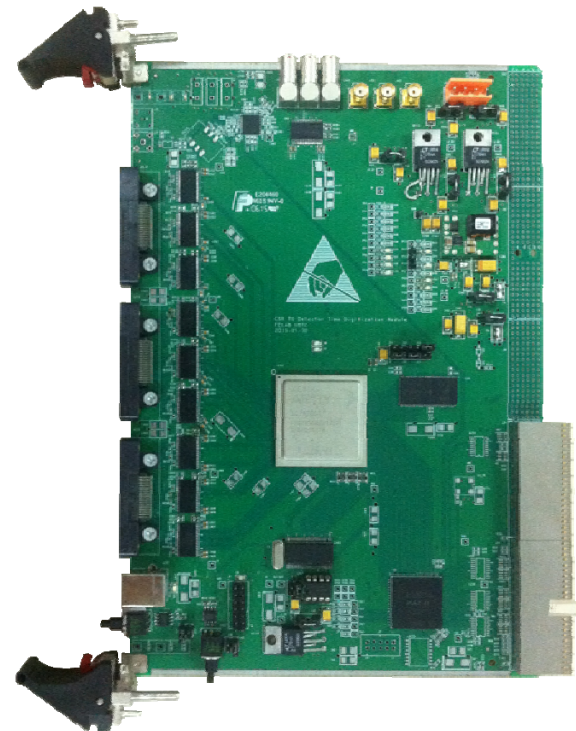
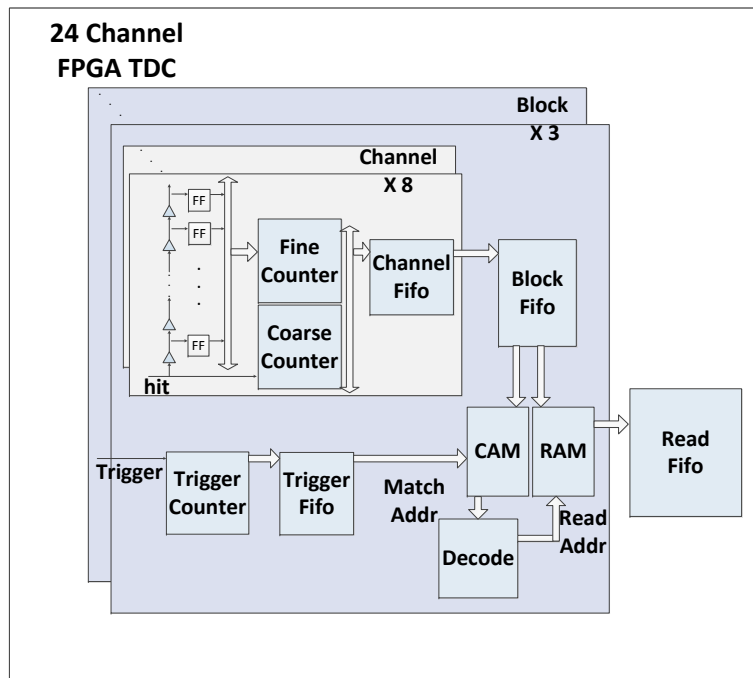
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INSTRUMENTS & INSTRUMENTATION	Q2
PHYSICS, APPLIED	Q2

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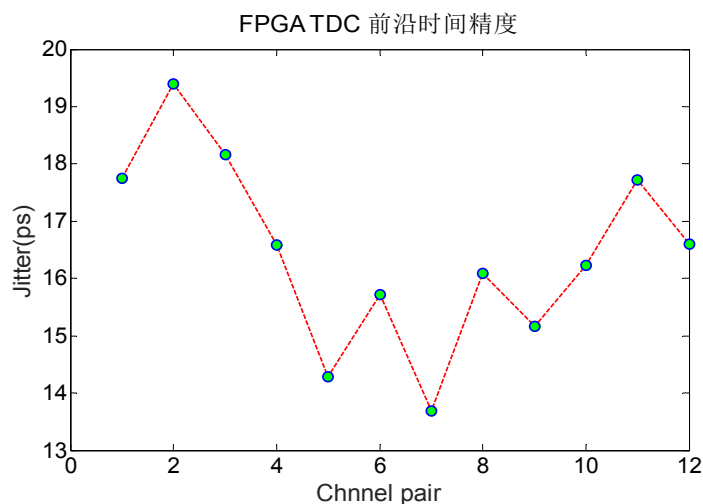
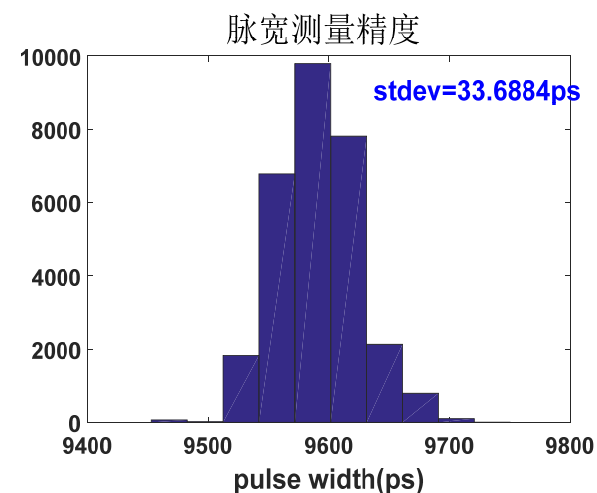
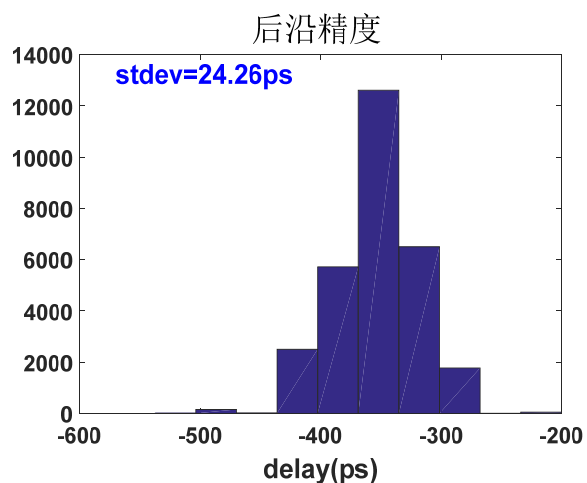
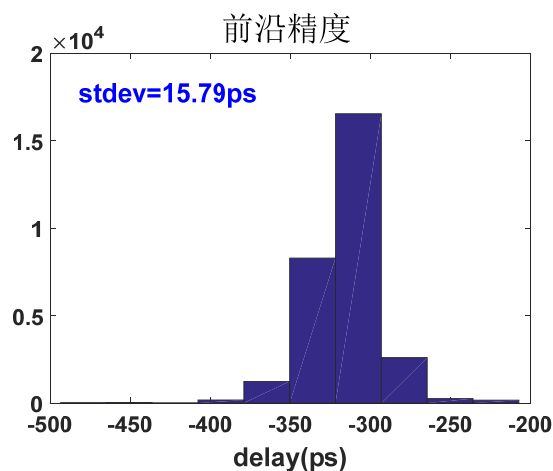
1.2 FPGA TDC研究

- ▶ 每个FPGA中集成24个TDC通道（前后沿测量）
- ▶ 时间精度 ~ 25 ps
- ▶ 包括Trigger Match功能
- ▶ 基于PXI 6U标准的数据读出接口
- ▶ 将实际应用于兰州重离子加速器（HIRFL）CSR外靶实验T0探测器读出电子学中



1.2 FPGA TDC研究

典型精度测试结果



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◆ 物理实验读出电子学芯片电路研究

◇ 1.1 ASIC研究

◇ 1.2 FPGA TDC研究

◆ 大型物理实验读出电子学工程项目上的工作

◇ 1.3 LHAASO WCDA读出电子学

◇ 1.4 兰州重离子加速器CSR外靶实验读出电子学

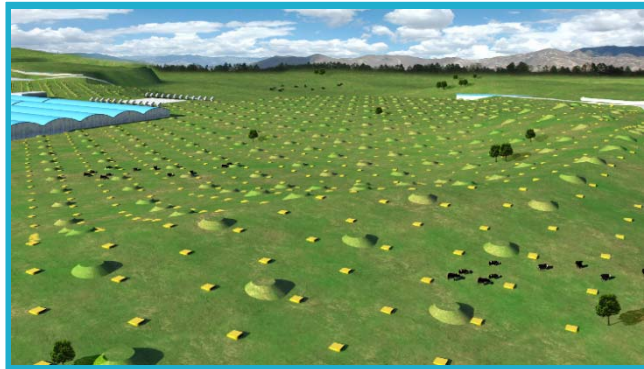
◆ 高速高精度模拟-数字变换研究

◇ 1.5 波形数字化研究

◇ 1.6 数字化束流测量研究

1.3 LHAASO WCDA读出电子学系统

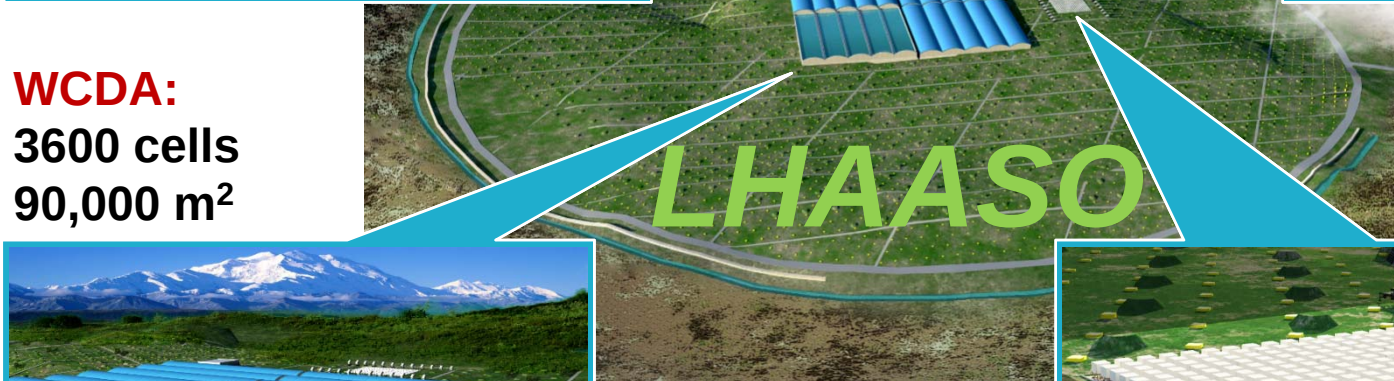
- “国家发改委十二五”规划 -- 大型高海拔空气簇射观测站（LHAASO）中的水切伦科夫探测器阵列（WCDA），负责读出电子学系统设计



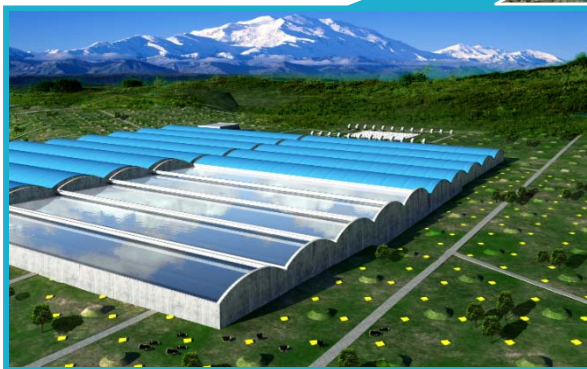
KM2A:
5635 EDs
1221 MDs



WFCTA:
24 telescopes
1024 pixels
each



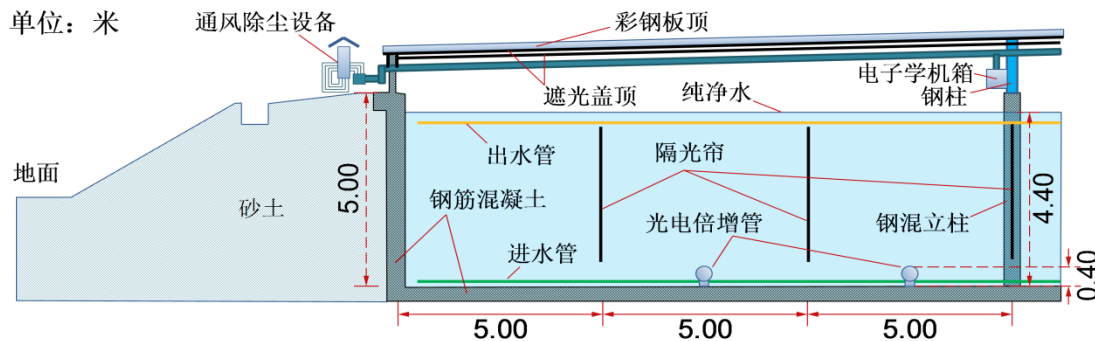
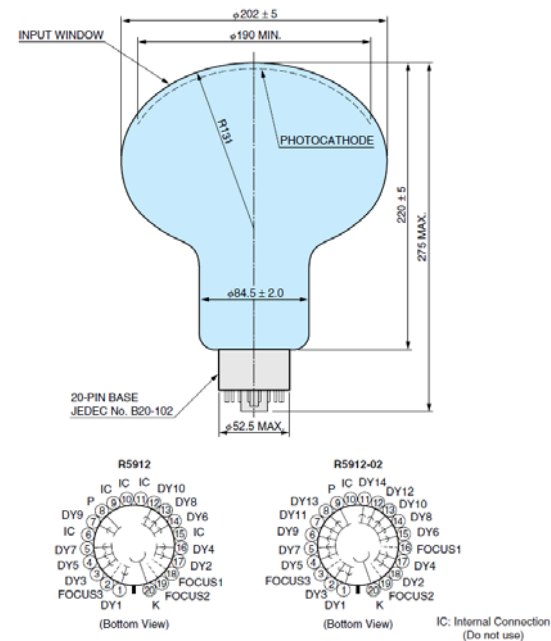
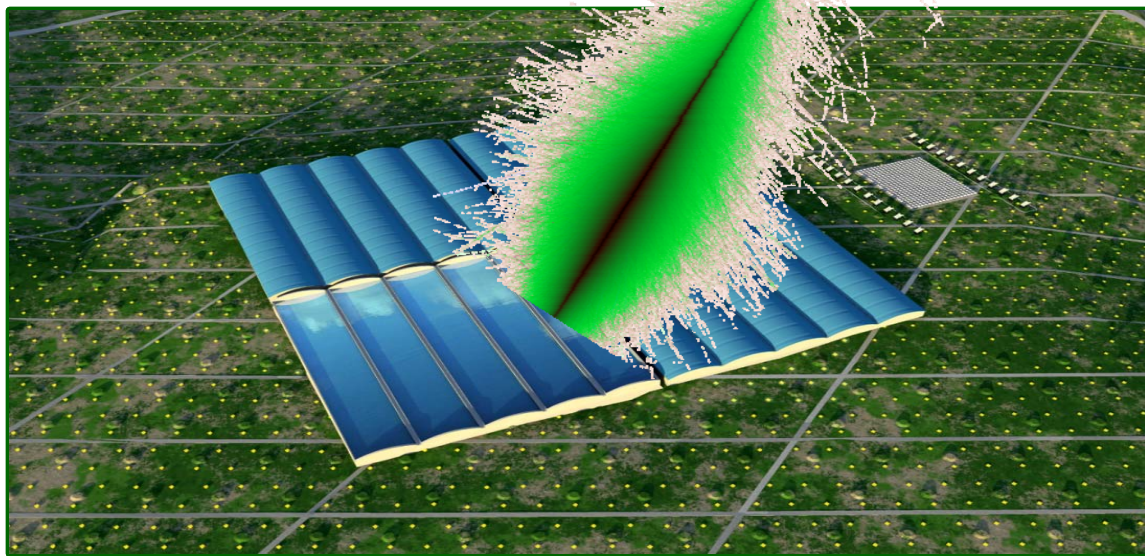
WCDA:
3600 cells
90,000 m²



SCDA:
452 detectors



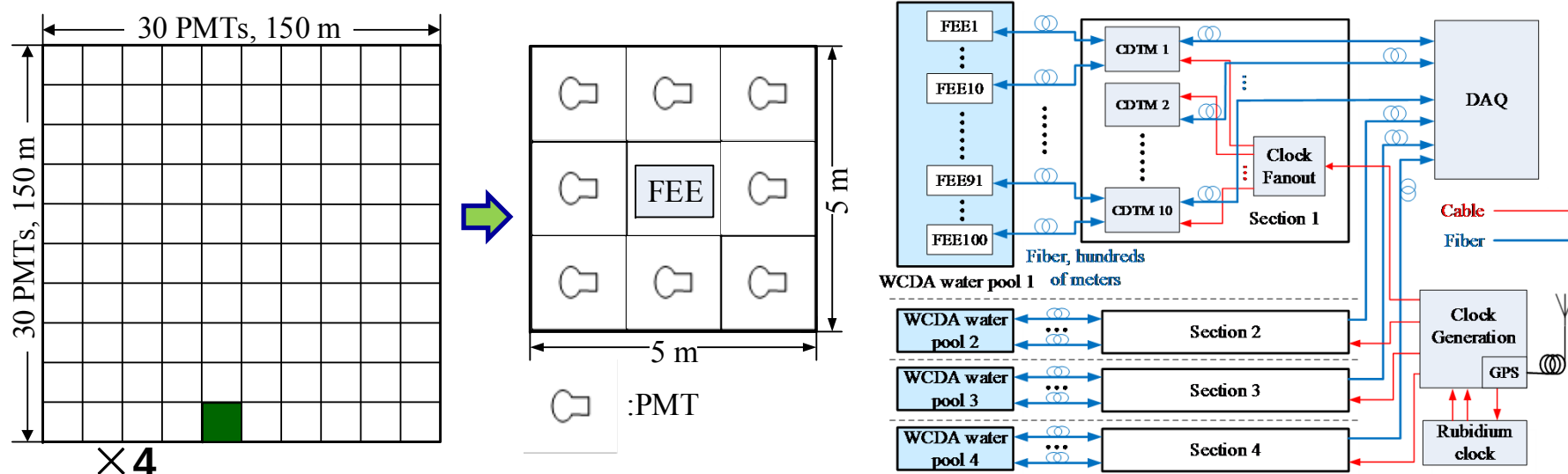
WCDA (Water Cherenkov Detector Array)



PMT: Hamamatsu R5912, 8 inch



1.3 LHAASO WCDA读出电子学系统

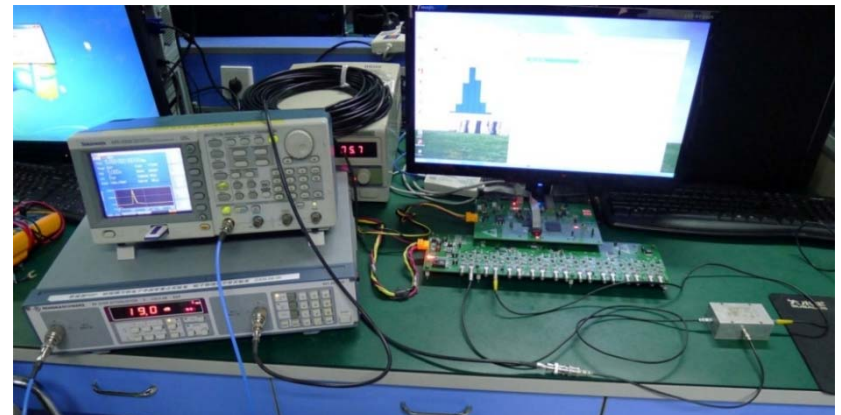
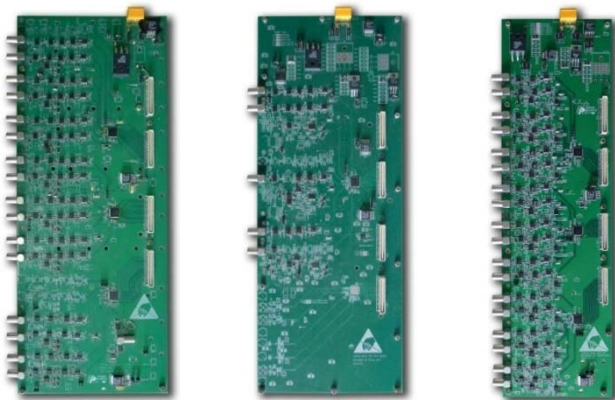
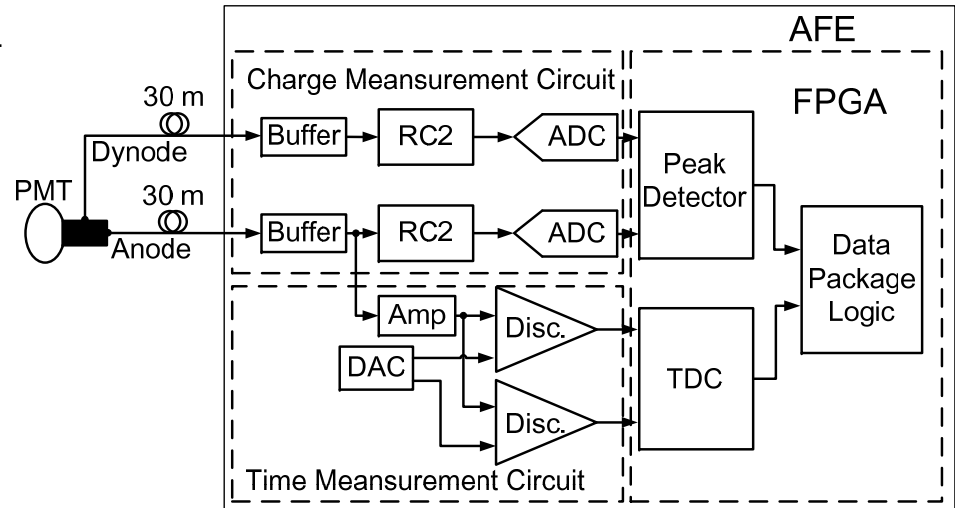


- ▶ 4400 m高海拔，四个150 m × 150 m WCDA共计9万m²
- ▶ 3600个读出通道，1 ~ 4000倍动态范围内的高精度时间及电荷测量
- ▶ 大尺度空间下的时钟分发及自动补偿
- ▶ 基于光纤的时钟、数据及命令的融合传输
- ▶ 完全无硬件触发(“Triggerless”)构架的数据读出技术

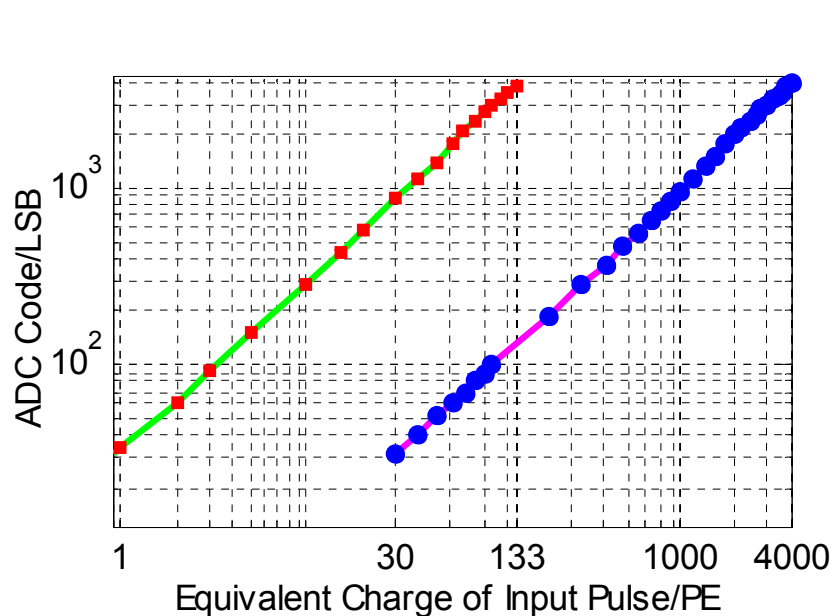
1.3 LHAASO WCDA读出电子学系统

大动态范围内高精度时间及电荷测量电子学验证和原型系统

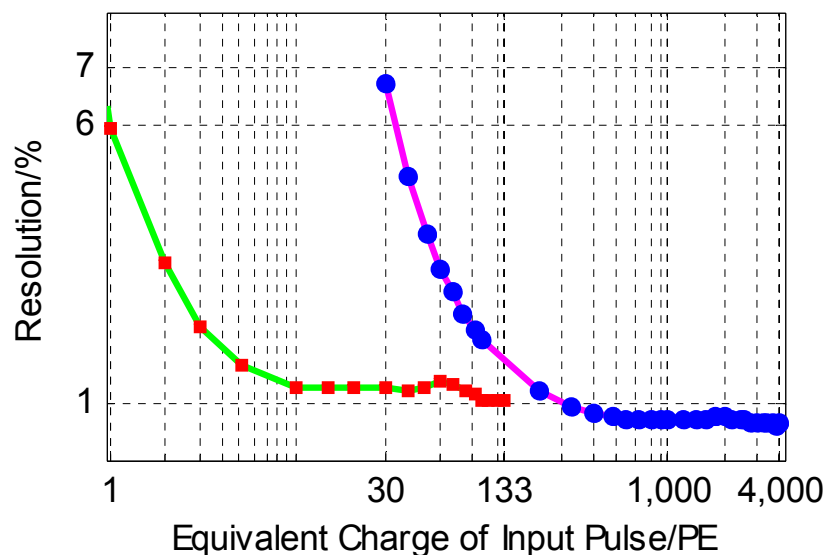
Kernel Task	Requirement
Bin size of time measurement	< 1 ns
RMS of time measurement	< 0.5 ns
Dynamic range of time measurement	2 μ s
Minimum interval of two hit signals	100 ns
Dynamic range of charge measurement	S.P.E. ~ 4000 P.E.
Resolution of charge measurement	30% @ S.P.E.; 3% @ 4000 P.E.
Channel number	3600



电荷精度测试结果



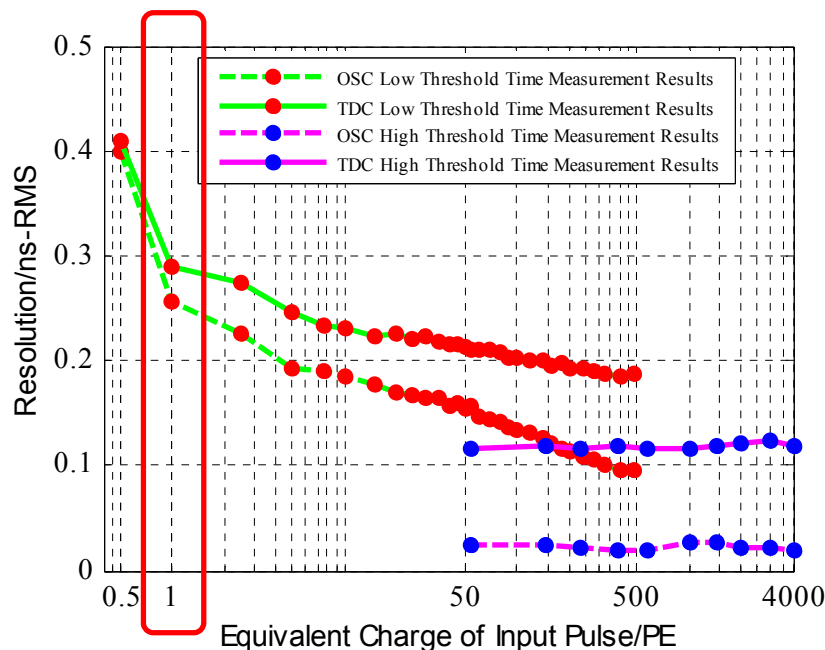
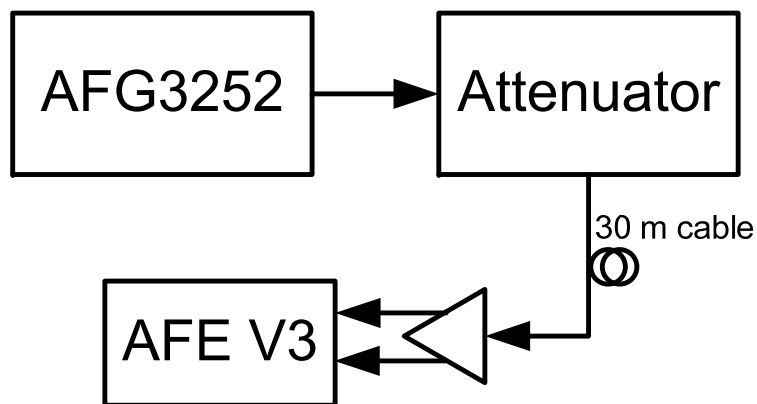
(8th Dynode)



▶ 实验室测试结果

- ◇ Using PMT output signal (2、17、35、130、640、4000PE)
- ◇ Charge resolution
 - <10% (@ S.P.E)
 - <2% (@4000 PE)

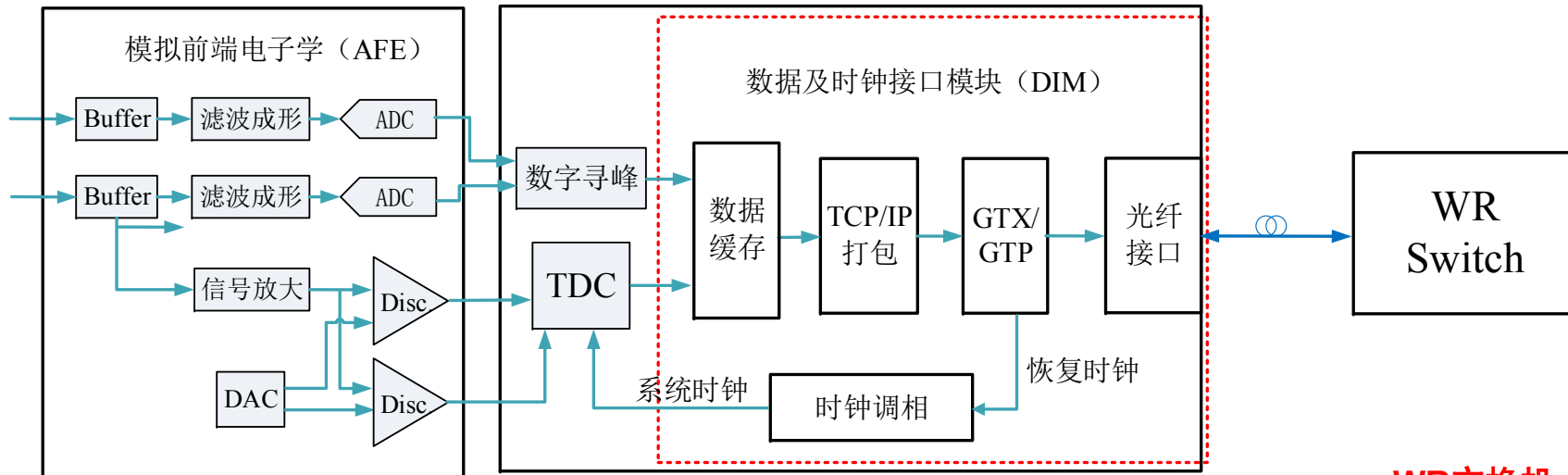
时间精度测试结果



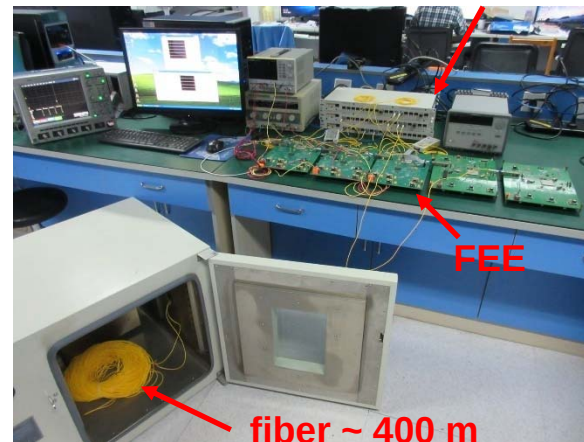
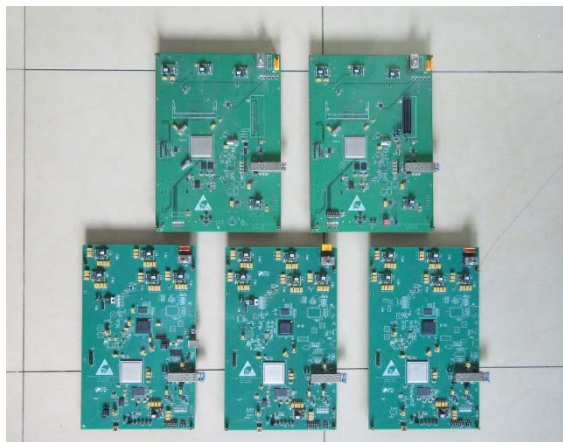
- ▶ 时间精度好于0.5 ns RMS
- ▶ 此处TDC量化误差同时作用于最终结果，所以精度指标稍差于使用示波器测量时的结果

1.3 LHAASO WCDA读出电子学系统

大尺度空间分布的多节点高精度时钟相位自动补偿及
基于千兆以太网的TCP/IP数据传输验证及原型系统

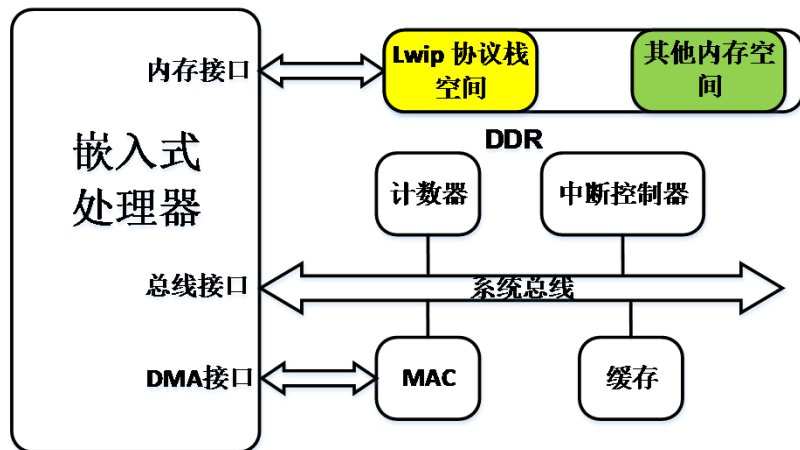


- ▶ 数据及时钟接口：
 - TCP/IP 打包与上传
 - 接收WR 时钟，对齐
 - 命令解析

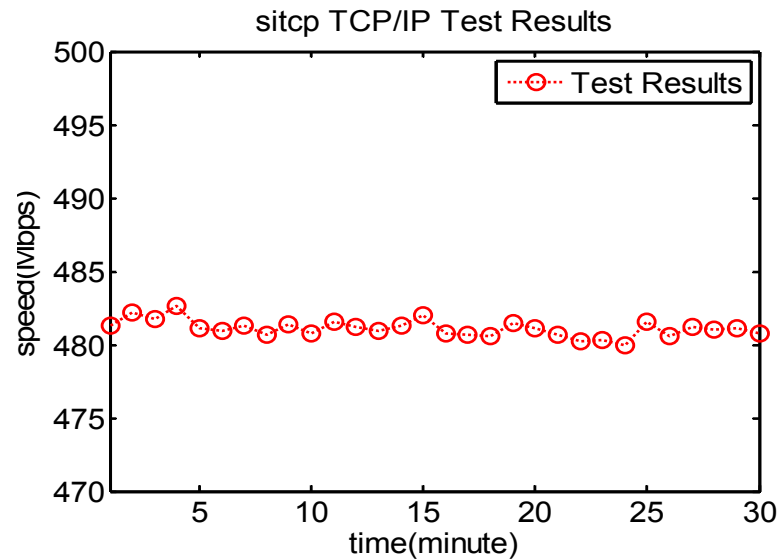
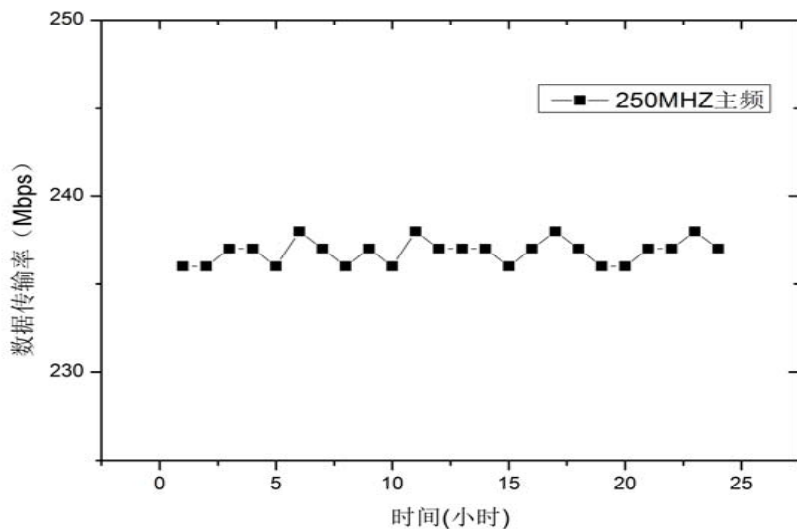
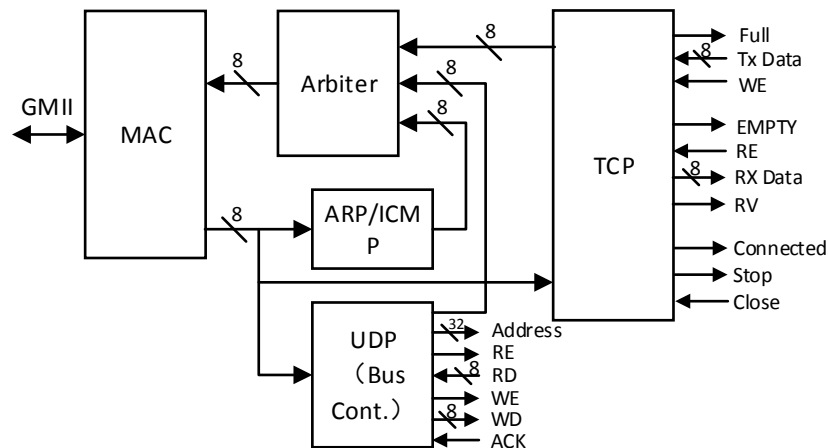


1.3 LHAASO WCDA读出电子学系统

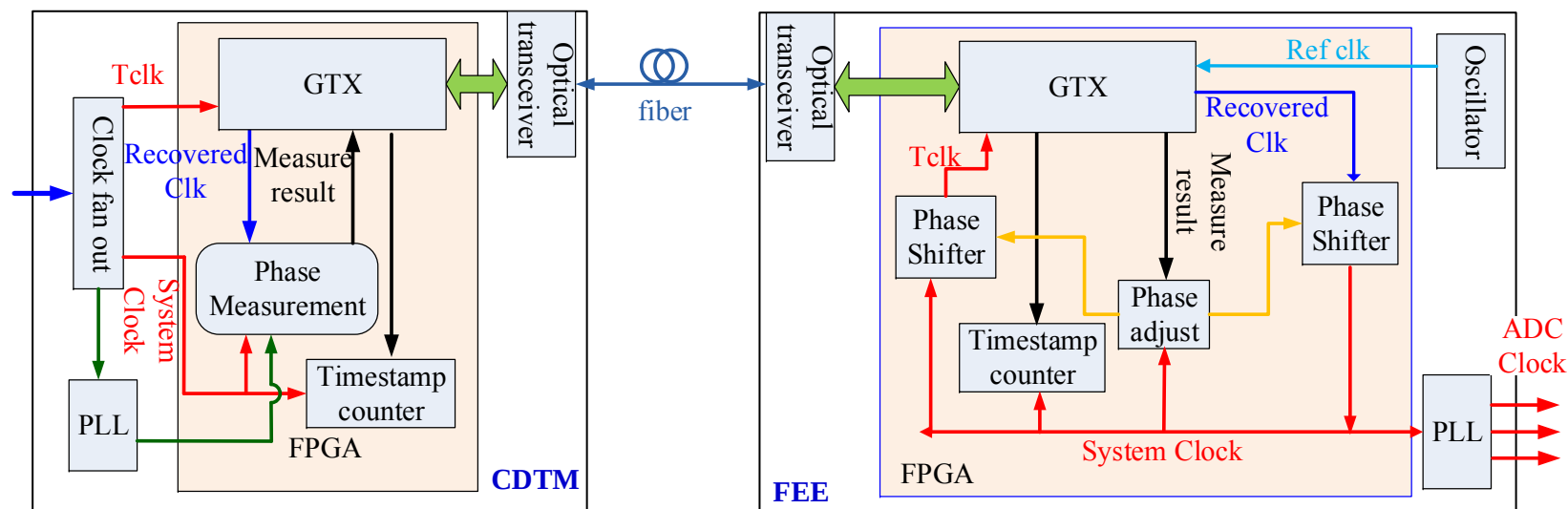
嵌入式系统：PowerPC, Microblaze



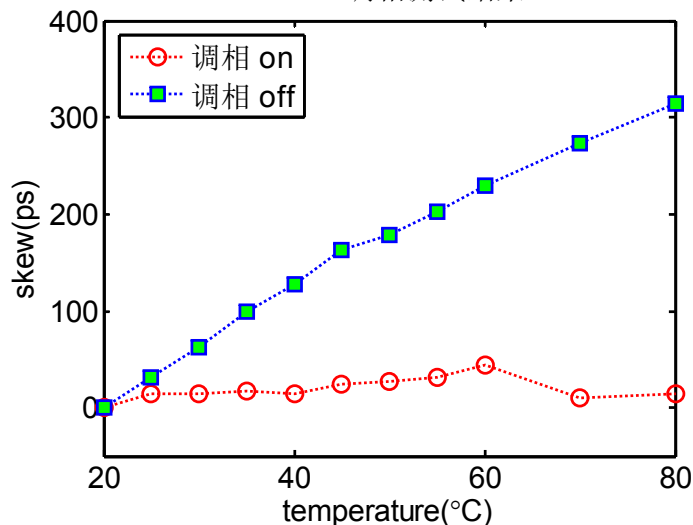
SiTCP



基于自定义PTP协议的时钟相位自动补偿



WRPC调相测试结果



在White Rabbit (WR) 协议基础上进行优化和提升，基于延时增量动态分配技术和FPGA精确相位调整实现长距离多节点时钟相位自动补偿

- IEEE Transactions on Nuclear Science
- 国家发明专利申请公示中

1.3 LHAASO WCDA读出电子学系统

- ▶ 2015年6月11日，LHAASO WCDA电子学定型评审会在重点实验室顺利举行。
- ▶ 评审委员会认为此原型电子学系统各项性能均达到设计目标，技术定型顺利通过评审。



LHAASO 项目经理部（筹）文件

2015（办字 01 号）

LHAASO-WCDA 读出电子学设计定型评审结论通知

水切伦科夫探测器阵列（Water Cherenkov Detector Array, WCDA）是“国家发改委十二五”规划项目“高海拔宇宙线观测站（Large High Altitude Air Shower Observatory, LHAASO）”的主体阵列之一，具有高计数率、单光电子测量、大动态范围、大尺度空间分布等特点，其读出电子学系统技术指标高、设计难度大。

中国科学技术大学核探测与核电子学国家重点实验室经过 2 至 3 个版本的电子学设计、测试进行优化并顺利完成设计定型，在原型系统设计中采用了许多创新的技术和方法，如大动态范围内的高精度时间及电荷测量技术、大尺度空间的多节点时钟相位自动补偿技术、时钟和数据及命令的融合传输技术等，成功攻克了相关的关键技术难题。

LHAASO 项目经理部（筹）对中国科学技术大学核探测与核电子学国家重点实验室在 LHAASO 项目中的重要贡献深表谢意，希望中科大合作组在未来的合作中做出更大的贡献。

LHAASO-WCDA 读出电子学设计定型评审会”具体的评审内容和

LHAASO项目经理部的设计定型评审结论：

“经过2至3个版本的电子学设计、测试进行优化并顺利完成设计定型，在原型系统设计中采用了许多创新的技术和方法...，成功攻克了相关的关键技术难题。

LHAASO 项目经理部（筹）

2015年7月2日

1.3 LHAASO WCDA读出电子学系统

Articles in Progress

Precise Clock Synchronization in the Readout Electronics of WCDA in LHAASO

IEEE Transactions on Nuclear Science

Manuscript Number

TNS-00169-2015

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IEEE TRANSACTIONS ON NUCLEAR SCIENCE

Precise Clock Synchronization in the Readout Electronics of WCDA in LHAASO

Lei Zhao, Member, IEEE, Shaoping Chu, Cong Ma, Xingshun and Qi An, Member,

Abstract—The Water Cherenkov Detector Array (WCDA) Water

IEEE Transactions on Nuclear Science

审稿人评价:

I really enjoyed reading the article. It is well-structured, illustrated and written....

please consider sharing your work with the WR community, I'm sure everyone would be very excited about your work.

阅读此文章是一个非常愉快的过程。此论文写得很好...建议将此论文与WR领域的人员共享,我相信大家对你的工作会感到惊喜。

measurement, WCDA.

UNIVERSITY OF SCIENCE AND TECHNOLOGY

- Chinese Physics C, accepted 通讯作者
- Chinese Physics C, 38, 016101-1 – 016101-5 (2014) 第一作者
- Chinese Physics C, 37, 126101-1 - 126101-7 (Dec. 2013) 通讯作者
- 核电子学与探测技术, 34(6), 684-688 (2014年6月) 通讯作者

IB157584F



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北京市海淀区西三环北路 87 号 11 层 4-1105 室
中科专利商标代理有限公司 任岩

发文日:

2015 年 07 月 07 日

国家发明专利、申请号: 201510390265.1、申请公示中、名次1/5



申请号或专利号: 201510390265.1

发文序号: 2015070700441170

专利申请受理通知书

根据专利法第 28 条及其实施细则第 38 条、第 39 条的规定, 申请人提出的专利申请已由国家知识产权局受理。现将确定的申请号、申请日、申请人和发明创造名称通知如下:

申请号: 201510390265.1

申请日: 2015 年 06 月 30 日

申请人: 中国科学技术大学

发明创造名称: 高精度时钟分发和相位自动补偿系统及其相位调节方法

目录

1. 科研工作

◆ 物理实验读出电子学芯片电路研究

- ◇ 1.1 ASIC研究

- ◇ 1.2 FPGA TDC研究

◆ 大型物理实验读出电子学工程项目上的工作

- ◇ 1.3 LHAASO WCDA读出电子学

- ◇ 1.4 兰州重离子加速器CSR外靶实验读出电子学

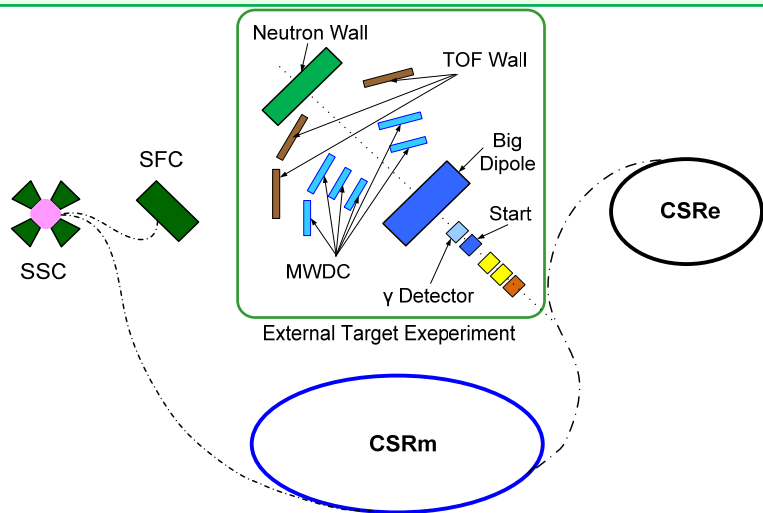
◆ 高速高精度模拟-数字变换研究

- ◇ 1.5 波形数字化研究

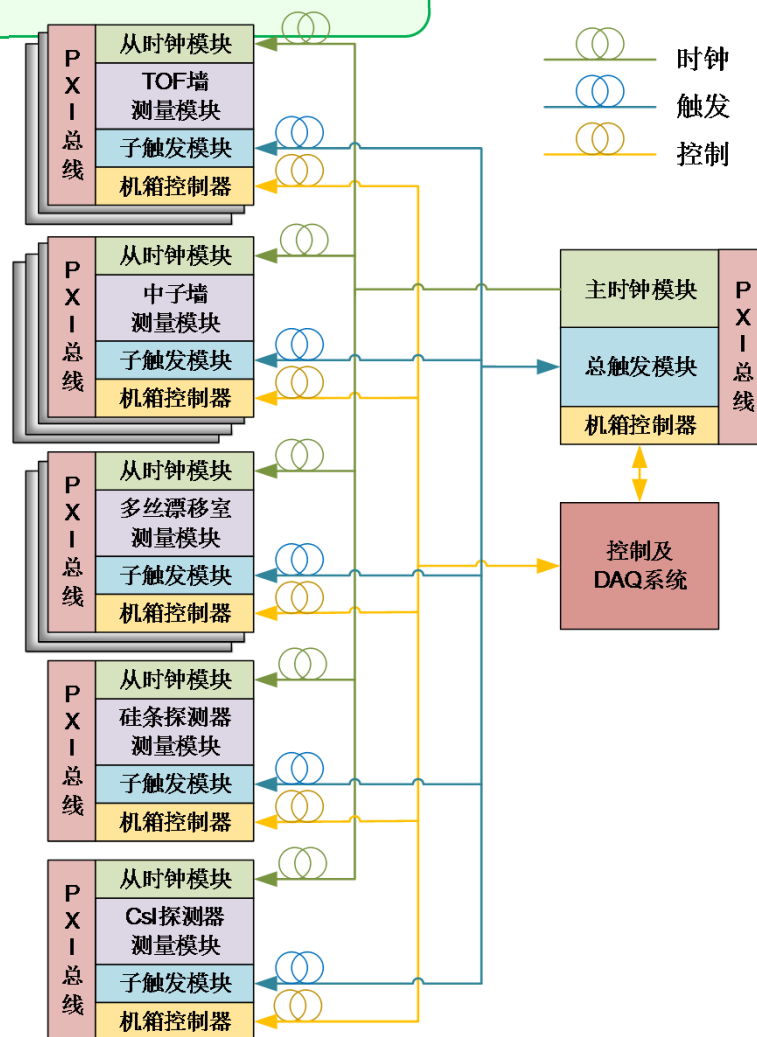
- ◇ 1.6 数字化束流测量研究

1.4 HIRFL CSR外靶实验读出电子学

兰州重离子加速器装置（HIRFL）CSR（Cooling Storage Ring） 外靶实验读出电子学系统



- 完成包含MWDC、TOF和Neutron Wall多个探测器的读出电子学系统
- 高精度、高集成度（100 ps，128 chl；25 ps，16 chl）电子学系统的设计
- 基于光纤实现多个分布式机箱中的电子学模块的时钟同步和触发信号传输



1.4 HIRFL CSR外靶实验读出电子学

探测器	总通道数	模块个数	单模块通道数	时间精度
MWDC	3000	24	128	100 ps
TOF Wall	360	23	16	25 ps
Neutron Wall	504	32	16	25 ps

- 目前已完成预研小系统的设计、测试、联调及验收
- 已完成MWDC数字化模块复制（50个，每个模块128通道，~ 100 ps）
- 完成TOF/中子墙读出模块复制（60个，每个模块16通道，时间精度~25 ps）
- 完成全局时钟、触发电子学的设计，基于百米光纤实现全局时钟及触发信号的传输

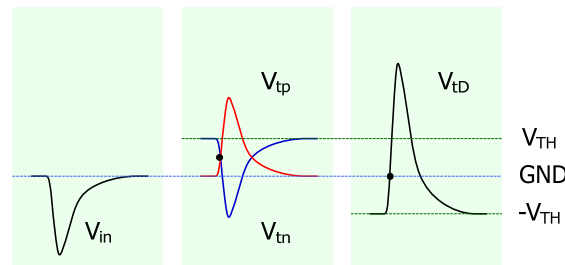
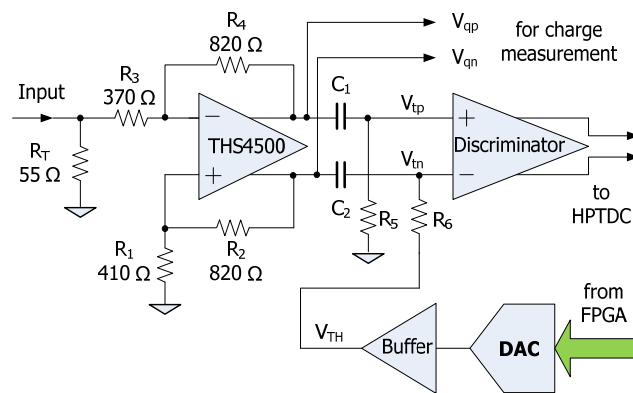
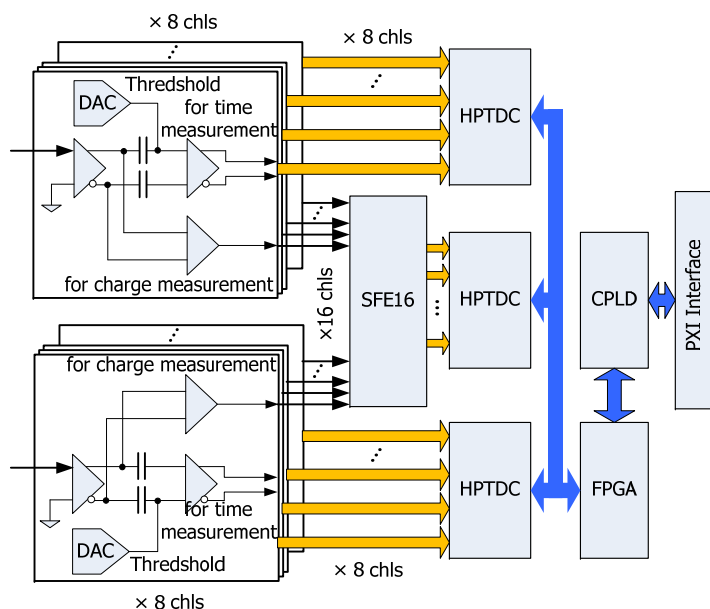
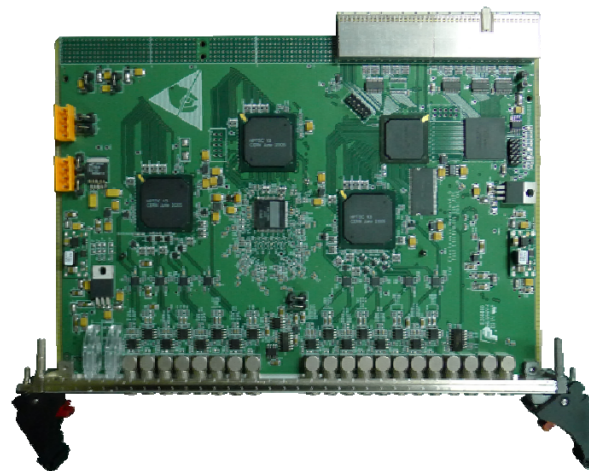


- **Journal of Instrumentation**, 9, C07003-1 – C07003-9 (2014) 第一作者
- **Nuclear Science and Techniques**, 1, 010401-1 – 010401-6 (2014) 第一作者

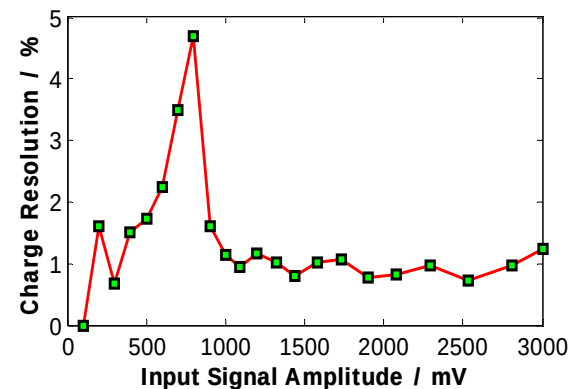
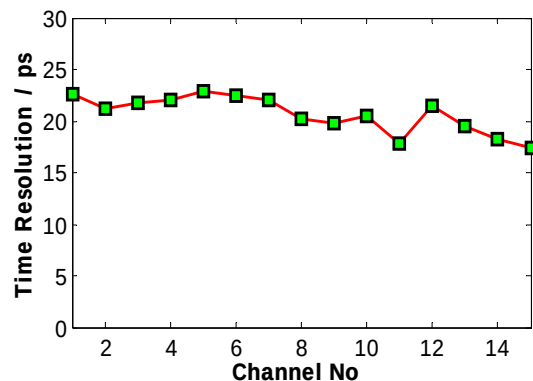
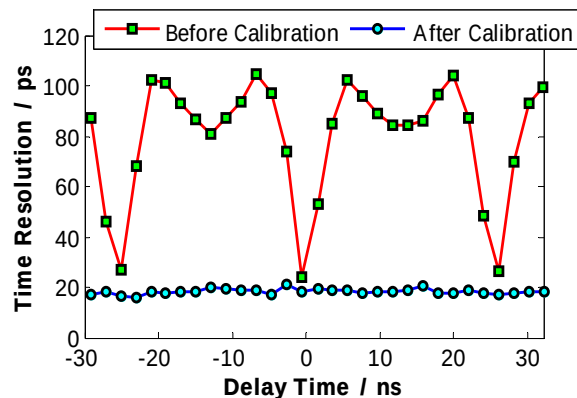
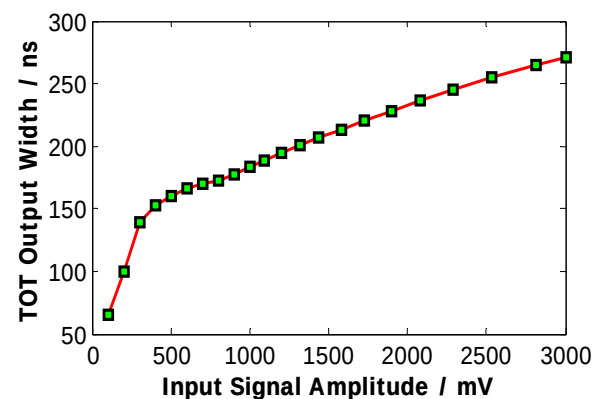
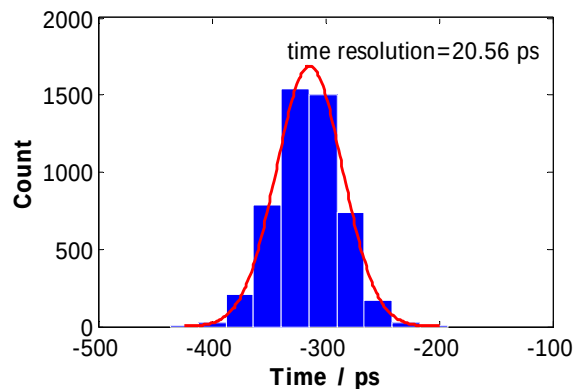
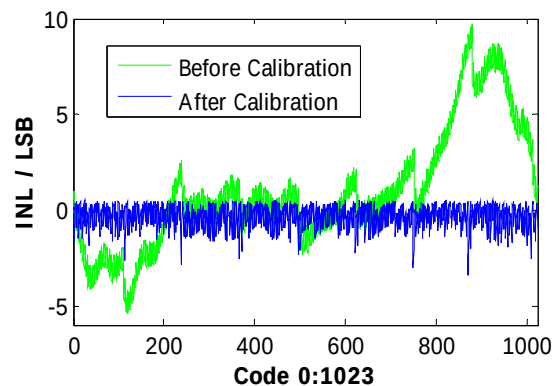
JCR® 类别	JCR 分区
INSTRUMENTS & INSTRUMENTATION	Q2

16通道高精度时间及电荷测量模块

- 集成16个通道
- 同时进行高精度时间及电荷测量
- 25 ps时间测量精度
- PXI 6U标准插件

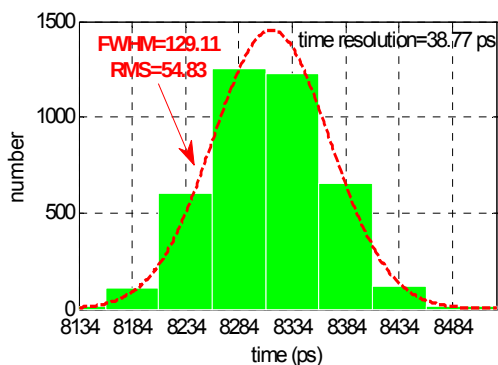
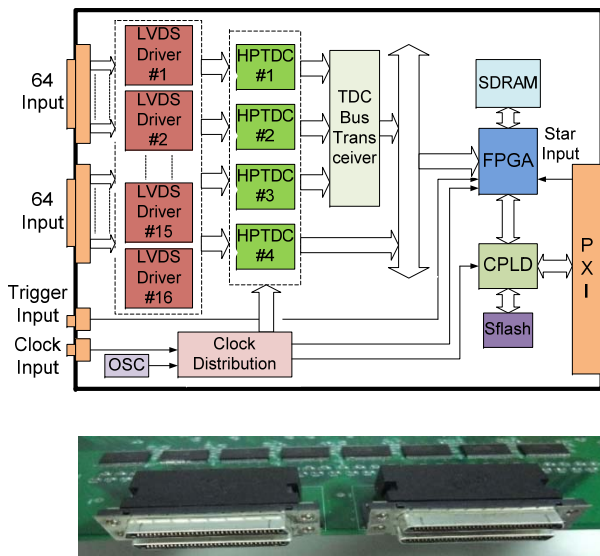


16通道高精度时间及电荷测量模块

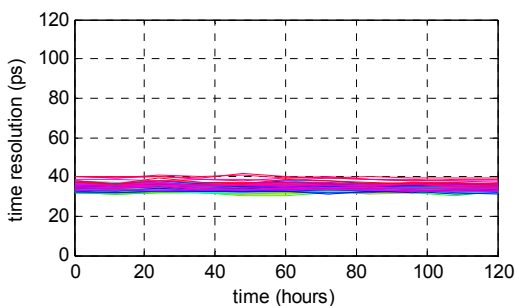


128通道高集成度时间数字化模块

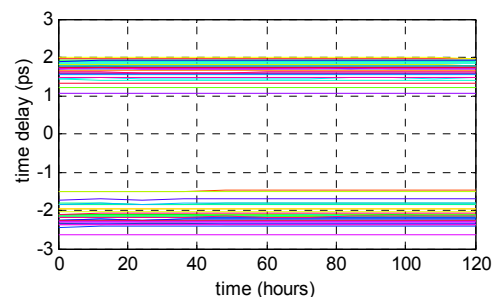
- ▶ 集成128个通道
- ▶ 高精度时间数字化
- ▶ 100 ps时间测量精度
- ▶ PXI 6U标准插件



典型时间精度结果



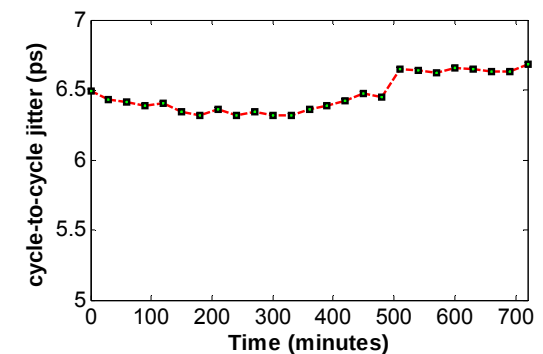
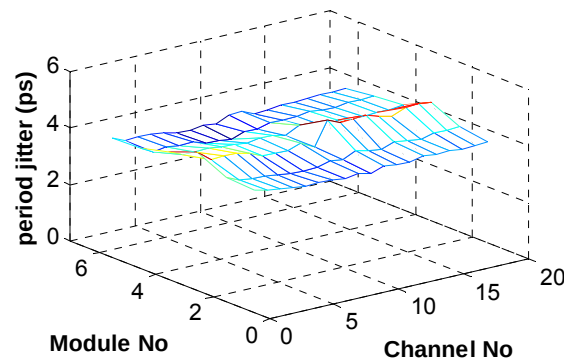
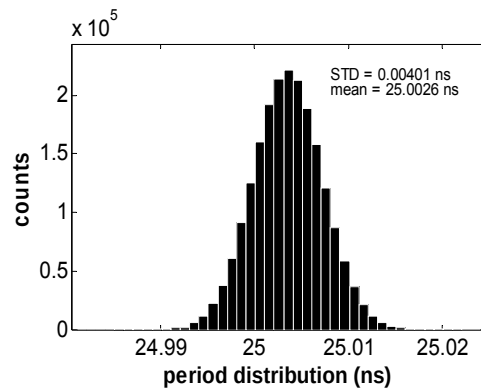
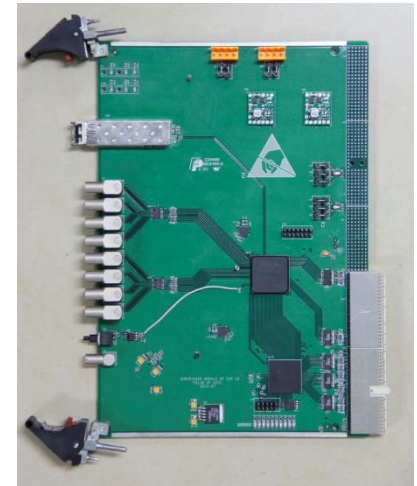
时间精度



平均值

长期稳定性测试结果

基于光纤传输的时钟及触发电子学



1.4 HIRFL CSR外靶实验读出电子学

- ▶ 2014年12月8日至12月15日，赴中科院近物所与探测器联合调试



CSR 外靶实验闪烁体探测器读出电子学系统 研制合作项目验收结论

合作项目名称： CSR 外靶实验闪烁体探测器读出电子学系统研制

合作方： 中科大快电子学实验室

合作方项目负责人： 安琪 教授

项目开发人： 赵雷、李敏、康龙飞、刘金鑫

测试负责人： 余玉洪、赵雷

CSR 外靶实验闪烁体探测器读出电子学系统由中国科学院近代物理研究所委托中国科学技术大学快电子学实验室设计完成。以先前小系统中的 TOF 高精度时间测量 PXI 模块为基础，设计并进行飞行时间探测器和中子墙探测器的电子学系统构建和测试，为下一步 CSR 外靶物理实验做准备。该电子学系统包括高精度时间及电荷测量模块、高精度时钟产生及扇出模块、FPGA 数字信号处理逻辑代码、PXI 接口逻辑代码构成了完整的 CSR 外靶实验闪烁体探测器读出电子学系统所必须的硬件、软件实物。该项目于 2013 年 4 月正式立项，目前已顺利完成 60 套 PMT 读出的 PXI 模块（简称：TOF 读出模块）及 5 套高精度时钟模块的复制。

2014 年 12 月 8 日至 12 月 15 日，中国科学技术大学快电子学实验室小组赴兰州近物所现场进行电子学系统测试，并实际与探测器系统进行了联调测试。电子学测试表明：每个时钟模块可实现 20 路高精度时钟的扇出；TOF 读出模块可以实现 16 个信号通道的高精度时

间及电荷测量，达到设计目标，其中时间测量精度达 25 ps，达到世界一流水平。

在测试现场，还将 TOF 读出电子学和时钟系统、触发系统，及以前设计完成的 MWDC 读出电子学进行了联合运行和测试，系统工作正常，探测联调结果正确并符合预期。

依据技术合作协议相关条款，合作方向近代物理研究所交付了合同规定的所有电子学模块、硬件电原理图、PCB 图、FPGA 代码源码、系统使用手册和现场测试报告数据。

现场测试结果表明此电子学系统满足合同各项要求，同意验收。

中国科学院近代物理研究所

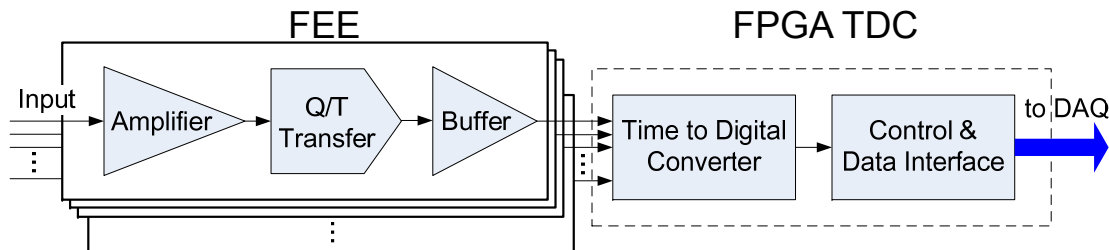
2014 年 12 月 15 日

（注：赵雷负责总体方案制定、工作安排；康龙飞负责硬件设计；李敏负责 FPGA 逻辑及 PXI 接口设计及调试；刘金鑫负责硬件复制及测试。）

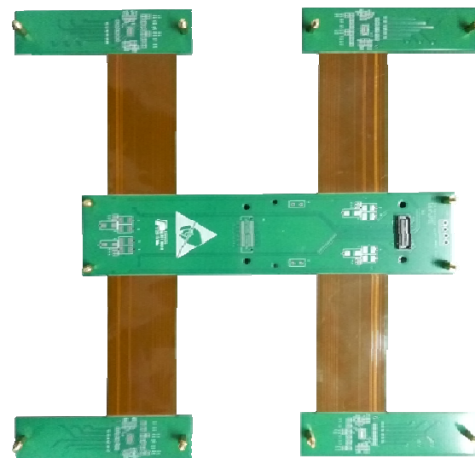
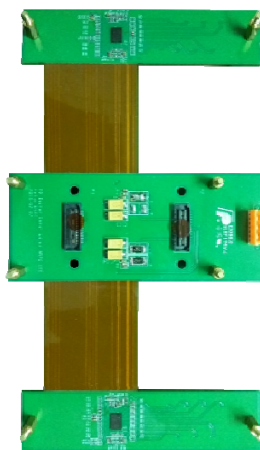
1.4 HIRFL CSR外靶实验读出电子学

兰州重离子加速器装置（HIRFL）CSR（Cooling Storage Ring）外靶实验T0探测器读出电子学系统

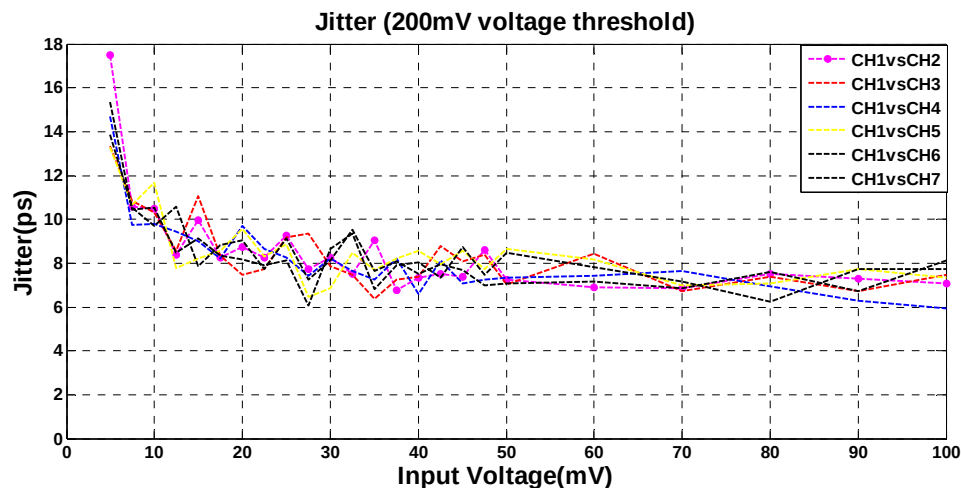
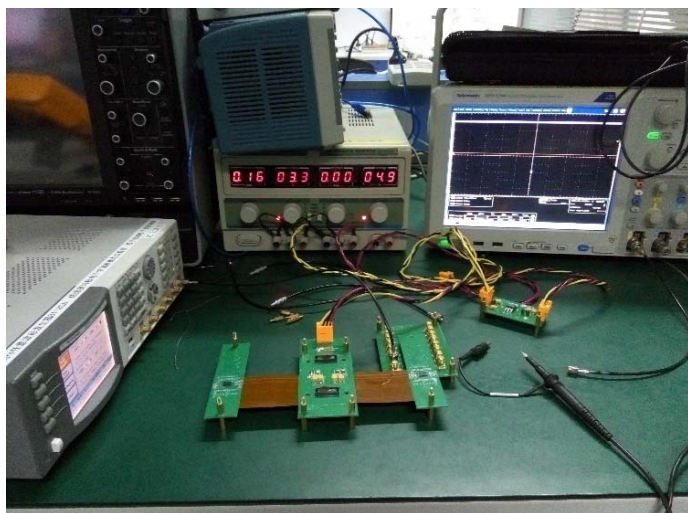
- ▶ 针对CSR外靶实验T0探测器读出需求，进行电子学系统的设计。
- ▶ 在此承担国家自然科学基金重点项目中的“读出电子学”课题。



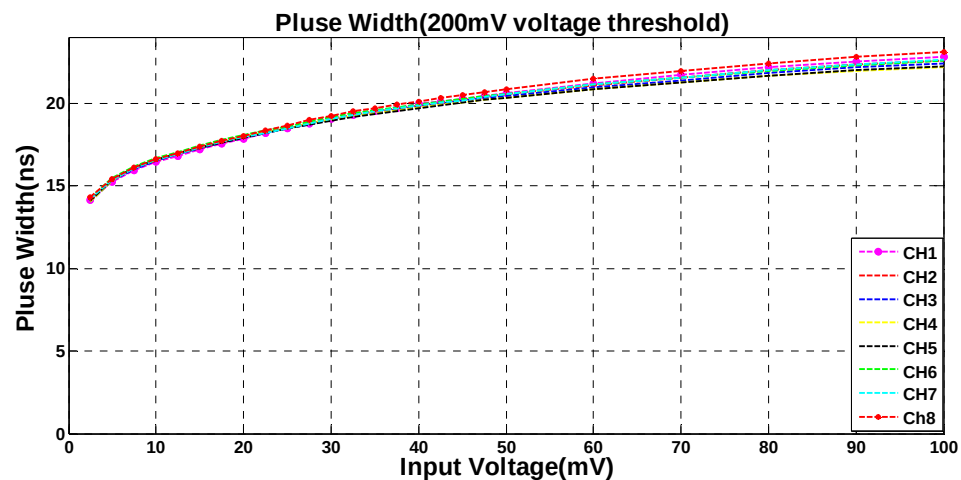
- ▶ 目前已完成FEE原型验证电子学设计以及T0 探测器的内层、外层MRPC读出FEE的设计。



T0探测器读出电子学系统 -- FEE

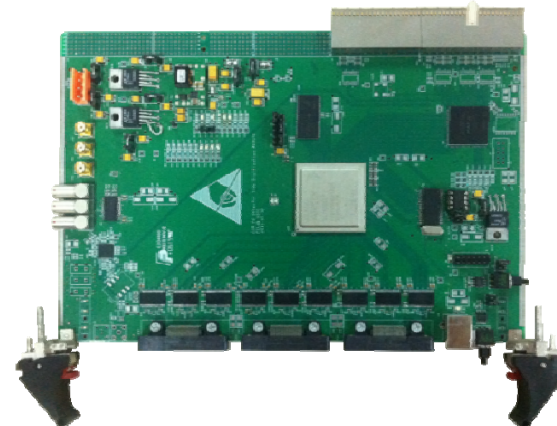
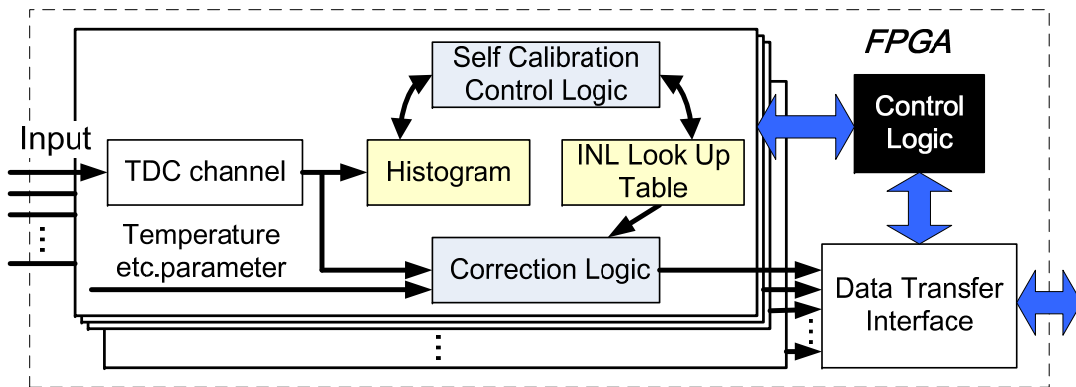


时间精度测试结果



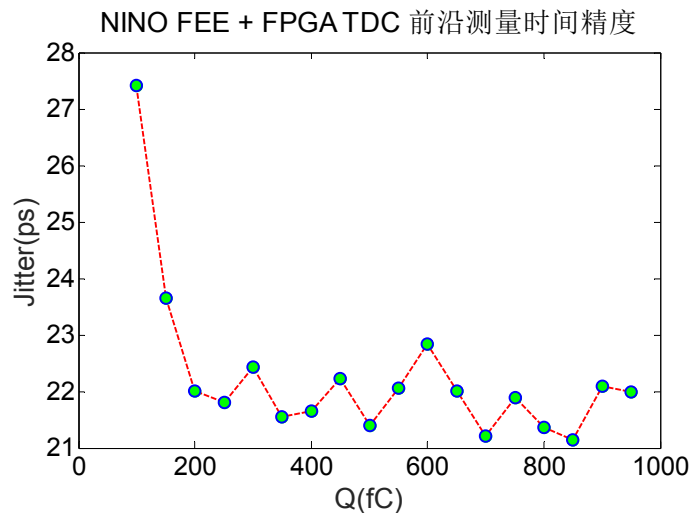
TOT输入输出转换曲线测试结果

T0读出电子学系统 -- 数字化模块



单片集成24通道, 双沿测量

Resource	Utilization	Available	Utilization %
FF	17365	267600	6.49
LUT	12817	133800	9.58
Memory LUT	432	46200	0.94
I/O	81	500	16.20
BRAM	168	365	46.03
DSP48	6	740	0.81
BUFG	6	32	18.75
MMCM	1	10	10.00



目录

1. 科研工作

◆ 物理实验读出电子学芯片电路研究

◇ 1.1 ASIC研究

◇ 1.2 FPGA TDC研究

◆ 大型物理实验读出电子学工程项目上的工作

◇ 1.3 LHAASO WCDA读出电子学

◇ 1.4 兰州重离子加速器CSR外靶实验读出电子学

◆ 高速高精度模拟-数字变换研究

◇ 1.5 波形数字化研究

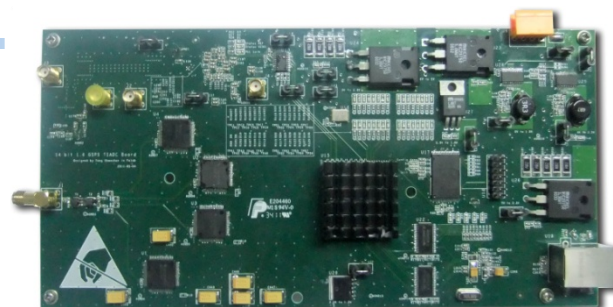
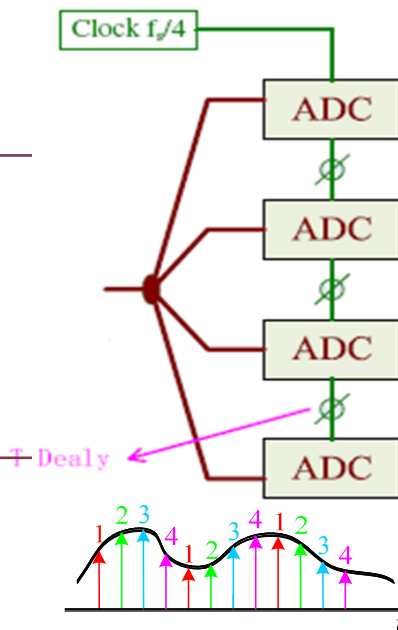
◇ 1.6 数字化束流测量研究

1.5 波形数字化研究

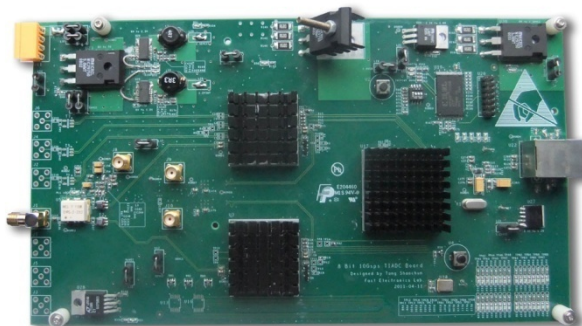
- ◆ 波形数字化是物理实验读出电子学一个新的研究方向，相比传统方法，能获得更丰富的物理信息。
- ◆ 基于超高速高精度模-数变换上的研究
 - ✓ 并行交替采样技术
 - ✓ 基于开关电容阵列的波形数字化技术

世界上代表性的采集系统

	采样率 (Gbps)	分辨率 (Bit)
ADQ108	7	8
ADQ1600	1.6	14



14 Bit@1.6 Gbps ADC系统



8 Bit@10 Gbps ADC系统



6 channel @ 5 Gbps
基于开关电容阵列的
波形数字化PXI插件

1.5 波形数字化研究

4588

IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 60, NO. 6, DECEMBER 2013

Time Measurement System Based on Waveform Digitization for Time-of-Flight Mass Spectrometer

Xiaofang Hu, Lei Zhao, Changqing Feng, Wei Zheng, Shubin Liu, and Qi An

IEEE Transactions on Nuclear Science 60, 4588-4594 (Dec. 2013)

Abstract—To guarantee a good resolution of a Time-Of-Flight Mass Spectrometer (TOF-MS), a high-performance time measurement system was required. This paper presents a time measurement system based on waveform digitization. The critical part, the 2-GSPS analog-to-digital converter is implemented using the Time-Interleaved Analog-to-Digital Conversion (TIADC) technique. Through a digital post-processing algorithm, the mismatch errors between the interleaving TIADC channels are corrected, which significantly improves the ADC performance. A Peripheral Component Interconnect (PCI) bus interface is used to communicate with a computer, achieving a data transfer rate up to 20 MByte/s using Direct Memory Access (DMA). Initial test results indicate that the system timing precision is about 196 ps Root-Mean-Square (RMS), which is good enough for the given requirements.

Index Terms—Direct memory access, time-interleaved analog-to-digital conversion, time-of-flight mass spectrometer, waveform digitization.

I. INTRODUCTION

TOF-MS is widely used in many domains due to its large dynamic range, high scan speed and simple architecture. Fig. 1 shows the block diagram of a TOF-MS. The molecules to be analyzed are firstly converted to different ions with corresponding values of m/q (m refers to the mass; q refers to the charge of the ion). These ions are then accelerated to a final kinetic energy W in acceleration region by a known electric field,

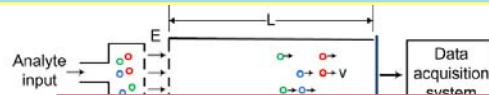


Fig. 1.

The TOF-MS system is used to measure the time-of-flight of ions. The ions are accelerated by an electric field and travel through a drift region. The time-of-flight is measured by a time-to-digital converter (TDC). The TDC is implemented using a time-interleaved analog-to-digital converter (TIADC) technique. The TIADC technique is used to convert the time-of-flight into a digital value. The digital value is then processed by a digital post-processing algorithm to correct the mismatch errors between the interleaving TIADC channels. The corrected digital value is then converted back into a time value. The time value is the time-of-flight of the ion. The time-of-flight is related to the mass-to-charge ratio (m/q) of the ion. The time-of-flight measurement is used to identify the ions.

Chinese Physics C Vol. 37, No. 11 (2013) 116102

A new method of waveform digitization based on time-interleaved A/D conversion*

YE Chun-Feng(叶春逢)^{1,2,3} ZHAO Lei(赵雷)^{1,2,1)} FENG Chang-Qing(封常青)^{1,2}
LIU Shu-Bin(刘树彬)^{1,2} AN Qi(安琪)^{1,2}

Chinese Physics C 37, 116102-1~116102-9 (Nov. 2013)

³ 705 Research Division of Electronic Engineering Institute, Hefei 230037, China

Abstract: Time interleaved analog-to-digital conversion (TIADC) based on parallelism is an effective way to meet the requirement of the ultra-fast waveform digitizer beyond Gsps. Different methods to correct the mismatch errors among different analog-to-digital conversion channels have been developed previously. To overcome the speed limitation in hardware design and to implement the mismatch correction algorithm in real time, this paper proposes a fully parallel correction algorithm. A 12-bit 1-Gsps waveform digitizer with ENOB around 10.5 bit from 5 MHz to 200 MHz is implemented based on the real-time correction algorithm.

Key words: waveform digitizer, time-interleaved analog-to-digital conversion, time-skew error, digital correction algorithms

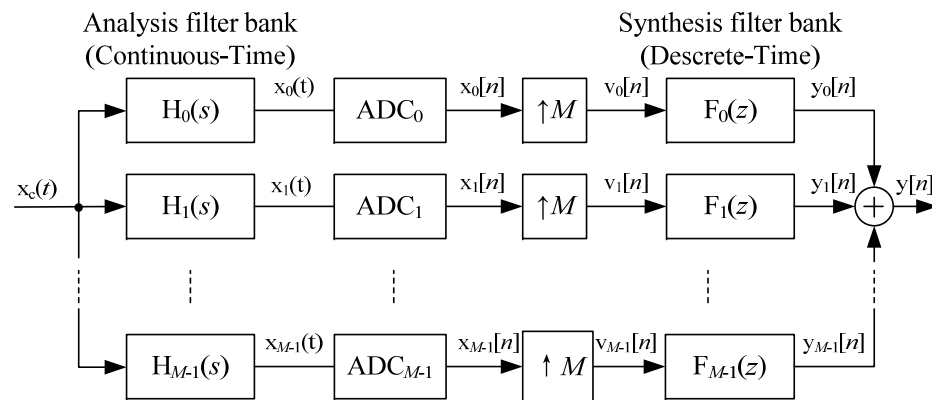
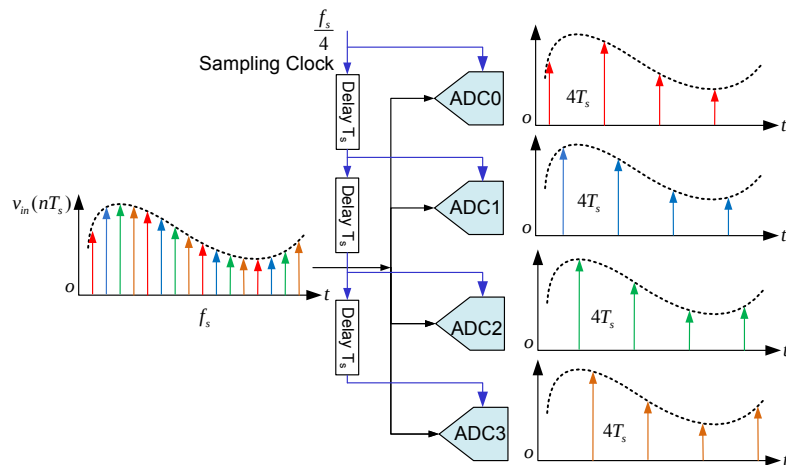
PACS: 07.05.Hd DOI: 10.1088/1674-1137/37/11/116102

1 Introduction

Compared with the traditional method based on charging integration, shaping, and low speed data acquisition, modern waveform digitizers (WFDs) can be utilized to obtain the most comprehensive physics informa-

readout electronics for LHAASO (the Large High Altitude Air Shower Observatory) KM2A [8], which is based on 12 bit ADCs with a sampling rate of 500 Msps. Considering that the rising time of photomultiplier tubes (PMTs) is about 3-4 ns, the sampling rate is not adequate to record the original waveform directly; thus a

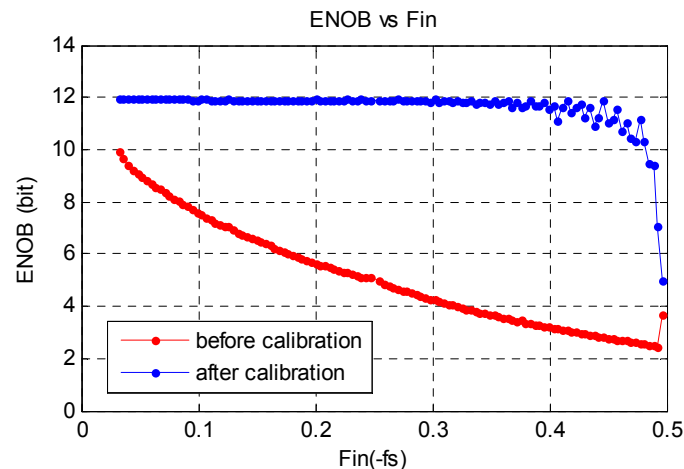
1.5 波形数字化研究



- Time interleaved A/D变换技术存在三种失配误差：

- 偏置失配误差 (Offset error)
- 增益失配误差 (Gain error)
- 时间相位失配误差 (Time-skew error)

- 探索基于新型数字修正算法进行宽带信号的修正



12 bit ADC修正效果仿真

目录

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◆ 高速高精度模拟-数字变换研究

◇ 1.5 波形数字化研究

◇ 1.6 数字化束流测量研究

1.6 数字化束流测量研究

- 束流测量关系到加速器物理实验的质量，传统的束流测量方法是基于全模拟调理的方式。

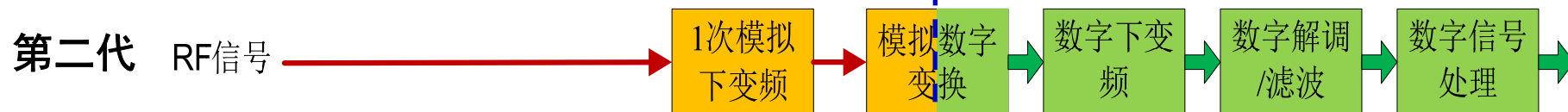
模拟信号处理领域

数字信号处理领域



代表：BEPCH中LINAC，美国先进光源ALS、韩国浦项光源PLS

◆ 高复杂度 ◆ 噪声 ◆ 非线性 ◆ 不一致性



代表：美国Los Alamos国家实验室的LEDA、Oak Ridge国家实验室的散裂中子源、德国GSI重离子加速器



代表：斯洛文尼亚的Instrumentation Technologies (IT) 公司研制的数字束流测量仪器Libera等系列

- 基于高速高精度模拟-数字变换技术，将实时数字化技术应用于加速器束流测量中，发展世界一流的数字化束测技术。

1.6 数字化束流测量研究

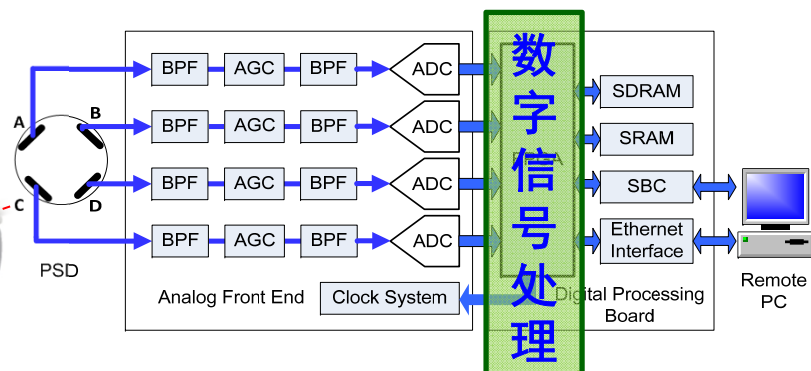
- 基于高速高精度模拟-数字变换技术，将实时数字化技术引入加速器束流测量中，发展世界一流的数字化束测技术
- 主要有相位（能量）测量、横向位置测量等方面
 - ▶ 束流横向位置测量 – 基于数字下变频技术的全数字化技术
 - 应用：上海同步辐射光源（SSRF）储存环
 - ▶ 束流相位及能量测量 – 基于中频信号正交采样技术的实时数字化技术
 - 应用：中国散裂中子源（CSNS）DTL
 - ▶ 相位及位置测量系统研究 – 基于射频信号直接正交欠采样的全数字化技术
 - 应用：中科院战略先导专项ADS

1.6 数字化束流测量研究

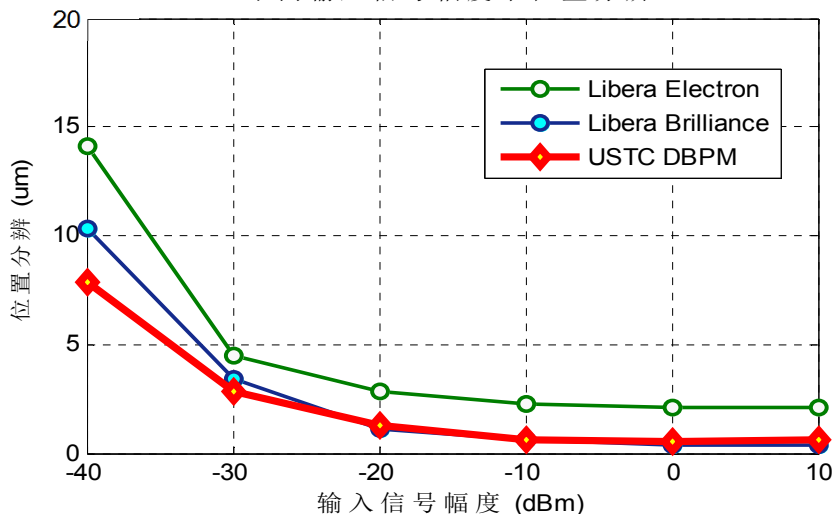
数字化束流位置测量



- 100 ps脉宽输入信号，1000倍动态范围
- 117.2799 Msps高速高精度ADC直接欠采样 + 数字IQ解调实时算法



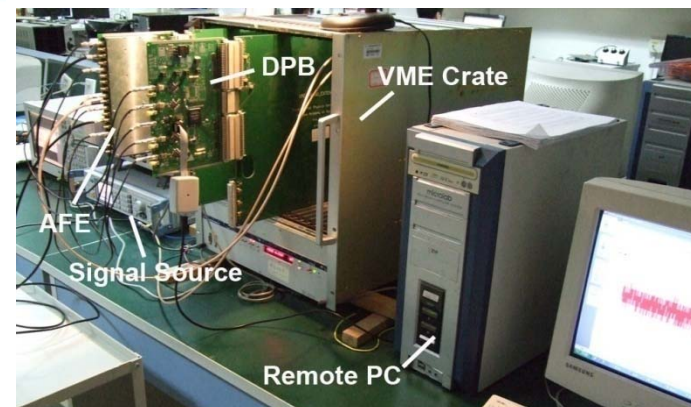
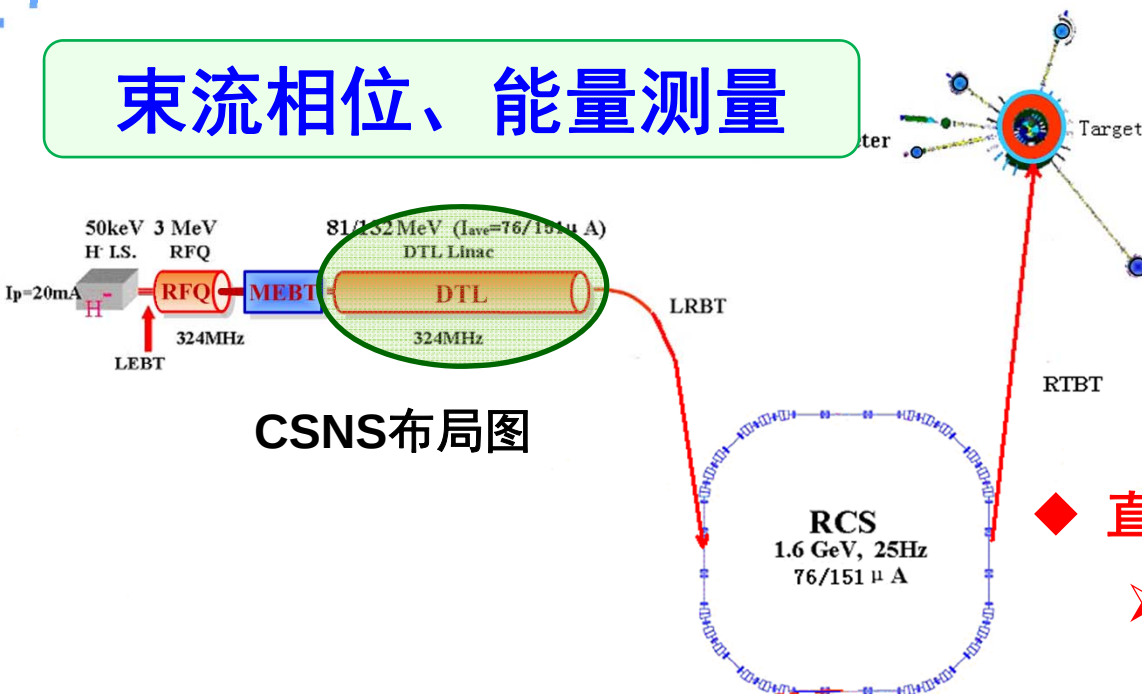
不同输入信号幅度下位置分辨



- 逐圈位置分辨测试结果 ($K_x=K_y=10$ mm)
- 关键性能指标好于世界主流代表性仪器 Libera Electron，与其新型系列性能相当。

1.6 数字化束流测量研究

束流相位、能量测量



◆ 直接IF正交采样技术

➤ 14 bit@46.96 Msps

◆ 系统测试结果： 动态范围： **57 dB**， 相位分辨好于 **0.1° (400 kHz)**



▶ BEPCII中LINAC相位测量系统： 全模拟技术

动态范围： **20 dB**， 相位分辨 **~0.2°**

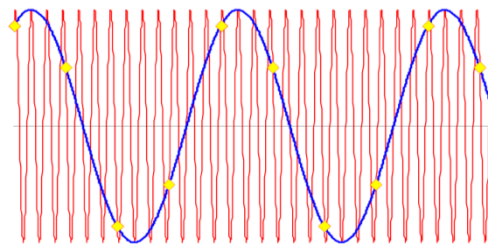
▶ LEDA中相位测量： 中频采样， 12 bit@2 Msps，

动态范围： **50 dB**， 相位分辨 **~0.2° (200 kHz更新率)**

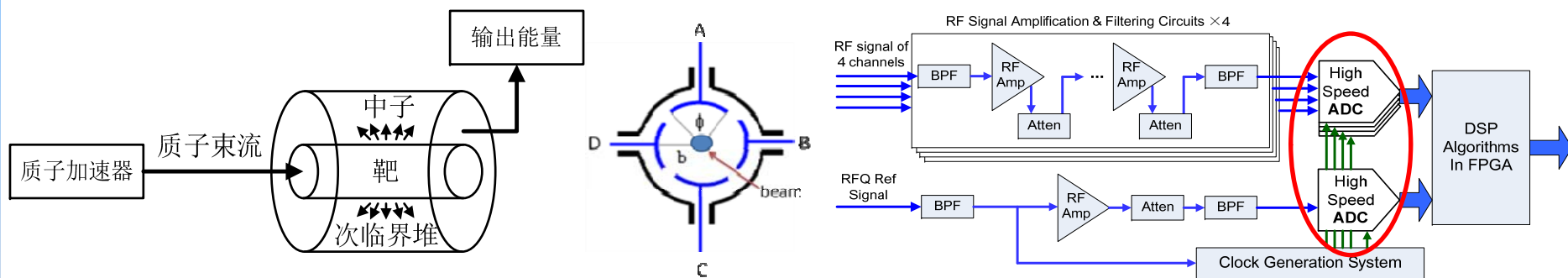
1.6 数字化束流测量研究

束流相位及位置测量

- 将束流相位及位置测量集成在单套系统中
- 基于全数字化的方案
- 以ADS质子加速器的束流测量需求为应用背景



14 bit @ 100 Msps

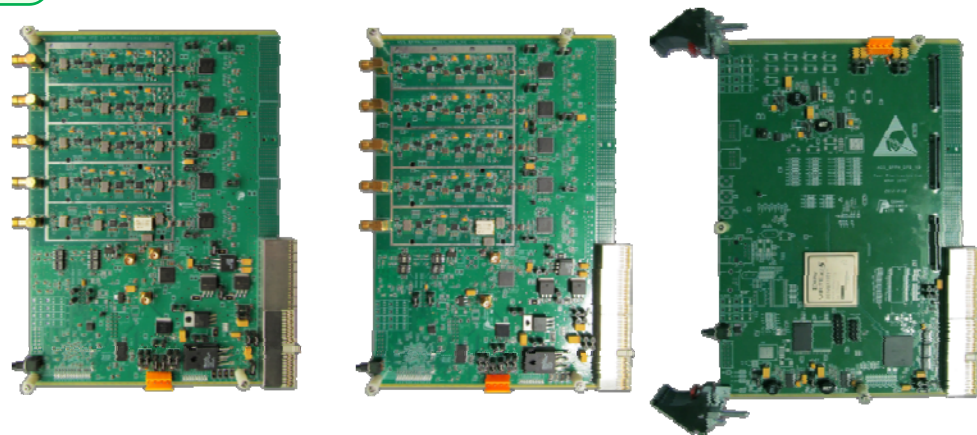
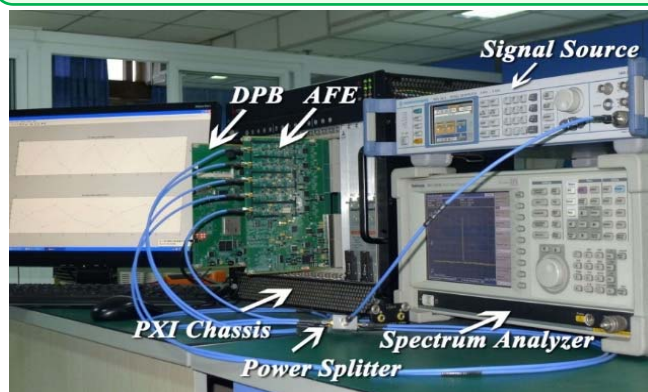


- 获国家青年科学基金（主持）、中国科学技术大学重要方向项目培育基金（主持）、及中科院战略先导专项子课题（任务负责人，XDA03020704)支持。

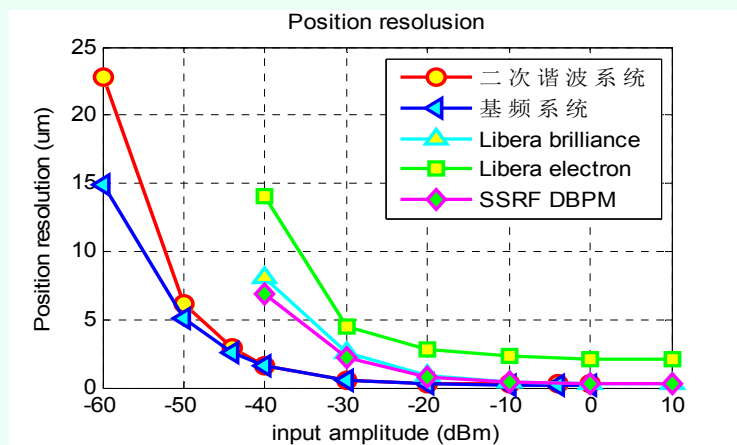
1.6 数字化束流测量研究

束流相位及位置测量

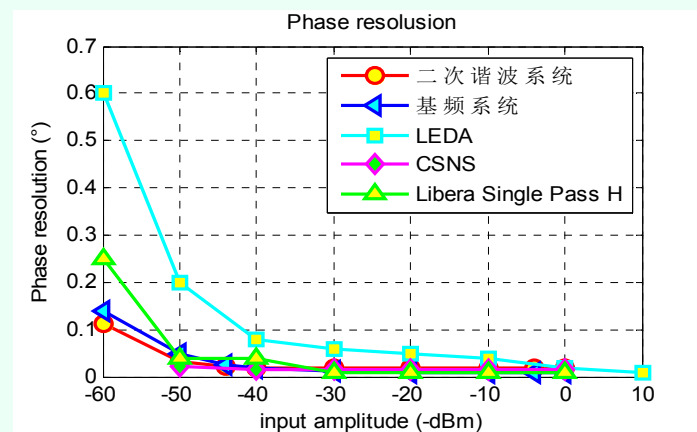
➤ 完成电子学系统的设计和系统测试



与国际典型的束流测量系统性能进行比较



位置测量精度对比



相位测量精度对比

1.6 数字化束流测量研究

数字化束流位置与相位测量系统 BPPM 测试结论

子课题名称: 数字化束流位置与相位测量系统
承担方: 中国科学技术大学快电子学研究所
子课题负责人: 安琪 教授
研究骨干: 赵雷、胡晓芳、高兴顺、汪海
测试负责人: 武军霞、张雍、赵雷、李峰

数字化束流位置与相位测量系统研制课题是中国科学院科技专项 ADS 质子直线加速器注入器 II 下设立的一子课题。中国科学技术大学快电子学实验室研制完成一套能够实现束流位置与相位同时测量的 BPM 电子学系统。该电子学系统将应用于直线加速器注入器 II RFQ 后 BPM 探头信号的分析处理。

BPPM 系统, 测量二倍频 325MHz 下该系统位置与相位长期(12 小时)与短期稳定度(1 分钟), 改变输入信号功率(-10dBm~-55dBm with step of -5dBm) 测量 BPPM 系统测量精度与稳定度。

- 结合 BPM 标定平台装置, 使用标准信号源输入正弦波信号, 经过二极管产生模拟束流信号, 通过 BPM 感应输出 RF 信号, 输入 USTC BPPM 测量系统, 测量在 162.5MHz 与 325MHz 某一信号功率(-40dBm@162.5MHz, -46dBm@325MHz)输入时, BPPM 系统与 BPM 标定平台系统联合长期稳定度(12 小时)。

- 以上测试步骤同时在斯洛文尼亚 IT 公司生产的 Libera Single Pass H (LSPH) 电子学系统上进行实验, 将 LSPH 与 USTC BPPM 系统测试结果进行对比, 得出现场联调测试报告(见附件一)。

实验室现场测试结论

1. 该电子学系统包含技术规格书中涉及的所有硬件接口, 4 路 RF

系统, 达到国际先进水平。

模拟前端电子学模块、数字信号处理模块等硬件系统、性能分析软件(含接口、用户界面), 信号处理器所必须的硬件、软件实物。联合测试件原理图、PCB 图、数字母板信号处理用 FPGA 动程序源码、上位机测试软件、电子学技术数据, 以上技术文档能是目前和后续类似信号帮助。

方案制定、系统调研、硬件设计及工作安排; 胡晓芳; 高兴顺负责 FPGA 代码开发及电子学系统测试的设计)。

中国科学院近代物理研究所

中科院近物所给出的现场测试结论:

“USTC BPPM 系统达到设计要求, 相比 LSPH (Libera Single Pass-H) 电子学系统, 由科大研制的 BPPM 电子学系统测量精度优于国外 LSPH 系统, 达到国际先进水平。”

功率(-10dBm~-55dBm with step of -5dBm) 测量精度与稳定度。

- 利用标准信号源和肖特基二极管模拟 BPM 输

定度为 $\pm 5 \mu\text{m}$, 相位长期稳定度为 $\pm 1^\circ$, 二倍频下, 位置长期稳定度为 $\pm 2.5 \mu\text{m}$, 相位长期稳定度为 $\pm 1^\circ$ 。

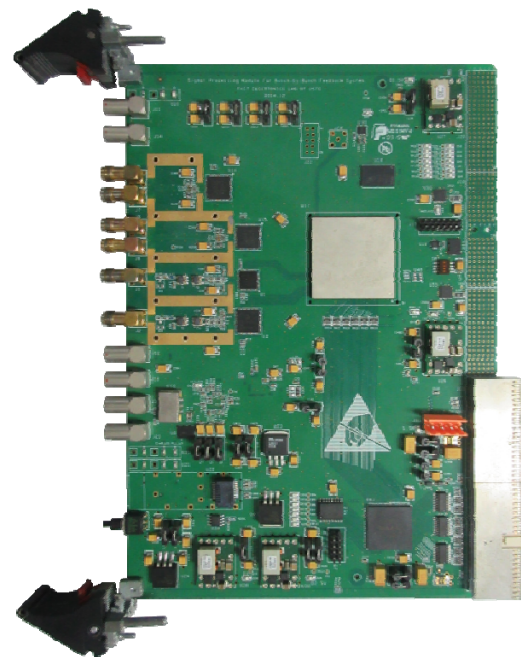
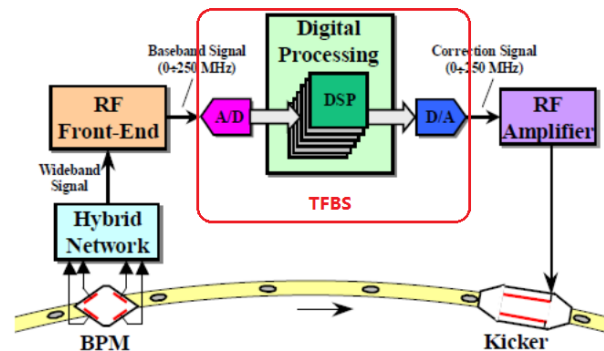
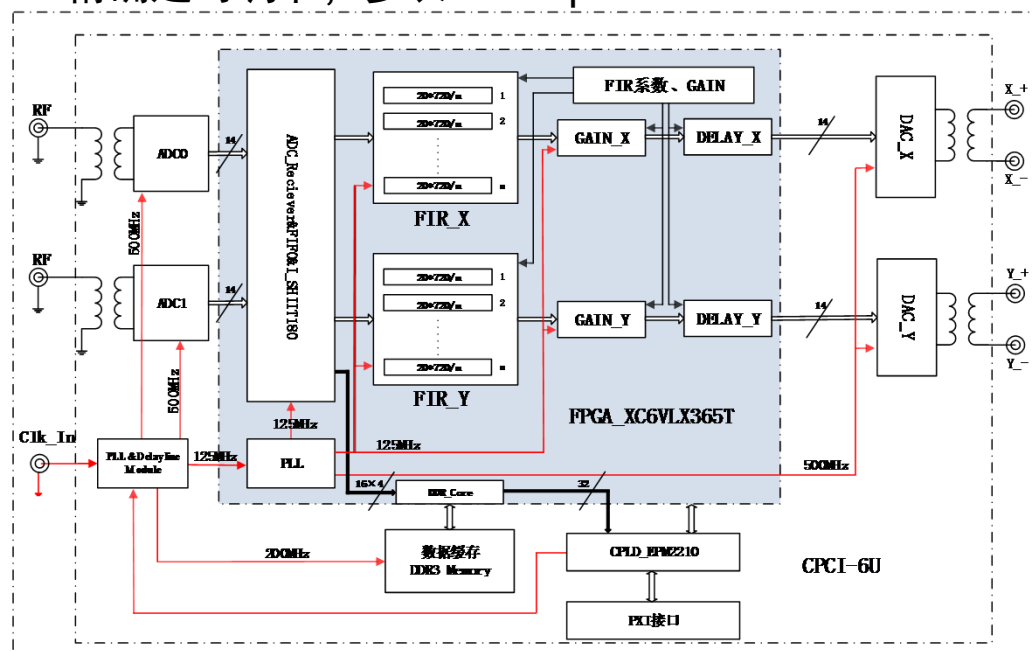
4. 实验室测试结果表明, USTC BPPM 系统达到设计要求。相比 LSPH 电子学系统, 由科大研制的 BPPM 电子学系统测量精度优于国外 LSPH 系

2014年1月带领测试小组赴中科院近代物理研究所进行数字化束流相位及位置测量系统的现场验收

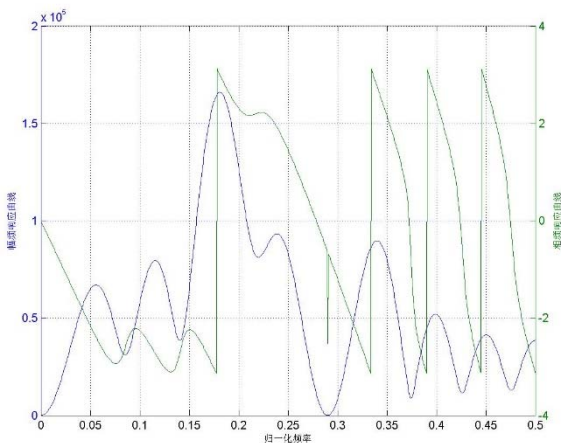
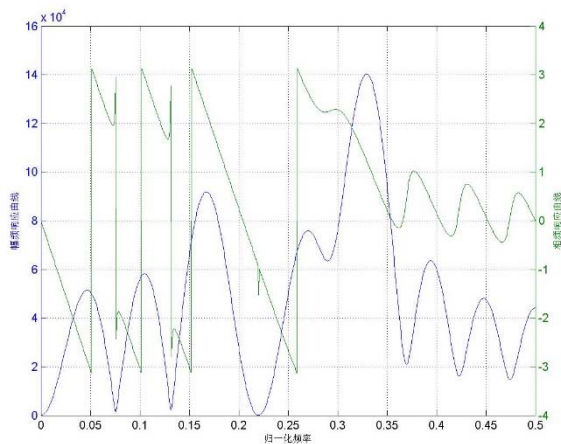
1.6 数字化束流测量研究

束流逐束团位置横向反馈系统

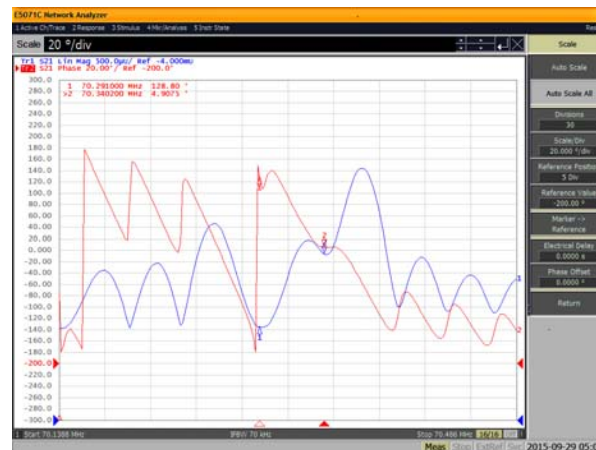
- 实时监控束流逐束团信号，实时采集、处理并输出反馈信号，从而保证束流运动在“黄金轨道”上。
- 500 Msps, 12 bit ADC
- 500 Msps, 14 bit DAC
- 基于FIR滤波器组的实时数字信号处理
- 精确延时调节，步长< 100 ps



束流逐束团位置横向反馈系统



Matlab仿真输出反馈幅频、相频特性



X方向



Y方向

实测输出反馈幅频、相频特性

1.6 数字化束流测量研究

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IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 61, NO. 1, FEBRUARY 2014

Beam Position and Phase Measurement System for the Proton Accelerator in ADS

Lei Zhao, Member, IEEE, Xingshun Gao, Xiaofang Hu, Shubin Liu, Member, IEEE, and Qi An, Member, IEEE

IEEE Transactions on Nuclear Science 61, 538-545 (2014)

Abstract—A prototype of a beam position measurement system is designed for the proton Accelerator Driven Sub-critical system. The Beam Position Monitor (BPM) design with a repetition frequency of 162.5 MHz would vary for more than 40 dB. By high-resolution analog-to-digital conversion, radio-frequency (RF) signals are directional streams by precisely adjusting the compared with the traditional method and quadrature-phase (IQ) data, it simplifies digital processing circuits. All signals are integrated within one field programmable logic device for a good system simplicity. Initial test results show this prototype achieves a phase resolution better than $5 \mu\text{m}$ range from -44 dBm to -4 dBm , well

Index Terms—ADS, analog-to-digital conversion, and phase measurement, IQ sampling.

I. INTRODUCTION

THE China ADS is now in the R&D solution for the reduction of radiation shown in Fig. 1, the proton beam from the LINAC is extracted to the target, transmute nuclear material and meanwhile produce a high-current proton accelerator is composed of parts in ADS. The accelerator includes an injector and a main LINAC section. The beam is injected by the injector to 10 MeV and then accelerated by the LINAC to 1.5 GeV [1].

In the R&D phase, two different designs for the injector are proposed, with Scheme I based on 162.5 MHz. These

IEEE NUCLEAR SCIENCE SYMPOSIUM & MEDICAL IMAGING CONFERENCE

21ST SYMPOSIUM ON ROOM-TEMPERATURE

SEMICONDUCTOR X-RAY AND GAMMA-RAY DETECTORS

Washington State Convention Center • Seattle, WA USA • 8-15 November 2014



Optimization of the Sampling Process for the Close Orbit Data in the Digital Beam Position Measurement for SSRF

Weihao Wu, Lei Zhao, Member, IEEE, Erlei Chen,



中华人民共和国国家知识产权局

国家发明专利、申请号：201410440504.5、申请公示中、名次1/5

100089

北京市海淀区西三环北路 87 号 11 层 4-1105 室
中科专利商标代理有限公司 任岩

2014 年 09 月 02 日



申请号或专利号：201410440504.5

发文序号：2014090200414330

申请人或专利权人：中国科学技术大学

发明创造名称：一种基于全数字化技术的束流位置和相位测量系统及方法

本年度科研项目

作为项目负责人承担科研项目

时 间	经费来源	课题名称	经费
2013.01 – 2015.12	国家自然科学基金青年基金	基于射频信号直接正交欠采样的新型数字化束流测量方法研究	24.00
2013.01 – 2016.12	国家自然科学基金重点基金之课题4	“CSR外靶上核物质状态方程的物理研究和实验准备” 之课题4 -- 读出电子学研究	80.00
2015.01 – 2017.12	校重要方向项目培育基金 (中央高校基本科研业务费专项资金)	基于SCA技术的高速波形数字化ASIC电路研究	80.00
2012.01 – 2014.12	校重要方向项目培育基金 (中央高校基本科研业务费专项资金)	ADS质子直线加速器实时数字化束流测量研究	100.00
2014.05 – 2015.04	核探测与核电子学国家重点实验室自主研究课题项目基金	基于放大成形技术的PMT大动态范围信号读出前端ASIC研究	15.00
2014.09 – 2016.08	中国科学院近代物理研究所	CSR外靶实验触发及时钟系统的研制	35.00
2015.06 – 2015.11	中国科学院深圳先进技术研究院	基于千兆以太网的PET实验数据传输原型模块	5.00
合 计 (万元)			339.00

本年度科研项目

作为科研骨干参与主要科研项目

时 间	经费来源	课题名称	名次	经费
2014.09 – 2015.12	中国科学院高能物理研究所	LHAASO WCDA读出电子学原型系统设计	2/15 项目 执行负责人	80.00
2014.07 – 2015.12	中国科学院上海应用物理研究所	上海光源束流横向反馈数据采集及处理设备研制	2/6	20.00
2011.01 – 2015.12	国家空间科学中心	暗物质粒子探测卫星--电磁量能器及其读出电子学研究	4/10	50.00
合 计（万元）				150.00

本年度论文列表 (1)

(1) 第一作者或通讯作者发表/录用的SCI期刊论文

1. **Lei Zhao**, Shaoping Chu, Cong Ma, Xingshun Gao, Yunfan Yang, Shubin Liu, Qi An, “Precise Clock Synchronization in the Readout Electronics of WCDA in LHAASO”, *IEEE Transactions on Nuclear Science*, accepted.
2. **Lei Zhao**, Weihao Wu, Jianfeng Liu, Yu Liang, Jiajun Qin, Li Yu, Shubin Liu, Qi An, “Prototype of a front-end readout ASIC designed for the Water Cherenkov Detector Array in LHAASO”, *Journal of Instrumentation*, Vol. 10, Mar. 2015, pp. P03015-1 –P03015-13.
3. **Lei Zhao**, Linsong Zhan, Xingshun Gao, Shubin Liu, Qi An, “Application of Real-time Digitization Techniques in Beam Measurement for Accelerators”, *Chinese Physics C*, accepted.
4. Weihao Wu, **Lei Zhao** ☆, Erlei Chen, Shubin Liu, Qi An, “Research into the sampling methods of digital beam position measurement”, *Nuclear Science and Techniques*, Vol. 26, No. 3, Jun. 2015, pp. 030402-1 – 030402-6.
5. Cong Ma, **Lei Zhao** ☆, Yuxiang Guo, Jianfeng Liu, Shubin Liu, Qi An, “Analog Front-end Prototype Electronics for the LHAASO WCDA”, *Chinese Physics C*, accepted.
6. Weihao Wu, **Lei Zhao** ☆, Yu Liang, Li Yu, Jianfeng Liu, Shubin Liu, Qi An, “Evaluation of a front-end ASIC for the readout of PMTs over a large dynamic range”, *Chinese Physics C*, accepted.
7. Erlei Chen, **Lei Zhao** ☆, Li Yu, Jiajun Qin, Yu Liang, Shubin Liu, Qi An, “Test system of the front-end readout ASIC for the WCDA in LHAASO”, *Nuclear Science and Techniques*, accepted.

(2) 第一作者或通讯作者发表/录用的国际会议论文

1. Jianfeng Liu, **Lei Zhao** ☆, Li Yu, Yu Liang, Jiajun Qin, Cong Ma, Weihao Wu, Shubin Liu, Qi An, “Evaluation of a front-end ASIC prototype for the readout of PMTs in water cherenkov detector array”, *2015 IEEE 12th International Conference on Electronic Measurement & Instruments*, Jul. 16-19, 2015, Qingdao, China.
2. Linsong Zhan, **Lei Zhao** ☆, Longfei Kang, Jinxin Liu, Min Li, Shubin Liu, Qi An, “The Clock System in Readout Electronics System for the External Target Experiment in CSR of HIRFL”, *2015 International Conference on Advanced Electronics and Communications Engineering (AECE2015)*, Feb. 8-9, 2015, Shanghai, China. ISTEP收录
3. Weihao Wu, **Lei Zhao** ☆, Erlei Chen, Shubin Liu, Qi An, “Optimization of the Sampling Process for the Close Orbit Data in the Digital Beam Position Measurement for SSRF”, presented in *2014 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC)*, Nov. 2014, Seattle, USA.

本年度论文列表（2）

（3）第一作者或通讯作者发表/录用的其他期刊论文

1. 康龙飞, 赵雷 ☆, 李敏, 周家稳, 刘树彬, 安琪, “HIRFL CSR外靶实验读出电子学预研系统”, 原子能科学技术, 第49卷, 第1期, 2015年1月, pp.154-161.
2. 高兴顺, 赵雷 ☆, 康龙飞, 刘树彬, 安琪, “兰州反应显微成像谱仪实验中多路定标器的设计”, 原子核物理评论, 第32卷, 第1期, 2015年3月, pp. 73-79.

正在审稿及撰写中的论文

1. Jianfeng Liu, Lei Zhao ☆, Li Yu, Yu Liang, Jiajun Qin, Yunfan Yang, Weihao Wu, Shubin Liu, Qi An, “An Analogue Front-End ASIC Prototype Designed For PMT Signal Readout”, under second review in *Chinese Physics C*.
2. Xingshun Gao, Lei Zhao ☆, Jinxin Liu, Xiaofang Hu, Shubin Liu, Qi An, “Real-Time Phase Correction based on FPGA in the BPPM System for the LINAC in ADS”, planned to submitted to *IEEE Transactions on Nuclear Science*.
3. Min Li, Lei Zhao ☆, Jinxin Liu, Yiming Lu Shubin Liu, Qi An, “The Trigger System for the External Target Experiment in CSR of HIRFL”, planned to submitted to *Chinese Physics C*.
4. 夏品正, 赵雷 ☆, 邓佩佩, 董若石, 刘树彬, 安琪, “HIRFL CSR外靶实验T0探测器前端电子学原型模块设计”, 投稿到原子核物理评论。

本年度专利

专 利

- “高精度时钟分发和相位自动补偿系统及其相位调节方法”、申请号：201510390265.1、发明专利、申请公示中、名次1/5
- “一种基于全数字化技术的束流位置和相位测量系统及方法”、申请号：201410440504.5、发明专利、申请公示中、名次1/5

本年度获奖

获 奖

- 2015年1月 获奖“安徽省高等学校省级教坛新秀”。
- 2014年10月 获“近代物理所教师奖”。

学术服务

➤以下SCI期刊审稿人：

- ▶ *IEEE Transactions on Nuclear Science*
- ▶ *IEEE Transactions on Instrumentation and Measurement*
- ▶ *Review of Scientific Instruments*
- ▶ *Journal of Instrumentation*
- ▶ *Digital Signal Processing*
- ▶ *Chinese Physics C*
- ▶ *Nuclear Science and Techniques*

➤以及其他核心期刊审稿人：

- ▶ 核技术（中文版）
- ▶ 原子核物理评

➤核电子学ASIC Workshop组委会成员。由中科院高能所、清华、科大联合发起

谢 谢