第十二届全国粒子物理学术会议
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SOI pixel detector for the charged particles

（分会场5：关键实验技术和装置、探测器及电子学）

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2016/8/24

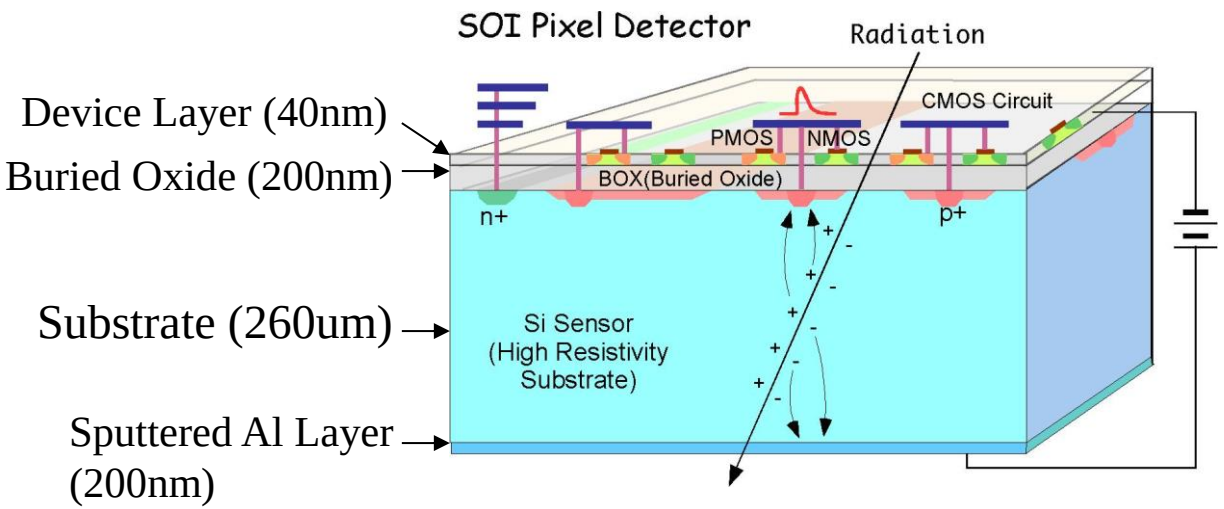
Outline

- Introduction
  - Concept, process parameter, people, IHEP activities
- Characterization of SOI technology
  - Single point resolution
  - Radiation hardness
- Chip developments for future e^+e^- collider
  - SOFIST for ILC
  - CPV for CEPC
- Summary and outlook

Introduction

- Acronym of Silicon On Insulator
  - Front-end in the top device layer;
  - Sensing diodes in the bottom bulk layer;
  - Contacts through the dioxide make connections;
- Challenges
  - Mutual interference between front-end and sensing diodes
  - TID vulnerable due to Buried-Oxide.

Sandwiched structure



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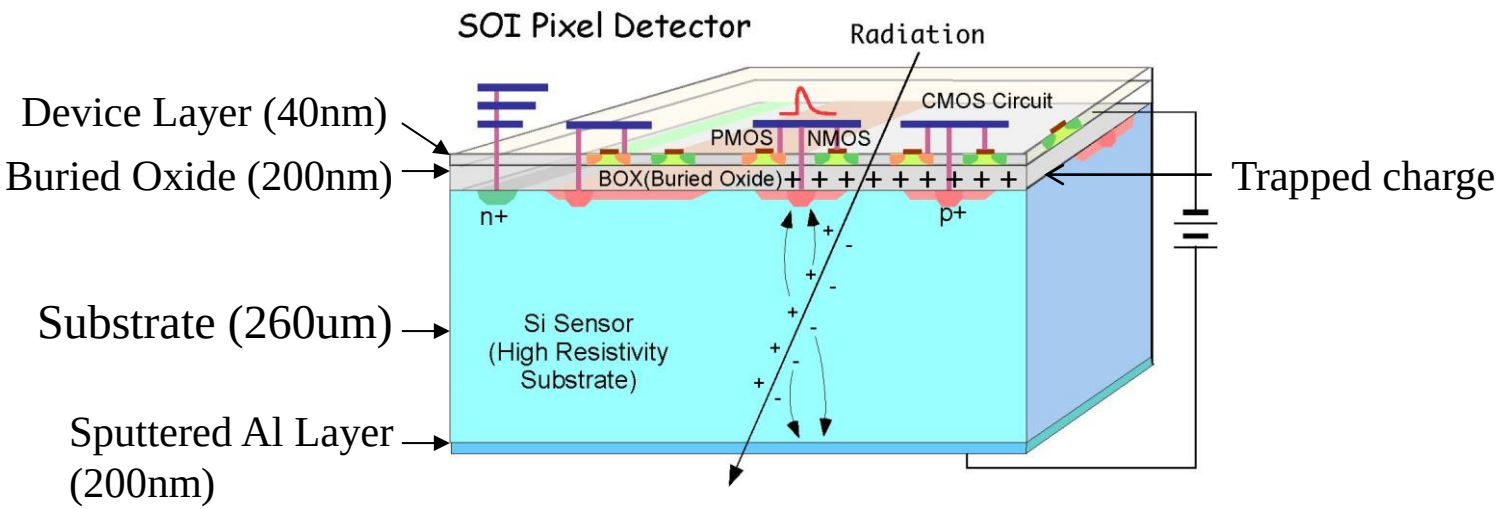
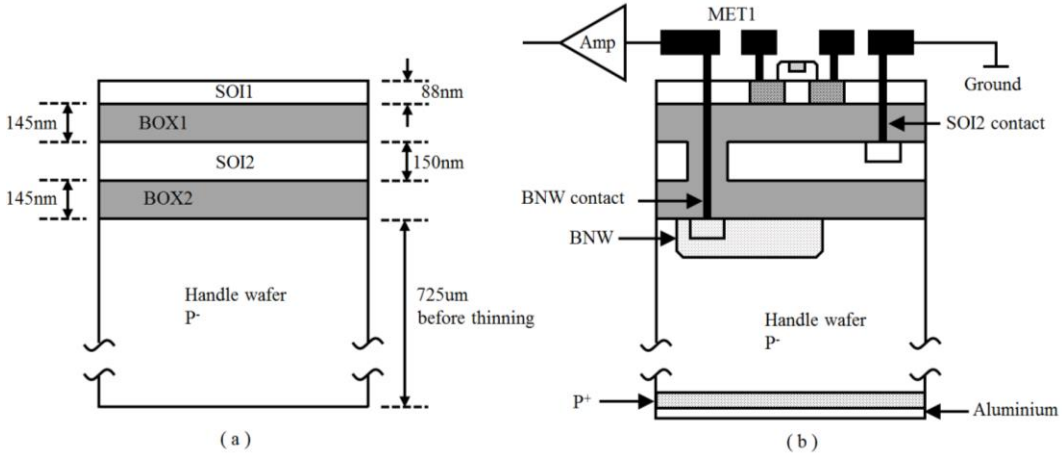


Double-SOI process

- Double-SOI wafer
  - Second SOI layer as shielding between Front-end and sensing diodes
  - Compensation voltage can be applied to mitigate TID effect



Double-SOI wafer before and after process

- Lapis FD-SOI pixel process
  - 0.2um CMOS, 1 Poly, 5 Metal layers
  - 8-inch wafer, 720 um thick
  - High resistive substrate: Cz (n) ~700 Ω-cm, FZ(n) > 2k Ω-cm, FZ(p) ~25k Ω-cm etc.
  - Backside process: Mechanical Grind, Chemical Etching, Back side Implant, Laser Annealing and Al plating

SOIPIX collaboration

http://rd.kek.jp/project/soi/

- KEK group
  - Coordinator, process improvement, general development
- Riken group
  - XFEL application
- Kyoto U. group
  - Space X-ray observation
- LBNL group
  - Tracking of high momentum charged particles
- Fermi Lab group
  - Study of mutual interference
  - 3D integration
- IHEP group
  - Synchrotron radiation X-ray imaging
  - Pixel sensor for CEPC vertex
- More than 10 other groups not listed here
  - …

IHEP activities

- Chips developed
  - INTPIX2P5 (2012) → Chinese Physics C, Vol. 40, (2016), 016202
  - CPIXteg3/3b (2013-2014) → NIMA, 831 (2016), 44; arXiv:1507.05394
  - CPV1/2 (2015-2016) → Evaluation is underway

- China-Japan mini-workshop on SOIPIX
  - 2013, IHEP, KEK, IME, SARI, Xi'an Jiaotong U. http://indico.ihep.ac.cn/event/3011/
  - 2016, IHEP, KEK, IME, Osaka U., Kanazawa U., CNU http://indico.ihep.ac.cn/event/6189/

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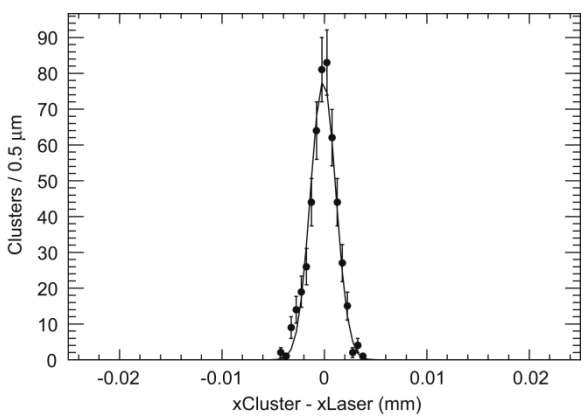
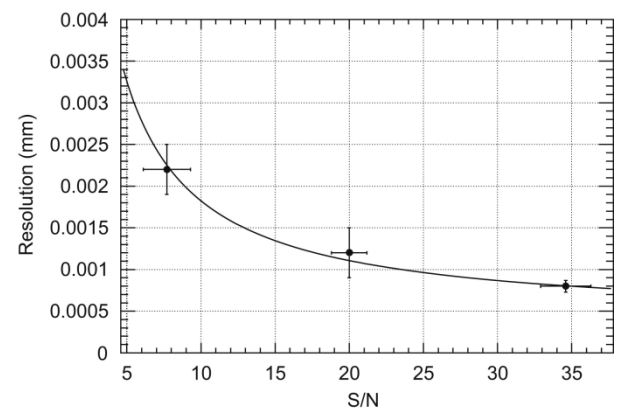
Single point resolution (1060nm laser test)

Reference: Marco Battaglia et al., NIMA 604 (2009) 380-384

- LDRD-SOI-1
  - 160×150 pixels on a 10 um pitch
  - Analog section implement a simple 3-transistor architecture
  - Reverse bias voltage limited below 15 V by back gate effect
  - 5um Gaussian spot of focused laser beam
  - SP resolution = 1.2um @ S/N = 20



Reverse biased 7V, S/N =20
SP resolution = 1.2um



Reverse biased 7V,
SP resolution as a function of S/N

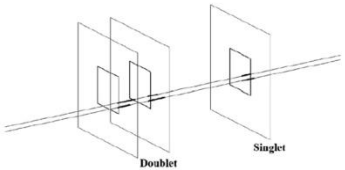
Single point resolution (300 GeV π^- beam test)

Reference: Marco Battaglia et al., NIMA 676 (2012) 50-53

- SOImager-2
  - 256×256 pixels on a 13.75 um pitch
  - 3-T analog readout
  - Reverse bias up to 130V enabled by BPW implant
  - Tracks reconstructed using 3 DUT layers
  - Thin/Thick sensors consistent with simulation

Measured average S/N ratio, detection efficiency and single point resolution σ_{point} for thin and thick SOI sensors.

SOI sensor	V_d (V)	d (μm)	Cluster ⟨S/N⟩	Efficiency	σ_{point} (μm)
Thin	30	60 ± 5	25.0	0.90 ± 0.04	3.1 ± 0.80
64um	50	64 ± 3	28.2	0.94 ± 0.03	1.7 ± 0.50
	70	64 ± 3	28.8	0.96 ± 0.03	1.8 ± 0.60
	90	64 ± 3	31.2	0.98 ± 0.02	1.9 ± 0.70
Thick	30	60 ± 8	23.3	0.89 ± 0.03	1.36 ± 0.04
250um	50	103 ± 5	47.4	$0.98^{+0.02}_{-0.04}$	1.12 ± 0.03
	70	122 ± 5	52.7	$0.99^{+0.01}_{-0.05}$	1.07 ± 0.05



1.63um

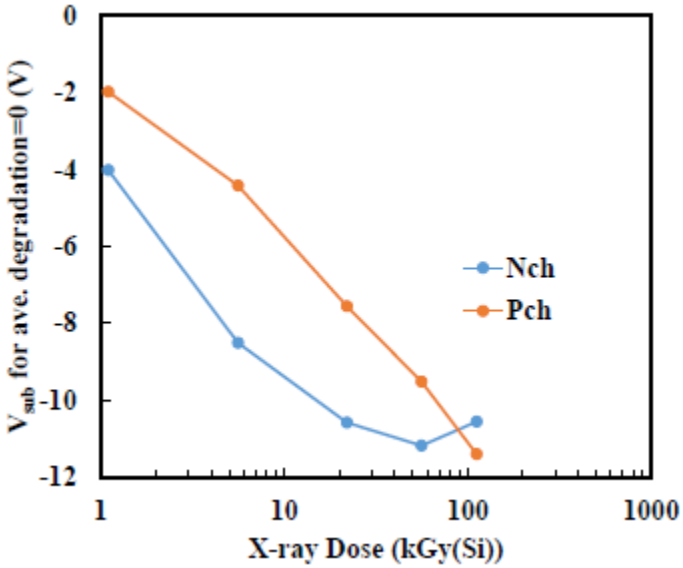
Simulation prediction

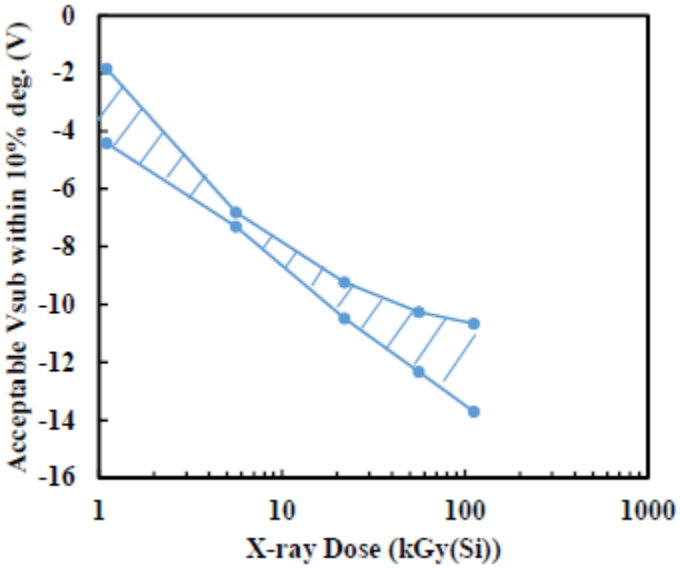
1.07um

Radiation hardness (device level)

Reference: Ikuo Kurachi, et al., http://indico.ihep.ac.cn/event/6189/

- Radiation damage mechanisms
  - SEU / TID / Non-ionized damage
- Measures to enhance TID tolerance
  - Optimization of transistors doping recipe (LDD)
  - Double SOI compensation
- Up to 100 kGy achieved by combining above two measures.
  - Drain current change less than 10%.

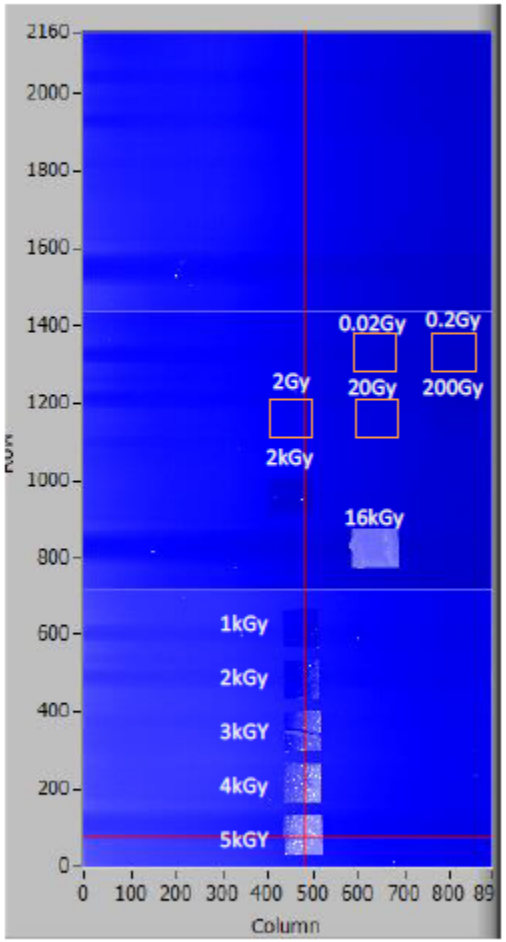


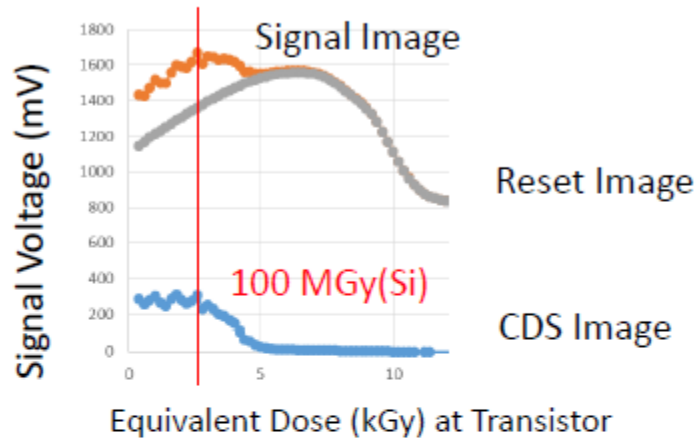


Reference: T. Hatsui, FEE2016, June, 2016

X-ray Radiation Hardness: Sensor Level

BL29XU Beamline @ SPring-8





Target Performance: 1 Grad(Si) @ 7 keV input dose

Results: Operational up to 10 Grad(Si)
(equivalent to 250 krad(Si) @Transistor layer)

At 1 Grad(Si) (end of life), dynamic range is reduced by 2.5 % (20 mV)

Consistent with results obtained by a wafer-level high-throughput evaluation on the transistors[1-3].

1) T. Kudo et.al., IEEE TNS (2014) Vol. 61(3), p. 1444.
2) I. Kurachi, et.al., IEEE Trans. Electr. Dev. (2015), Vol. 62(8), p. 2371
3) I. Kurachi, et.al., IEEE Trans. Electr. Dev. (2016), Vol. 63(6), p. 2293.

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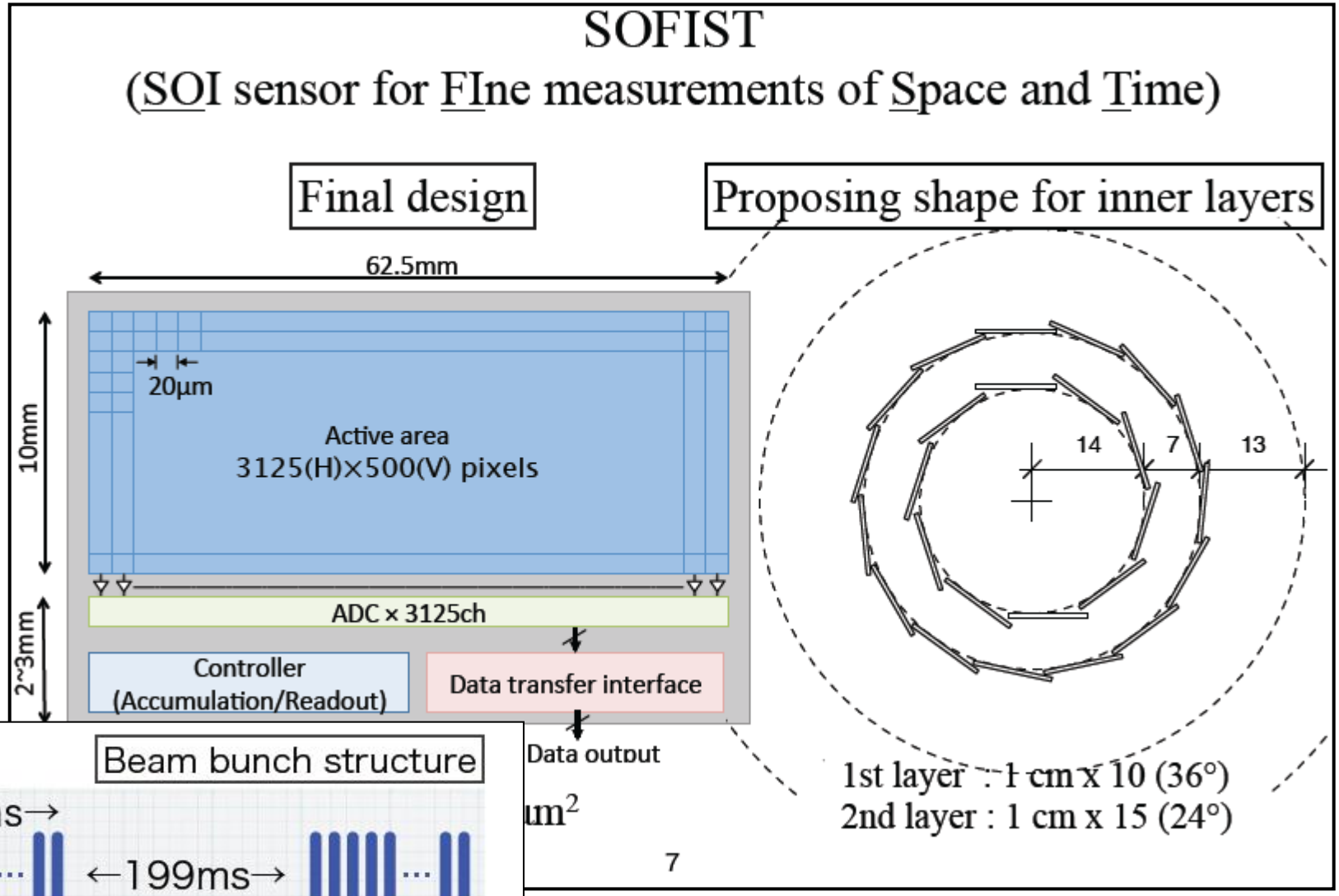
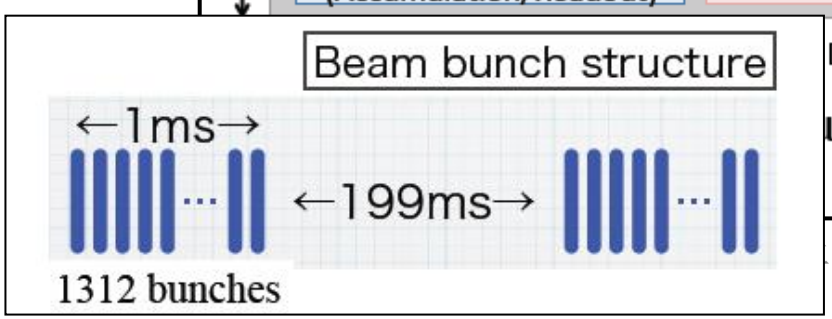
SOFIST for ILC

Reference: Manabu Togawa, http://indico.ihep.ac.cn/event/6189/



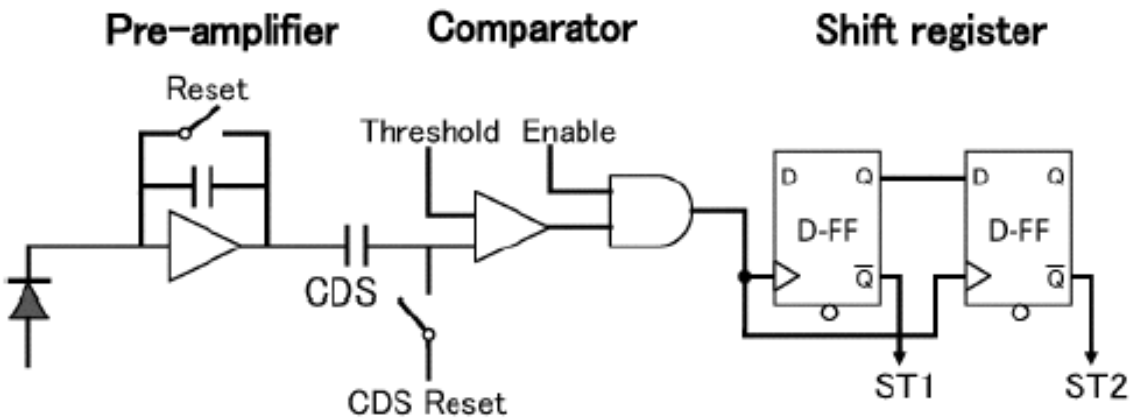


Reference: Miho Yamada, http://indico.ihep.ac.cn/event/6189/

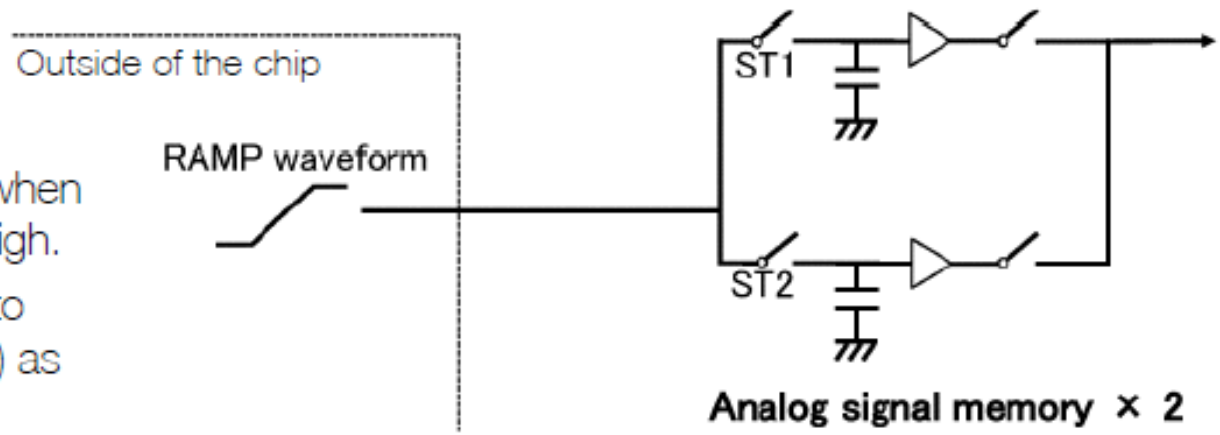
Time Stamp Pixel

designed by S. Ono (KEK)

- Pre-amplifier
  Charge Sensitive Amp.
- Comparator
  Chopper Inverter type
- Shift register
  D-FF



1) Input a RAMP waveform.
2) Open a store switch (ST1) when a comparator changes to High.
3) Keep the voltage of RAMP to the analog memory (DMOS) as a time stamp.
4) in the same way for 2nd hit.



Analog signal memory × 2

CMOS SW + DMOS (25 fF)

Reference: Miho Yamada, http://indico.ihep.ac.cn/event/6189/

Analog Pixel

designed by S. Ono (KEK)

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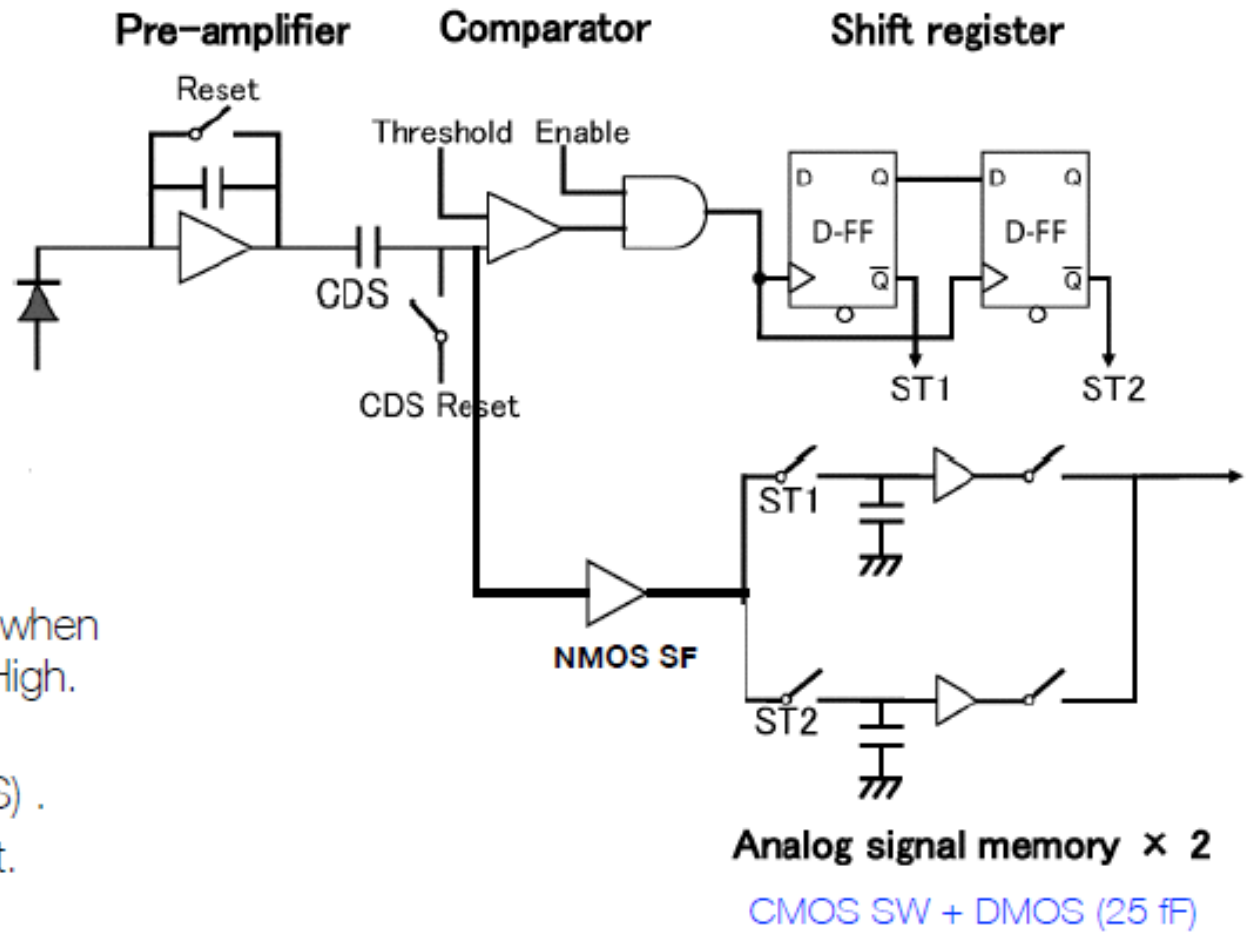


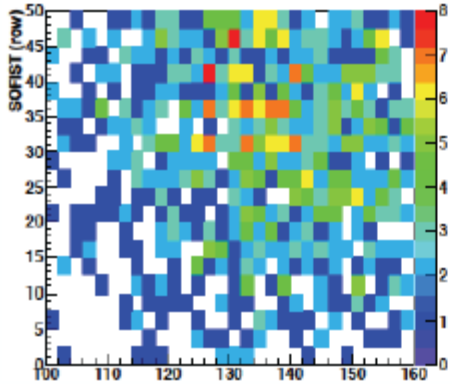
1) Input a analog signal.
2) Open a store switch (ST1) when a comparator changes to High.
3) Keep the analog signal to the analog memory (DMOS) .
4) in the same way for 2nd hit.

→ Implement all the functions of Time stamp pixel / Analog pixel in 25 × 25 μm^2 pixel.

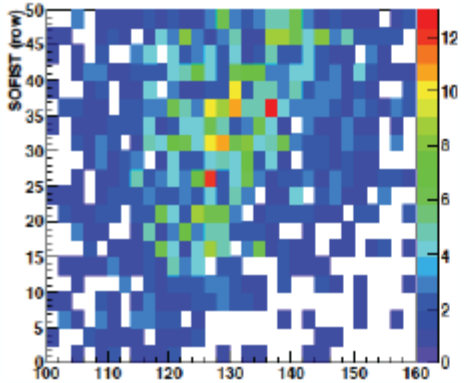
Reference: Shun Ono, http://indico.ihep.ac.cn/event/6189/

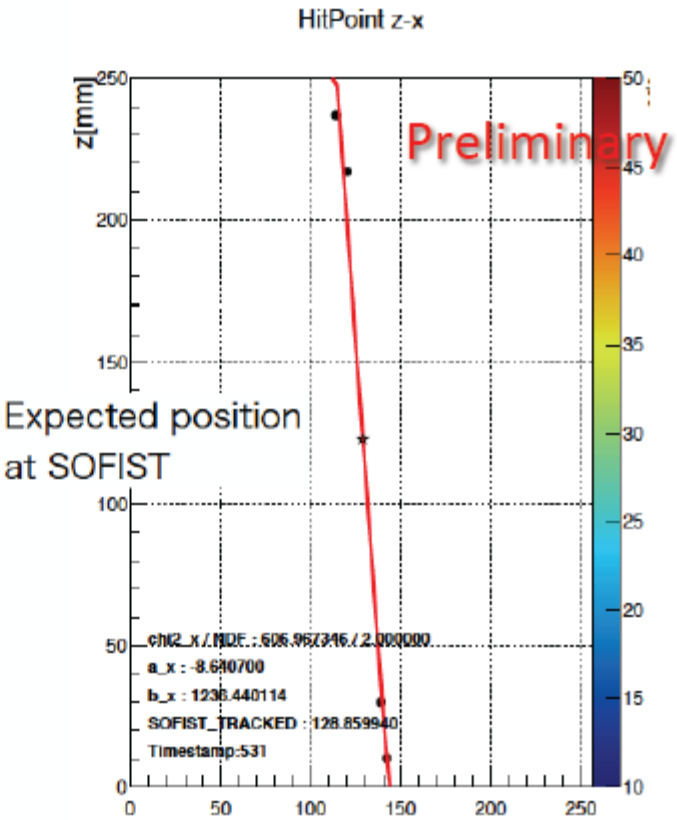
SOFIST Ver.1: Beam test (Tracking)

w/o timestamp matching



w/ timestamp matching

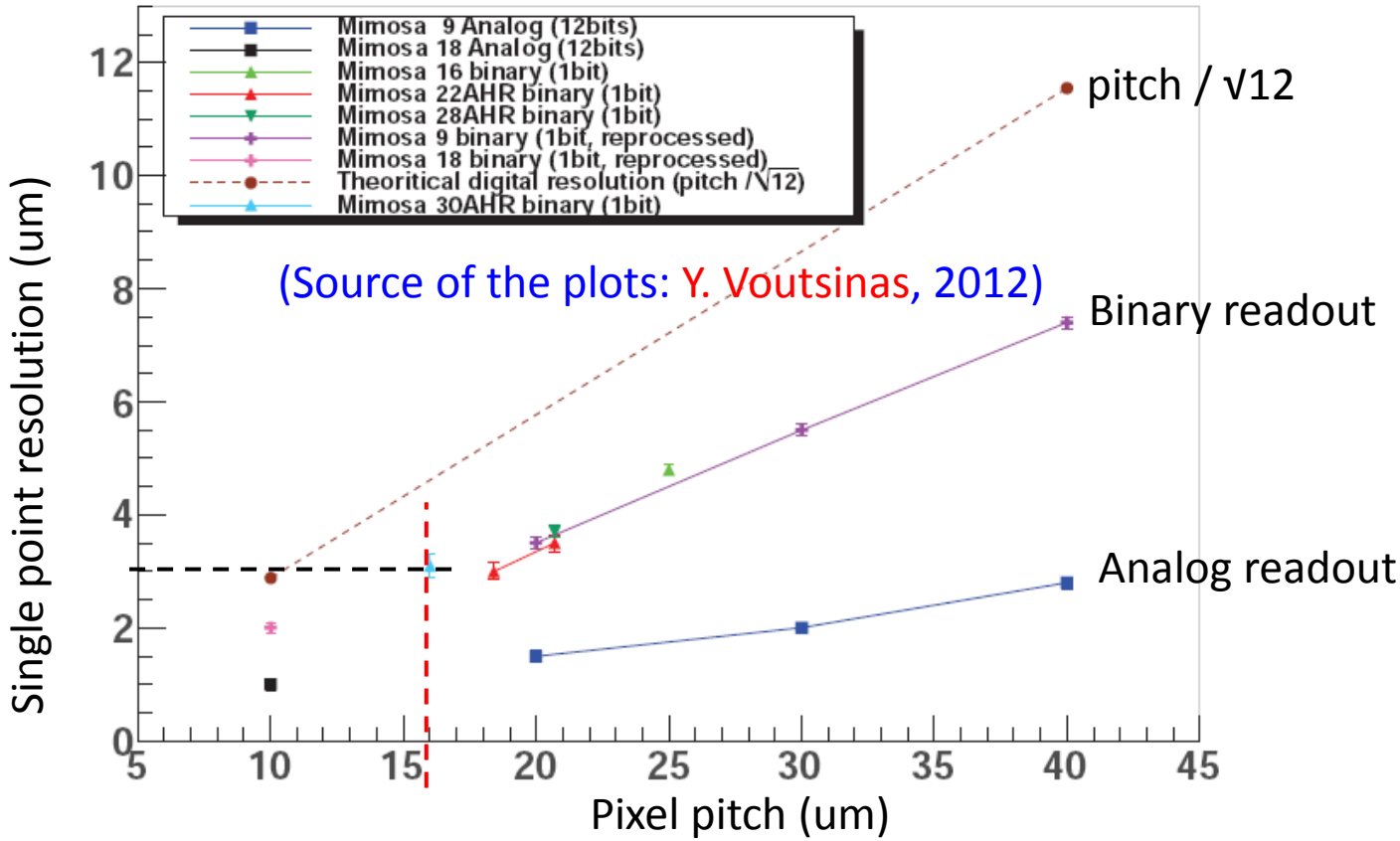




Analyzed by D.Yamamoto, Y.Sawada (Osaka Univ.)

CPV for CEPC

- Compact Pixel for Vertex
  - Digital pixel (in-pixel discrimination) for low power consumption
  - Small pixel size, 16um pitch



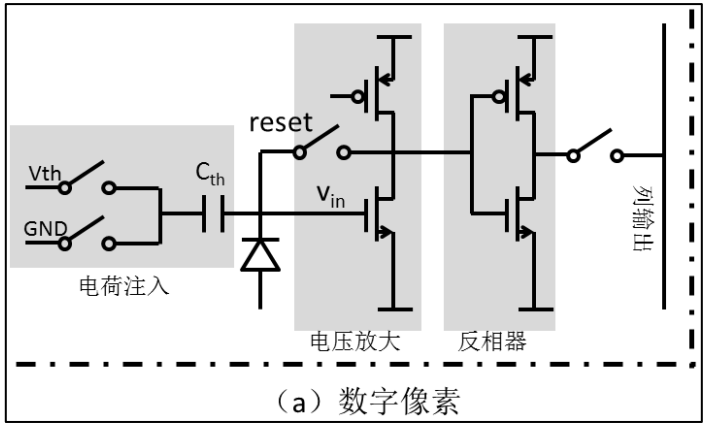
(Source of the plots: Y. Voutsinas, 2012)

A comparison of digital pixels

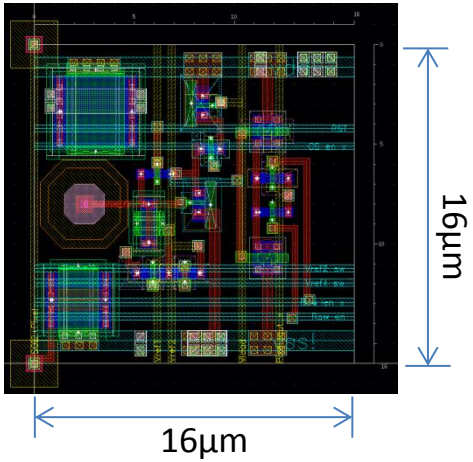
	ASTRAL	ALPIDE	CPV
Process technology	*0.18 μm* CMOS		0.2 *μm* SOI
Readout strategy	Rolling shutter	asynchronous	Rolling shutter
Readout time	20 μs	<2 μs	
Power	85 mW/cm^2	39 mW/cm^2	
Pixel size	$22 \times 33\ \mu m^2$	$28 \times 28\ \mu m^2$	$16 \times 16\ \mu m^2$
Spatial resolution	$\approx 5\mu m$		Expected < $3\mu m$
Total signal for MIP	$\approx 1600\ e^-$ ($\approx 20\mu m$ epi-layer)		$\approx 4000\ e^-$ (back thinning to $50\mu m$, fully depleted)

- SOI offers opportunity to explore very compact pixel circuit
  - 2~3 times larger MIP signal

- CPV1
  - CS voltage amplifier + inverter
  - Threshold charge injected to sensing node
  - 16*16 μm pixel size
  - Pixel array: 64*32 (digital) + 64*32 (analog)
  - Double-SOI process for shielding and radiation Enhancement
  - Submitted June, 2015
- CPV2
  - In-pixel CDS stage inserted
  - To improve RTC and FPN noise
  - To replace the charge injection threshold
  - Submitted June, 2016

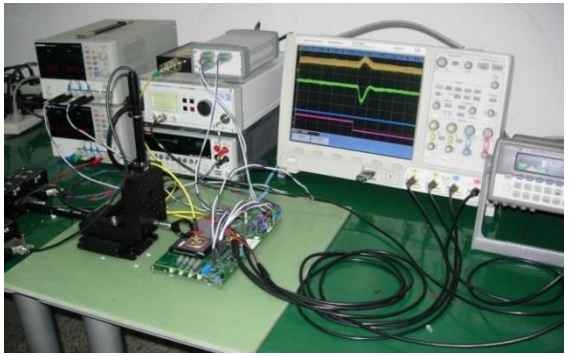


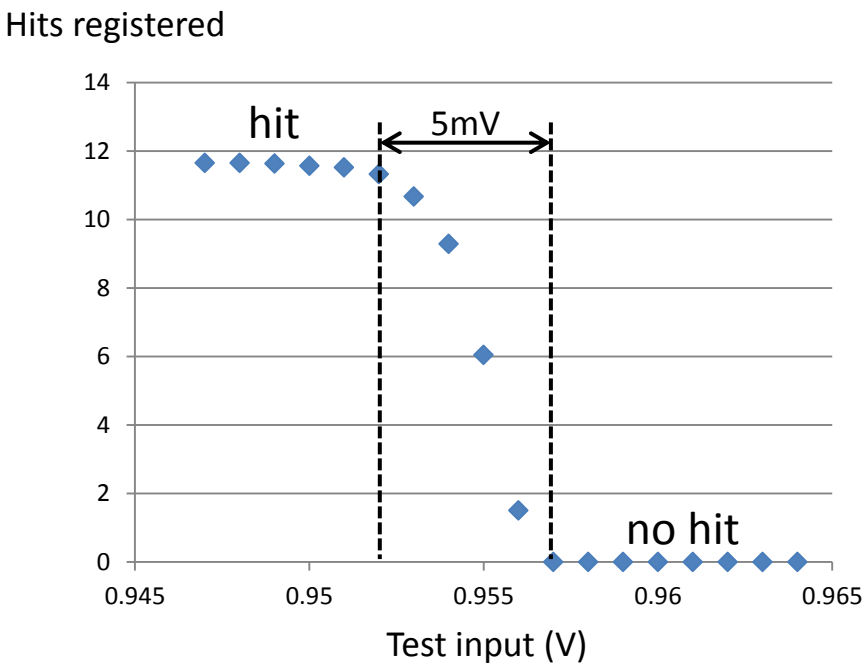
CPV1 digital pixel

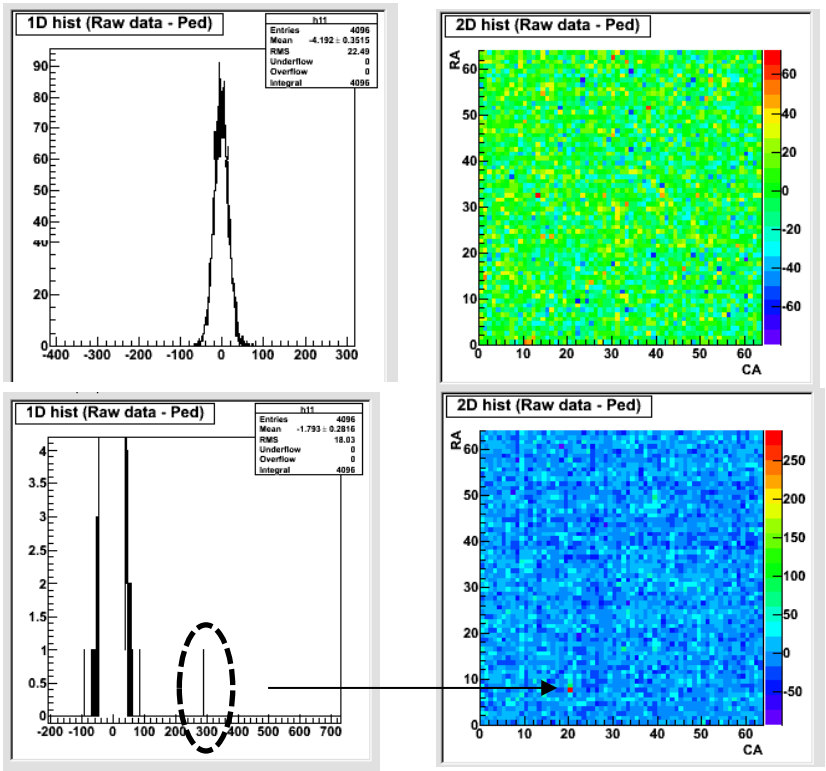


CPV1 lab test

- Chip circuit function verified on single pixel
  - Voltage gain of amplifier ~ 10
  - Threshold scan
  - Temporal noise ~ 17e$^-$
- Radiative source response observed
  - ^{55}Fe signal ~ 1600e$^-$







Summary and outlook

- Newly-developed Double-SOI process is able to
  - Shield the mutual interference between front-end and sensing diodes
  - Improve TID tolerance up to 100kGy
- Different strategies to pursue a monolithic sensor for future e^+e^- collider
  - Time-stamped analog sensor for ILC
  - Compact digital sensor for CEPC

- Sensor specifications for CEPC vertex can not be fixed until the accelerator design settles down.
- Sensor R&D will follow the general requirement:
  - Spatial resolution ~ 3um
  - Time stamp 1~100 us
  - Power consumption ~ 50mW/cm^2
  - Radiation tolerance: 0.1 ~ 1 Mrad/year, 10^{11} ~ 10^{12} MeV n_{eq}/cm^2/year

Acknowledgements

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- And the CAS Center for Excellence in Particle Physics (CCEPP)