山东大学
SHANDONG UNIVERSITY

粒子物理与粒子辐照
教育部重点实验室

Investigation of CMOS pixel sensor with 0.18 um CMOS technology for CEPC tracking detector

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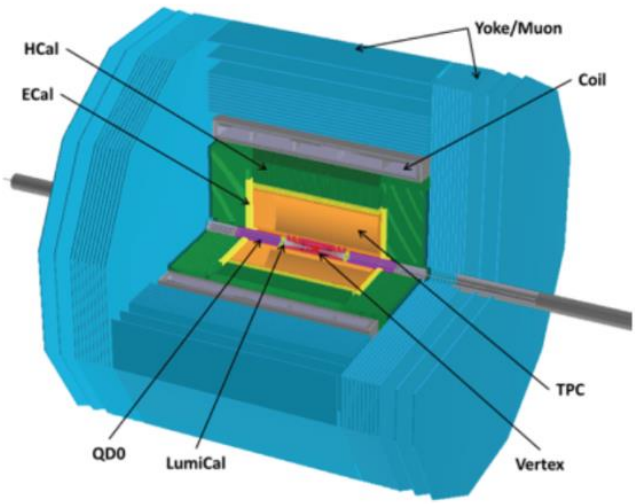
Outline

- **Introduction**
  - ★ CEPC detector
  - ★ Silicon tracker requirements
- **CMOS pixel sensor for silicon tracker**
  - ★ CPS technology
- **Charge collection simulation**
  - ★ Pixel size
  - ★ Diode geometry
- **Prototype chip design**
- **Summary & outlook**

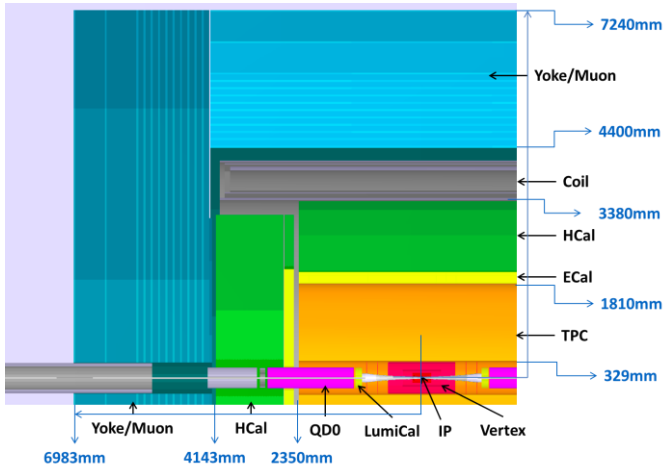
Introduction

- **The Circular Electron Positron Collider (CEPC) proposed by the Chinese high energy physics community is aiming to measure Higgs particles and their interactions precisely.**
  - vertex
  - silicon tracker
    - SIT (Silicon Inner Tracker)
    - SET (Silicon External Tracker)
    - FTD (Forward Tracking Disk)
    - ETD (End-cap Tracking Disk)
  - TPC (Time Projection Chamber)
  - calorimetry: ECAL, HCAL
  - superconducting solenoid
  - muon detector

- **Requirements of silicon tracker**
  - Silicon envelope concept as for the ILD detector
  - Complementary to the TPC
  - Precise momentum measurement
  - Low material budget



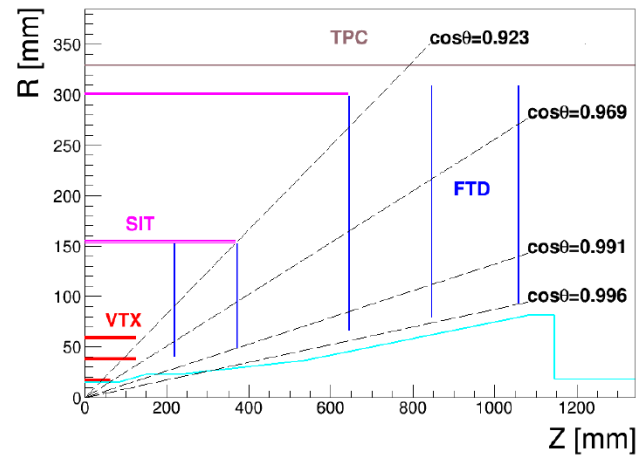
CEPC detector concept



Overview of the CEPC detector

Introduction

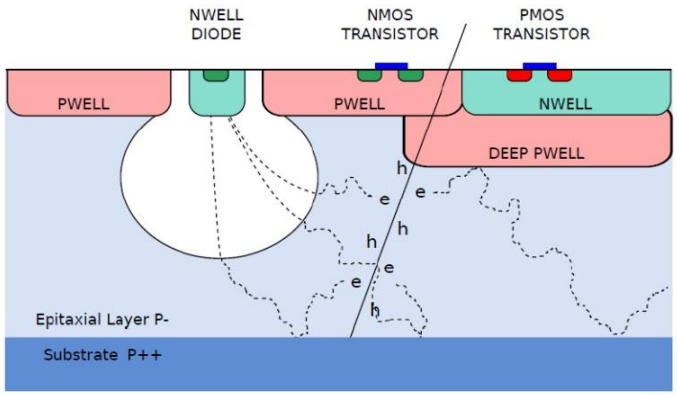
- **Basic sensor for the silicon tracker**
  - Silicon microstrip sensors
    - P^+-on-n technology
    - Area of 10 × 10 cm^2
    - Pitch of 50 μm, σ_{sp} < 7 μm
    - Thickness < 200 μm
  - Pixel detectors as VTX for the two innermost FTD
- **Alternative option**
  - Pixelated silicon sensors based on CMOS technology



Preliminary layout of the silicon tracker

Detector		Geometric dimensions			Material budget $[X/X_0]$
SIT	Layer 1:	$r = 153$ mm,		$z = 371.3$ mm	0.65%
	Layer 2:	$r = 300$ mm,		$z = 664.9$ mm	0.65%
SET	Layer 3:	$r = 1811$ mm,		$z = 2350$ mm	0.65%
FTD	Disk 1:	$r_{in} = 39$ mm,	$r_{out} = 151.9$ mm,	$z = 220$ mm	0.50%
	Disk 2:	$r_{in} = 49.6$ mm,	$r_{out} = 151.9$ mm,	$z = 371.3$ mm	0.50%
	Disk 3:	$r_{in} = 70.1$ mm,	$r_{out} = 298.9$ mm,	$z = 644.9$ mm	0.65%
	Disk 4:	$r_{in} = 79.3$ mm,	$r_{out} = 309$ mm,	$z = 846$ mm	0.65%
	Disk 5:	$r_{in} = 92.7$ mm,	$r_{out} = 309$ mm,	$z = 1057.5$ mm	0.65%
ETD	Disk:	$r_{in} = 419.3$ mm,	$r_{out} = 1822.7$ mm,	$z = 2420$ mm	0.65%

CMOS pixel sensor for silicon tracker

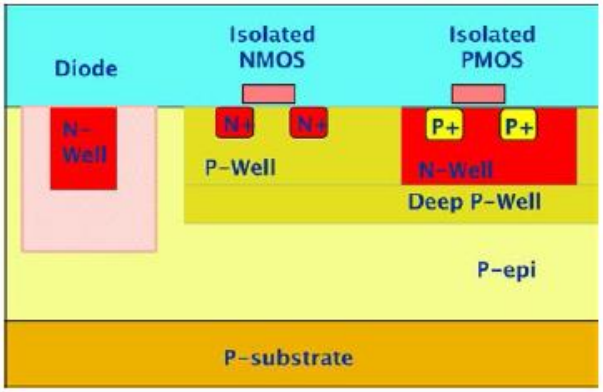


- **Prominent features of CPS**
  - High granularity
    - High spatial resolution (< 3 µm)
  - Very thin
    - Thickness can be thinned down to 50 µm
  - Signal processing in the same chip
    - Relax downstream electronics and syst. (→ cost, material budget)
  - Standard CMOS fabrication technology
    - Low power, cheap, fast multi-project run turn-around
    - Room temperature operation
- **Technology already under production & development for detectors**
  - STAR-PXL, ALICE-ITS, ILD-VXD
- **CPS has a very high potential**
  - R&D try to exploit the potential of CPS at best with industrial technology
    - Manufacturing parameters not optimised for future particle detection

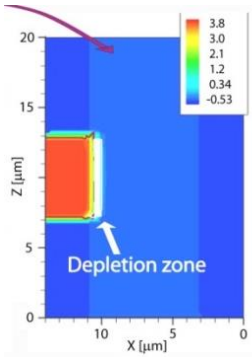
    → 0.18 µm process: high-res epi-layer, speed, smaller feature size, …

CMOS pixel sensor for silicon tracker

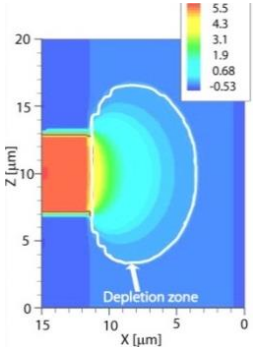
- **Moving to a 0.18 µm CMOS process (TowerJazz) for R&D**
  - Deep P-well (quadruple well technology)
    - Full CMOS circuit implementation in-pixel such as discriminator & ADC
  - 6 metal layers (instead of 4)
    - High integration, reduce dead zone
  - High-res epitaxial layer 1 – 5 kΩ·cm
    - Improve charge collection efficiency
  - Thin gate oxide
    - Improve radiation tolerance
  - Stitching
    - multi-chip slabs



Standard epitaxial layer

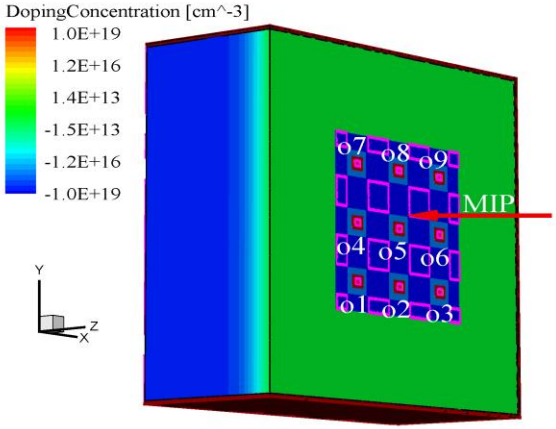


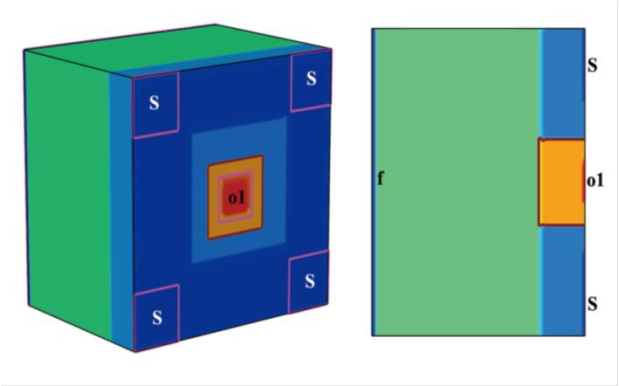
High resistive layer



Charge collection simulation

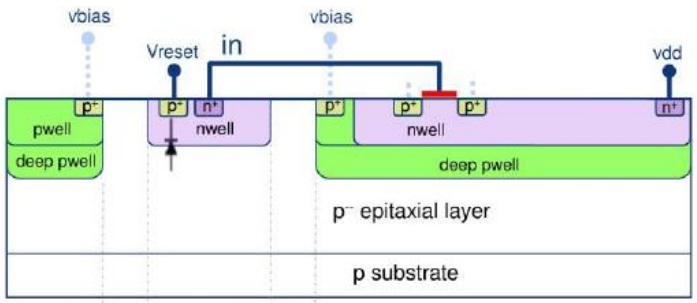
- **Motivation**
  - Study charge collection efficiency (CCE) with different pixel size and diode geometry
- **Simulation with TCAD tool**
  - Pixel size
  - Diode geometry
  - Thickness of the epitaxial layer: 18 μm
  - Resistivity of the epitaxial layer: 1 kΩ·cm
  - Power supply: 1.8 V
  - Simulation structure: 5×5 cluster
  - Particle hits right at the center of the pixel
- **Pixel size selection**
  - 21 × 21 μm^2, 21 × 42 μm^2, 21 × 84 μm^2
    - Compare with the pixel in MIMOSA34
    - Observe the CCE variation

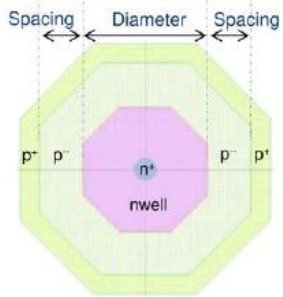


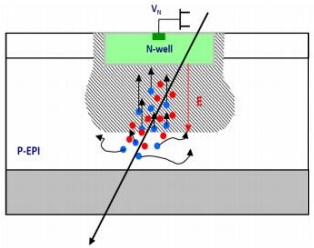


Charge collection simulation

- **Sensing diode geometry**
  - Nwell is octagon and should be small
    - Improve SNR → $U_{signal} = Q_{collection}/C$
    - BUT not too small since $Q_{collection}$ ~ CCE
  - Surrounding Pwell (P+) is opening
    - Improve charge collection efficiency

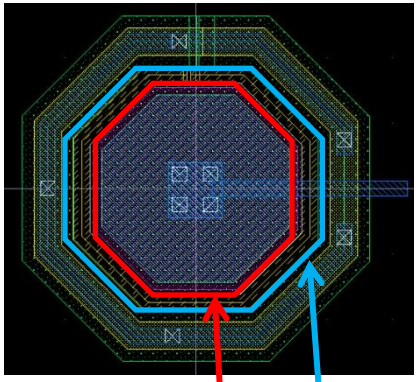






Pixel	P1	P2	P3	P4	P5	P6	P7	P8	P9
Pitch(x)(µm)	21	42	84	21	42	84	21	42	84
N(D)	1	1	1	1	1	1	1	1	1
F(D)(um²)	11	11	11	5	18	18	15	44	50
S(D)(um²)	8	8	8	4	12	12	6	20	20

- **N(D) = number of diodes in each pixel (1)**
- **F(D) = footprint of diode (diode area + pwell opening): 5, 11, 15, 18, 44 & 50 µm²**
- **S(D) = surface of diode: 4, 6, 8, 12 & 20 µm²**

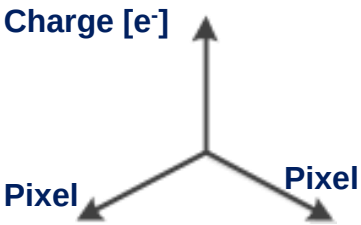


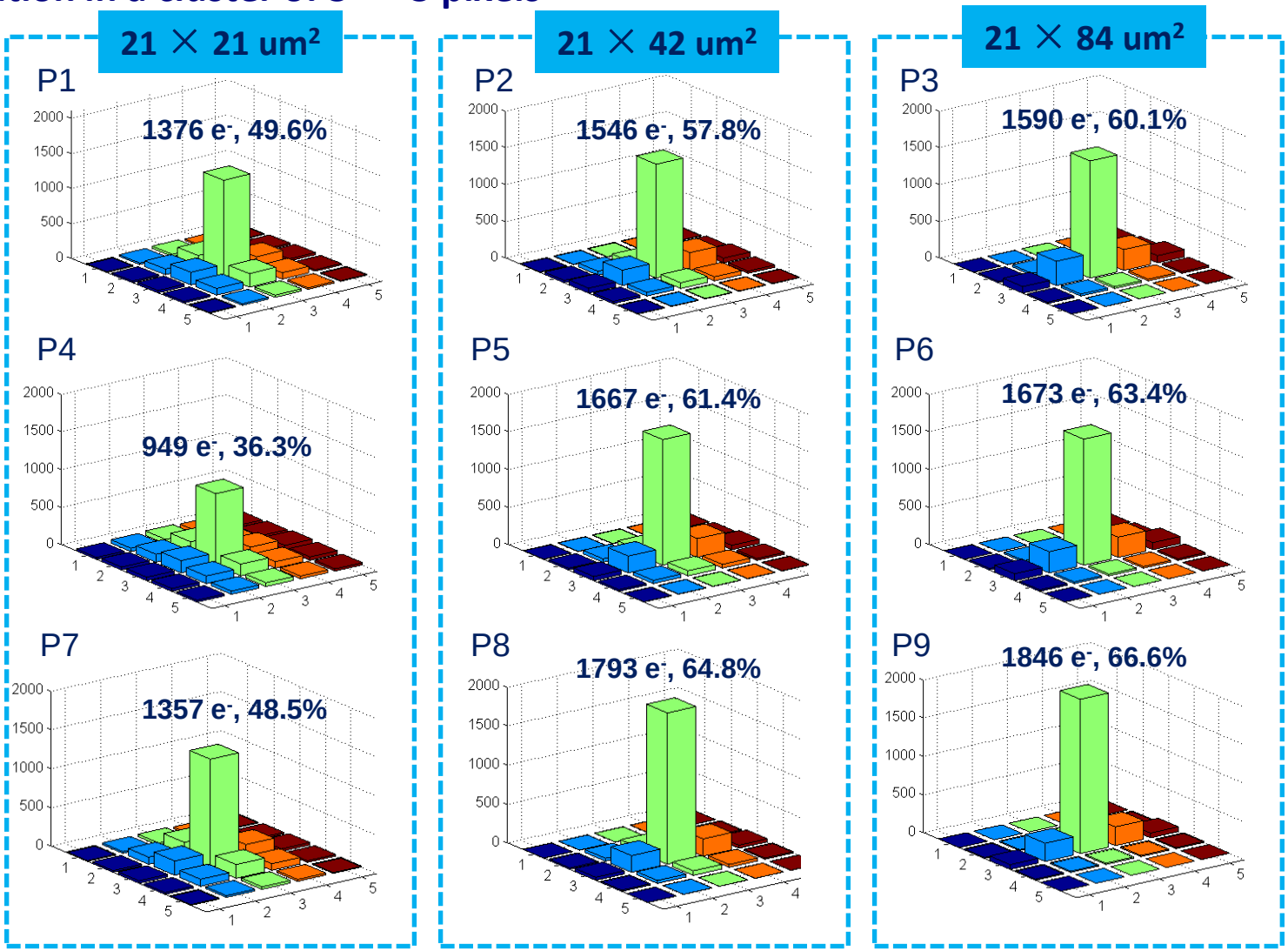
Surface of Diode

Footprint of Diode

Charge collection simulation

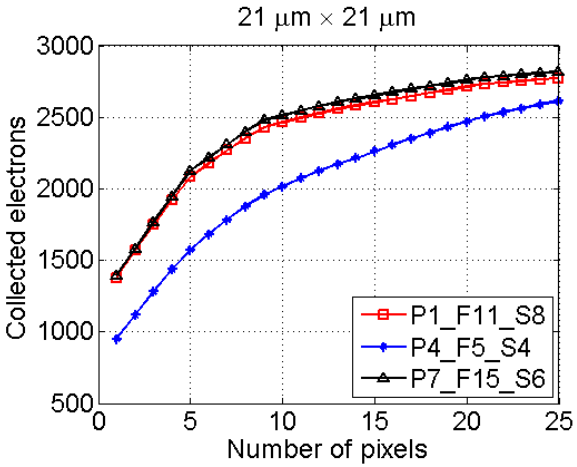
- **Charge distribution in a cluster of 5 × 5 pixels**

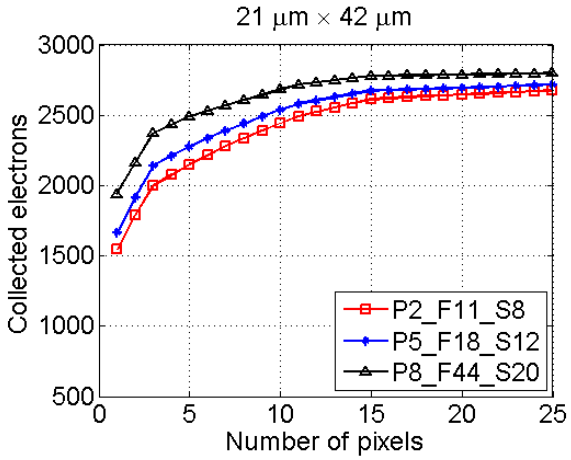


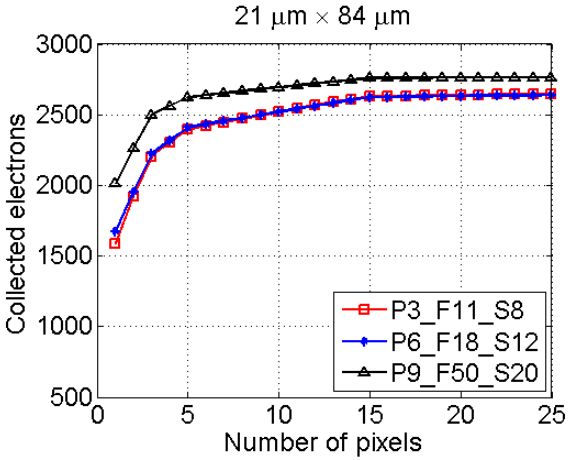


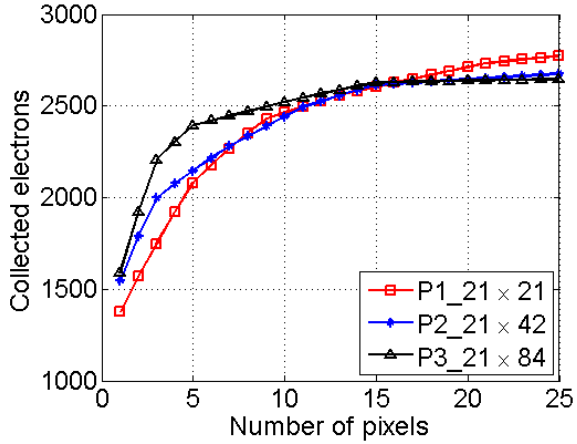
Charge collection simulation

- **Collected electrons in a cluster of 5 × 5 pixels**





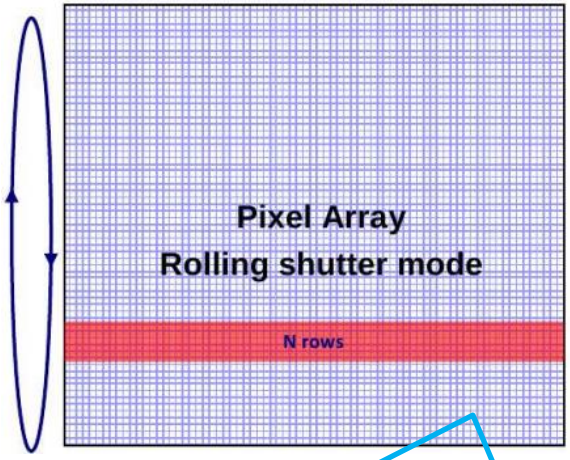


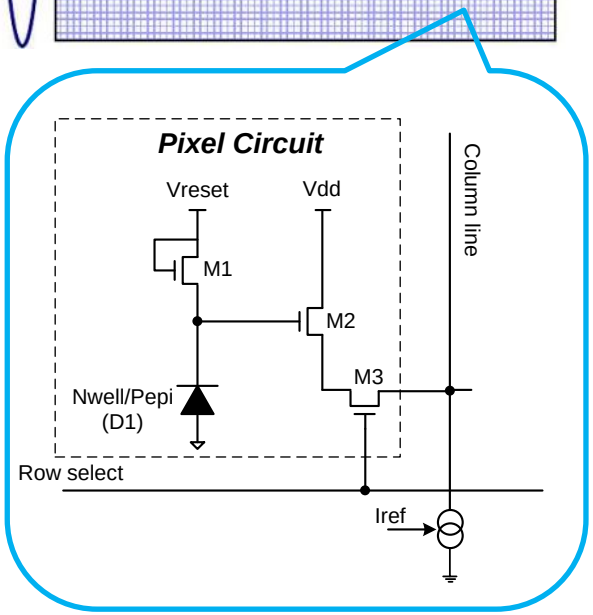


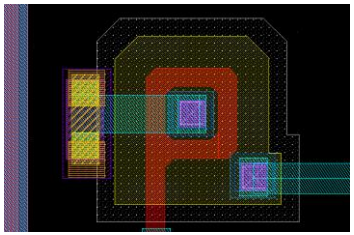
Pixel	P1	P2	P3	P4	P5	P6	P7	P8	P9
Pitch(x)(μm)	21	42	84	21	42	84	21	42	84
N(D)	1	1	1	1	1	1	1	1	1
F(D)(um^2)	11	11	11	5	18	18	15	44	50
S(D)(um^2)	8	8	8	4	12	12	6	20	20

Prototype chip design

- **The chip contains:**
  - 9 blocks
    - Basic block: 64 rows × 16 columns
    - Rolling shutter readout mode
    - 32 μs integration time at 2 MHz clock frequency
    - 16 parallel analog outputs
    - Sensitive area: 2 × 7.88 mm^2
  - 3T pixel structure
    - The reset transistor is connected in permanent reloading (similar behavior of a diode)
    - 50 μA current load in each column
    - Diode is staggered in large pixel
      - ★ Improve charge collection efficiency (charge sharing)
    - Gate-enclosed NMOS transistors
      - ★ Improve radiation tolerance
    - P+ guide ring

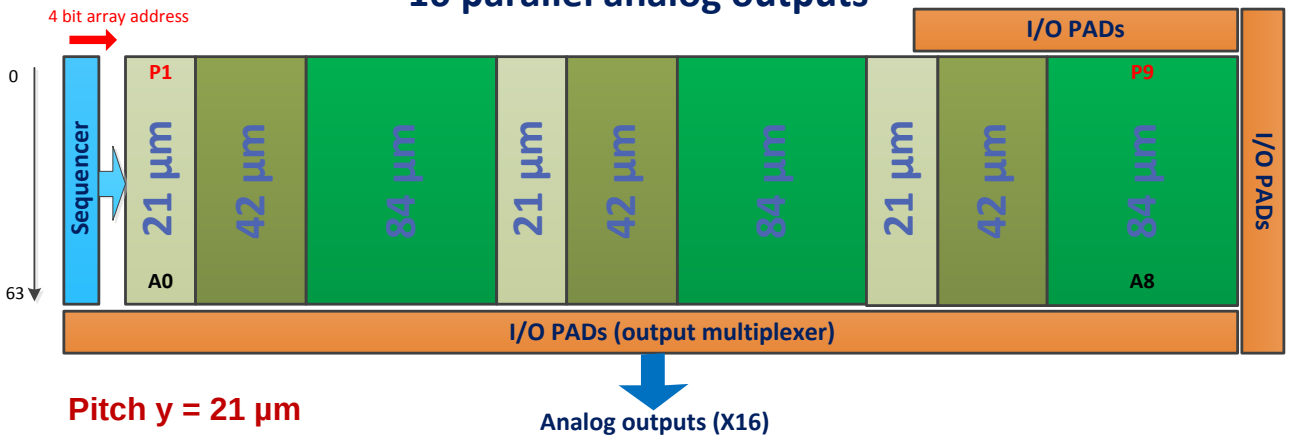




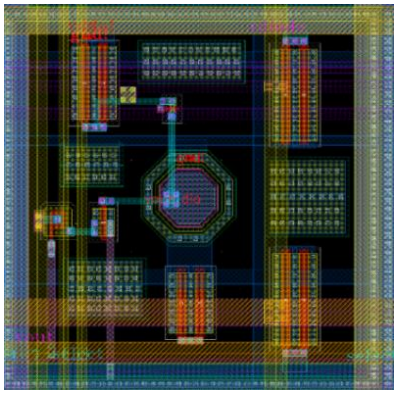


Prototype chip design

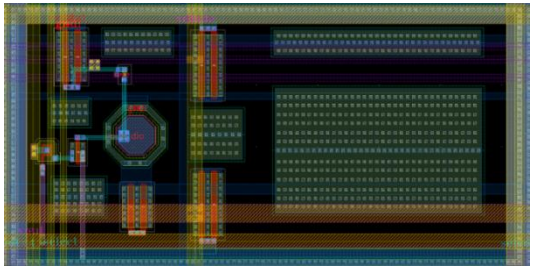
9 blocks of 16 columns x 64 rows
16 parallel analog outputs



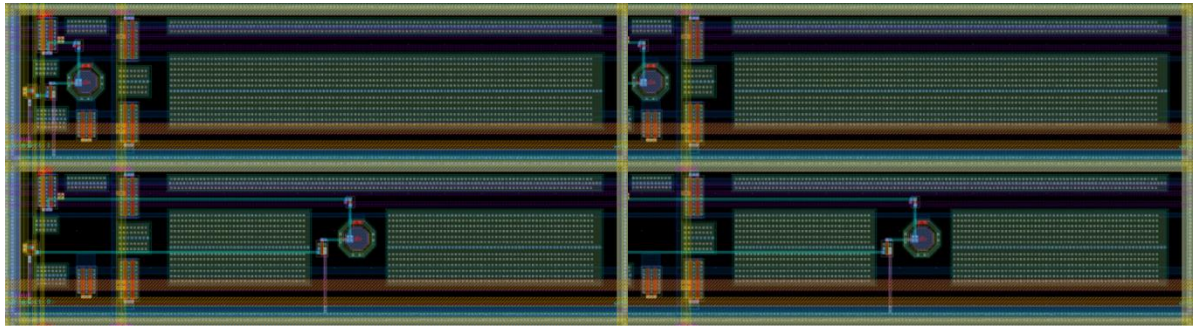
Pitch y = 21 µm



P1 (21 × 21 µm²)

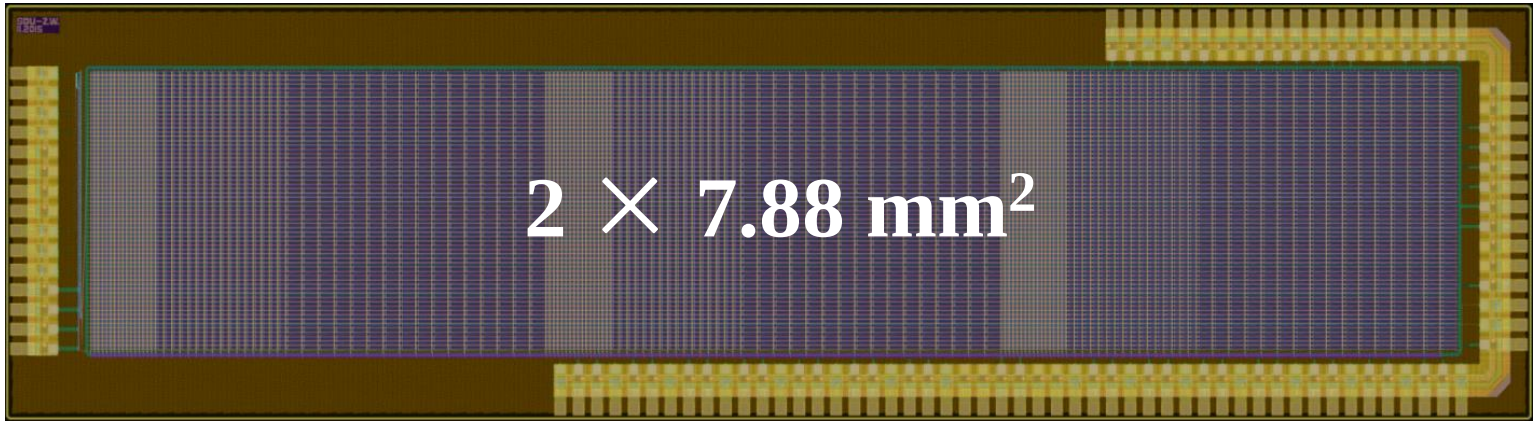


P2 (21 × 42 µm²)



Diode staggered pixel to pixel
P3 (21 × 84 µm²)

Summary & outlook



- **Tower CIS November 2015 submission**
- **9 blocks of 64 rows ×16 columns with analog read-out**
- **Integration time:** 32 μs @ 2 MHz input clock
- **Preliminary TCAD simulation to understand the impacts on charge collection, including:**
  - ✓ Pixel size
  - ✓ Collection diode area (surface, footprint)
- **First prototype with 0.18 μm CIS technology aiming for CEPC inner tracker**
- **TCAD simulation results will be verified with laboratory test**
- **The test is being prepared and the preliminary test results will be shown, complemented with an outlook on further design improvements**

谢谢！

Motivation for developing CMOS pixel sensors

- **Physics driven requirements**
  - Single point resolution < 7 μm
    - High granularity
  - Material budget ≤ 0.65% X_0/layer
    - Low power consumption
    - Thickness can be less than 50 μm
- **Running constraints (beam related background)**
  - Pixel occupancy (typical ≈ 0.5%: tracking strategy dependent)
    - High read-out speed
  - Radiation tolerance
- **Specific balance between conflict requirements**
  - Physics driven specifications have the priority
  - R&D rather perform to match running condition driven specifications