ATLAS tracker phase II upgrade and the HV/HR CMOS technology

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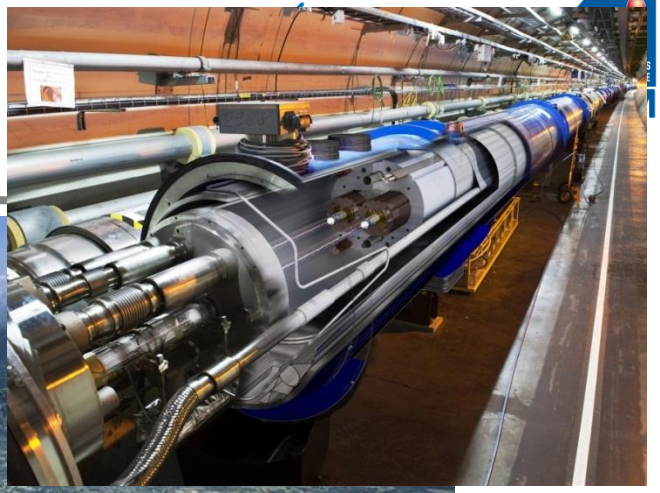
IHEP EPC seminar

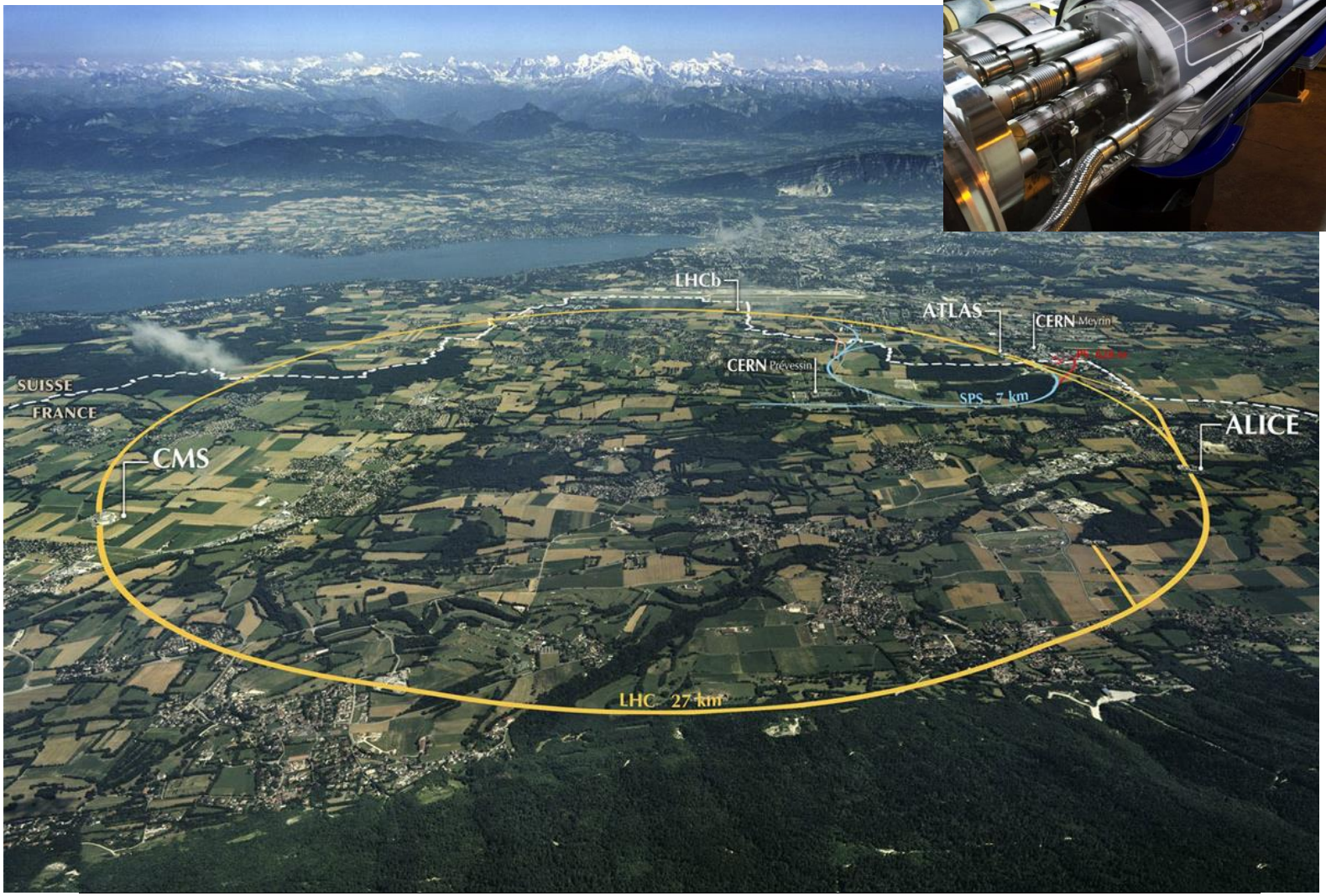
Content

- ATLAS tracker today.
- Inner Tracker (ITk) phase II ATLAS upgrade program.
  - HL-LHC environment.
  - CMOS pixels in the ITk.
- HV/HR CMOS program.
  - Recent highlight:
    - focus on demonstrator program.
  - Plans.

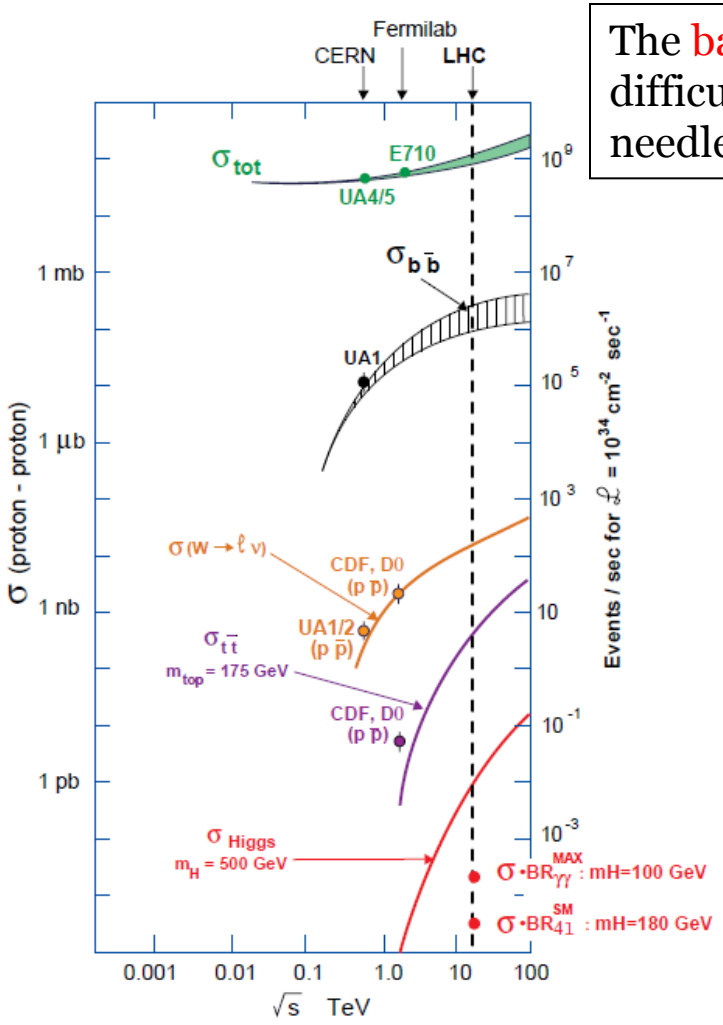
- Perspectives and conclusion.

CERN and the Large Hadron Collider





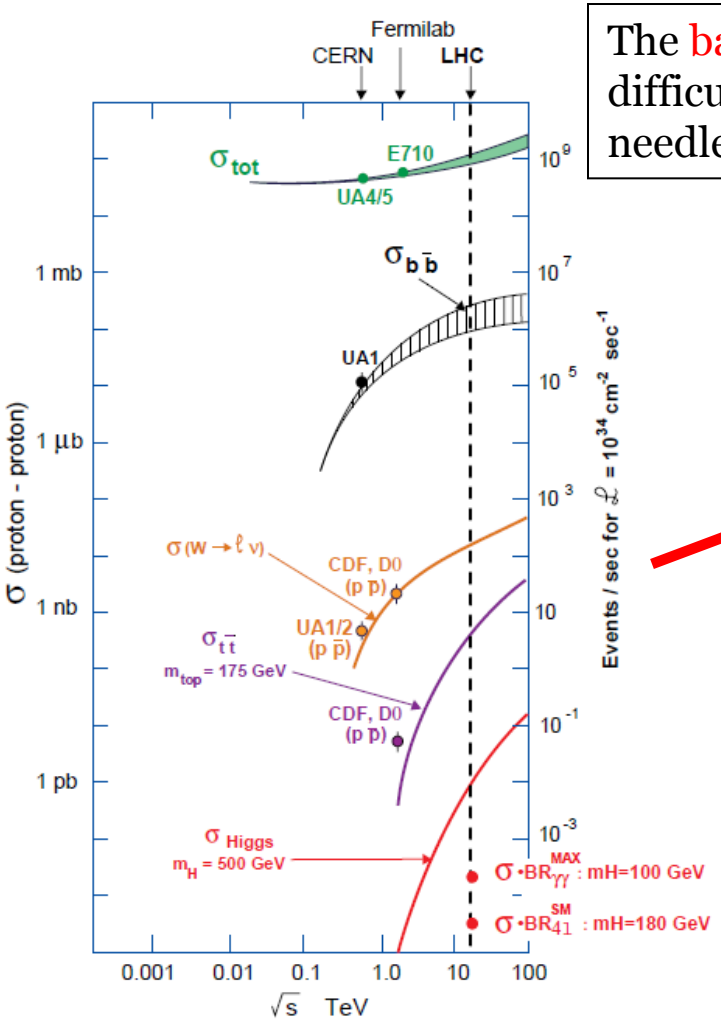
Searching for H in LHC



The background curse: More difficult then ”looking for a needle in a haystack”...

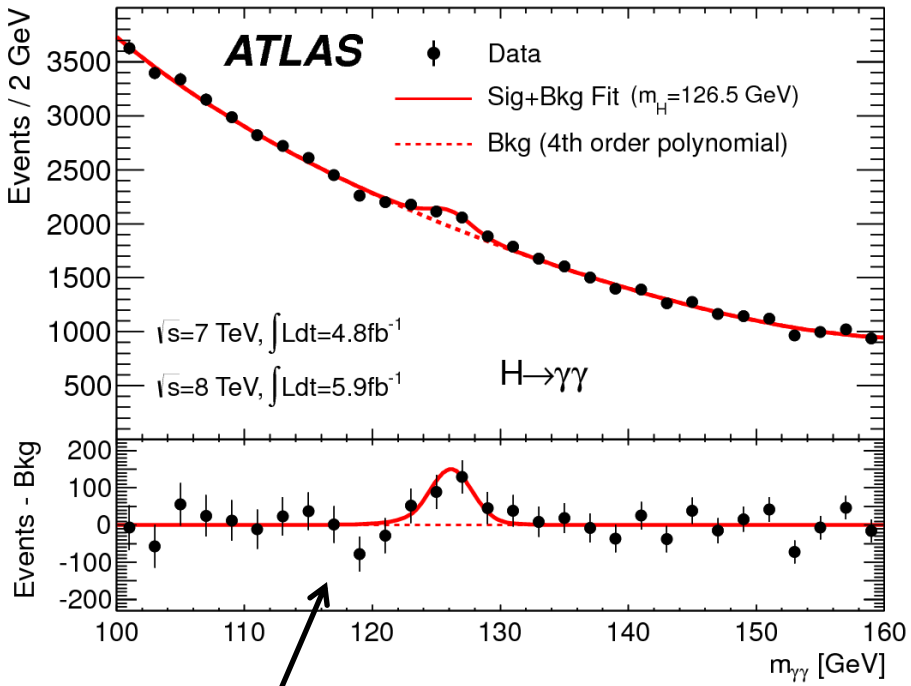
Searching for H in LHC

The background curse: More difficult then ”looking for a needle in a haystack”…



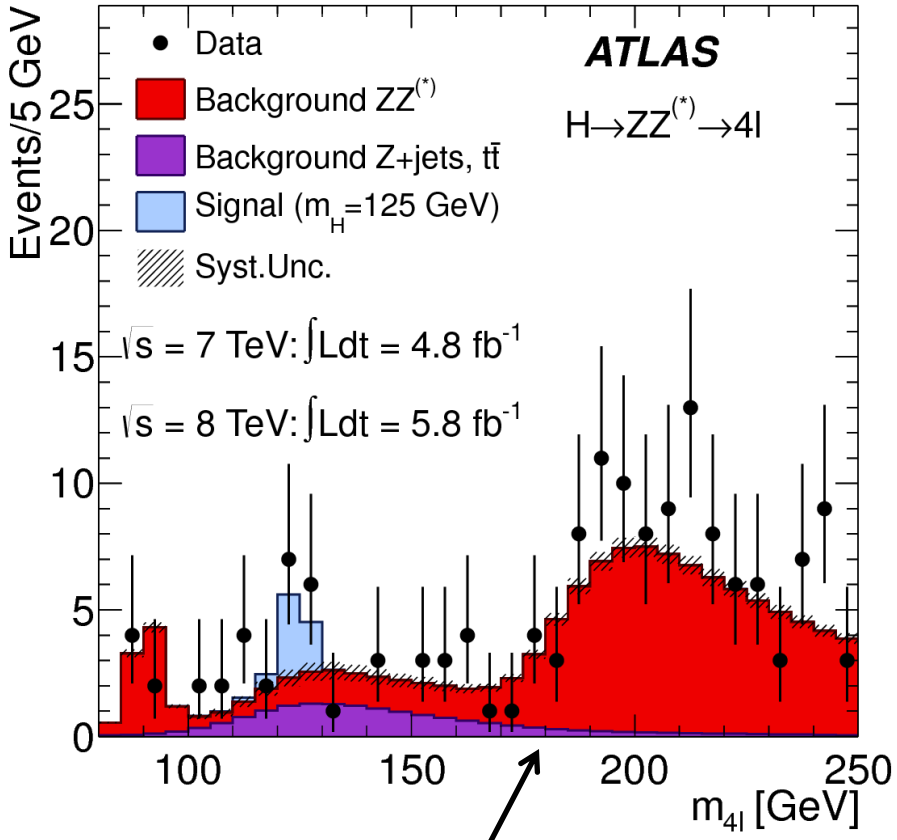
2012: Higgs discovery in ATLAS (& CMS)

Higgs in 2 photons -2012-



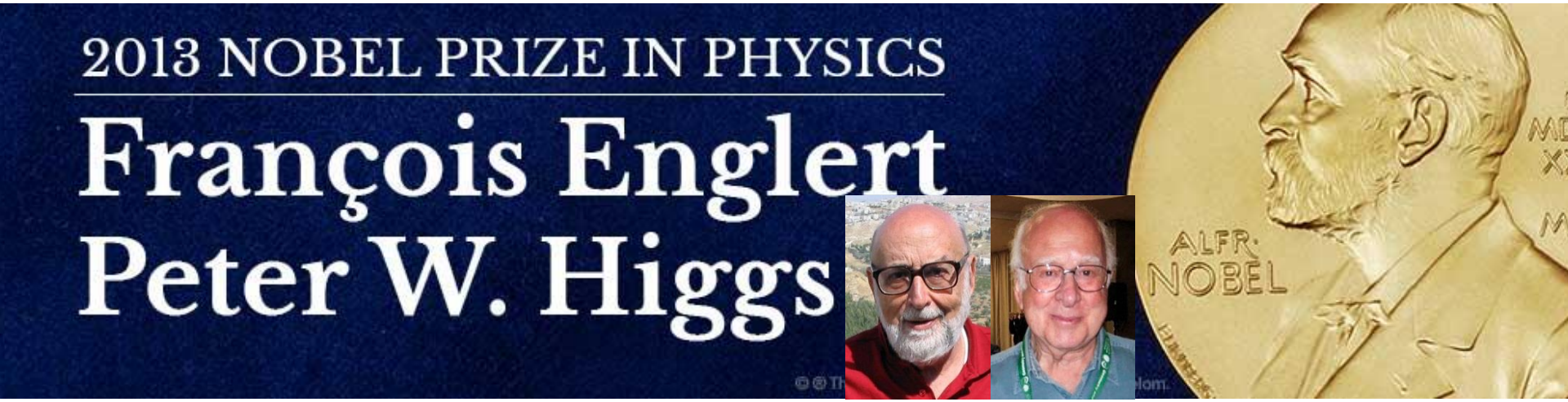
High background, but big signal!

Higgs in ZZ*-2012-



Small background, but very small signal

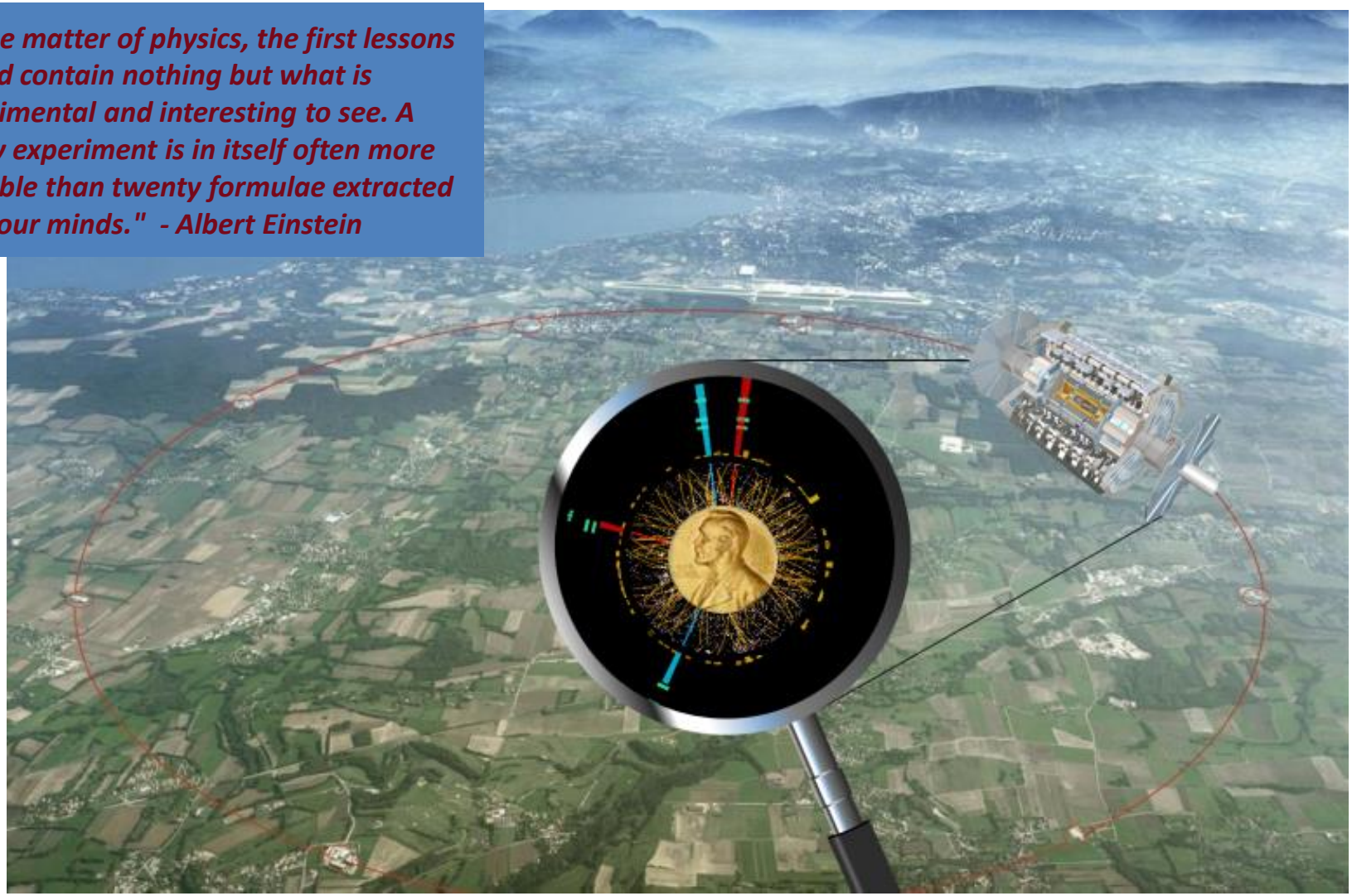
Nobel Price in Physics 2013



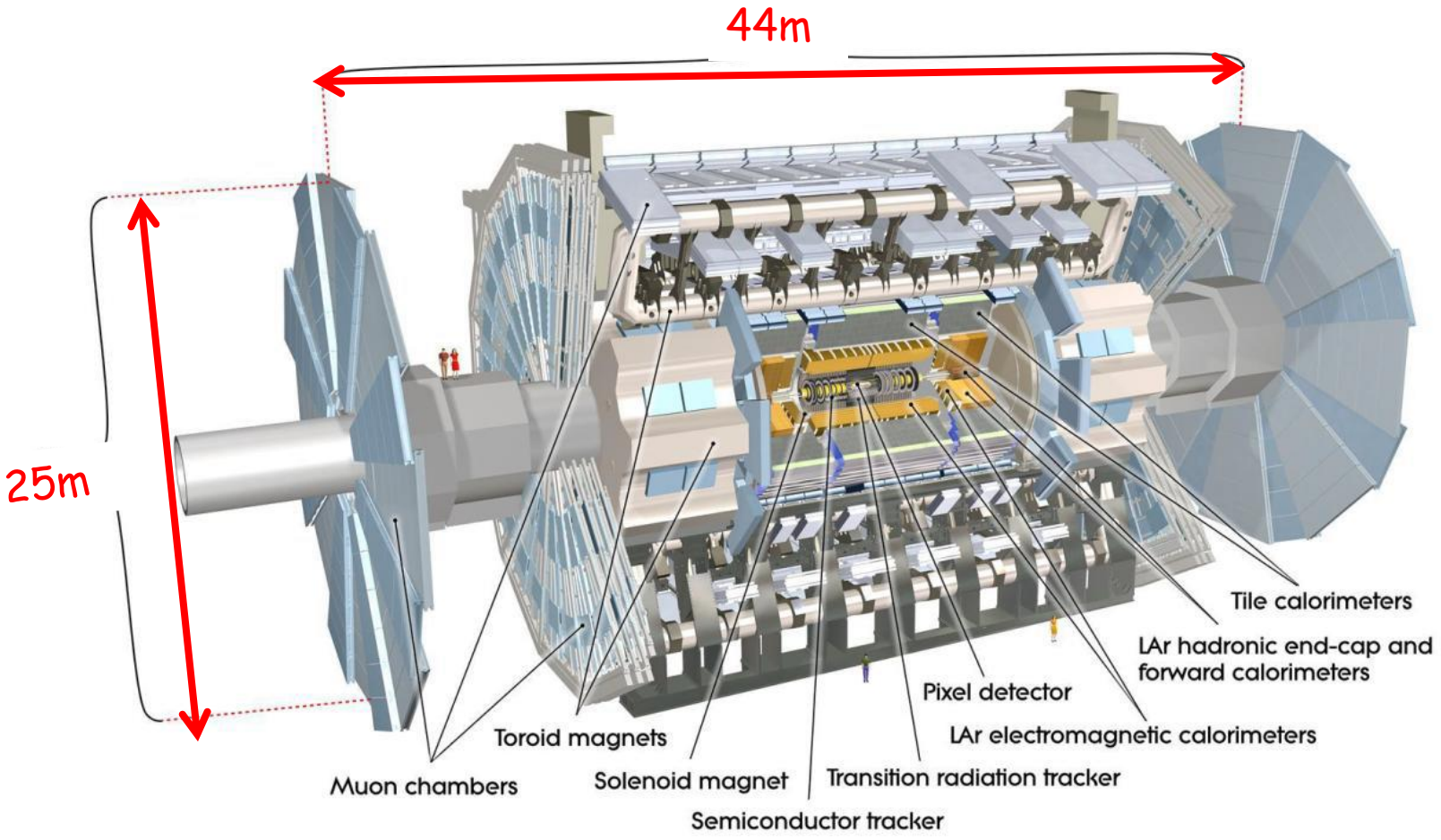
« ***for the theoretical discovery of a mechanism that contributes to our understanding of the origin of mass of subatomic particles, and which recently was confirmed through the discovery of the predicted fundamental particle, by the ATLAS and CMS experiments at CERN's Large Hadron Collider*** »

Nice magnifying glass!

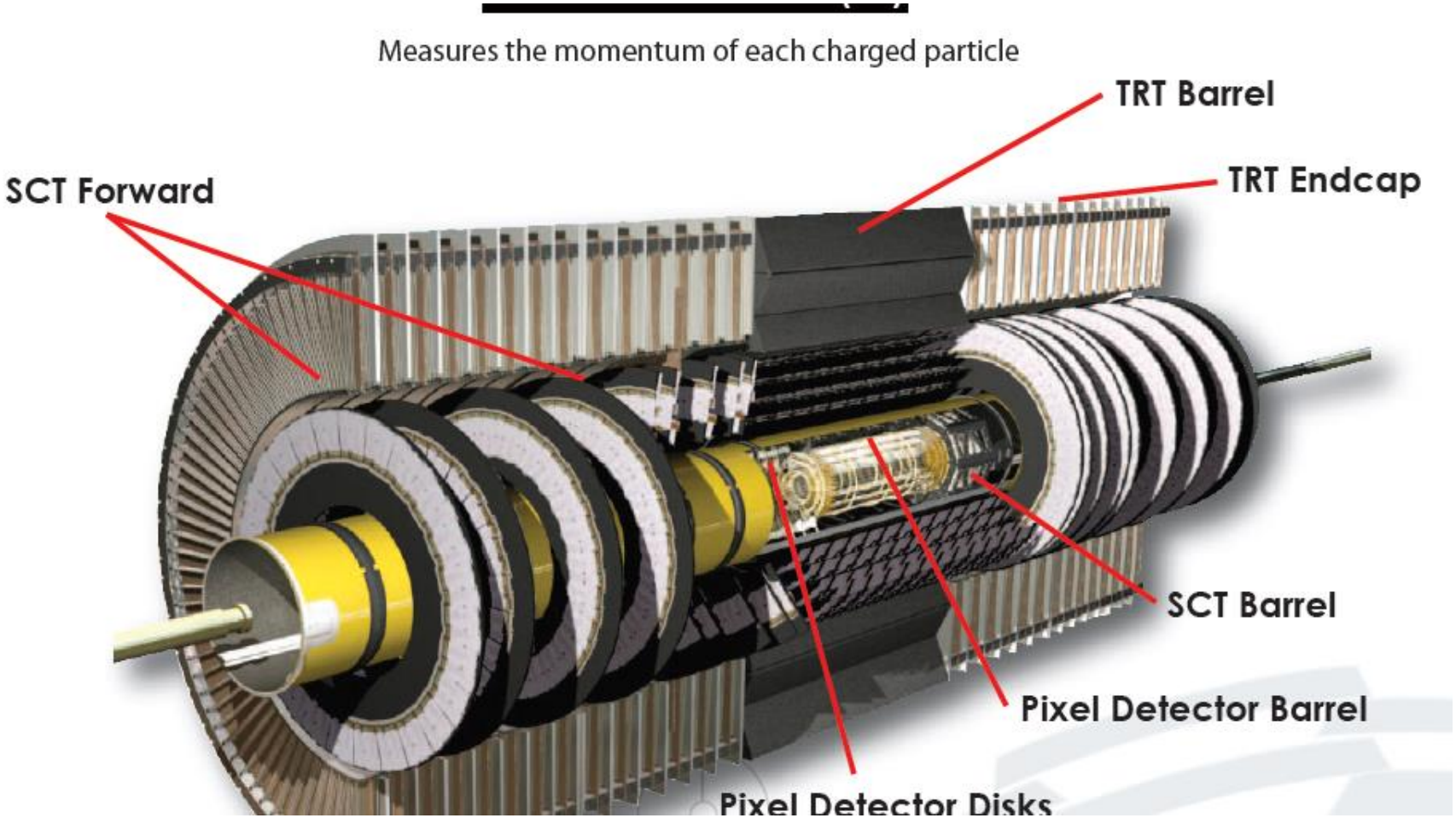
"In the matter of physics, the first lessons should contain nothing but what is experimental and interesting to see. A pretty experiment is in itself often more valuable than twenty formulae extracted from our minds." - Albert Einstein



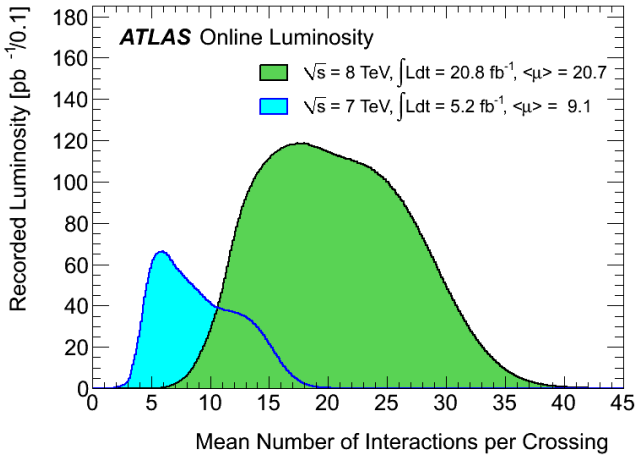
Our magnifying glass: ATLAS

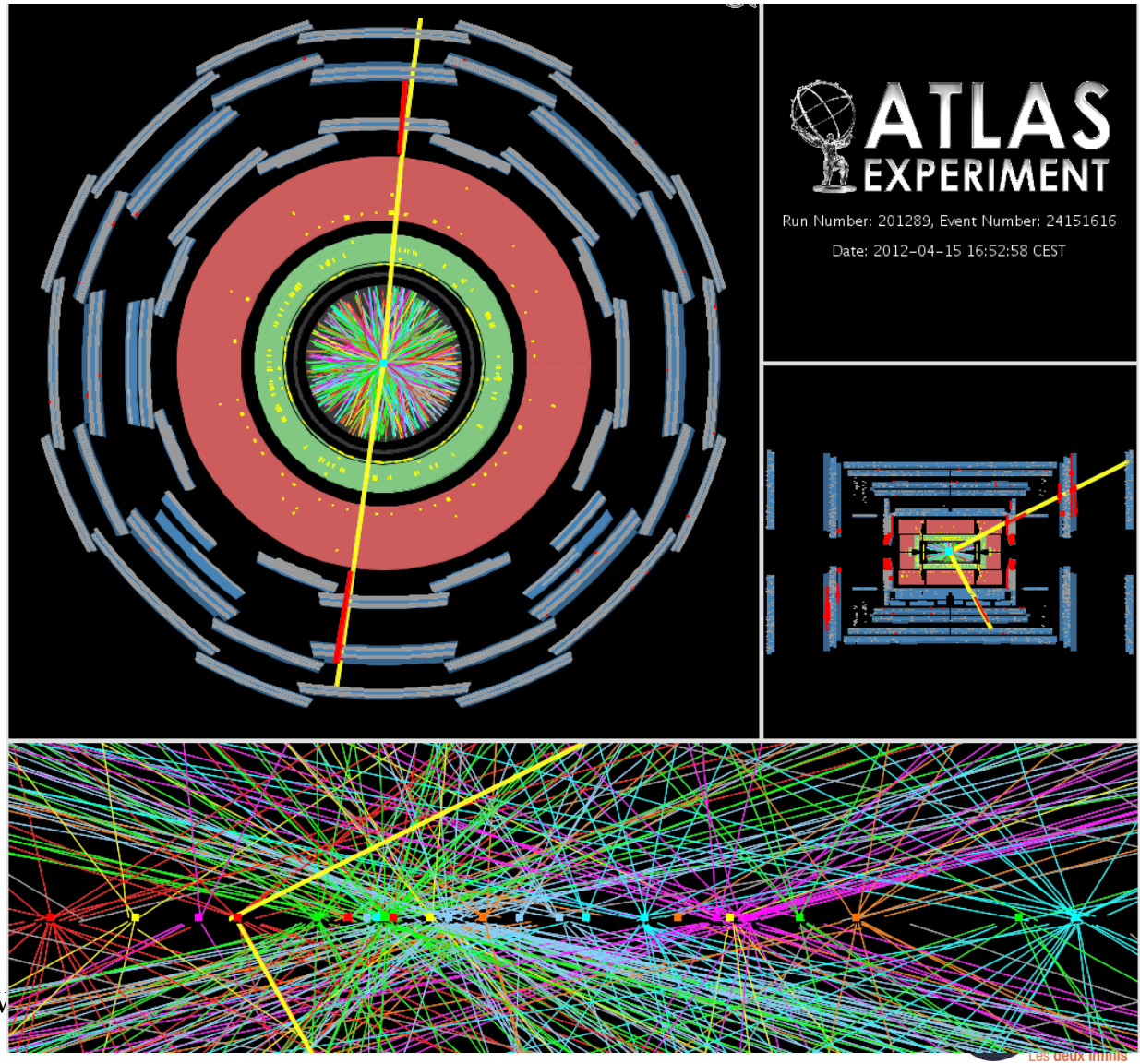


ATLAS silicon tracker (now 10m² → 200m² in future!)



Environnement LHC (pile-up)



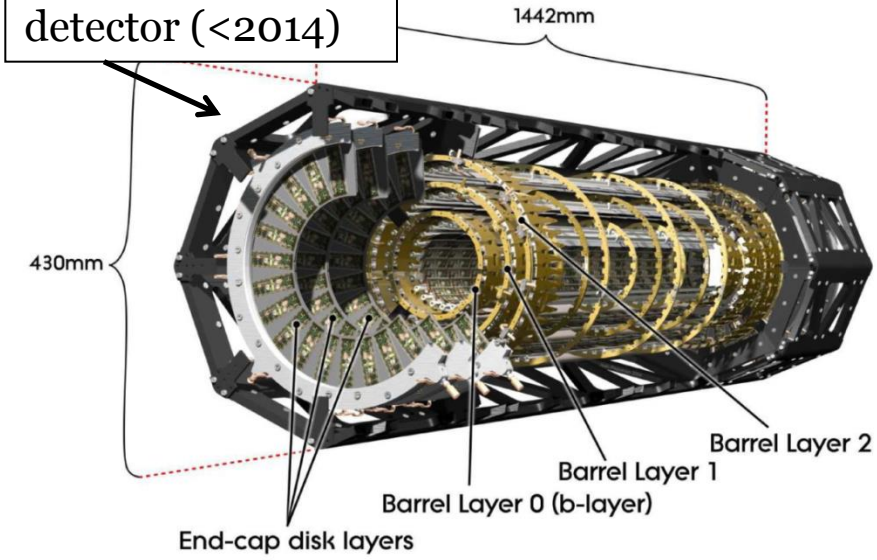


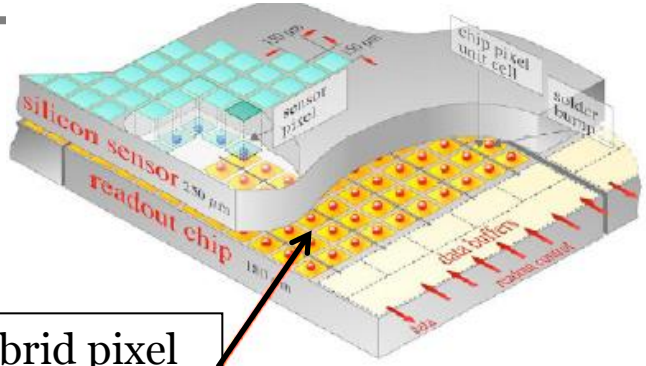
High pile-up due to 50 ns Bunch Crossing

Example: Z-boson with 25 reconstructed pile-up vertices

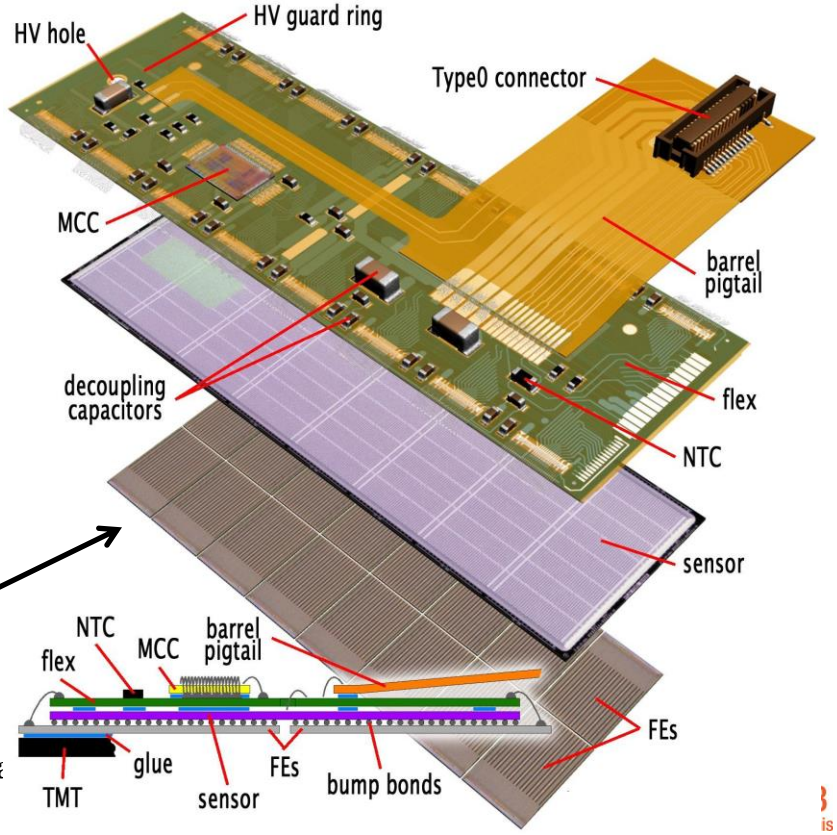
Pixel detector (now ~1.5 m², futur ~10m²)

ATLAS Pixel detector (<2014)





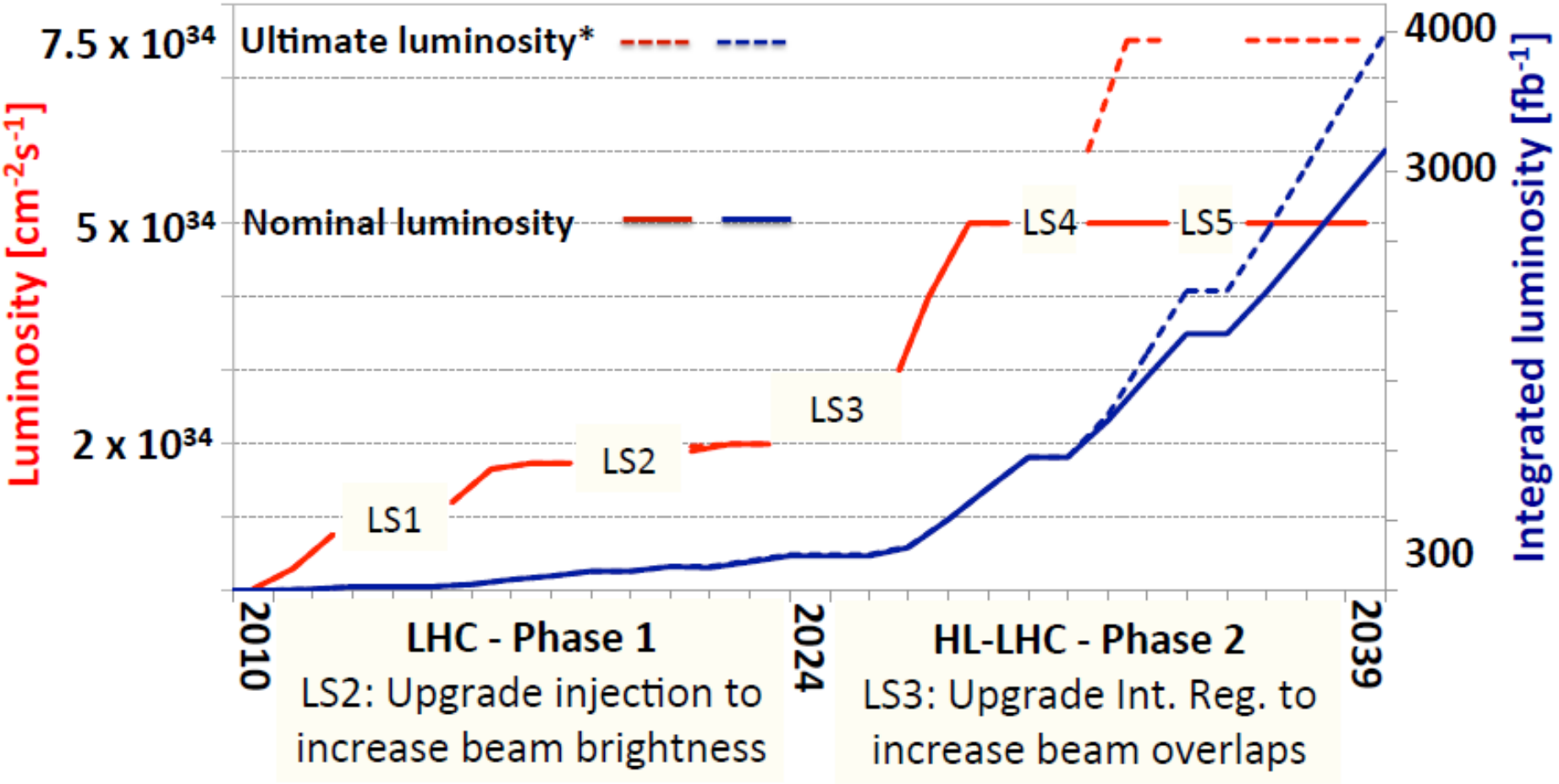
Hybrid pixel



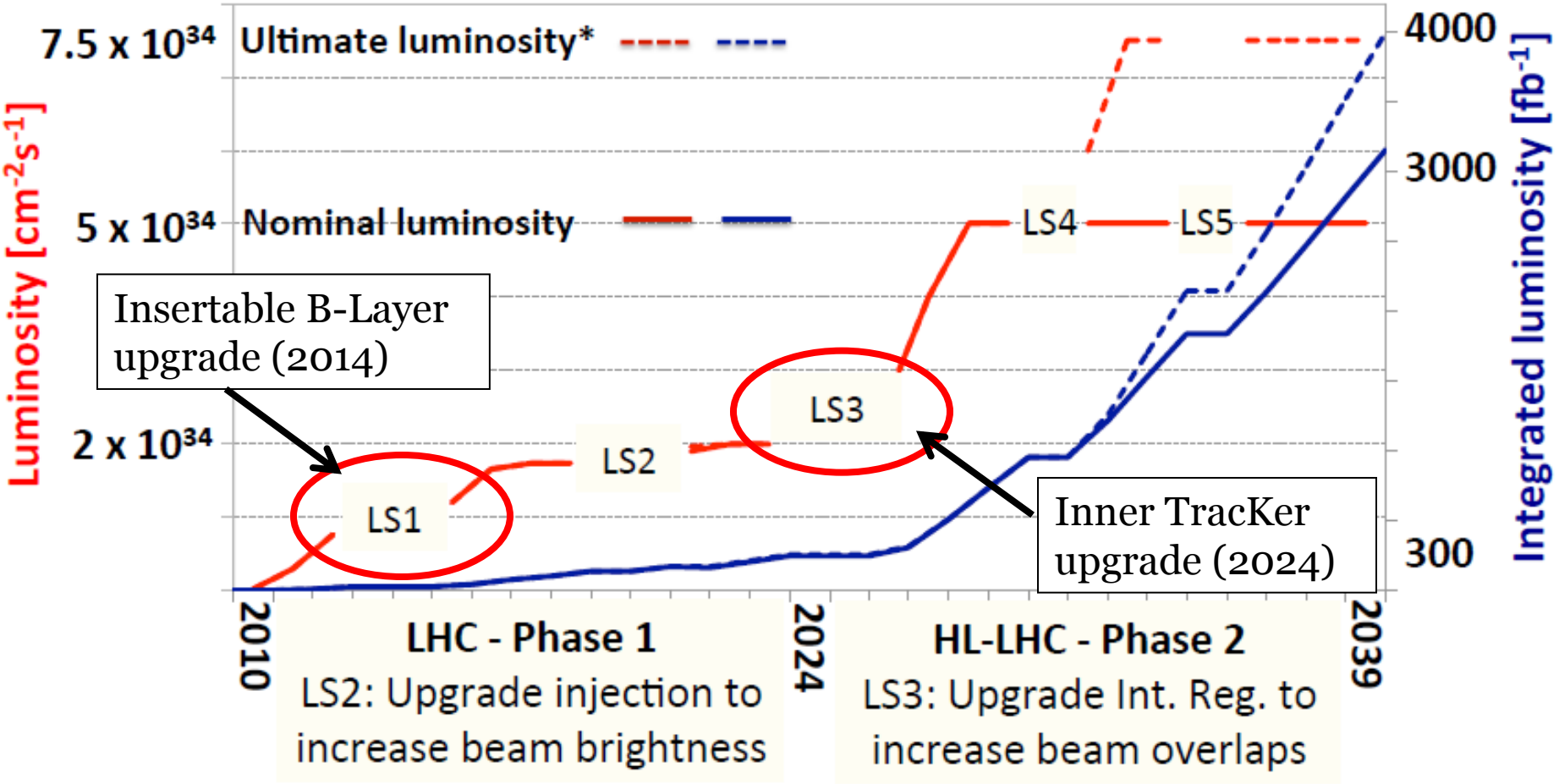
The initial ATLAS pixel detector: 87 millions pixels of size 50×400μm², in a 3-layer cylinder, cooled down at -15ºC, measuring particle crossing 40 millions times per second!

Original hybrid module

Long Shutdowns & Upgrades



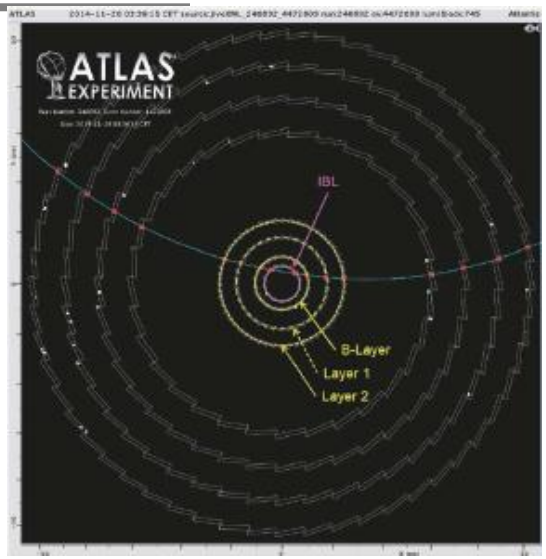
Long Shutdowns & Upgrades

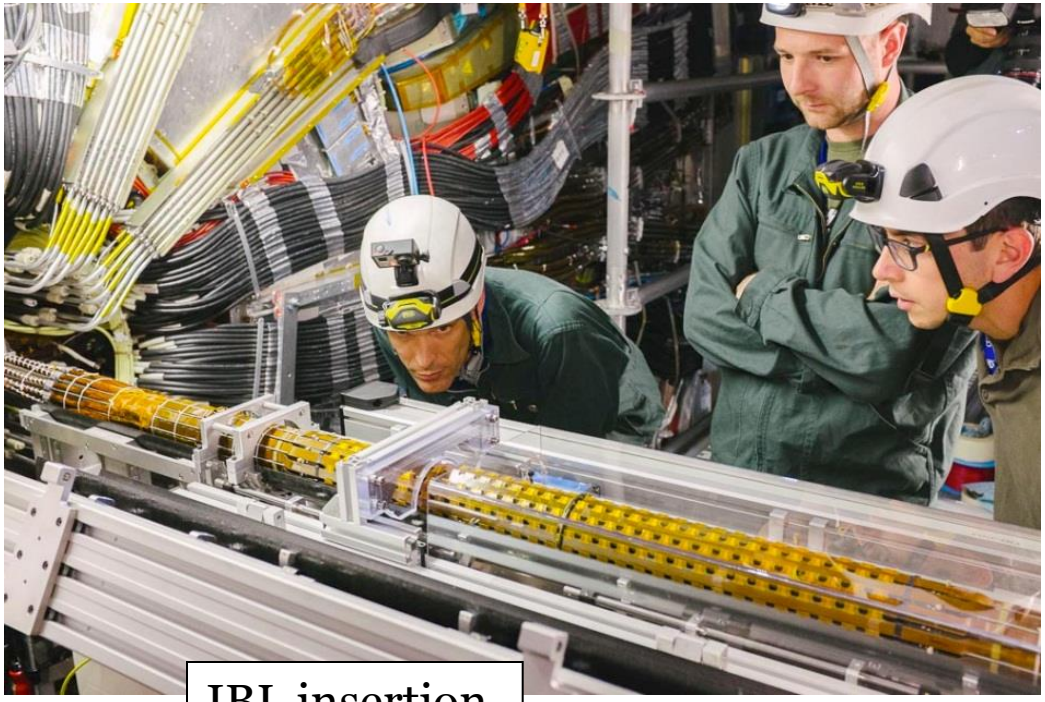


IBL upgrade

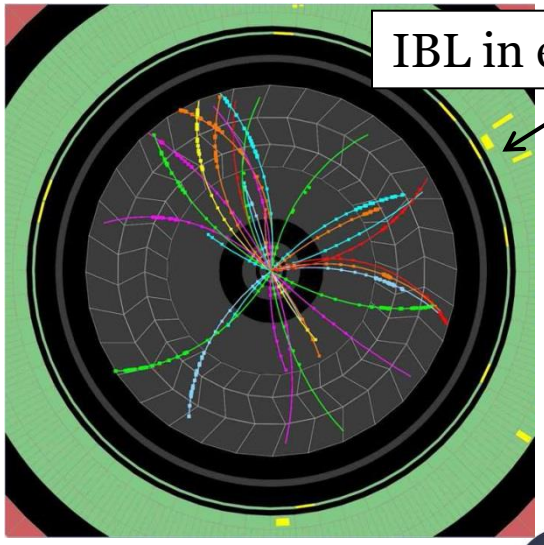
- 2014: The IBL upgrade!

IBL w. cosmic





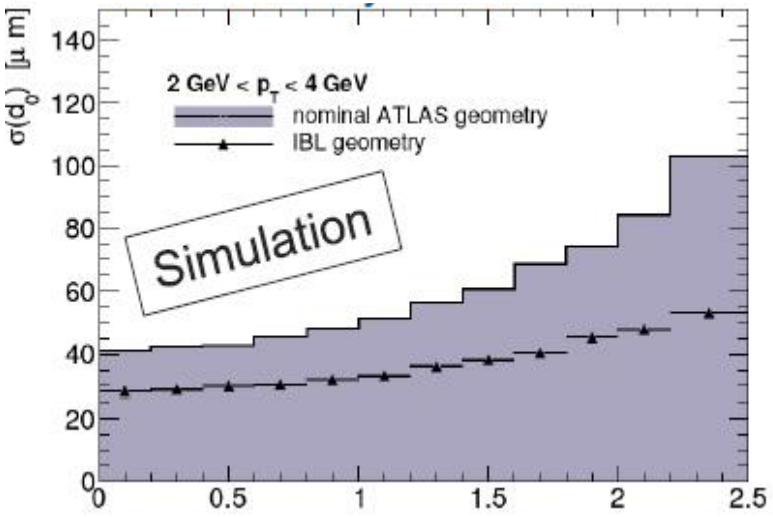
IBL insertion

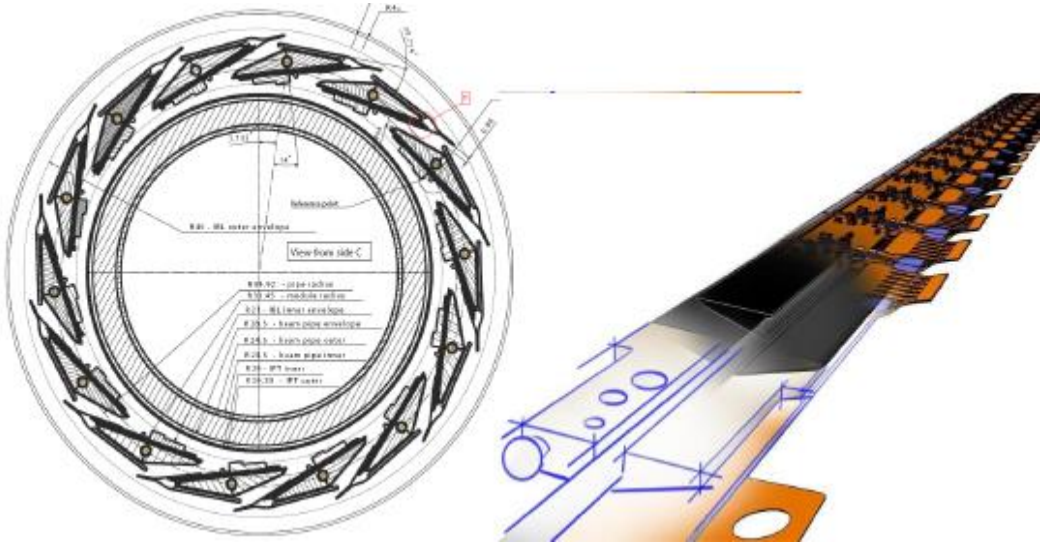


IBL in event

IBL motivation

- Improve b-tagging performances:
  - Impact parameter resolution improves by factor ~2.
  - Light jet rejection at higher pileup >2 better (for fix b-tag efficiency).
- Increase robustness of pattern recognition, in particular in case of B-layer modules failures.
- New innermost layer between beam pipe and initial inner layer.
  - 2 mm mechanical clearance!
- Short distance to interaction point:
  - High particle flux.
  - High occupancy (10^{-4} → 10^{-3} / pix.)
  - Radiation damage 250 MRad.

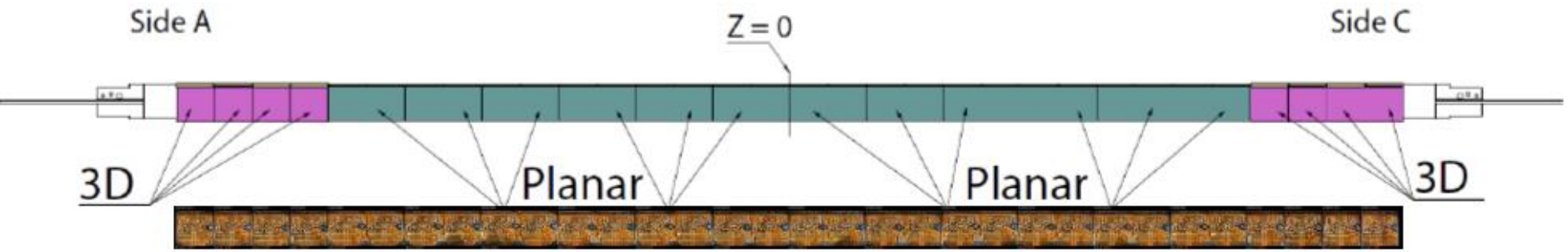




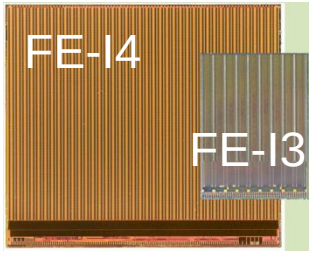
IBL staves

IBL staves are based on 2 technologies:

- 14 staves:
  - 12 planar n-in-n double chip modules (sensor fabricated by CiS).
  - 8 single chip 3D modules (sensor fabricated by CNM and FBK).
- FE-I4B readout chip, IBM 130nm technology
- 12.042.240 pixels, 250 x 50 μm².
- Radius: 3.27 cm, ~70 cm long.



Electronics for the IBL



The FE-I4

Need for a new FE for IBL?

→ Higher hit rate → local memories.

→ Smaller pixel size: granularity.

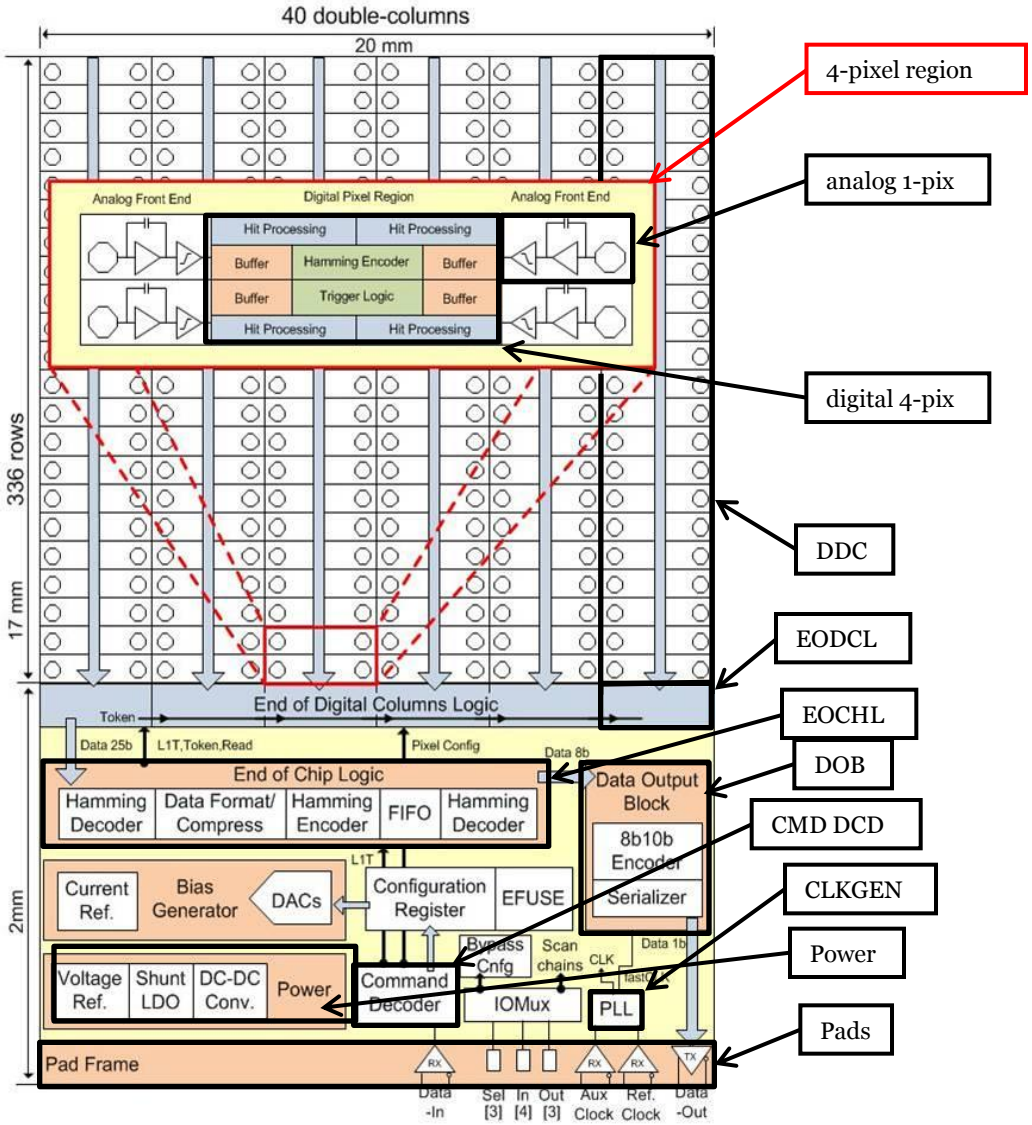
→ Reduced periphery & bigger chip: high active area fraction

→ Simple module: No MCC, digital functions into the FE.

→ Power efficient design & new concepts: Analog design; digital activity down.

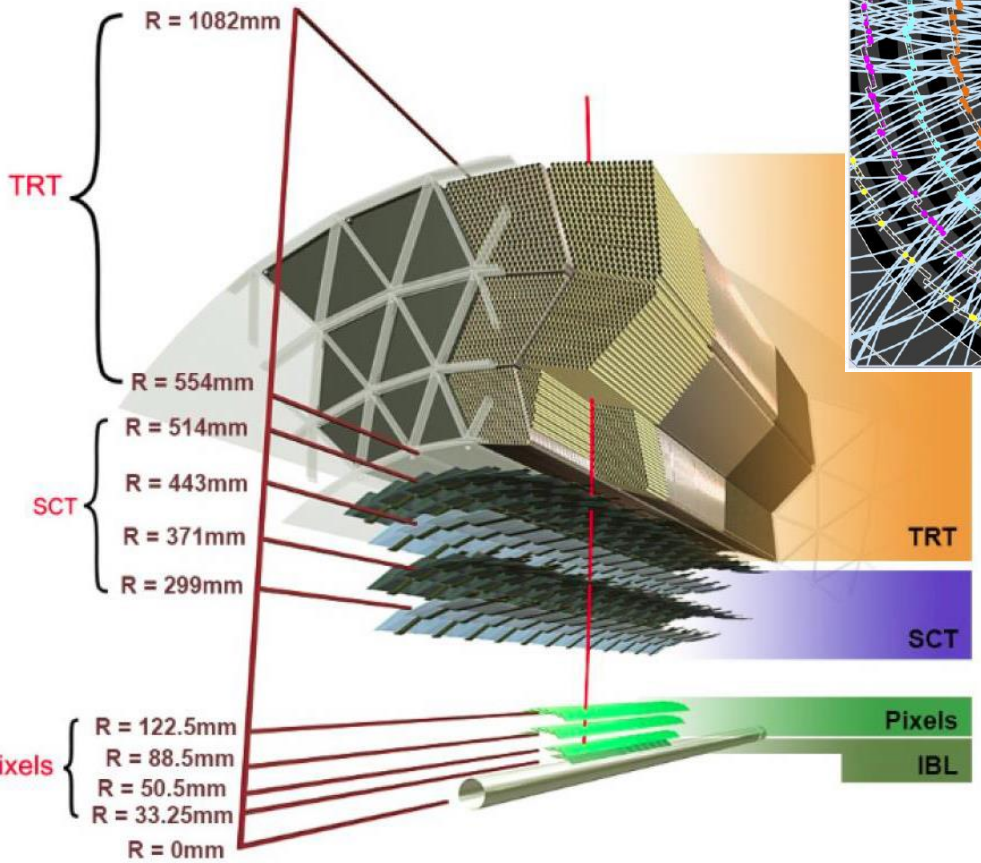
New technology:

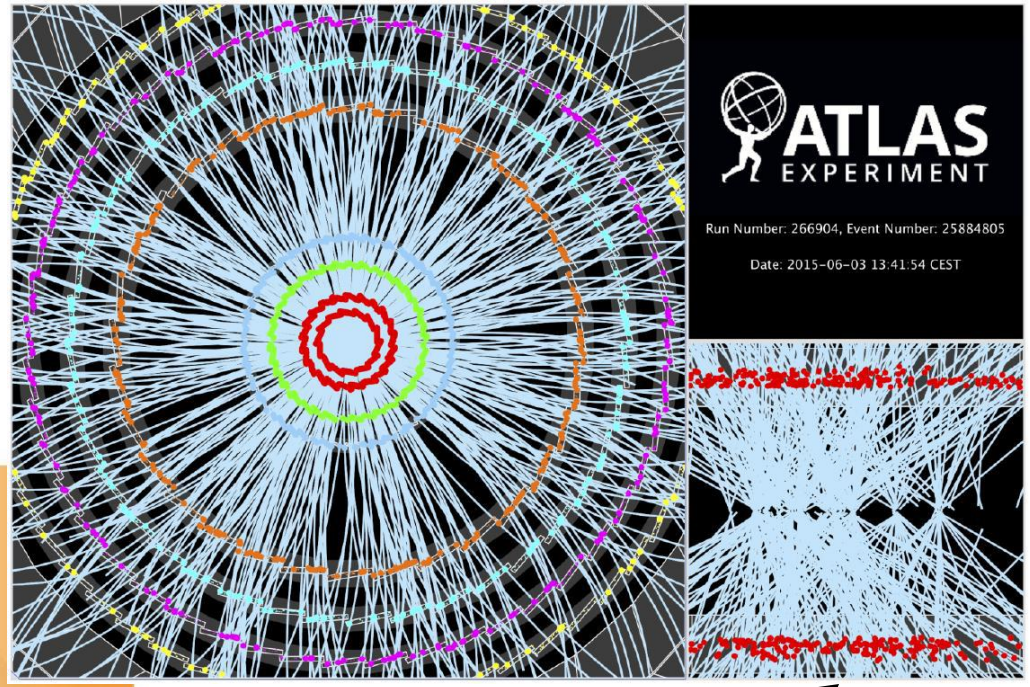
IBM 130→ Higher integration density digital circuits, radiation-hardness (no ELT), availability timescales of our experiments.



Run II operation: 4 pixel layers

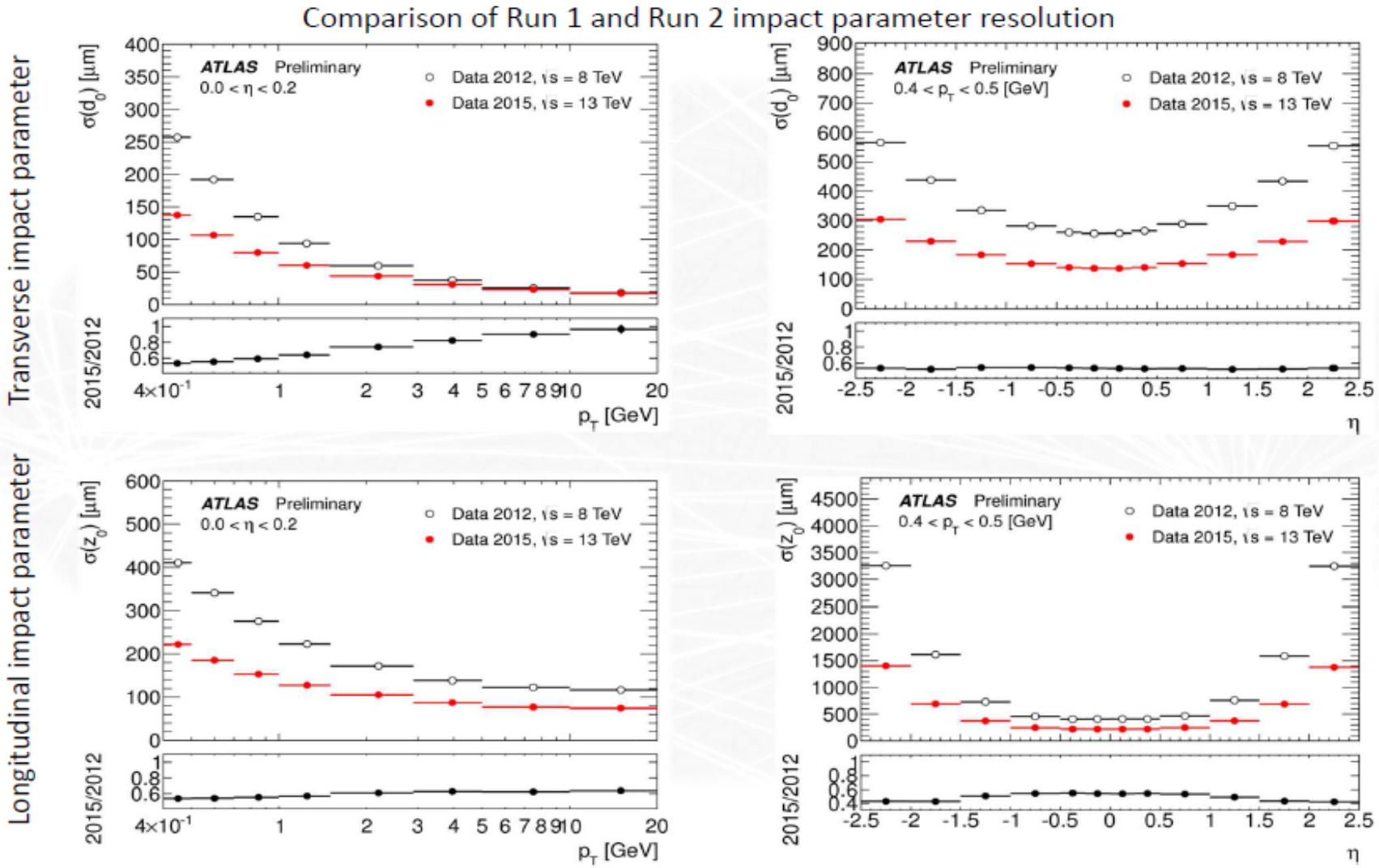
Configuration for Run II and Run III → 2022





Multiple vertices disentangled with the IBL!

Tracking improvement with IBL



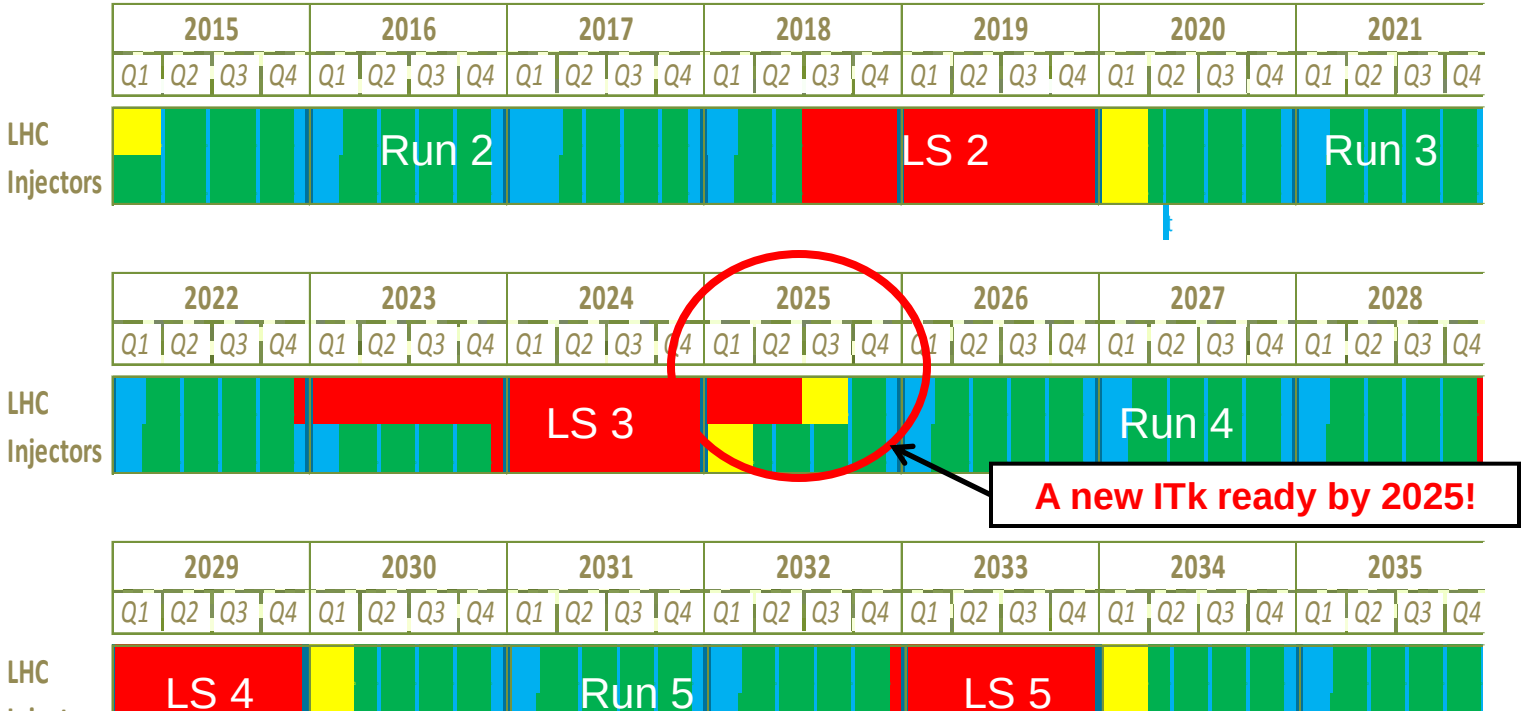
HL LHC schedule

Only EYETS (19 weeks) (no Linac4 connection during Run2)

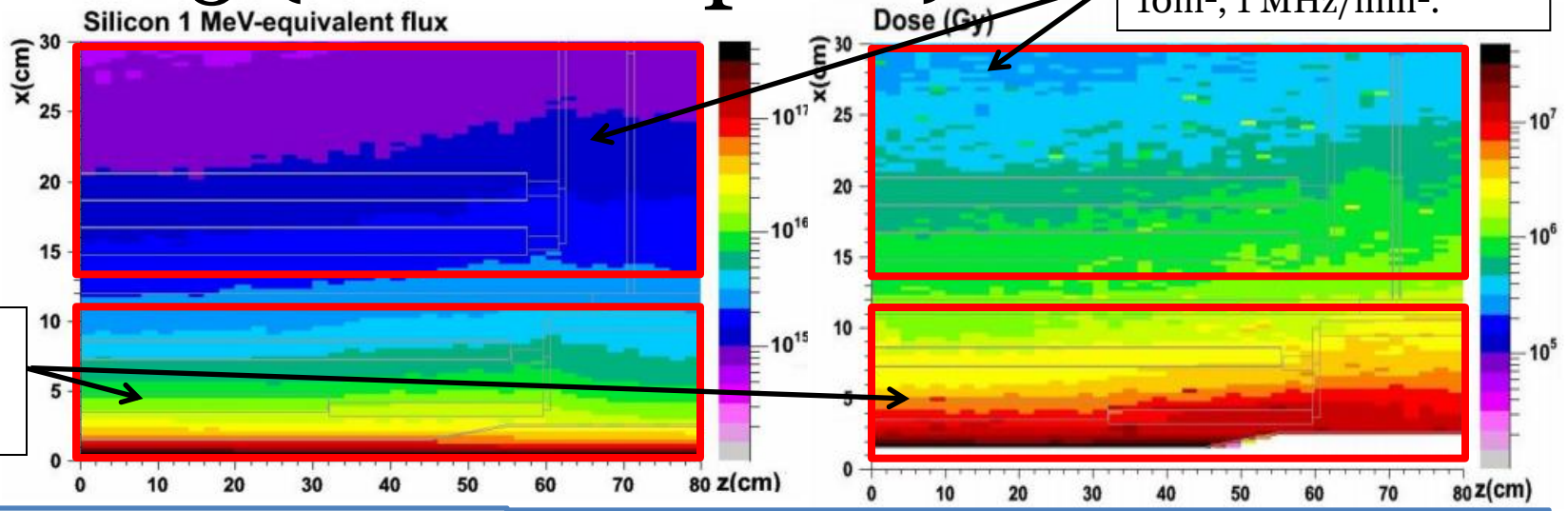
LS2 starting in 2018 (July) 18 months + 3months BC (Beam Commissioning)

LS3 LHC: starting in 2023 => 30 months + 3 BC

injectors: in 2024 => 13 months + 3 BC



HL-LHC environment >2025 (focus on pixel)



Fluence at 5 cm radius:
NIEL: ~1-2•10^{16} n_{eq} cm^{-2}
TID: ~500-1000 MRad

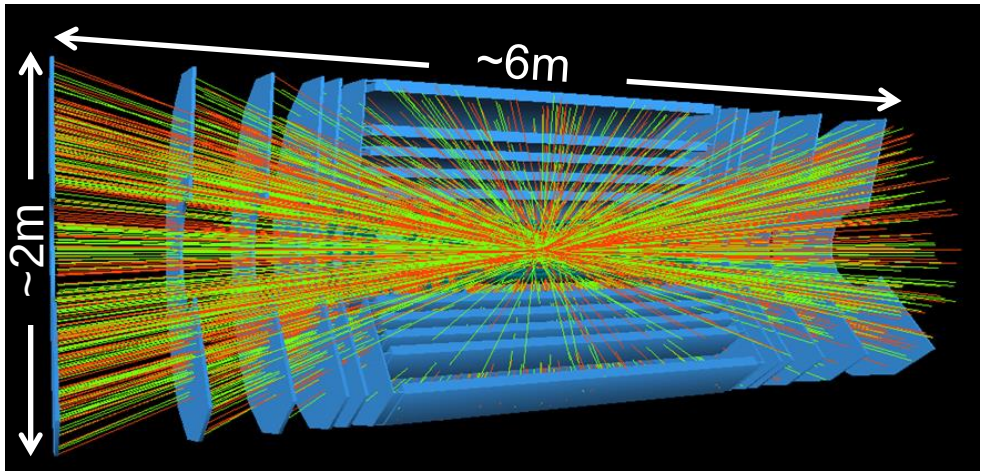
The new Inner Tracker should be rad-hard and cope with high occupancy.

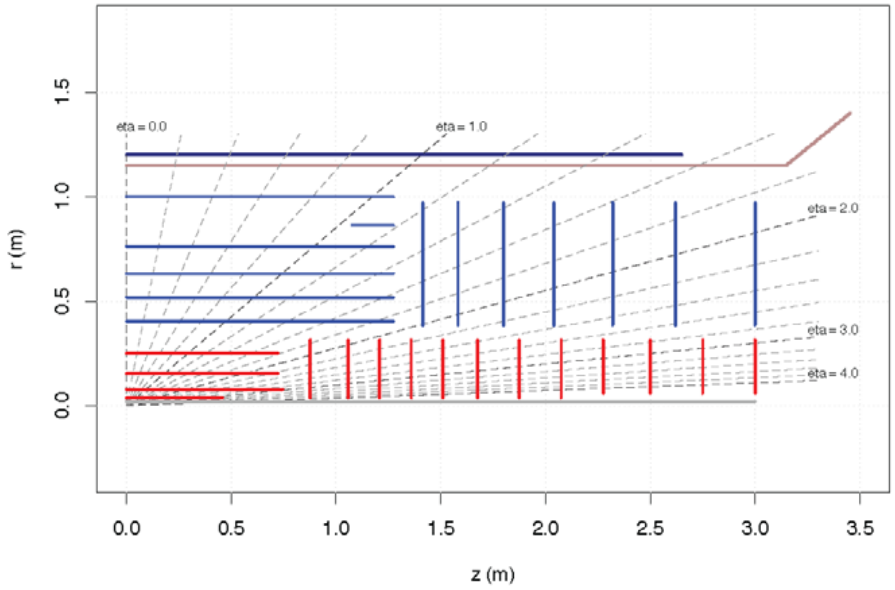
A first possibility for pixels is **the use of a hybrid technology**:

- •Sensor: planar silicon or 3D, diamond…
- •Readout-Out Chip: deep-submicron rad-hard ICs (130nm,65nm)=> high granularity=> high resolution, low occupancy → RD53

A second possibility is **an integrated technology** (electronics INTO the sensing element) → HVCMOS. Level of integration has range (passive → "smart" pixels → fully monolithic).

New ITk





- **Pixel: (R<40cm?)**

→ 5 barrel layers

  - Inner 2: 3D/planar/CMOS
  - Outer 3: planar/CMOS

- 13m² silicon
- ~5000 6 Gb/s links
- **Strip Tracker:**

→ 4 barrel layers

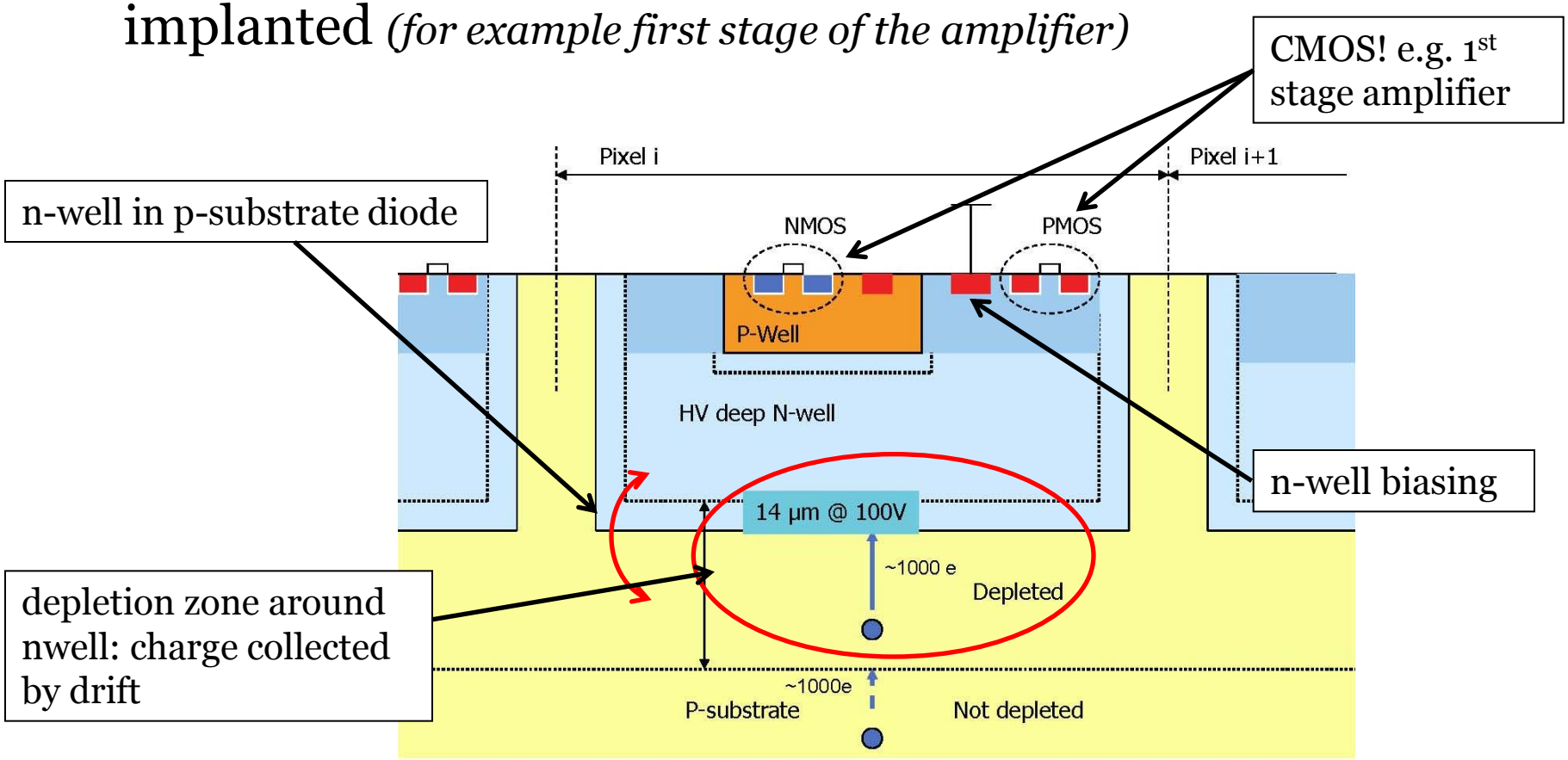
- Default: Double- sided

Si-strips but could be CMOS !

- ~200 m² silicon
- 2300 10 Gb/s links

Sketch of HV-CMOS concept

- N-well in the P substrate where CMOS transistors are implanted *(for example first stage of the amplifier)*



Advantage of HVCMOS pixels

- Collection of charge by drift → rad-hardness /speed.
- Commercial processes in large 8in or 12in wafers → potentially much cheaper than custom sensors.
- Potential for cheap bonding process (capacitive coupling gluing → CCPD, oxide or Cu-Cu bonding).
- Potential for smaller pitch due to separation sensor+analog tier and digital tier (a la 3D!): dedicated digital IC or use available IC with sub-pixel coding in CMOS tier

  (explanations on sub-pixel encoding later in this talk)
- Thin depleted zone (15-100µm) reduce cluster size at large η (reduce data rate, enhance 2 tracks resolution, better rad-hard)

CMOS sensor implementations

Passive CMOS sensors	Active sensor + Digital chip	Active Sensor with standalone readout
• Study charge collection • Passive Sensor to hybrid detector • Possible cost advantage	• Hybrid detector for high hit rates • On-sensor Digital functionality like sub pixel encoding • CCPD hybrid detector	• Thin monolithic CMOS sensor (DMAPS) • Analog stage optimization • On-chip digital readout

- **Several concepts**:
  - **With digital tier**: For initial prototypes, FE-I4 digital tier is available, for final FE-RD53 (TSMC 65nm) will be suitable.
  - **Low occupancy layers** (outer pixel, even strips) can be made in one tier with classical column or periphery readout architecture reducing the cost for large areas → real monolithic concepts.

Use cases for CMOS pixels in ITK 2024

- Restricted here to pixel detector
- **Inner pixel** layers (R=3-6 cm). Strong radiation hardness demand to ~500 MRads. Use of FE-RD53 in 65nm technology with 50x50 um pixel size. Four CMOS 25x25 um sub-pixels with thickness <50 um? "à la 3D elect." → Higher granularity!

- **Outer pixel layers** R> 15 cm. ~100 MRads. Use FE-Ix digital tier with HVCMOS pixels 50x250 um or smaller. Low cost bonding (gluing or C4 bumps) mandatory for cost reasons.
- **Outer pixel layers** R>15 cm. ~100 MRads. Use Full monolithic CMOS chip with classical column readout . Simpler modules, cheaper technology…

Pixel and Strip CMOS RD

- Weekly meeting organized from 08.11.2011.
- Started as Bonn-Berkeley-CERN-CPPM-Geneva-Heidelberg collaboration.
- CPIX → Chairs S. Rozanov / N. Wermes.
- Number of institutes currently involved: ~15-20 + strips, Karlsruhe-Berkeley-Bonn-CERN-Geneva-CPPM-Gottingen-Prague-IRFU-Glasgow-Oxford-Liverpool-INFN-Genova-Milan-SLAC-UCSC-…
- Many prototypes produced!

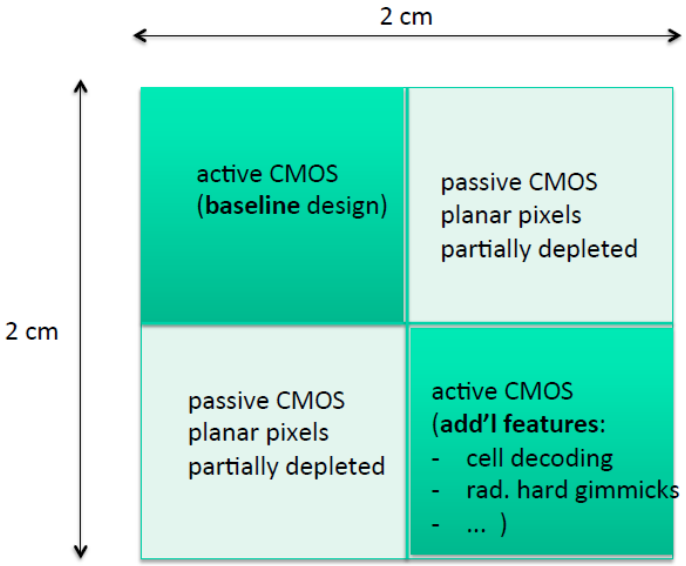
.

- In this context: "CMOS demonstrator task force" end 2014 **→ large size demonstrators.**

Goals for pixels: 2015/6

- Large area demonstrator for 2015/6: HVHR-CMOS capacitively coupled to FE-I4B. Need to demonstrate:
  - Operate **1×1 or full size 2×2 cm²** demonstrator.
  - Low noise (**<1% pixels masked**).
  - MIP **>99 % detection efficiency**.
  - Limited radiation hardness (**~100 Mrad, ~10.^{15} n_{eq}.cm^{-2}**).
  - Glue **coupling** (but bump-bonding explored in //).
  - Module: **Wire-bonds**.
  - **Granularity**: conservative 50×250 µm² or more aggressive 33×125 µm² .
  - **Depleted zone of order 100 µm** or less.

Demonstrator Task Force 2015



- FE-I4 size, with FE-I4 like pixels ($50 \times 250 \mu m^2$).
- Different types of sensor (passive / active baseline / active aggressive).
- For easier characterization, readout to be also provided with no FE-I4 attached.
- ATLAS ITK TDR.

- Decide on 2 (max. 3) technologies for demonstrator.

Demonstrator needed to be:

- Based on first prototypes.
- Survey of available processes + TCAD simulations of CMOS sensors.
- Signal and efficiency: High interest in HR processes.
- Coupling: AC or DC. Investigate TSV (lower priority).
- Irradiation: Electronics rad-hardness, charge collection efficiency → Xrays / neutrons / protons.
- Test system development.

CMOS demonstrator program thus far

from N. Wermes 09/05/2016

Technology	comments	Groups involved in design (D) & characterization	prototypes	demonstra-tor	monolithic
AMS 350/180 nm HV, >10 Ωcm	3-well process extensive tests	Karlsruhe (D), GVA, Liverpool (D), CPPM, Glasgow, Oxford, Barcelona (D), BN, CERN,	✓ CCPDv1 – v4 (180nm) + FE-I4	✓ H35_DEMO 350 nm (back 1/2016)	H35_DEMO has monolithic part
Global Foundry 130 nm HR: 3 kΩcm	huge vendor	CPPM (D), Karlsruhe (D), Geneva, Bonn, CERN	✓ HV2FEI4_GF		
Tower Jazz 180 nm, 1-3 kΩcm, epi	little dedicated attention so far	Bonn (D), Strasbourg (D)	✓ ? Pegasus_1&2 stand alone, monolithic	ALPIDE developments	
ESPROS 150 nm HR: 2 kΩcm	back contact in process, generic design not for LHC	Bonn (D), Prague (D)	✓ EPCB01, EPCB02 stand alone		
XFAB 130 nm 0.1 – 1 kΩ SOI	**SOI technology**	Bonn (D), CERN CPPM	✓ XTB01, XTB01	planned ?!	planned ?!
Toshiba 130 nm 3 kΩcm	designs not yet thoroughly tested	Bonn (D)	✓ TSB01		
LFoundry 130 nm 2-3 kΩcm	extensive tests	Bonn (D), CPPM (D), IRFU (D) SLAC (D), CERN, Glasgow	✓ CCPD_LF CCPD_LF + FI-I4	✓ CCPD (CPPM, IRFU, Bonn) (subm. Feb. 16)	MONOPIX_01 **(5/2016)** (Bonn, CPPM, IRFU) COOL_01 (SLAC)
ST-M (BCD8) 160 nm selectable kΩcm	bipolar+CMOS+ DMOS epi selectable	INFN Milano (D), Genova, Bologna, IIT Mandi	✓ KC53AB Testchip	planned TPM1	

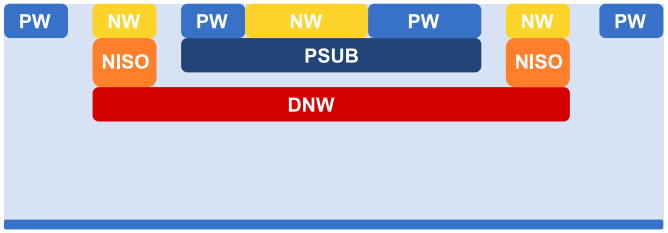
Demonstrator in LF technology

Background

- Team: Bonn/CPPM pursue long standing collaboration → HV/HR-CMOS LF since ~2014. IRFU has joined forces more recently on this topic (2015).
- **LFOUNDRY technology & projects**

LFoundry CMOS3E technology:

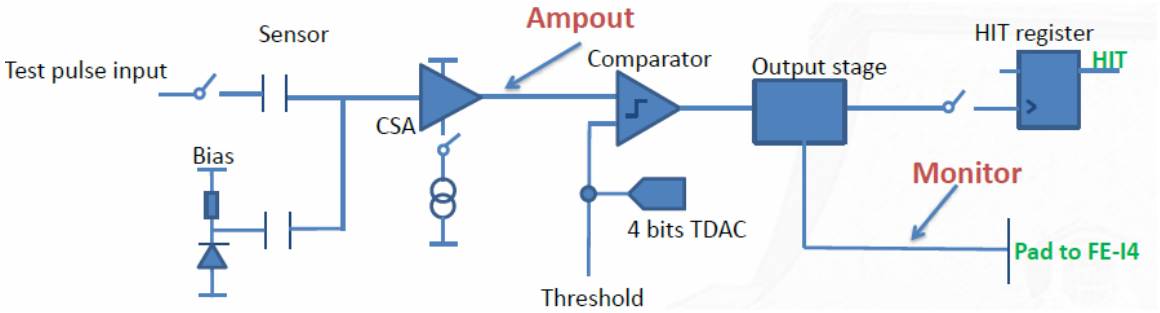
- 150nm CMOS (Avezzano, Italy)
- 2kΩcm p-type bulk
- Deep NWell available in real triple-well process
- HV process
- Thinning and back size metallization possible
- MLM3 (25.840mm x 9.505mm)



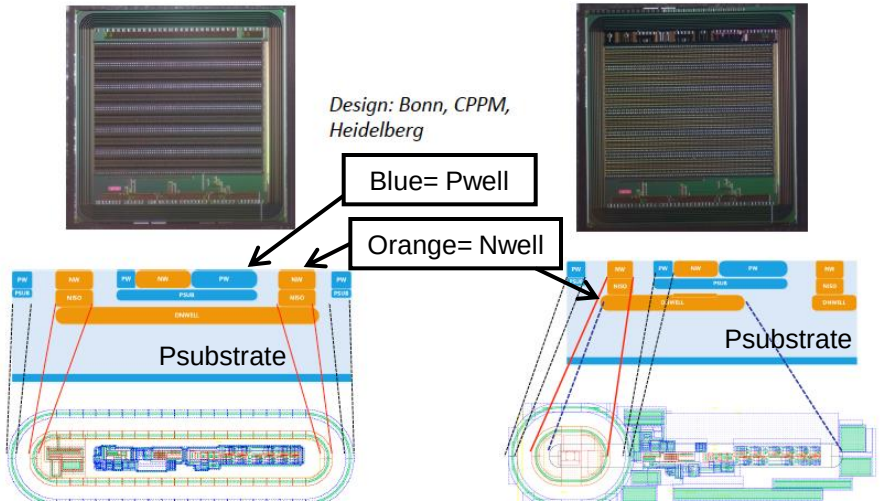
LFoundry Projects

- CCPD-LF VA chip : 5 x 5 mm² (Bonn, CPPM,KIT) submitted july 2015
- CCPD-LF VB chip : 5 x 5 mm² (Bonn, CPPM,KIT) submitted july 2015
- LFCPIX VA chip : 10 x 10 mm² (Bonn, CPPM, IRFU) submitted Feb 2016
- LFCPIX VB chip : 10 x 10 mm² (Bonn, CPPM, IRFU) submitted Feb 2016
- LF_MONOPIX_01 chip : 10 x 10 mm² (Bonn, CPPM, IRFU) submission April 2016
- COOL 1 chip : 12 x 10 mm² (SLAC, UCSC, KIT) submission April 2016

LF VA/VB 2015 version

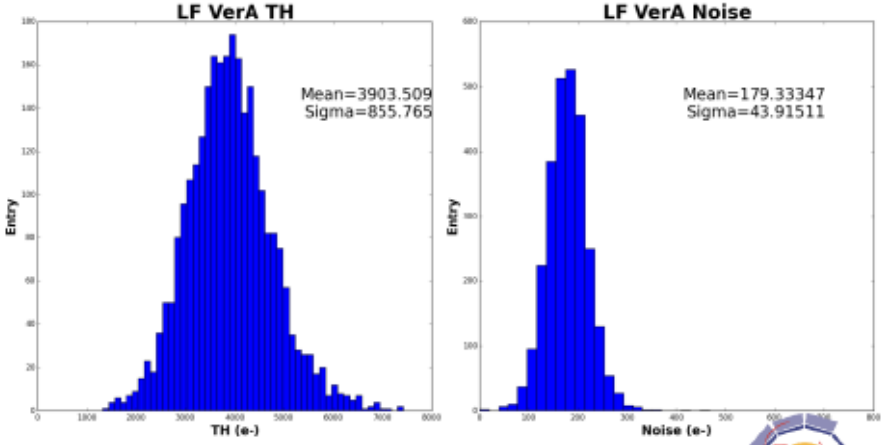


- **CCPD LF VA**
  - CMOS inside collection electrode
  - Test structures: NMOS and PMOS transistors
- **CCPD LF VB**
  - Smaller collection electrode
  - Test structure: diodes

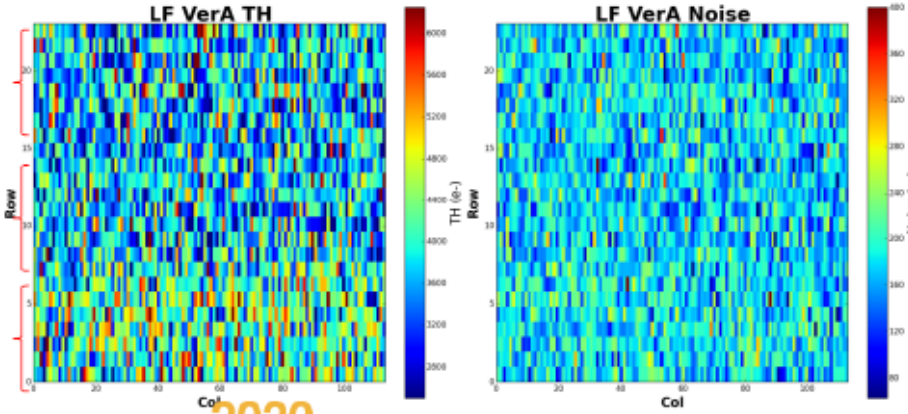


CCPD-LF irradiated to 100Mrads protons beam

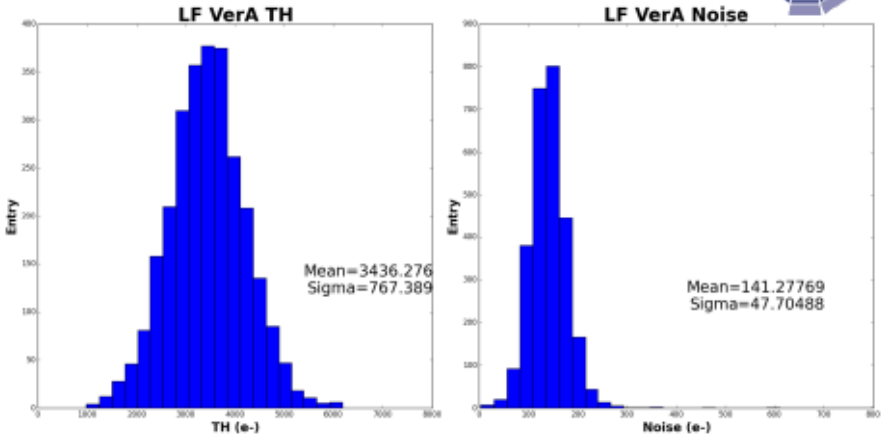
5 MRads



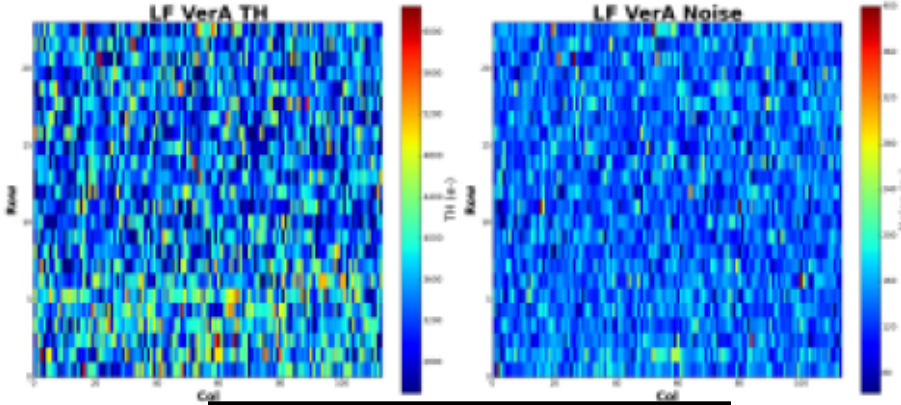
5 MRads



100 MRads



100 MRads



AIDA 2020

Jian Liu (CPPM/Shandong)

The pixels electrical parameters not really affected by the protons irradiation (10-20% variations)

LFoundry (first submision results)

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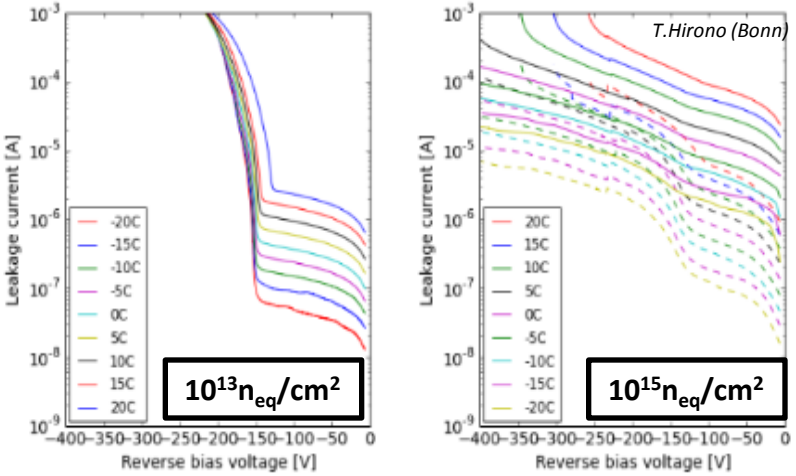
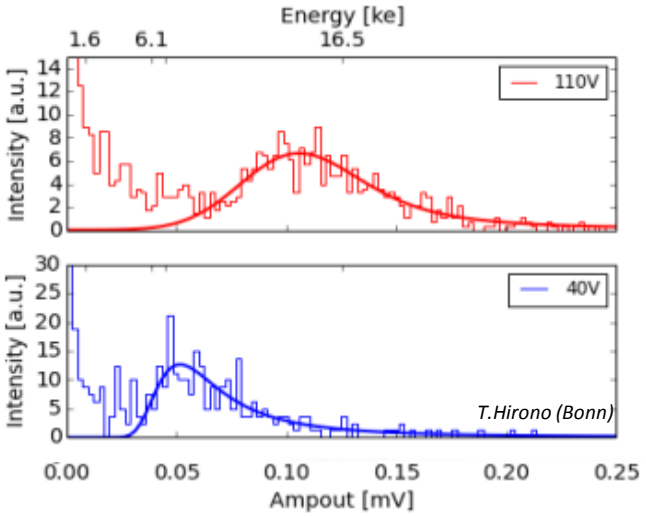
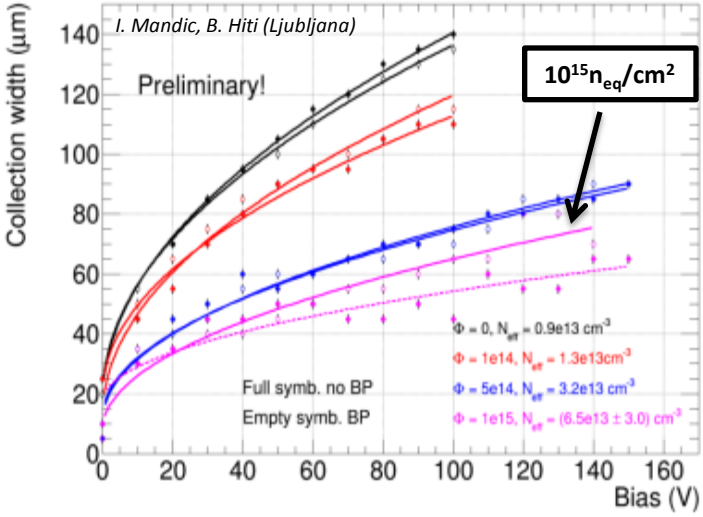
Sensor reverse current



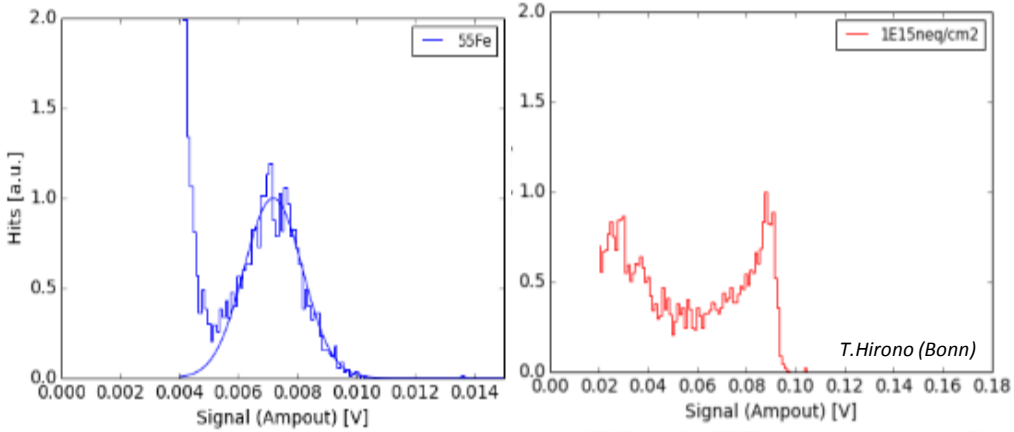
MIP (3.2 GeV) spectrum (before radiation)



Collection width (edge-TCT)



Sepctrum of ^{55}Fe and ^{241}Am after $10^{15}n_{eq}/cm^2$



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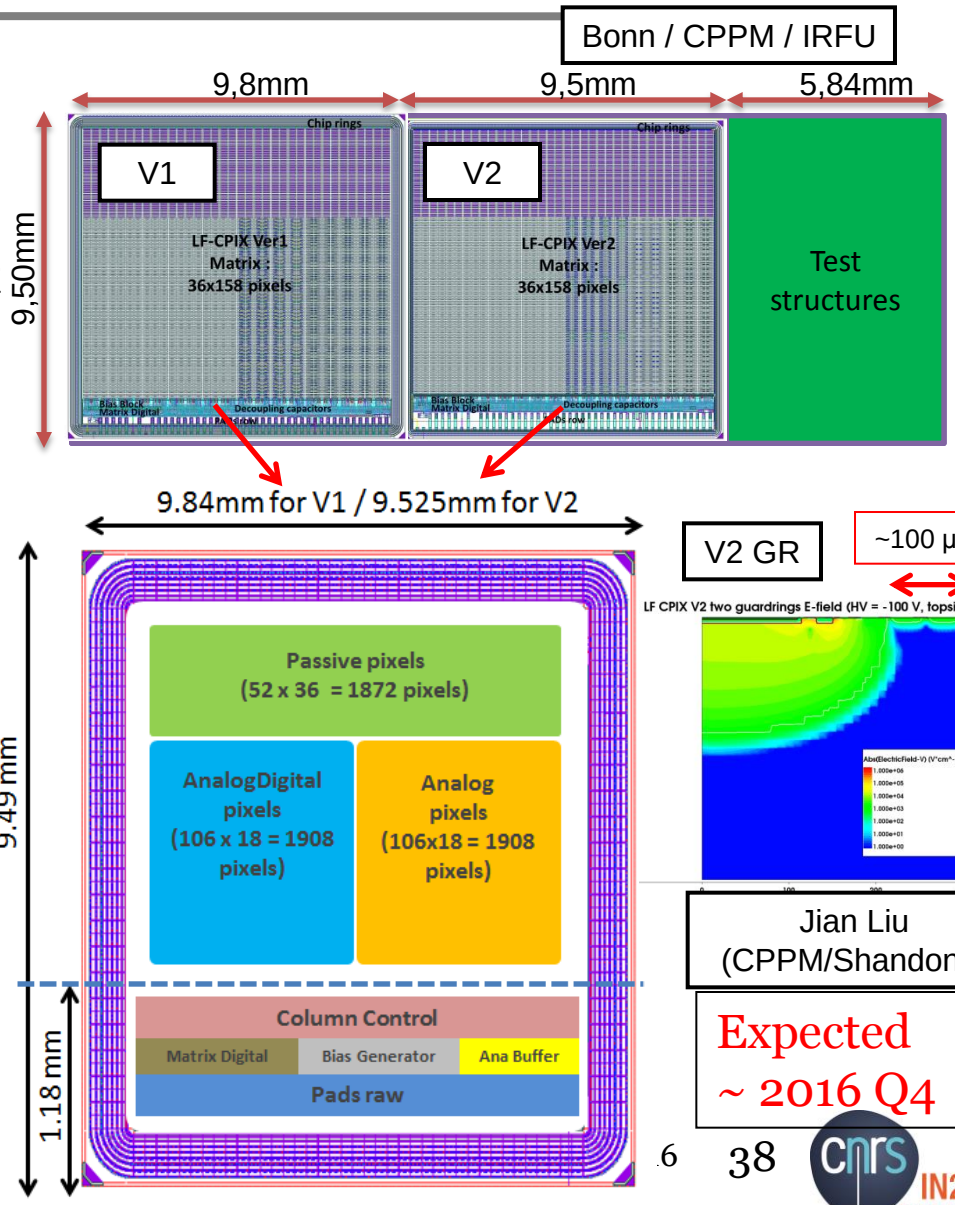
10×10 mm² demonstrator

- Feb. 2016: MLM3.
- V2: V1 + new guard ring strategy.

Bottom matrix: Col. ctrl, bias gene., analog buff., glob. config./SR readout

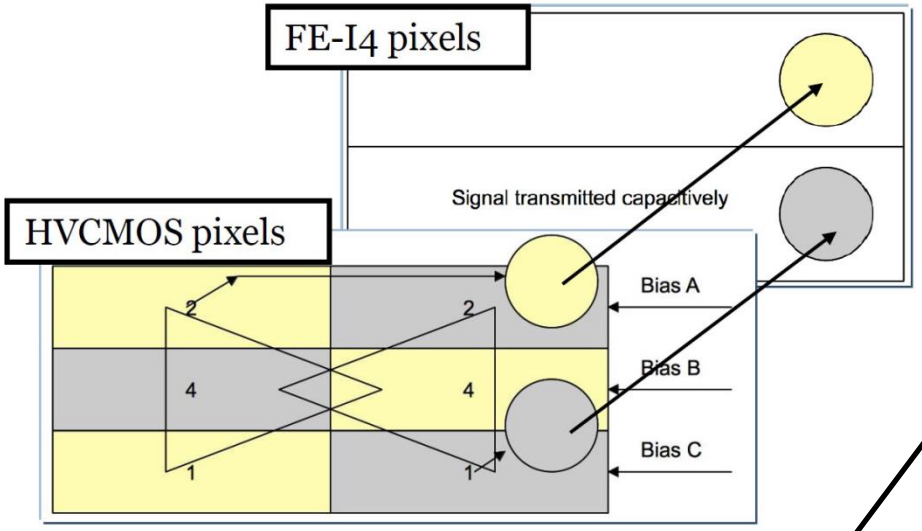
Pixel Matrix :

- Pixel 250µm×50µm (FEI4-like)
- All pixels have bond pad to FEI4
- 3 sub-matrices :
  - **Passive**: only DNwell sense diode
  - **AnalogDigital**: à la LF VA, 4 flavors (different diode bias, diff. input transistors NMOS and PMOS).
  - **Analog**: preamp with complementary input CMOS, and 8 flavors (diode polarization, outputs "linear", "saturated" or "digital"...).
  - Preamp out / hitOR available for all pix

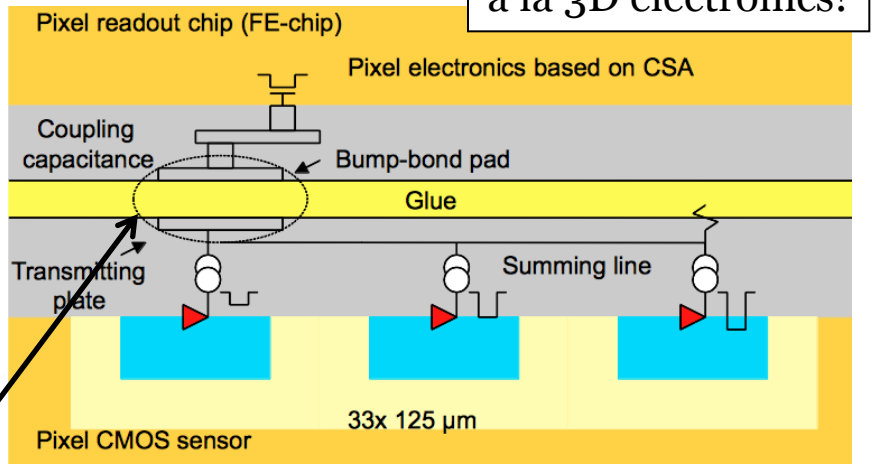


Readout -with larger pixels-

- Combine 3 pixels together to fit one FE-I4 pixel (50×250μm²), with HVCMOS pixels encoded by pulse height.

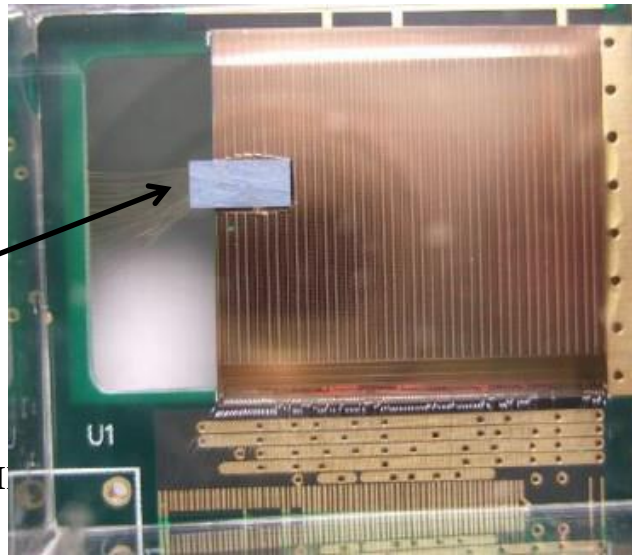


à la 3D electronics!



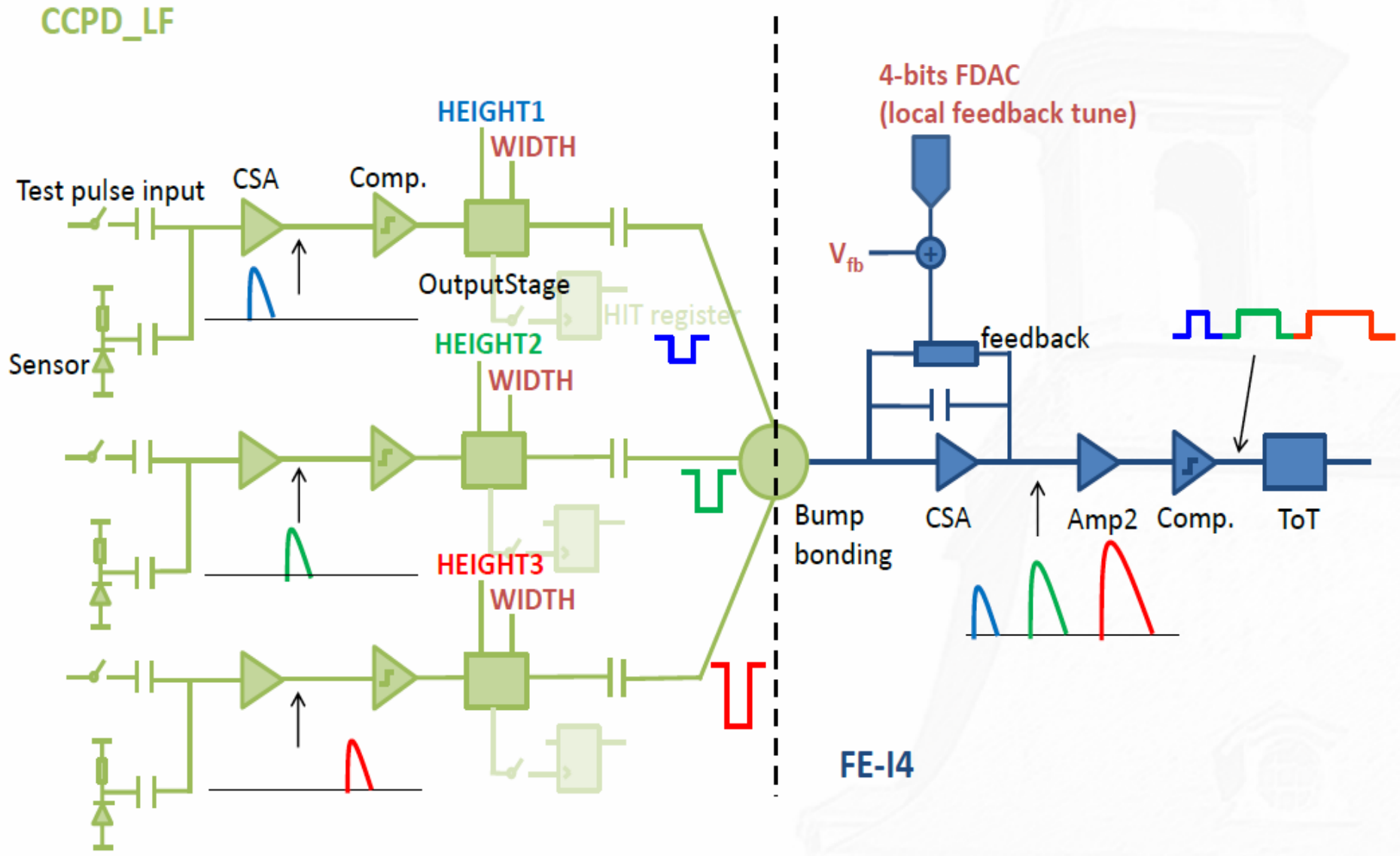
- Capacitive coupling OK: gluing!

(perspective to avoid bump-bonding?)

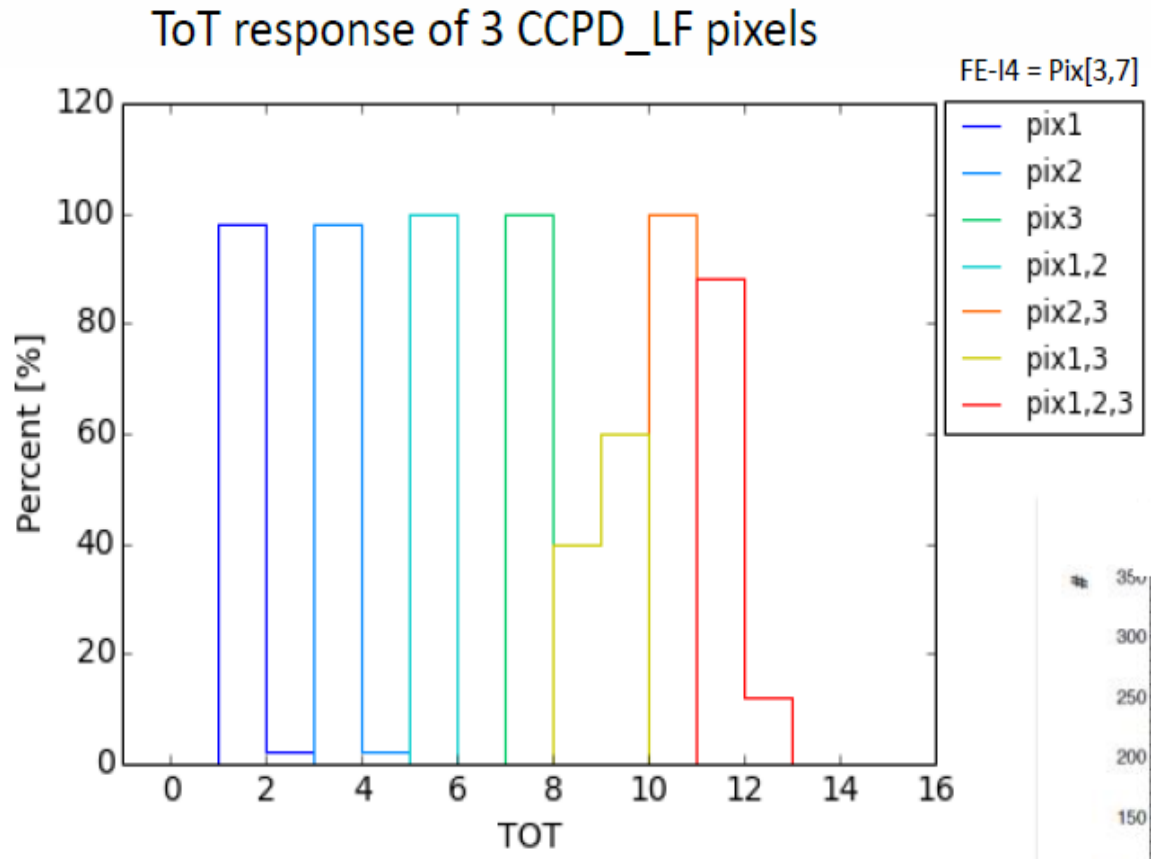


The tiny HV2FEI4p1 prototype glued on the large FE-I4

Readout of CCPD_LF and FEI4

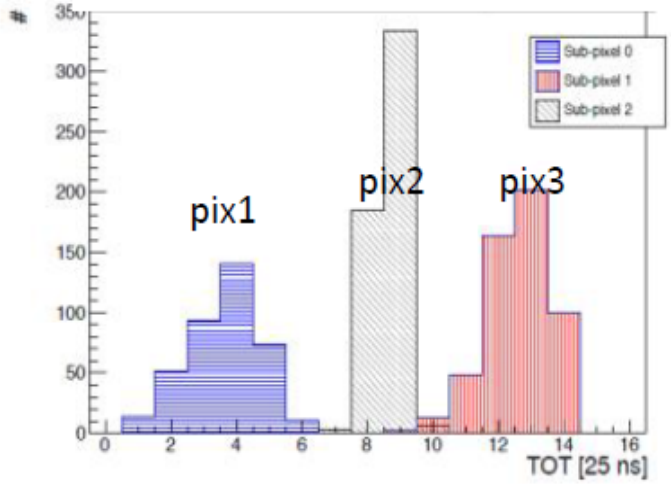


ToT dispersion of 1 “good” FE-I4 pixel (test pulse injection)



- Subpixel encoding works in some pixels
- Dispersion of ToT can be tuned to be ~2ToT

cf. ToT response of 3 HV2FEI4 pixels



M. Backhause Thesis (2014)

ToT value of a FE-I4 pixel (3.2GeV electron)

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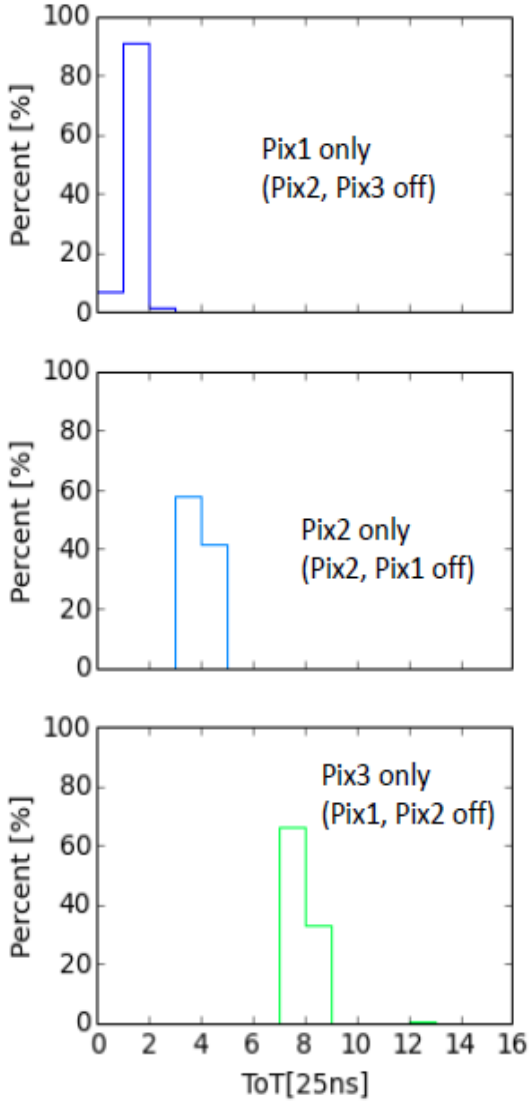
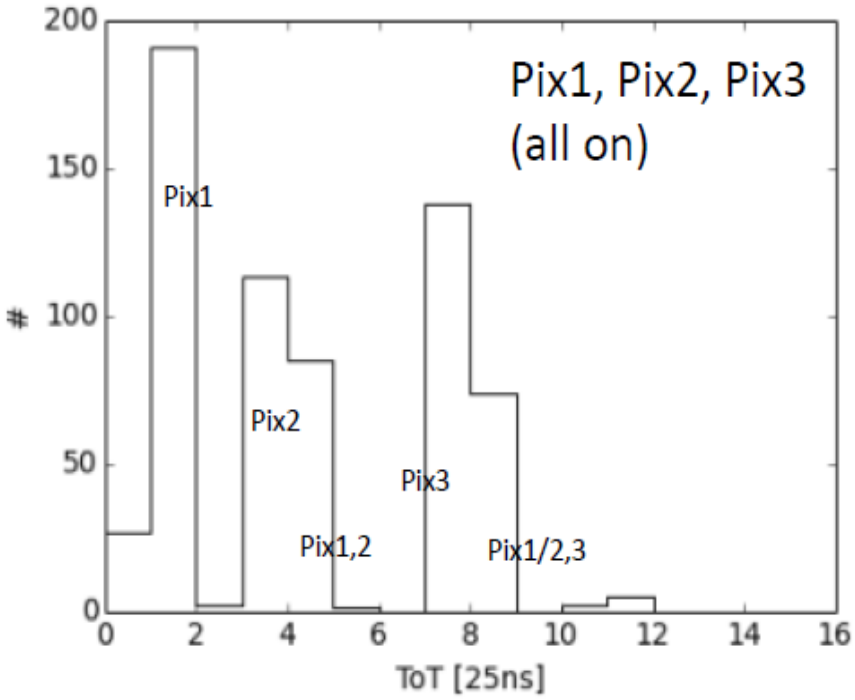
ToT response of a single FEI4 pix



ToT response of a single FEI4 pix

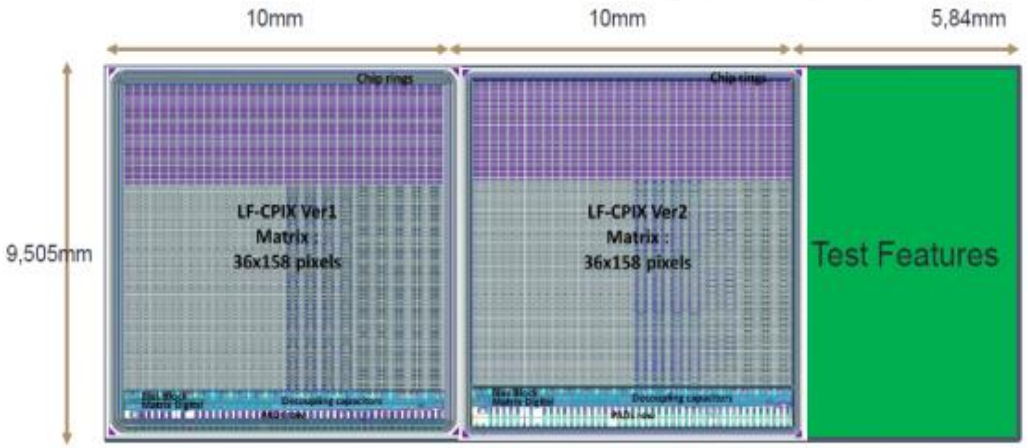


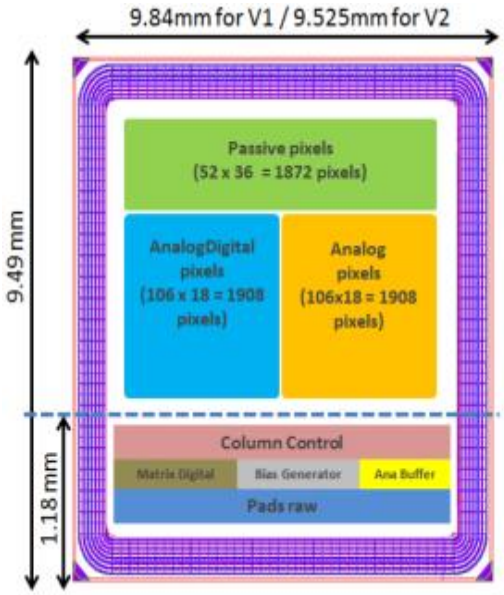
- Sub-pixel encoding works for real beam
- Detailed analysis is on-going

LF-CPIX Demonstrator + Fully Monolithic

LF-CPIX :

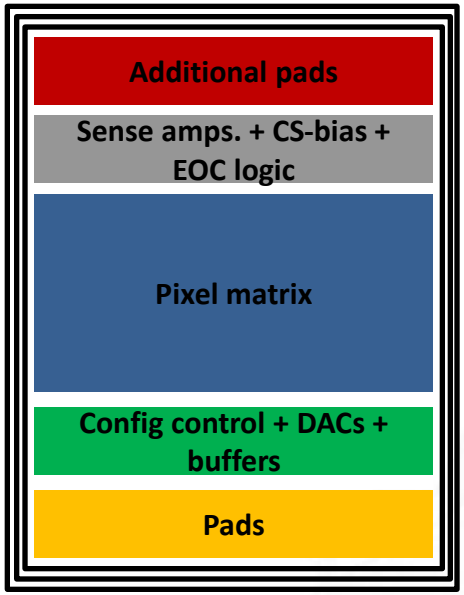
- 150nm CMOS (Avezzano, Italy)
- 2kΩcm p-type bulk
- Deep N-Well/P-Well available
- HV process
- CPPM + IRFU/CEA + Bonn

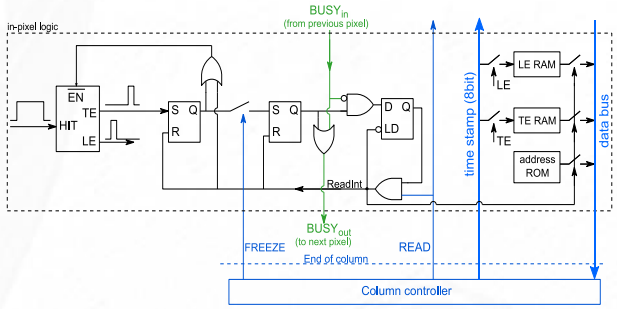




submitted 03/2016

LF-Monopix-01 Fully Monolithic





submission 05/2016

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2016+

- Module concept (coupling, TSV, etc…), study mechanics (power, cooling, etc…)
- Increased radiation hardness.
- Study efficiency at various test-beams (DESY, SLAC, CERN…).

- Now:
  - TCAD simulations → sensor designs.
  - Simulations Geant4-based. Parameters: granularity, sensor thickness , detector arrangement.
    - Two different goals:

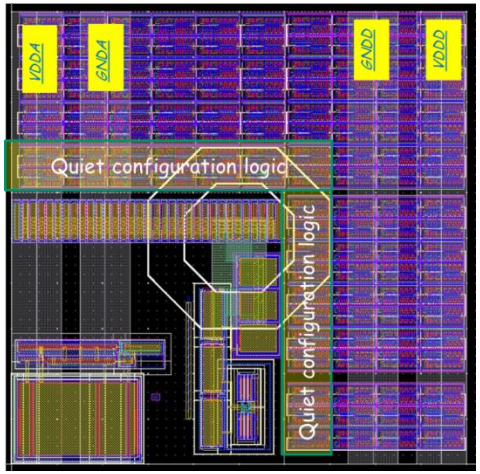
      1- Low cost, **large scale**, high yield. → outer layers

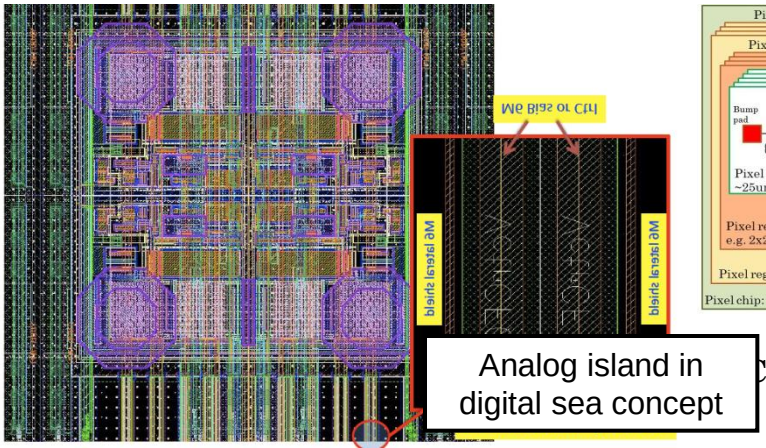
      2- **Ultimate performance** → small granularity!

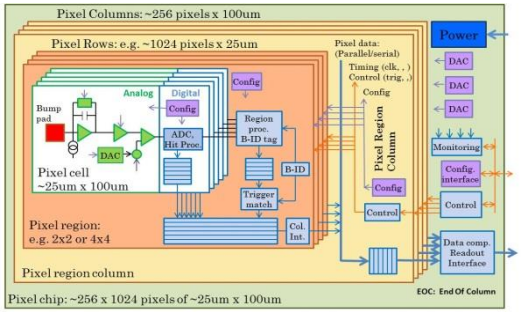
Related activities : RD53

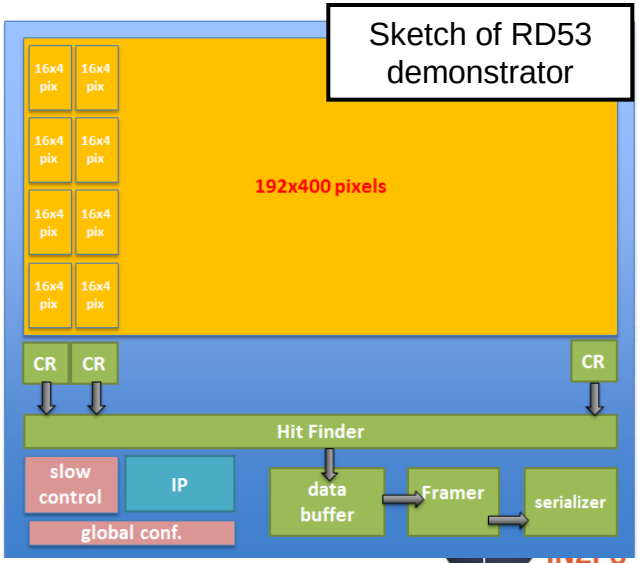
- RD from CERN since 2012. Transverse to ATLAS / CMS.
- ~20+ institutes / ~100+ collaborators.
  - Baseline TSMC 65nm.
  - Small pixels: 50×50 µm².
  - Large chip: 2× 2cm² / ~1 billion transistors.
  - High hit rates: ~2 GHz/cm².
  - High radiation: 0.5 GRad / ~10^{16} n_{eq}.cm^{-2}.
- Big demonstrator for end of year.

http://rd53.web.cern.ch/RD53/







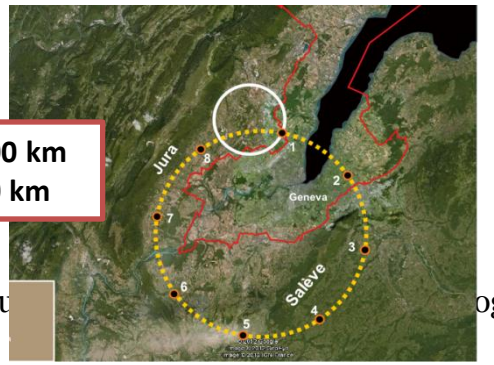


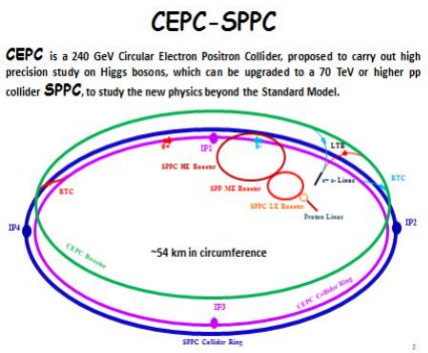
CMOS technology, Marlon Barbero,

Perspectives for HV CMOS

- All environments where low cost, large area, high resolution, fast readout and tolerance to radiation matter:
  - Synchrotron radiation imaging.
  - Medical imaging during proton therapy (tracking protons in pCT -proton Computed Tomography-).
  - …
- Technology transfer, experience of the group of Prof. Morel in CPPM (uses hybrid pixel technology for medical imaging)
- Technology transfer, spin-off from CPPM (uses hybrid pixel technology for synchrotrons applications).
- FCC or SppC.

15 T ⇒ 100 TeV in 100 km
20 T ⇒ 100 TeV in 80 km





Conclusion

- ATLAS: A rich physics program for many years, needs improved tracker → ITk project!
- CMOS Demonstrator Task Force → Large scale demonstrator available (AMS) or submitted (LF):

  → Waiting for these large size prototypes and extensive testing
- In concert with ATLAS/CMS RD53 electronics in TSMC 65nm.
- → New perspectives for better tracking at HL-LHC!

What to expect from ATLAS in coming months / years?

Conclusion

- ATLAS: A rich physics program for many years, needs improved tracker → ITk project!
- CMOS Demonstrator Task Force → Large scale demonstrator available (AMS) or submitted (LF):

  → Waiting for these large size prototypes and extensive testing
- In concert with ATLAS/CMS RD53 electronics in TSMC 65nm.
- → New perspectives for better tracking at HL-LHC!

More studies of Higgs boson, Beyond the Standard Model theories -SUSY- and expect the unexpected!