The phase 2 upgrade to the ATLAS tracker at CERN and the new HV/HR CMOS technology:

The LHC Phase II upgrade will lead to a significant increase in luminosity in year 2024, to pursue the ambitious physics goals of the LHC program (Higgs boson characterization, Beyond the Standard Model physics, etc…). Operating at a nominal leveled instantaneous luminosity of 5×10^{34} $cm^{-2}s^{-1}$ will be a challenge to the detectors and in particular to ATLAS innermost tracker. The new Phase II tracker requires enhanced granularity, reduced material budget and increased radiation hardness to all components. As the silicon area for a new tracker now amounts to hundreds of square meters, including a pixel detector area of order ~$10m^2$, the price tag on any used technology is a very relevant factor. In this talk, I will introduce the general context of the ATLAS Phase II program focusing on the Phase II tracker upgrade. A new technology called High Voltage / High Resistivity CMOS could bring some very interesting benefits in the design of a tracker. An international collaboration studies this new concept with the involvement of various vendors. I will describe here highlight results concerning this technology.