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# Development of the ABCStar ASIC for the ATLAS Silicon Strip Upgrade

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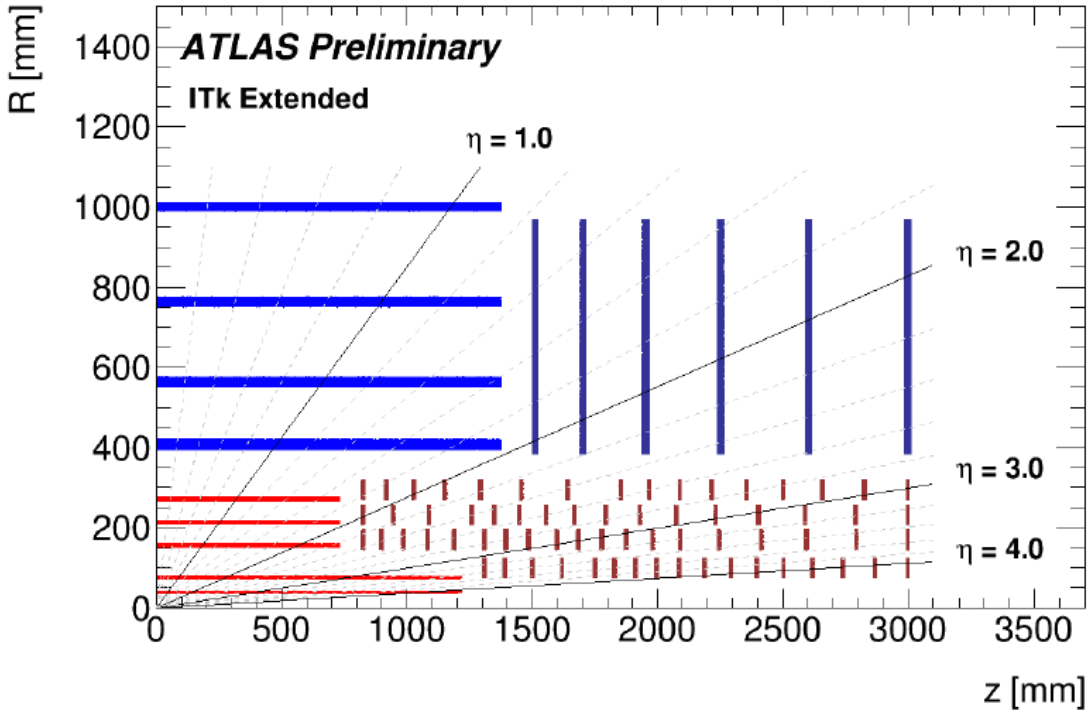
On behalf of the ITk Strip ASICs collaboration

# ITk Phase II upgrade

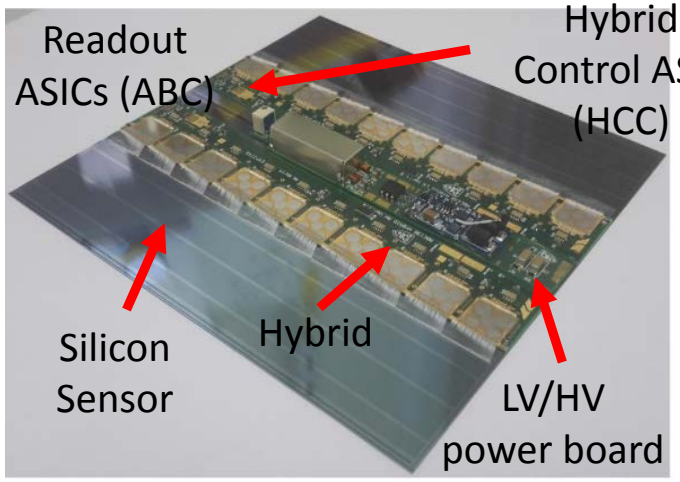



- The Phase II upgrade of the ATLAS Inner Detector is now named the ITk(Inner Tracker)
- It will be an all-silicon detector made up of pixel detector and strip detector
- A very large increase in size and complexity for strip

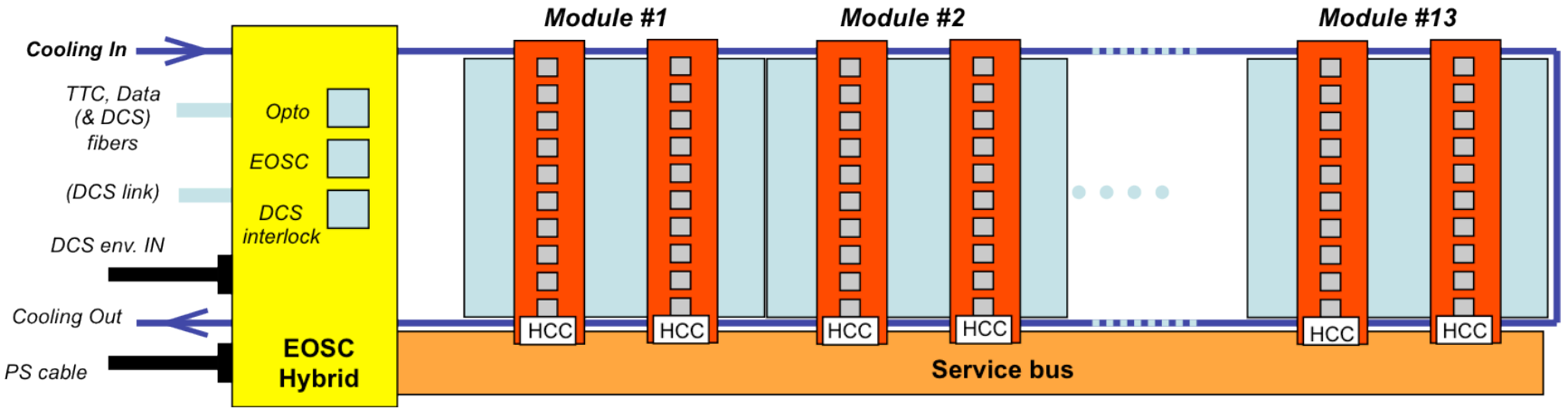
| The New ATLAS ITk Strip Tracker | | | | | | The Existing ATLAS SCT Tracker | | |
|---|---|---|---|---|---|---|---|---|
| Number of Full Length Double-Sided Staves | Number of Barrel Modules | Number of Double-Sided Petals | Number of End-Cap Modules | Number of Readout Channels | | Number of SCT Barrel Modules | Number of SCT End-Cap Modules | Number of Readout Channels |
| 196 | 10,976 | 384 | 6,912 | 60M | | 2,112 | 1,976 | 6.3M |

# Stave, Petal, Module concepts

- Barrel cylinders are segmented into staves
- End-cap disks are segmented into petals
- Module is the basic building block for stave and petal



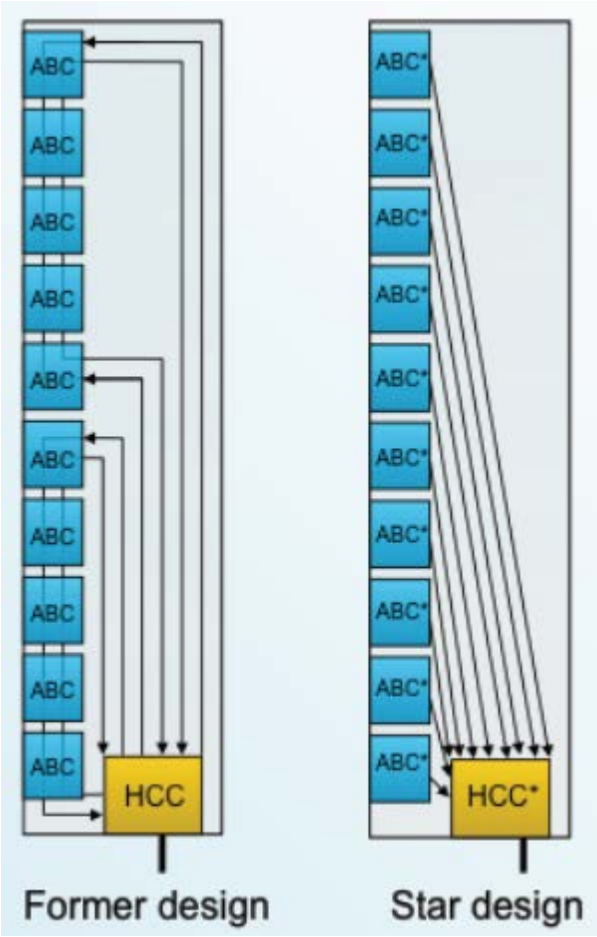

**Barrel Module with Short Strips**



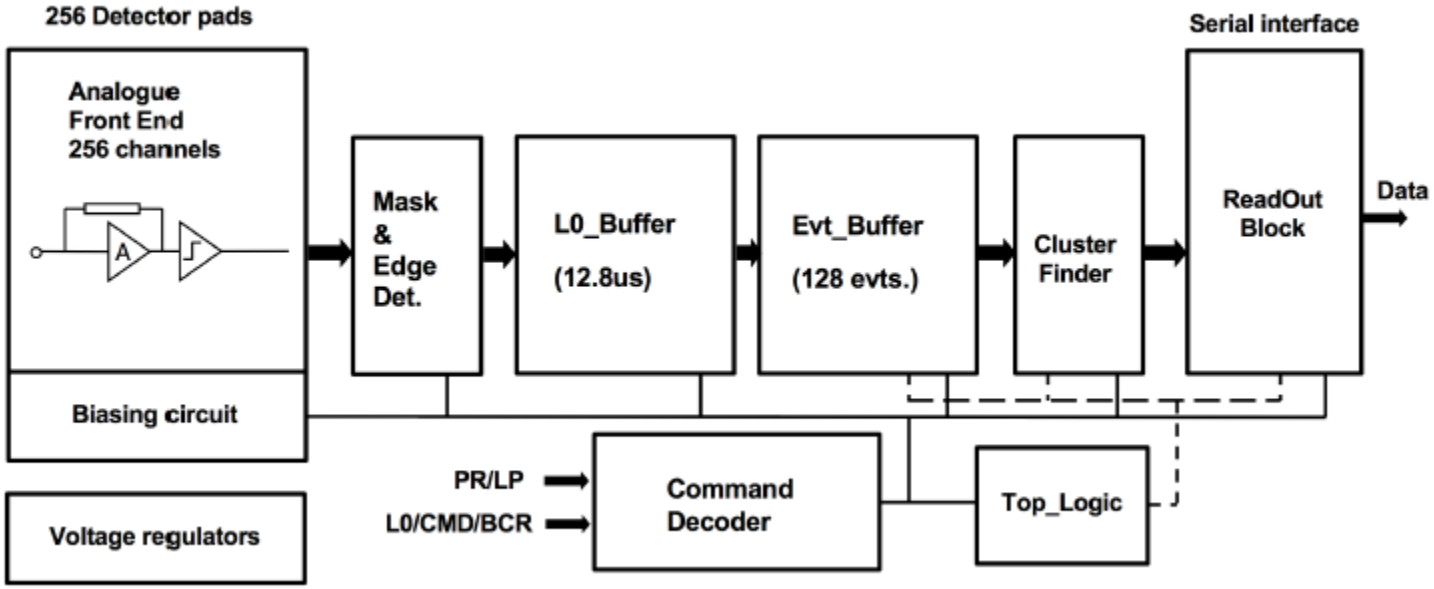

**Barrel stave with 13 modules**

# ABC130 to ABCStar

- From ABC130 to ABCStar
  - Change chip design to meet the requirement of increased trigger rate
  - Interface from ABCs to the HCC: Serial transfer of data to direct communication
- The ABCStar front-end ASIC
  - ABC--ATLAS Binary Chip
  - Star--Star readout with point to point connection

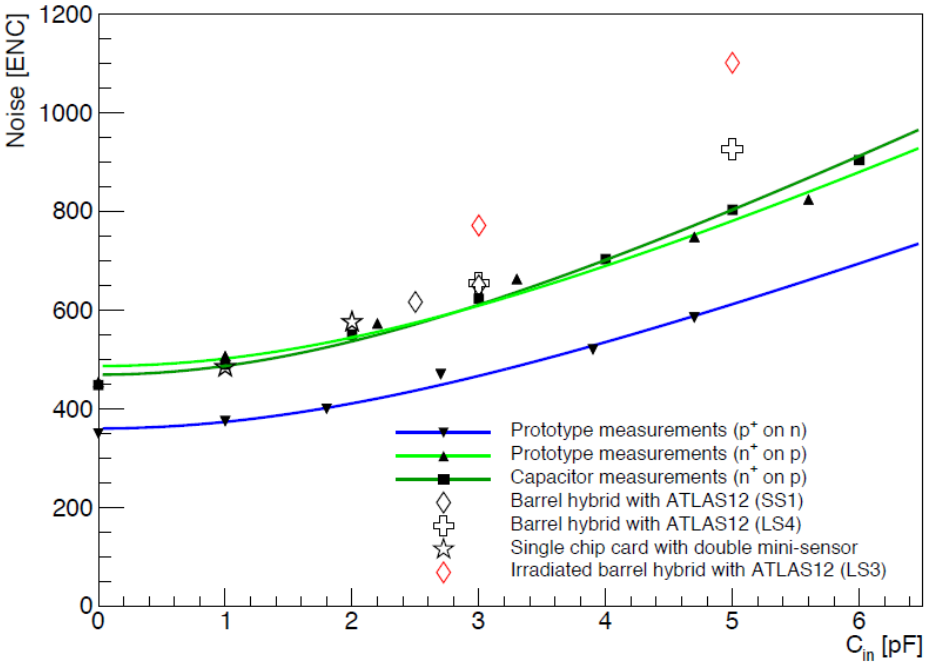


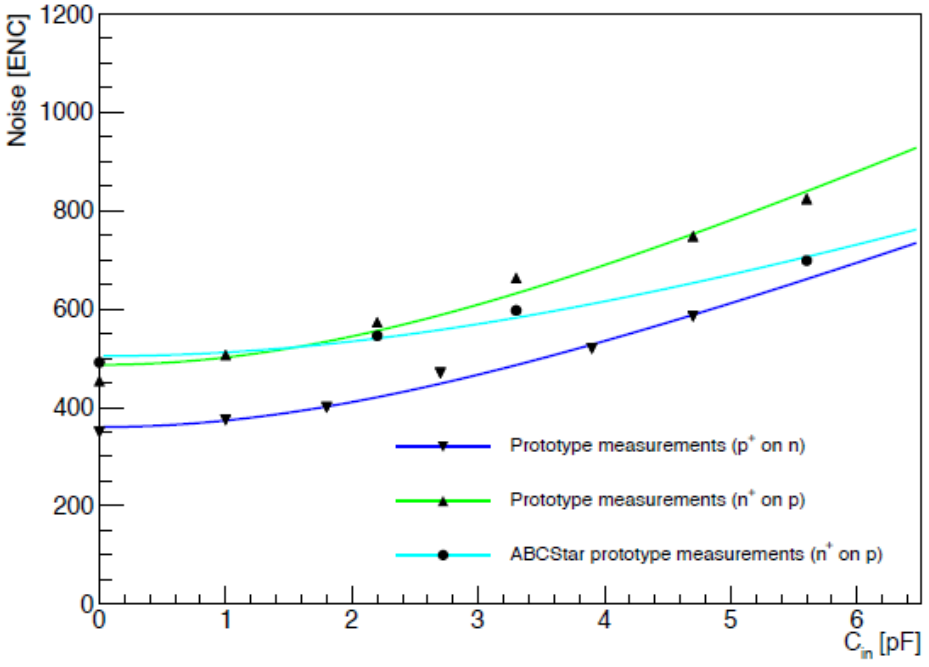
# ABCStar ASIC




- It uses the standard binary readout architecture
- Data path: amplifier, discriminator, input register block, pipeline, event buffer and a cluster algorithm to compress data for output
- It is being designed to support various trigger modes
- It will be built in GF130nm technology

# Front-end test and redesign

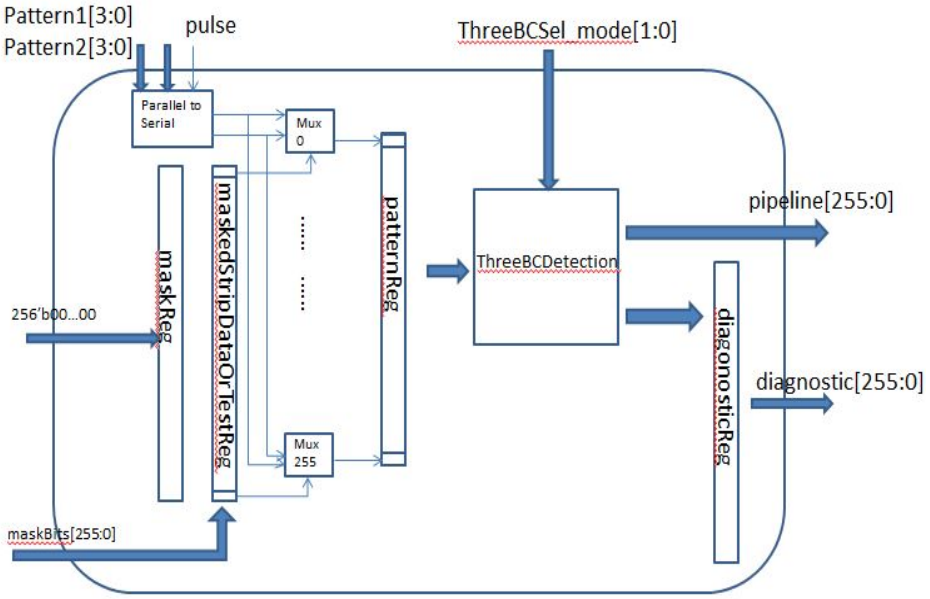



- A range of prototype: ABC130 front-end prototype, ABC130 single-chip test card, full barrel hybrid
- Connected to discrete capacitors: ENC for the prototype agrees well with hybrids and single chips
- Connected to sensors: noise increase due to strip resistance
- Noise increase for changed signal polarity → resistive feedback
- Excess noise after irradiation → Critical NMOS devices in enclosed geometry

# Input Registers block

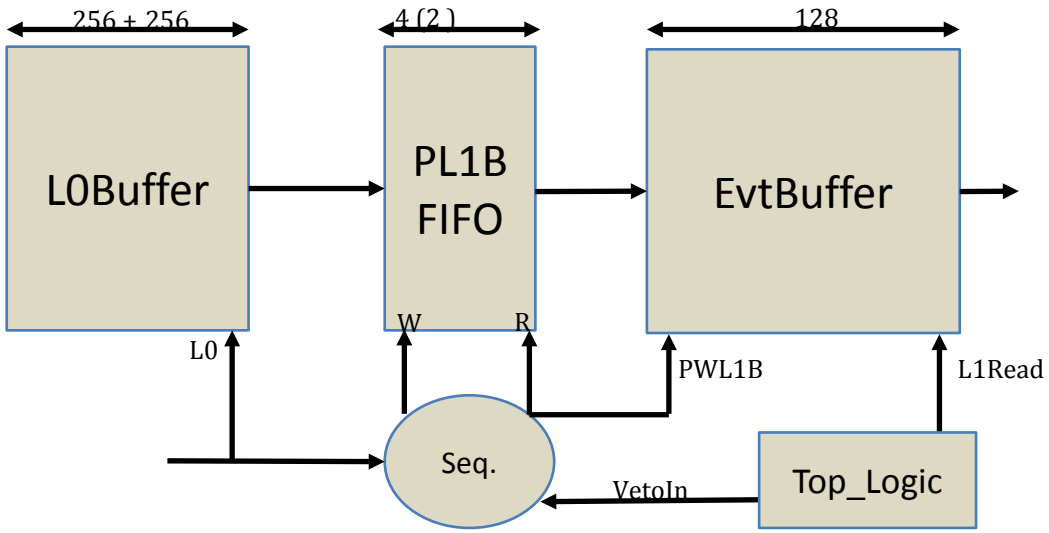
- Input register latches data with BC clock
- Mask/test registers for dual purpose
- Edge detection circuit with different selection criteria



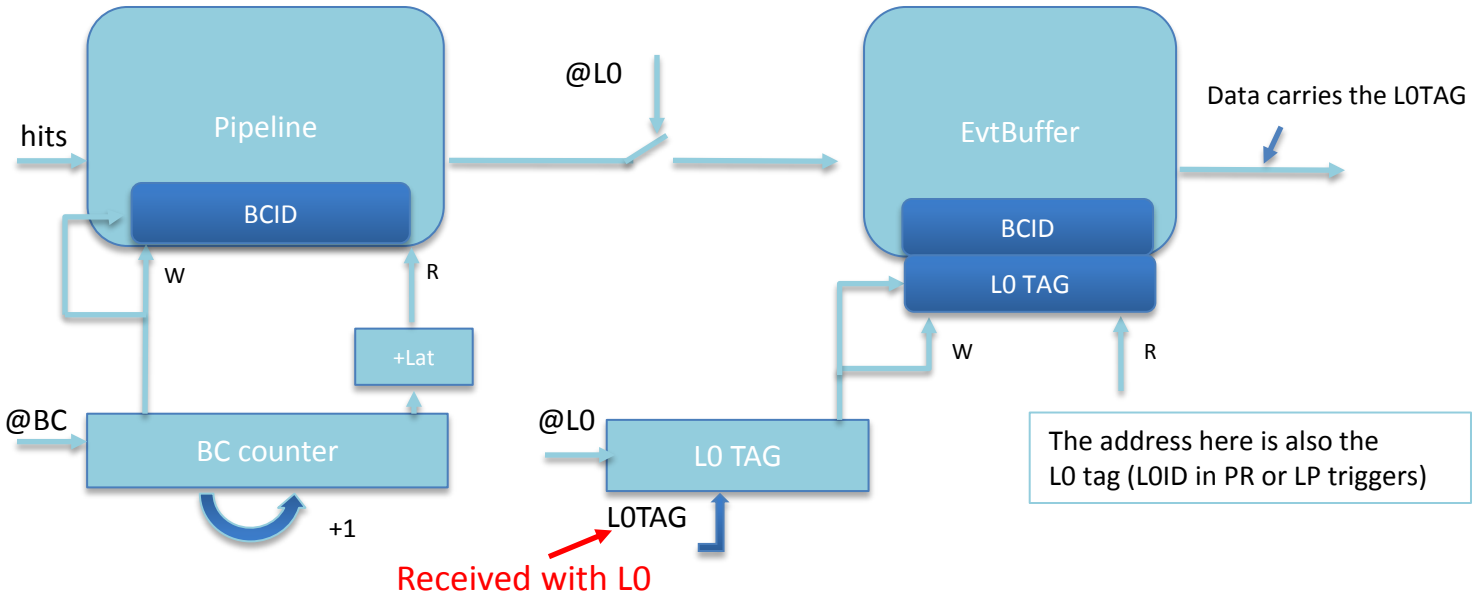

| Det_mode (1:0) | Name of Selection Criteria | Hit Pattern (Oldest data bit 1st on the left) | Usage |
|---|---|---|---|
| 00 | Hit | 1XX or X1X or XX1 | Detector alignment |
| 01 | Level | X1X | Normal Data Taking |
| 10 | Edge | 01X | Normal Data Taking |
| 11 | Clear | None | Special Mode |

# Two stage buffers

- The two stage buffers: Pipeline(L0Buffer) and EvtBuffer
- Basic memory IP: single port RAM
- Modification of buffer size
  - Pipeline(L0Buffer)extended to 512bit length
  - EvtBuffer reduced to 128bit length(128 events)
- Transfer 1 event per L0 from Pipeline to EvtBuffer(instead of 3)
- Intermediate FIFO to give the priority to EvtBuffer read operation, in case of consecutive L0s

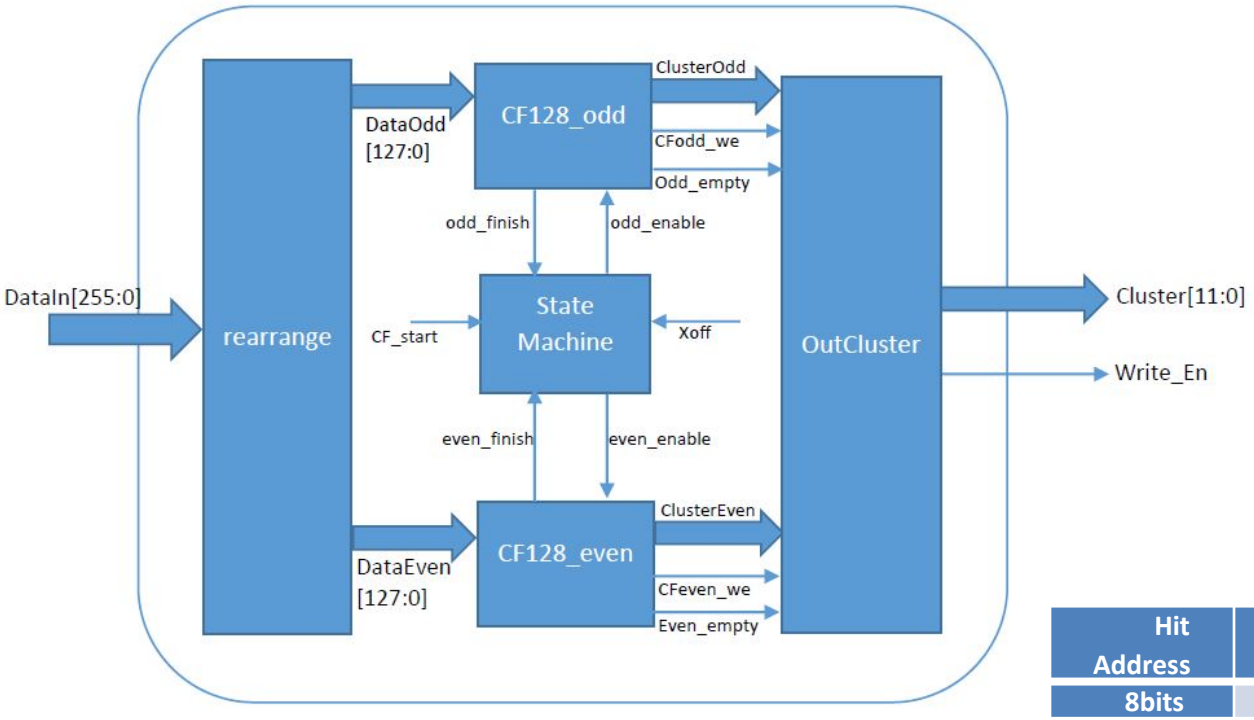


# L0 tag insertion




- The L0ID counter is very sensitive and require synchronization regularly
- We will employ new scheme--sending a L0tag with L0
- This helps to improve the reliability

# Cluster finder

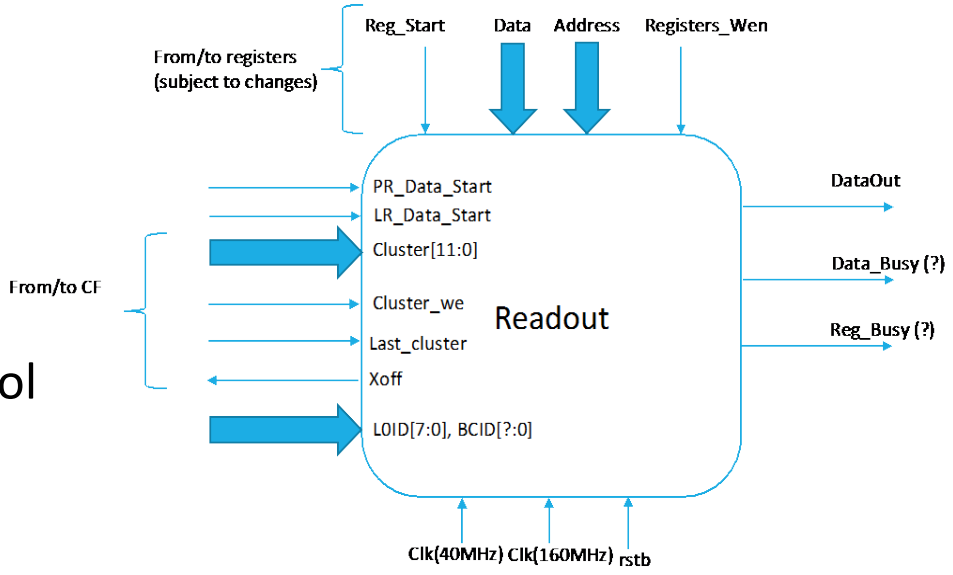


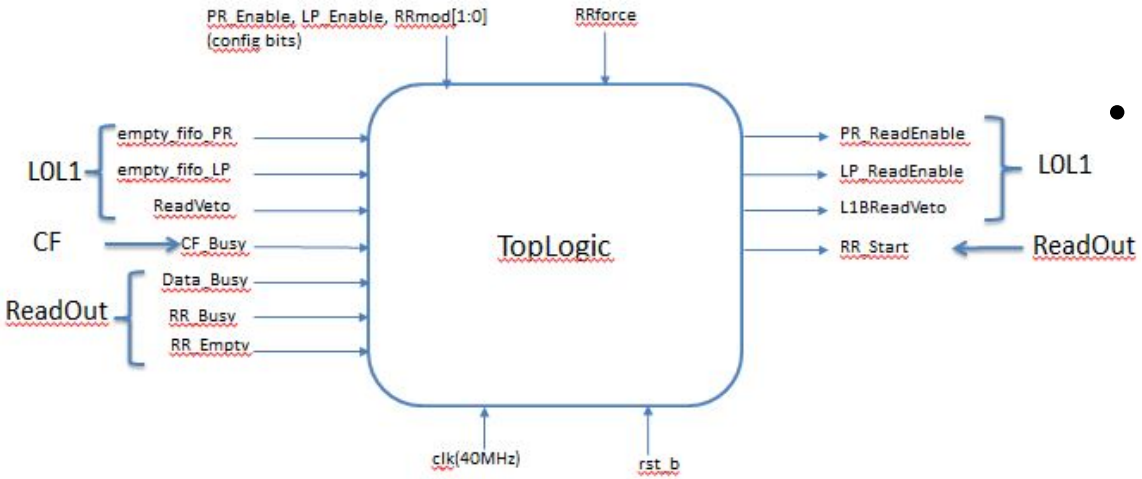

| Hit Address | Following 3 strip values | Last cluster |
|---|---|---|
| 8bits | 3bits | 1bit |

- Data reduction circuit, creating a cluster byte for channels found with hits
- The cluster finder takes in 256 bits of strip data and reports out 12 bit clusters at 40MHz

# Readout and TopLogic

- TopLogic
  - Sequencer for the control of EvtBuffer, ClusterFinder and ReadOut
  - Register readback control
  - PR/LP readout priority control




- Readout
  - Responsible for building data packets
  - A controller defines the order in which packets are formatted
  - Each packet is transmitted to the fast serializer

# Data formats and rates

- Packet framing

| Start Bits | Header | Payload | Trailer |
|---|---|---|---|
| 3 | 16 | 48 | 1 |

- Physics data header and payload

| TYP | L0ID | BCID |
|---|---|---|
| 4 | 8 | 4 |

| Last Cluster Flag | Cluster Address | Next Strips Pattern |
|---|---|---|
| 1 | 8 | 3 |

X 4 (max)

- Register readback packet header and payload

| TYP | Register Address | TBD |
|---|---|---|
| 4 | 8 | 4 |

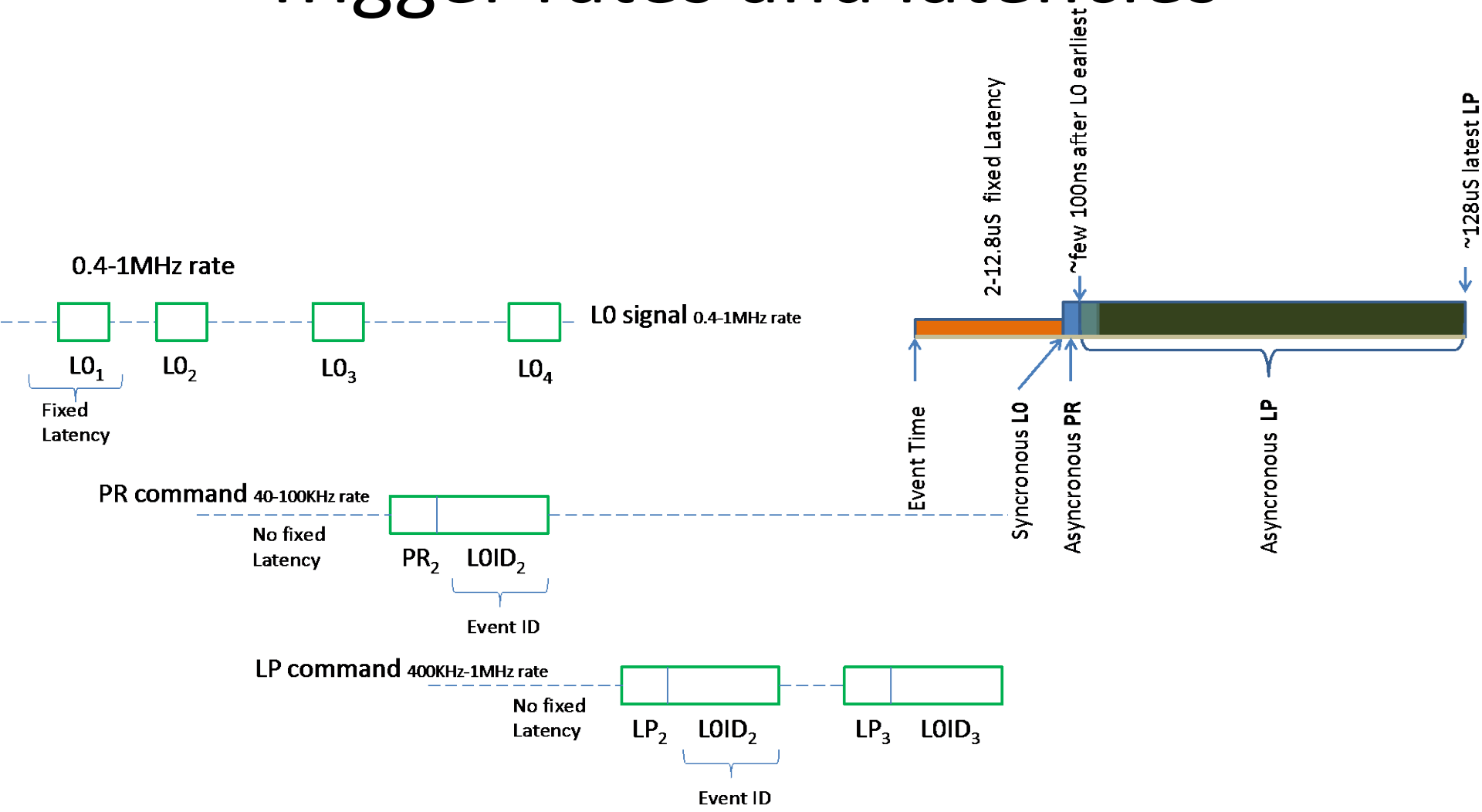
| Register Contents | Monitor Data |
|---|---|
| 32 | 16 |

- The output format is a variable length readout packet with maximum length of 68 bits
- The estimated average event size per chip is 2 to 3 clusters (therefore one 56 bits packet)
- The average data rate at the output of one ABCStar chip is 56 Mb/s
- 160Mb/s readout rate was rather chosen to reduce the transmission latency for L1-track

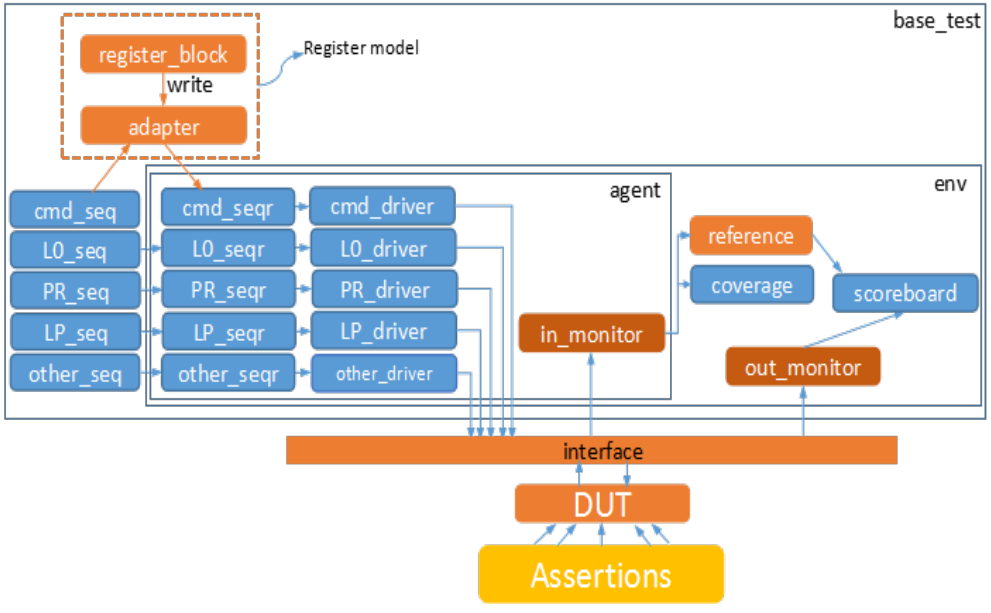
# Clock and control signals

| Name | Type | Description |
|---|---|---|
| RCLK | SLVS | 160MHz Clock input primarily intended for Data Readout |
| BC | SLVS | Beam Crossing Clock at 40MHz |
| L0_CMD/LCB 1) | SLVS | 80Mb/s, L0 Synchronous Trigger, CMD bits<br>(legacy mode of ABC130) |
| L0_CMD/LCB 2) | SLVS | 160Mb/s, L0 Synchronous Trigger, L0_tag, CMD and BCR bits<br>(6b/8b encoded frame, extending over 4BC) |
| LP_PR | SLVS | Physical line that receives the LP and PR triggers muxed at 80Mb/s |

# Trigger rates and latencies



# UVM setup for verification




| L0 | Lat. | LP | Lat. | PR | Lat. | Status |
|---|---|---|---|---|---|---|
| 1MHz Exponential | 6us | 400KHz Poisson | 12us | 100KHz Poisson | 12us | OK |
| 1MHz Exponential | 6us | 1MHz Poisson | 12us | No PR | | OK |
| 4MHz Exponential | 6us | 1MHz Poisson | 12us | No PR | | OK |
| 4MHz Exponential | 6us | 1MHz Poisson | 12us | 100KHz Poisson | 1.2us | OK |
| 4MHz Exponential | 6us | 600KHz Poisson | 12us | 400KHz Poisson | 100n s | OK |

- A top verification setup based on (UVM)Universal Verification Methodology was built for the current design of ABCStar.
  - Functional coverage with customized random stimulus
  - Result comparison with reference model through scoreboard
  - SystemVerilog assertions for validating key design features

to verify the current design under several possible trigger conditions

  - different rate, latency and distribution model of triggers

# Design options

- Power options for TID current bump mitigation
  - switch off the power of half of the pipeline in case of low L0 latency
  - extend the range of digital voltage regulator, lower voltage down to 1 volt for the digital part
- eFuse for chip identification
  - Adding an individual chip identifier programmed with eFuses (eFuses have to be burnt at the wafer test step)
- Analogue monitor of voltage and temperature
  - Adding an analogue monitor circuit like in the HCC to measure regulated VDDs, and temperature

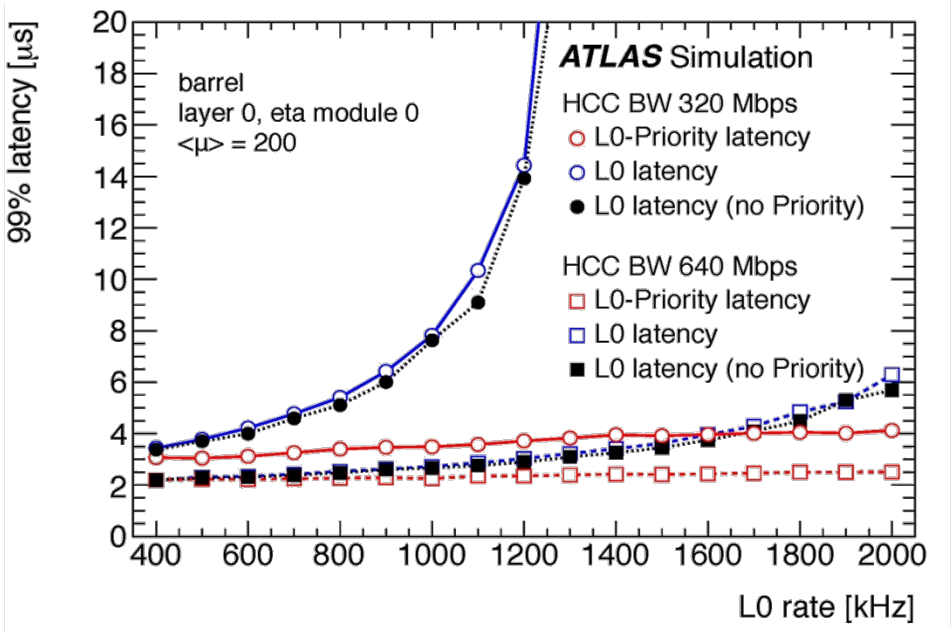
# Summary

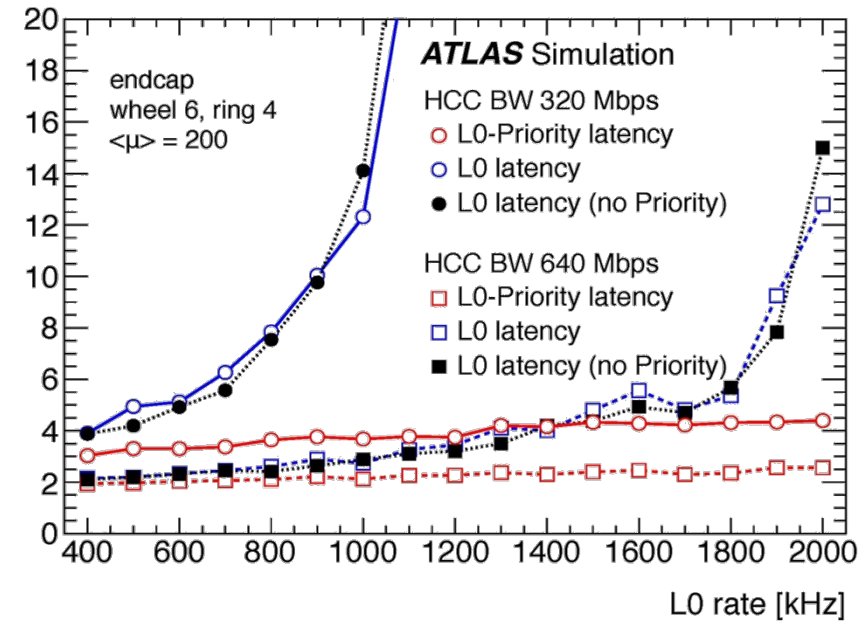
- Until now, many new features are adopted for ABCStar design
- And verification setup based on UVM has validated the function of present design
- However, some decisions need to be made soon, several issues to be solved
- At present, design and verification are still ongoing, many efforts needed

# Backup Slides

# Managing the 1 MHz L0 Rate

- The change to the “star” hybrid architecture was not the only concern with the increase to 1 MHz event readout rate:
- The latency requirement for L0-P trigger is below 5us, to feed data to L1-Track
- Here are simulations of the readout time at two different output bandwidths.




**The simulated latency for all data from 99% of all requests to arrive at the end of stave/petal for the highest occupancy Barrel and End-Cap layer module of the ITK as a function of the L0 rate for the scenario where all L0 events are read out from the detector. Detector occupancies commensurate with a mean occupancy of 200 separate pileup interactions per bunch crossing have been used.**