Studies Toward A Full Silicon Tracker for CEPC

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CEPC Detector Physics Study Group, 6/6/2016

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Outline

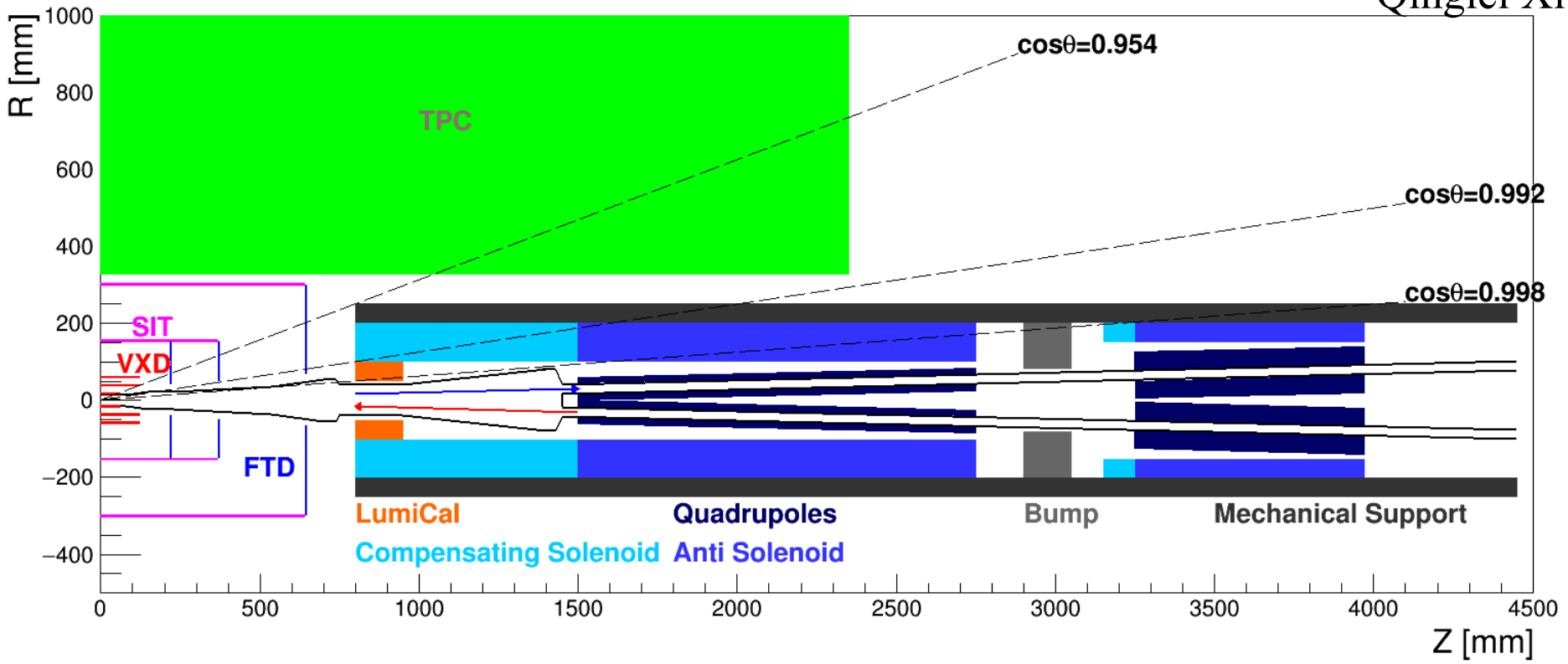
- Introduction
- Silicon tracking studies using CEPCV1 detector
- Optimizing a full Silicon tracker
- Implementing a new Silicon geometry (ongoing)
- Optimizing silicon tracking (ongoing).

Introduction

- Two design options of ILC detectors: ILD and SID, use very different design approaches, but overall performance at the end is quite similar.
- Starting from ILD/SID, we will re-optimize them for CEPC.
- A tracker design requirements:
  - CEPC is designed for CM energy up to 250 GeV and circular bunches
  - High efficiency and excellent track resolutions are essential:
    - $\sigma(1/pt) = 2\text{-}5 \times 10^{-5}$
    - $\sigma(d0) < 5\ \mu m$, $\sigma(z0) < 5\ \mu m$
    - Less material budgets
    - Hermeticity detector down to 10 degree in theta (?).
- Design concerns:
  - What's the optimal B field ? B=3.5T is possible ?
  - What's the closet radius for pixel detector? R=12 mm is possible?
  - What's the maximum theta coverage ?
  - With a smaller Si tracker volume, what's impact on PFA and cost ?

CEPC V1 + IR

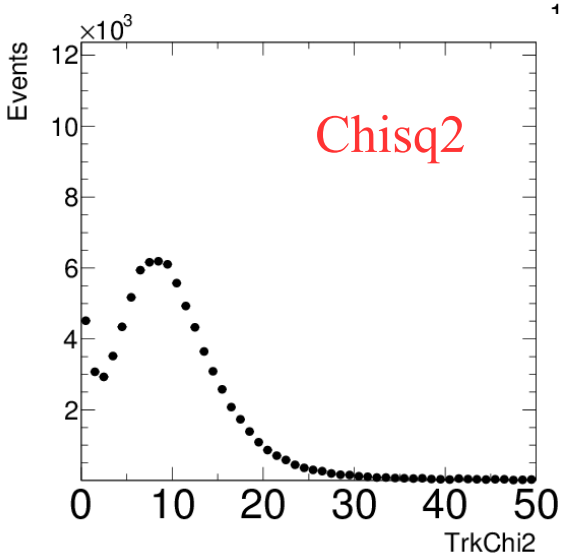
Qinglei Xiu

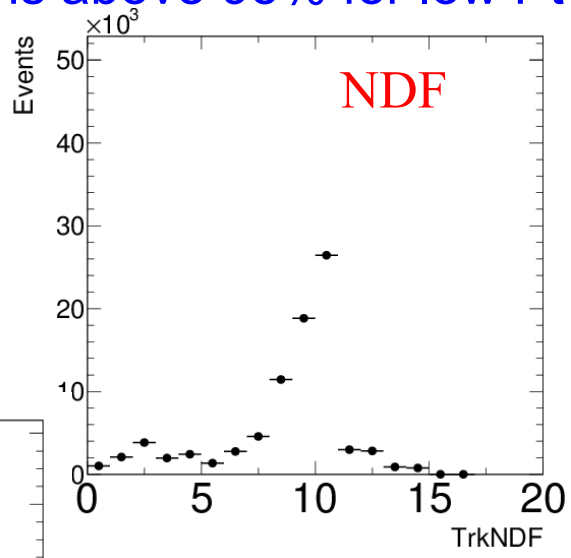


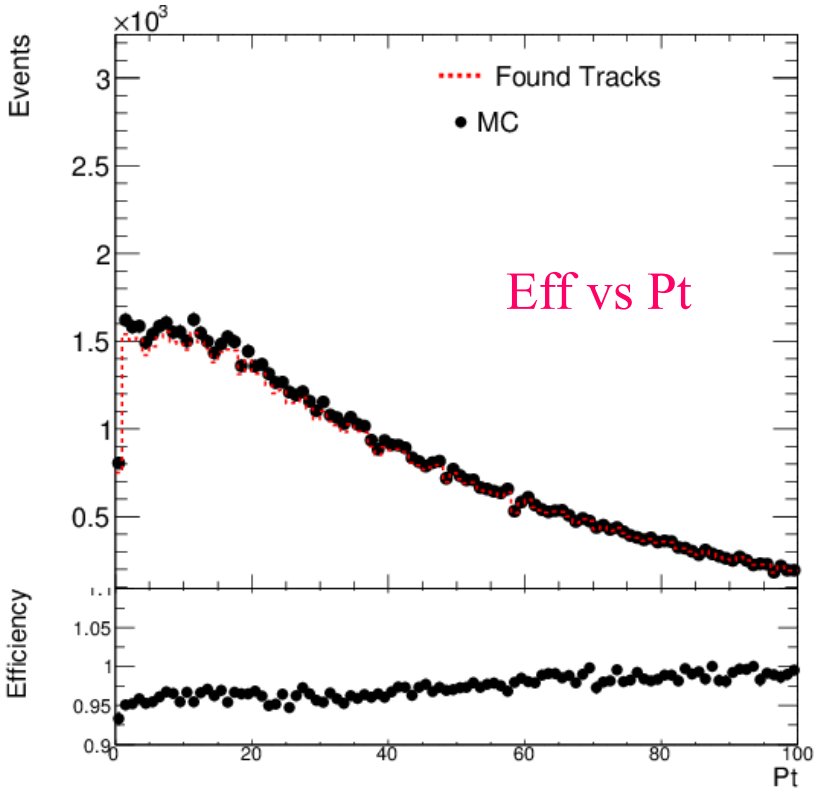
- CEPCV1 tracker contains TPC + Silicon
- Enough silicon layers, VTX(3 double layers)+SIT(2 double layers) +ETD+FTD, will provide excellent tracking capabilities as a redundancy.
- Case to study:
  - Does the silicon tracker provide adequate tracking without TPC ?
  - Can the tracker be improved with additional layers as a silicon tracker option ?

Silicon Tracking only using CEPCV1

- Simulated 100K single muon using CEPCv1, reconstructed using silicon only.
- The track chisq and number of degree of freedom look reasonable
- The track efficiency is above 95% for low Pt and raise up 100% for high Pt.

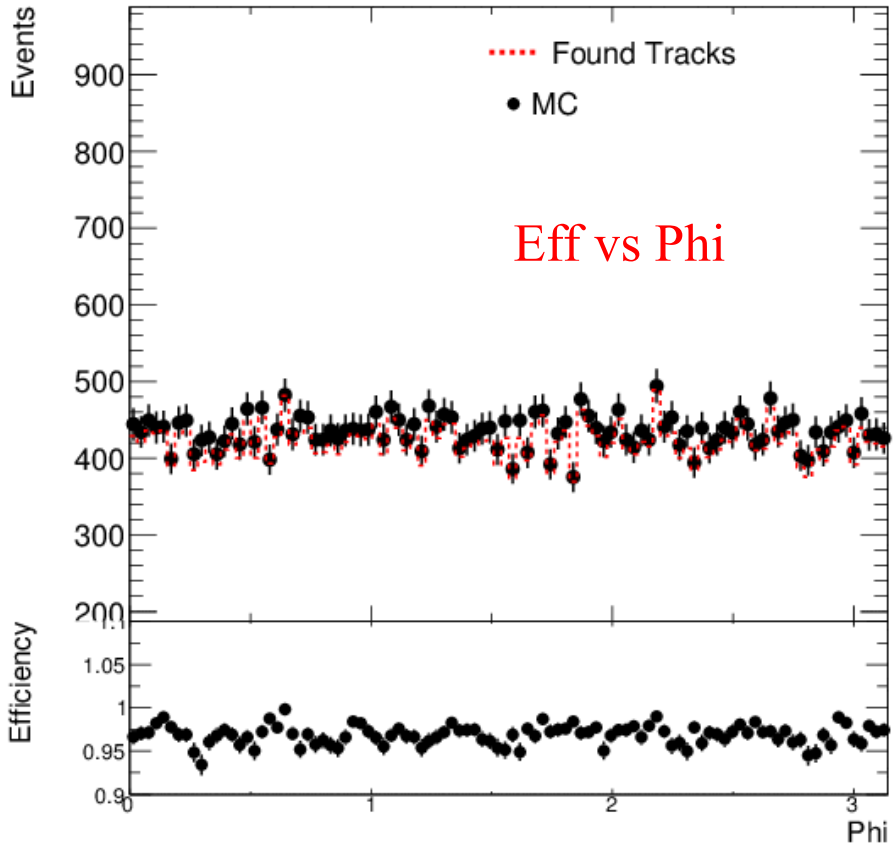


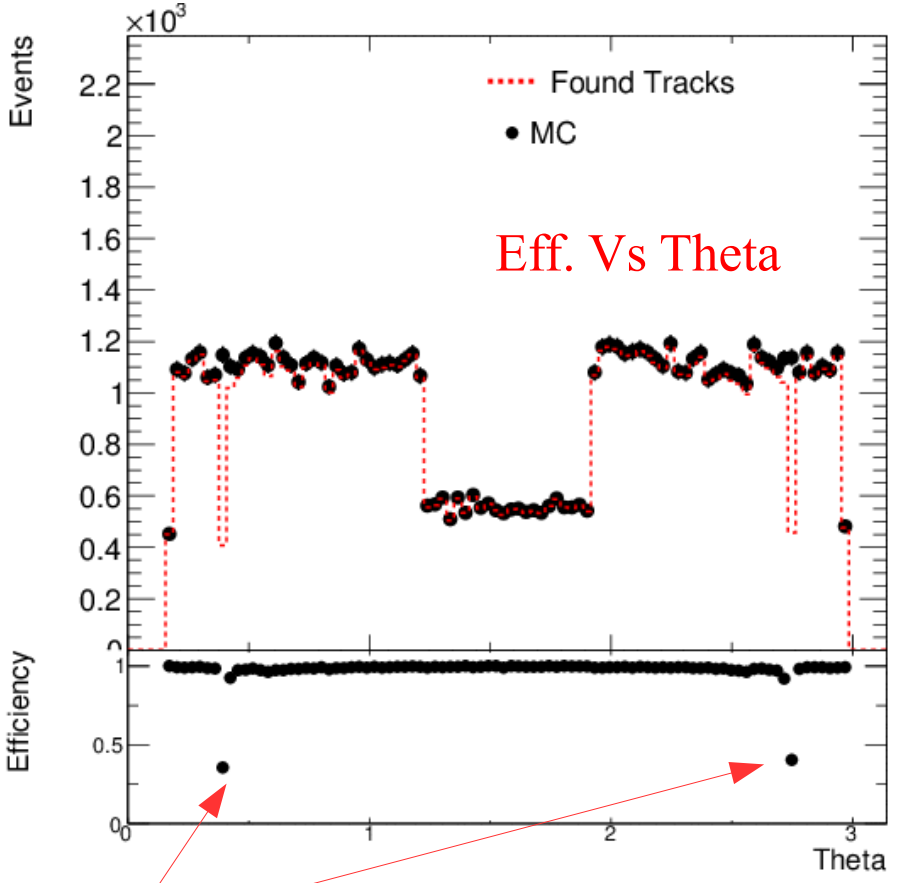




Silicon Only Tracking Efficiencies

- Track efficiency vs phi and theta are good except near overlap regions of Barrel and Endcap.

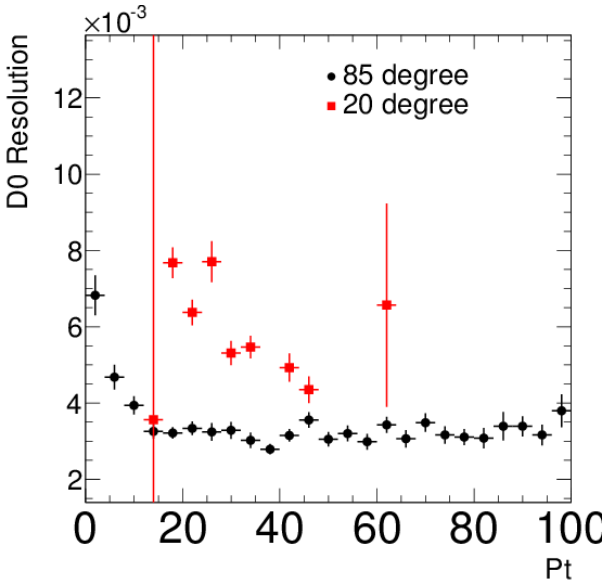


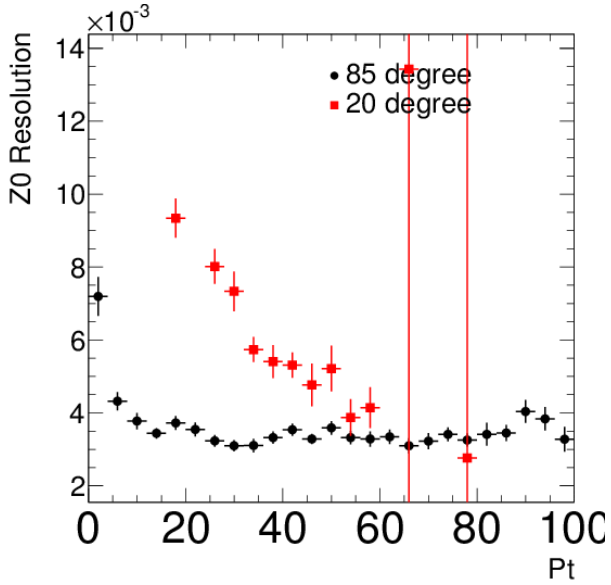


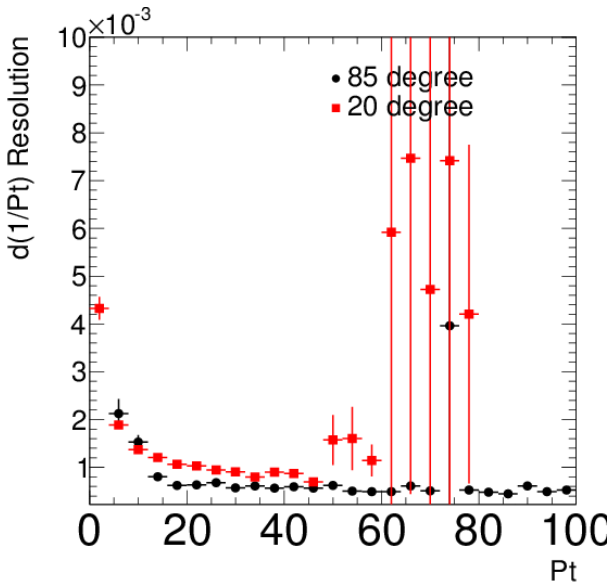
Barrel & Endcap overlap region

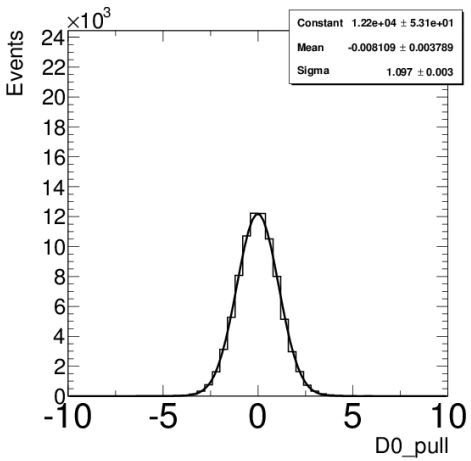
Silicon Track Resolutions

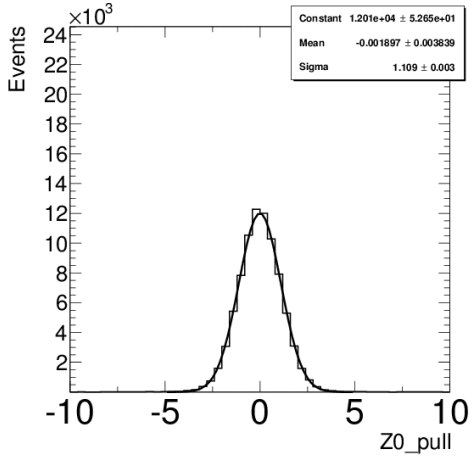
- Resolutions are met design goals and pulls are reasonable.

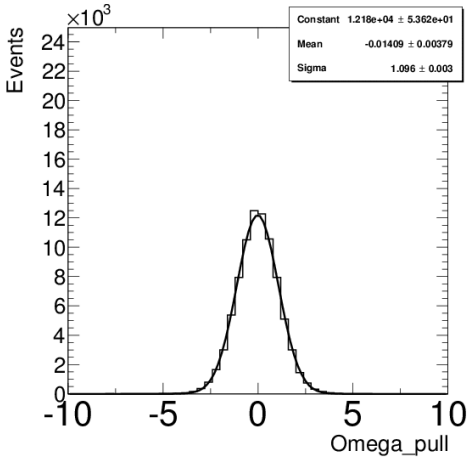






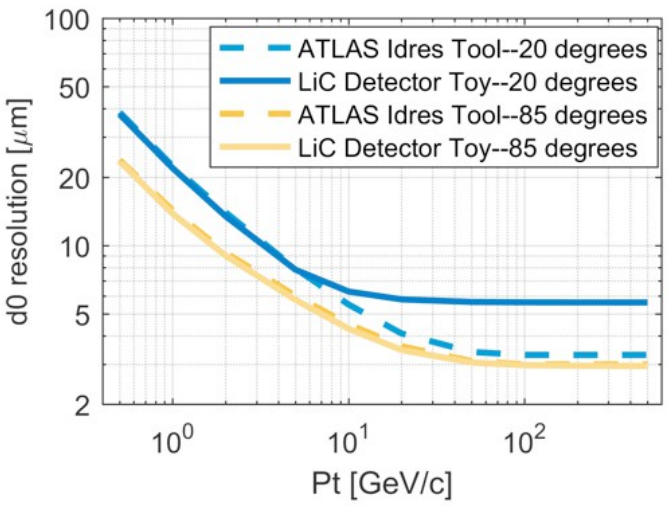


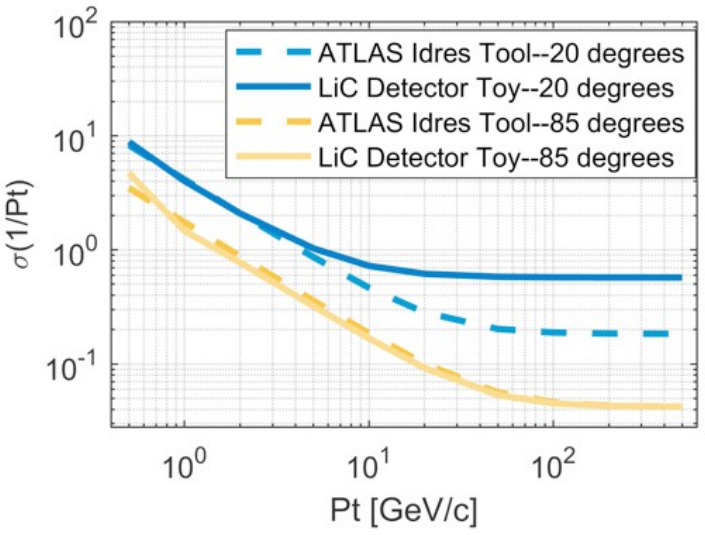




Optimizing a full Silicon Tracker

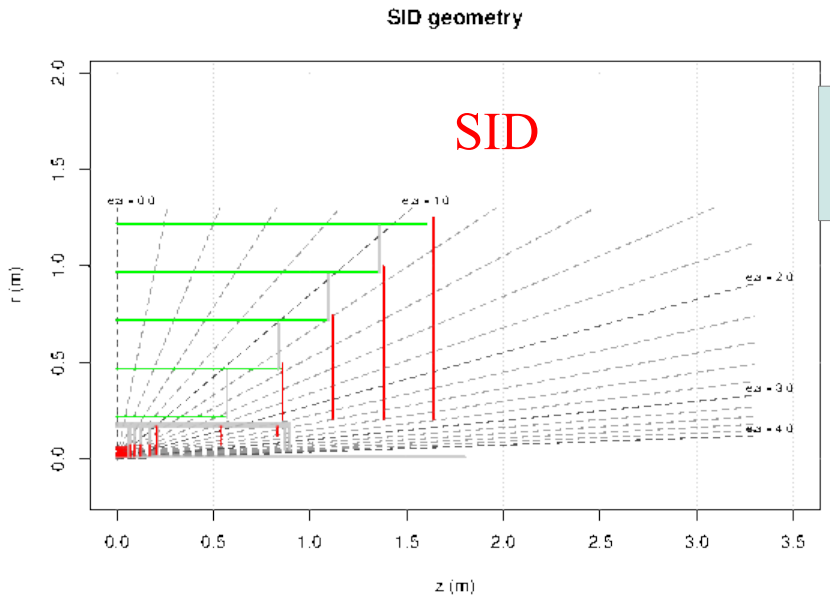
- Starting from SID, we optimize it for CEPC with following changes:
  - Reducing B field 5 T → 3.5T in order to compensate easily.
  - Changing single-sided strip in Barrel → Double-sided w small angle stereo
  - Add extra strip layer in barrel and endcap to compensate a lower B field.
  - Impact of material budget.
- Toy simulations:
  - Modified ATLAS Idres tool to predict tracking resolutions (Wei-Ming).
  - LDT from ILC tool (Liejian)
  - Excellent agreements except the d0 resolution in the endcap region.



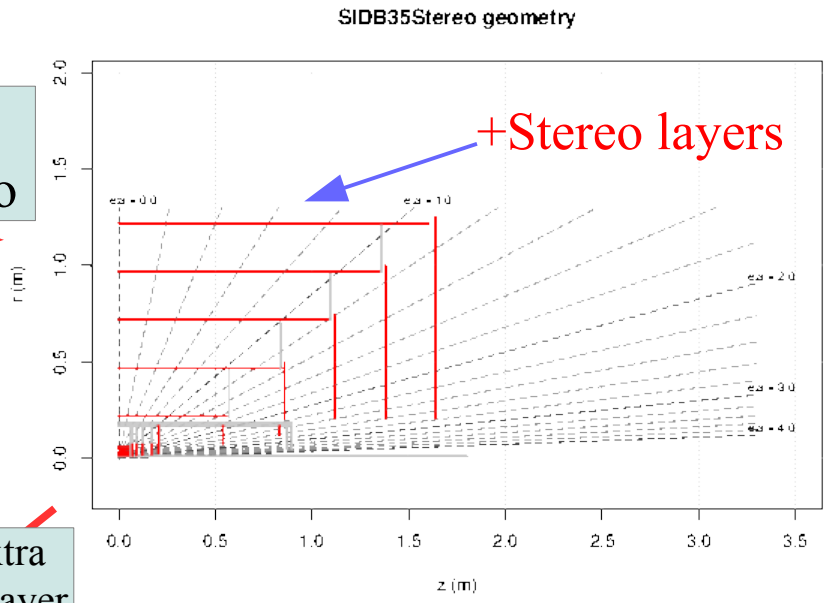


Liejian

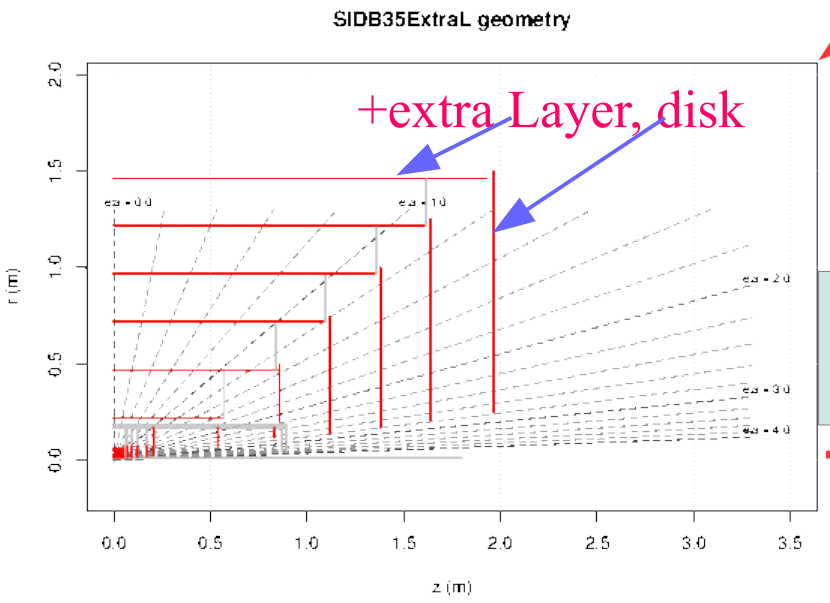
Silicon Layouts Considered



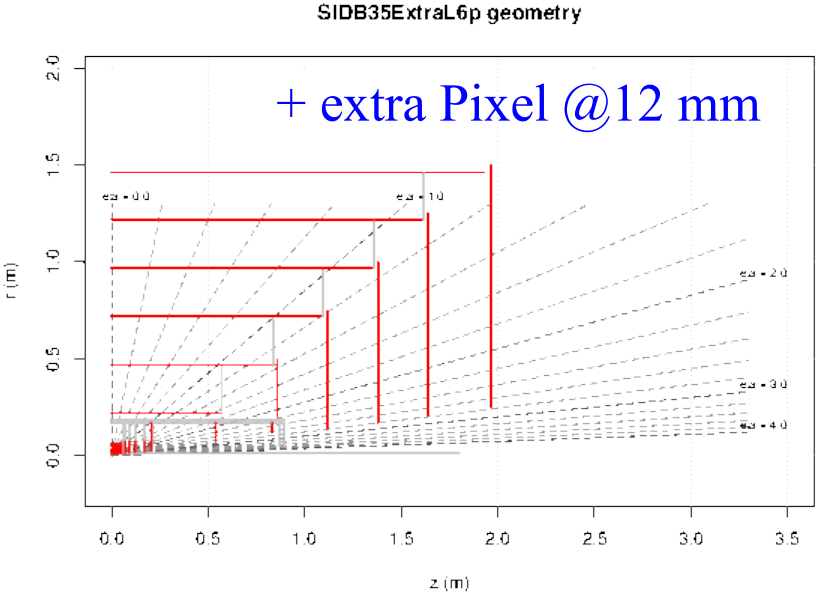
Add Stereo



Add extra Strip Layer

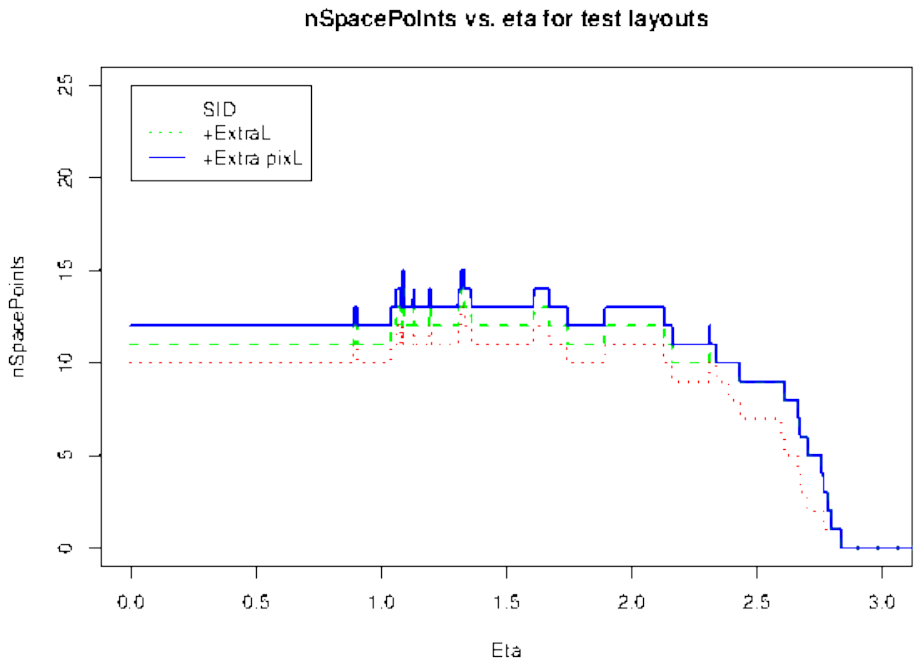


Add extra pixel layer @12mm

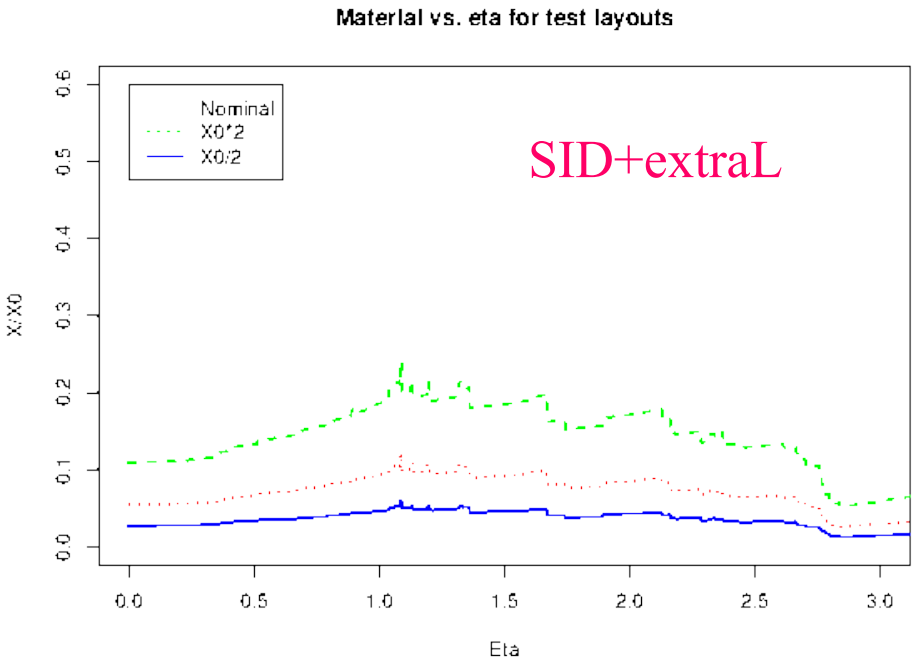


Expected Hits and Material Budget

- The number of hits >10 uniform up to eta=2.4:

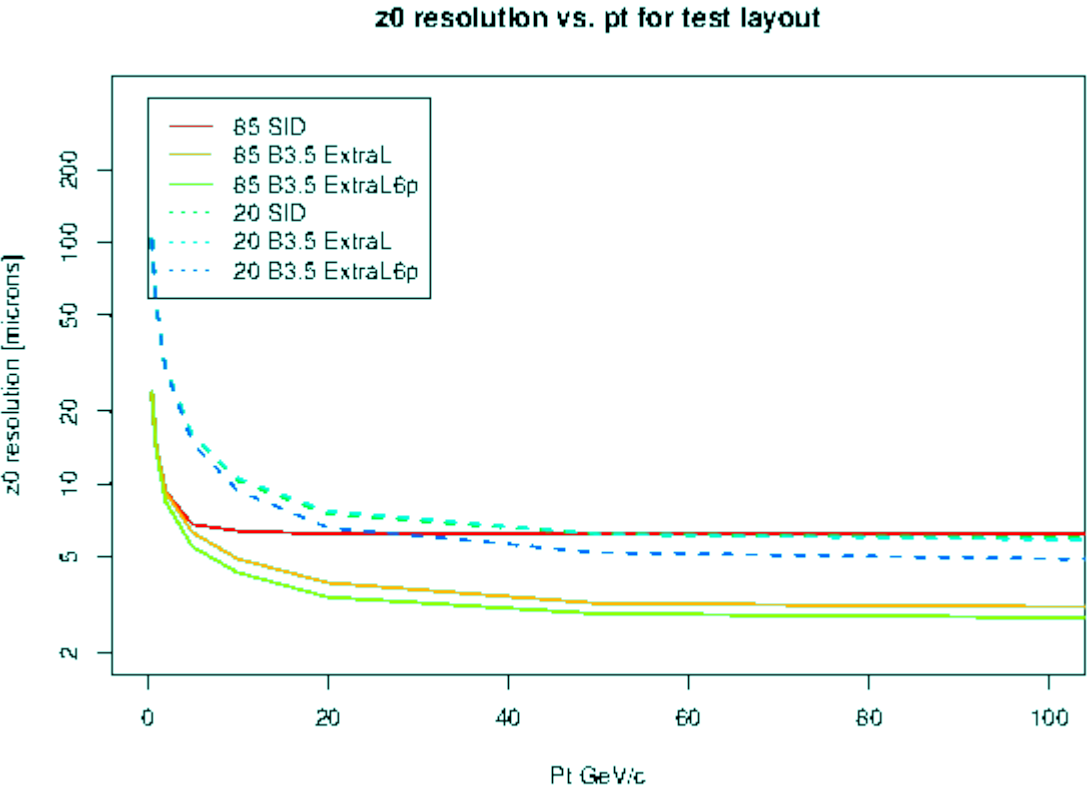


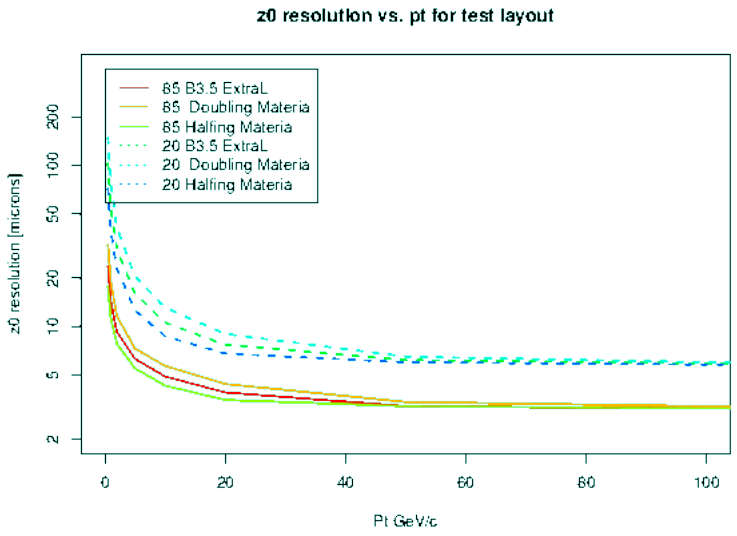
- Material vs eta is <10%
- double/half to see effects:



Z0 resolution

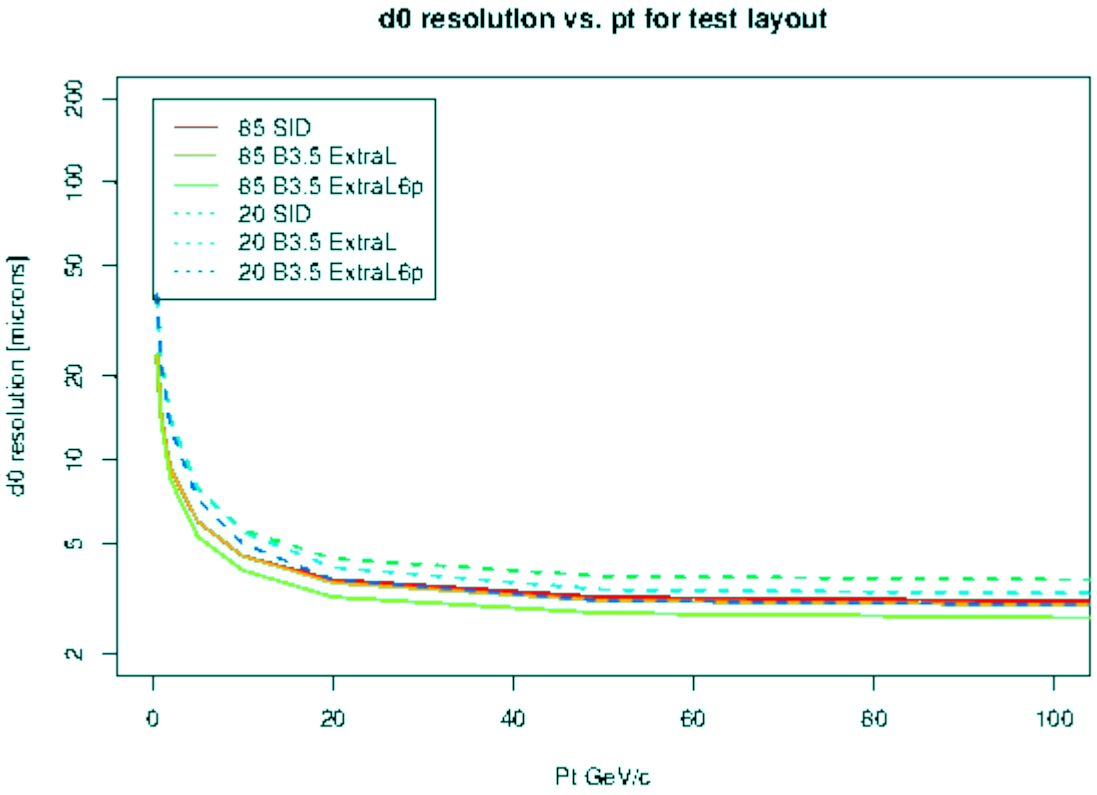
- For track at theta =85, 20 degree,
- Z0 improved significantly with stereo strip layers.
- Excellent Z0 resolutions and less X0 is better.

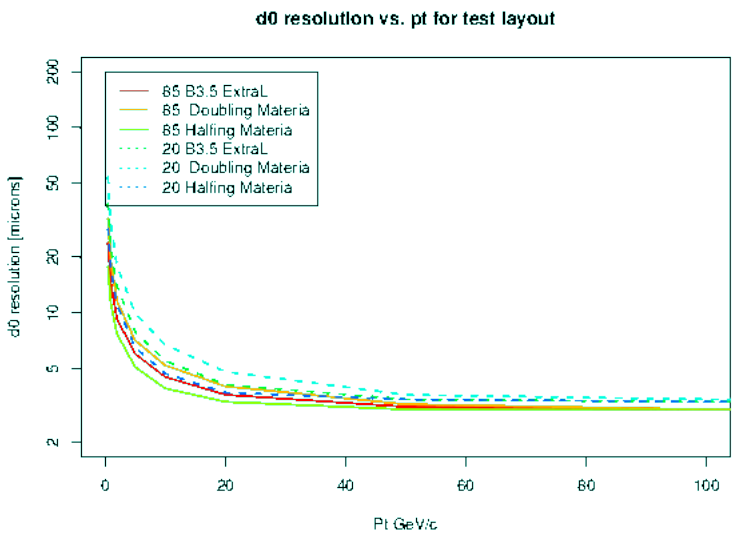




D0 resolution

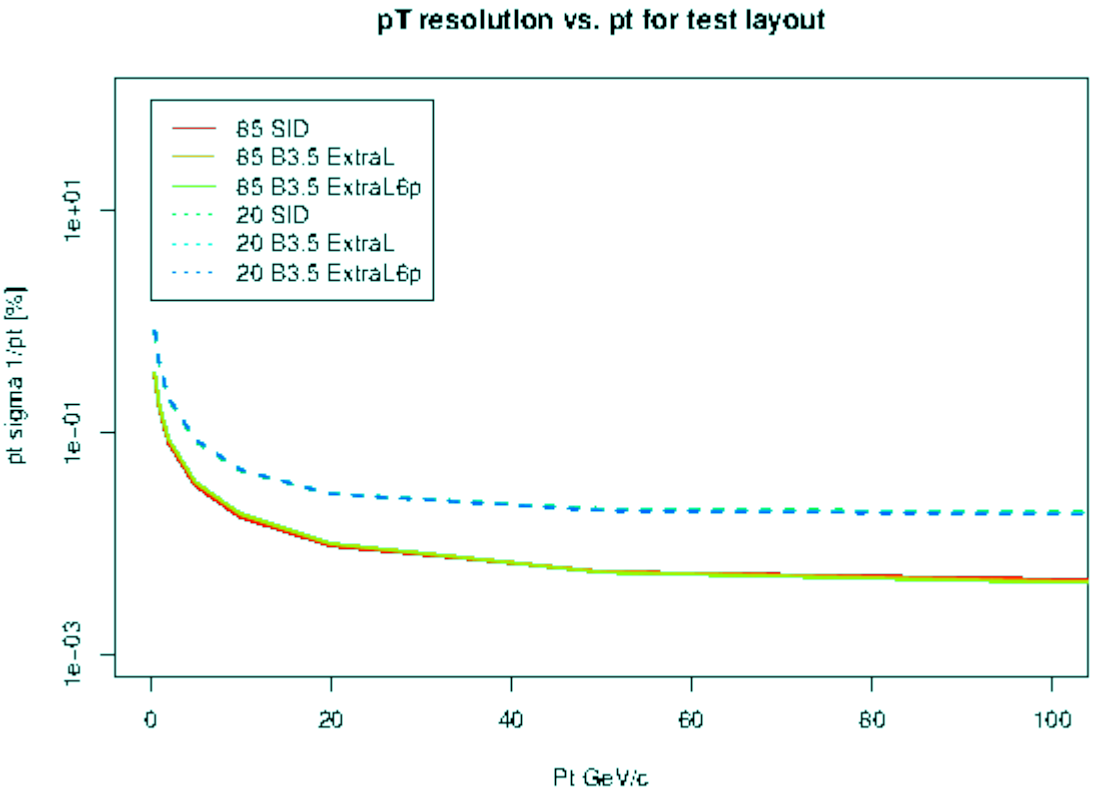
- For track theta =85, 20 degree,
- D0 seems similar for various layouts, but with extra pixel layer at 12.5 mm it improves D0 resolution significantly, and less X0 is better.

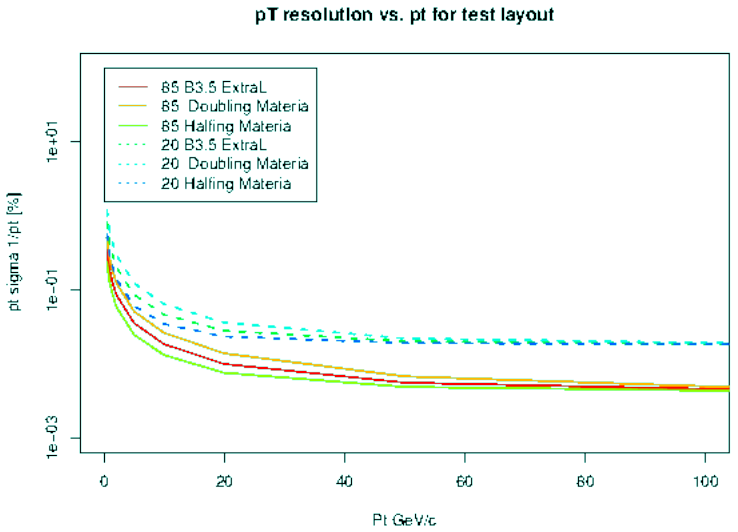




Pt resolution

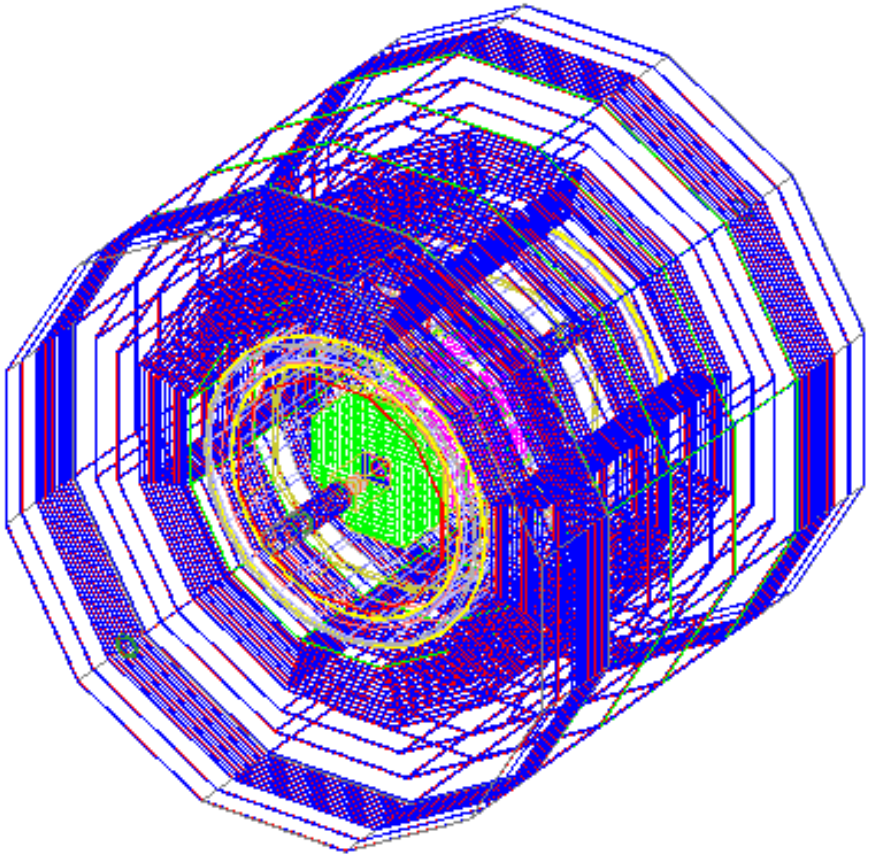
- For track theta =85, 20 degree,
- Pt depends on BL^2 that gives similar pt resolution, and less X0 is better.

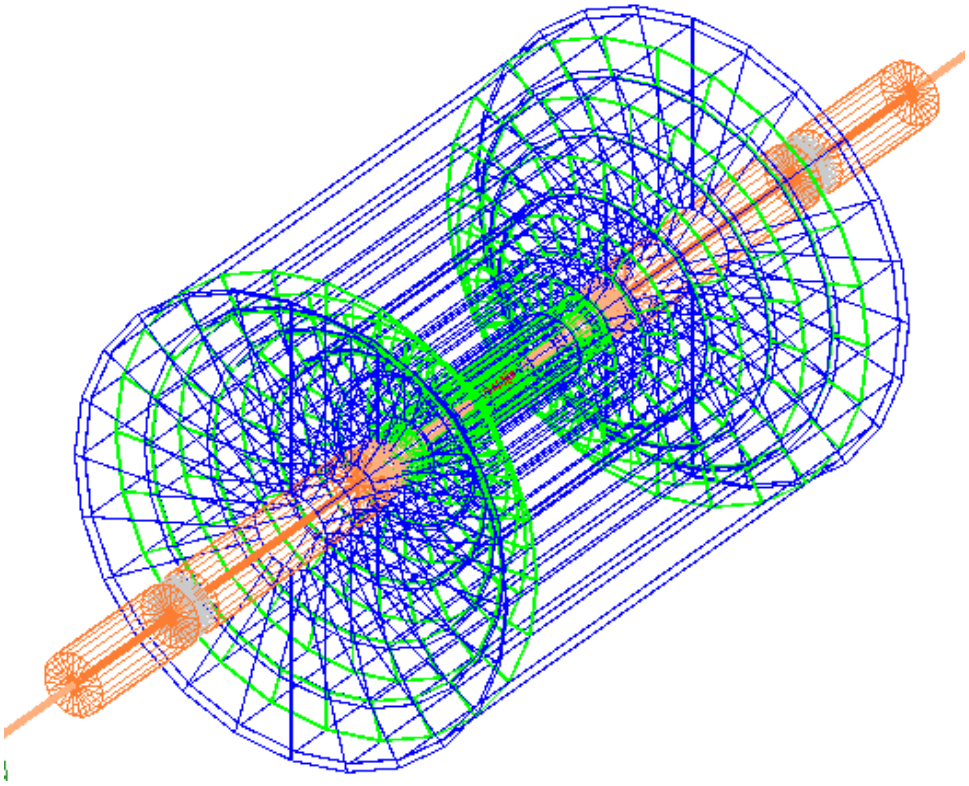




Quick Simulation tool for Silicon-Tracker

- Based on CEPC v1 (Chendong)
- Implementing a Silicon-based tracker in Mokka as cylinder.
- Reducing EM, Had calorimeters and Coil to fit a smaller silicon-tracker.





Next Steps

- The silicon tracking in CEPCV1 looks promising.
- A full silicon tracker option is optimized based SID design.
  - Using a lower B field B=3.5T, instead of 5 T , easy to compensate.
  - Changing single-sided to double-sided small angle stereo layers for strip detectors in the barrel region.
  - Add additional strip layer at r=1.46 m and extra pixel layer at 12.5 mm to improve the momentum and impact parameter resolutions.
  - Study of two-track separation to optimize the layer layout.
- Modifying CEPCV1 geom to have a full silicon option so that the silicon tracking reconstruction could work out of box.
- Understanding low efficiency near the overlap regions of barrel and endcap.
- Study the tracking performance between TPC+Silicon vs Silicon only.