PIXELS & SHORT STRIPS

SOME THOUGHTS BEFORE WE START…

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How to get started?

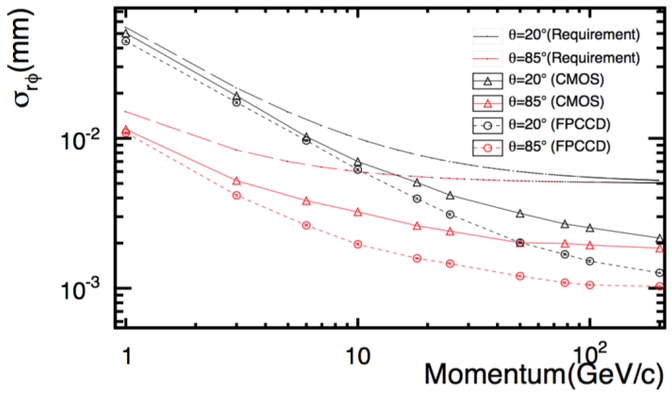
- Boundary Conditions & System Aspects
- Technology
- Architecture
- Sociology

Boundary Conditions & System Aspects

☑ Physics First!

impact parameter resolution

$$\sigma_{ip} = a \oplus \frac{b}{p \cdot \sin^{3/2}\theta}$$



ILD DBD 2012

Accelerator	a [μm]	b [μm·GeV/c]
LEP	25	70
SLC	8	33
LHC	12	70
RHIC-II	13	19
ILC	< 5	< 10

ILD LOI 2009

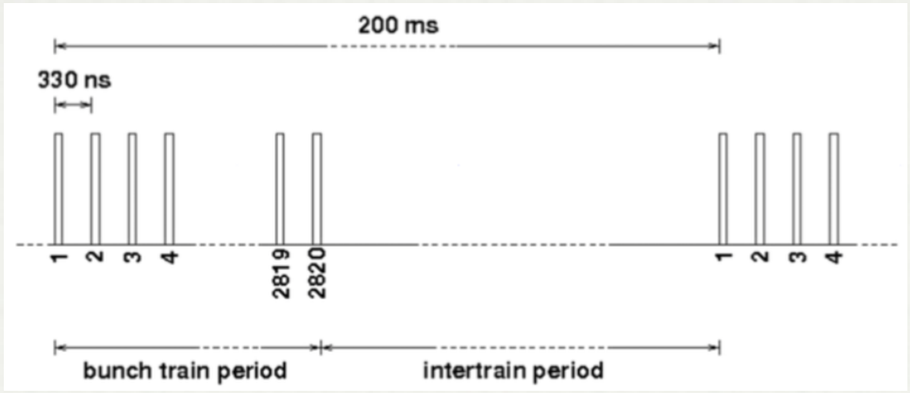
- a depends on the single point resolution and the ratio between the innermost radius and the lever arm:
  => σ_{sp} = 3 μm when R_{in} =16 mm and R_{out} = 60 mm

btw: what $R_{beamPipe}$ can be expected @CepC?

- b depends on the multiple scattering at the innermost radius:
  => thickness/layer = 0.15% X_0 [X_0 = 9.37 cm for Silicon]

The machine comes next:

what is the time structure of the beams?



at the ILC, it may look weird but it is very practical since the low duty cycle allows:

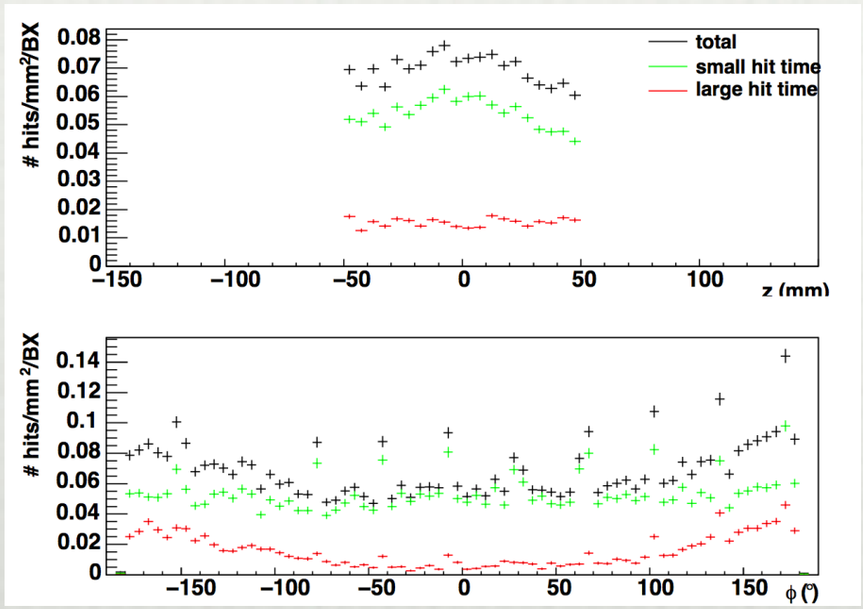
- to consider a Power Pulsing scheme
- a relaxed evacuation of time stamped data during the inter-train

What is the expected Beamstrahlung?

hit rate in the first layer of the ILD-VD

occupancy ~10^{-2} /50 μs

DeMasi, Winter, ArXiv: 0902.2707v1



It has an impact on:

- the granularity and the technology (affecting the cluster size)
- Time stamping
- read-out speed ⇢ architecture & power consumption

and what about the expected radiation levels?

Table 1
Comparison of the requirements of various vertex detectors, in terms of read-out speed (σ_t) and radiation tolerance related to the total ionizing dose (TID) and non-ionizing particle fluence.

Experiment-system	σ_t (μs)	TID (MRad)	Fluence (n_{eq}/cm^2)
STAR-PXL	$\lesssim$200	0.150	3×10^{12}
ALICE-ITS	10–30	0.700	10^{13}
CBM-MVD	10–30	$\lesssim$10	$\lesssim 10^{14}$
ILD-VXD	$\lesssim$10	$\mathcal{O}(0.1)$	$\mathcal{O}(10^{11})$
Super B factories	$\lesssim$20	5/yr	5×10^{12}/yr

Here we can possibly relax..

Baudot et al., NIM A732 (2013) 480

☑ Last but not least, the overall detector design:

- is the VD part of a full Silicon Tracker?
- is the experiment running trigger less?

Technology

- epi- less technologies (AMS 350 nm)
- low resistivity epitaxial layer, bulk (large catalogue)
- low resistivity epitaxial layer, OPTO tech (AMS 350 nm)
- low resistivity epitaxial layer, 3 wells (e.g. STm 130 nm)
- low resistivity epitaxial layer, 4 wells (e.g. INMAPS)
- **High Resistivity epitaxial layer, 4 wells (e.g. Tower Jazz 180 nm)**
- SOI on High resistivity Substrate (LAPIS, formerly OKI)
- Vertical integration (e.g. Tezzaron)

* low resistivity: ≈ 10 Ω cm, collection by diffusion
* high resistivity > 1 k Ω cm, collection by drift

Technology

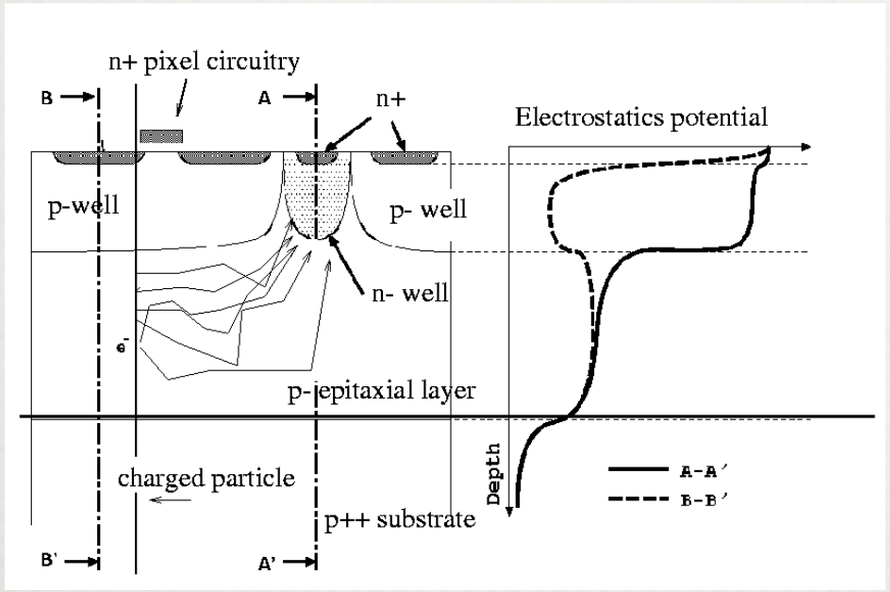
- epi- less technologies (AMS 350 nm):

Tested and dropped by the Strasbourg team (MIMOSA 4)
≈ 13 years ago

Technology

low resistivity epitaxial layer, bulk (large catalogue)

- standard, well established industrial fabrication process, granting a cost-effective access to state-of-the-art technologies



- based on the charge carrier generated in the epitaxial layer [2-14 μm thick, depending on the technology => SMALL signal (~80 e-h pairs/ μm)]

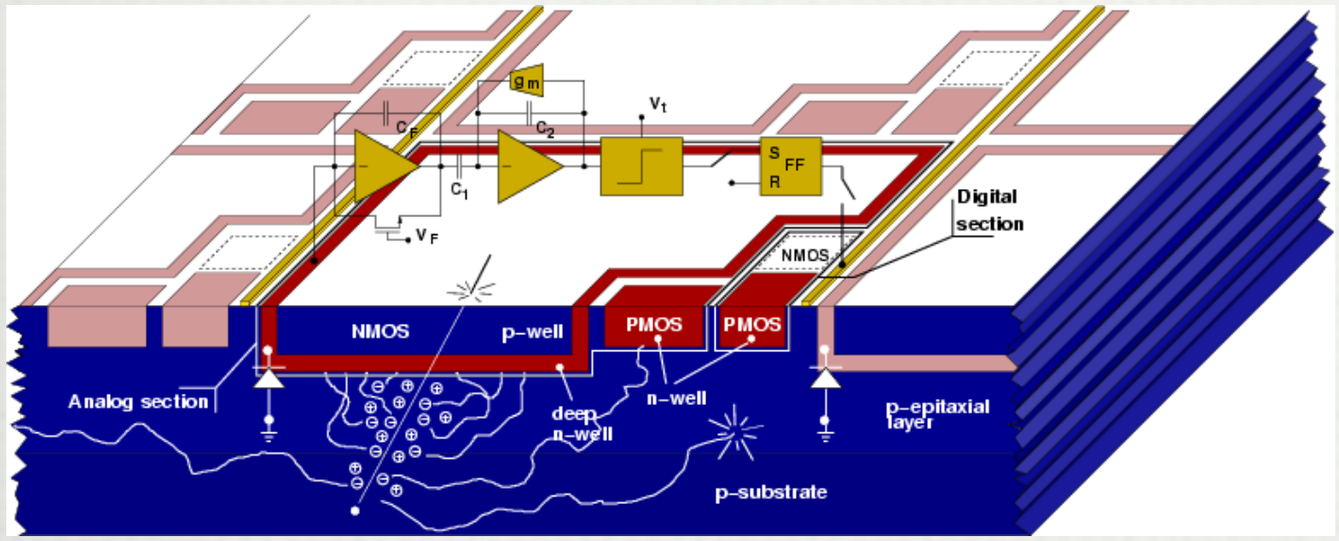
- diffusion detector vs [standard] drift sensors (the sensitive volume is NOT depleted => charge cluster spread over ~ 100 μm [10 μm] AND collection over ~ 150 ns [10 ns])

❖ Main drive from digital cameras
❖ Pioneered @ LEPSI Strasbourg in the late 90's:
- G. Deptuch at al, IEEE-TNS 49 (2002) 601
- R. Turchetta et al, NIM A458 (2001) 677

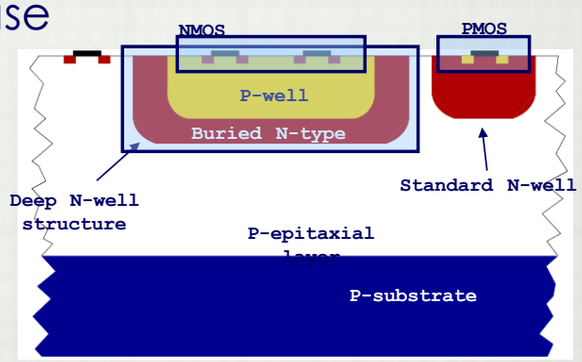
Fair enough but the possibility to have NMOS transistors only reduces the complexity of the electronics that can be integrated

Technology

- low resistivity epitaxial layer, 3 wells (e.g. STm 130 nm)



In triple-well CMOS processes a deep N-well is used to isolate N-channel MOSFETs from substrate noise



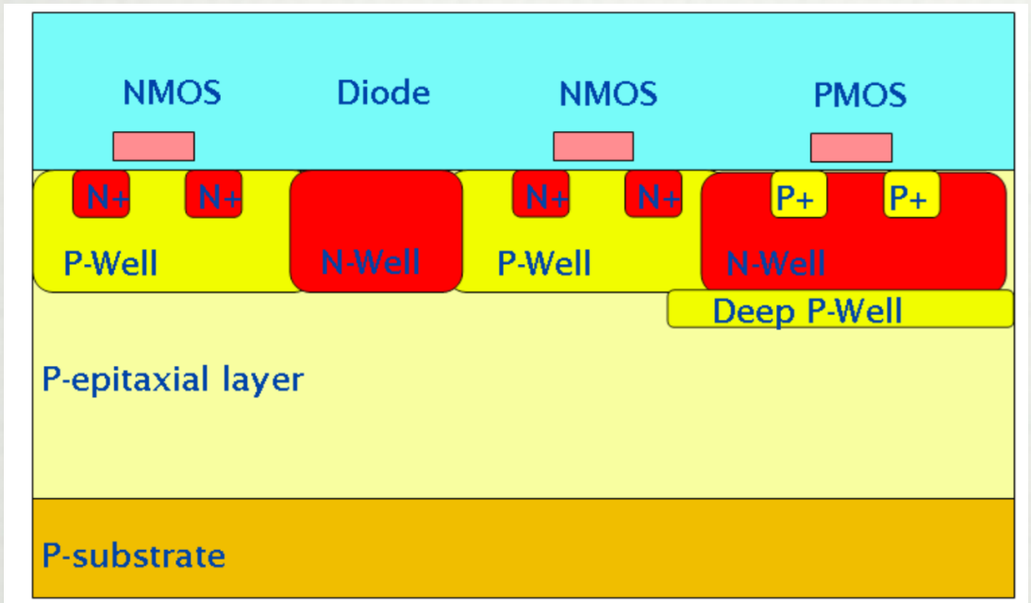
G. Traversi, V. Re, M.Ca. et al, IEEE TNS 56 (2009) 3002

Such features were exploited in the development of **deep N-well (DNW) MAPS** devices

Obviously a nice step forward BUT the auxiliary n-wells are a competitive path for the charge collection, inducing a dis-homogeneity in the sensor response
[a great technology for the designers possibly making the user's life a bit difficult]

Technology

- low resistivity epitaxial layer, 4 wells (e.g. INMAPS)



Nest the auxiliary n-wells in a deep p-well & avoid the competitive path

R. Turchetta et al., Sensors 2008, 8 5336-5351

Nearly ideal and it took about 7 years before the final step was taken, and a quadruple well technology was made available on a high resistivity substrate

Technology

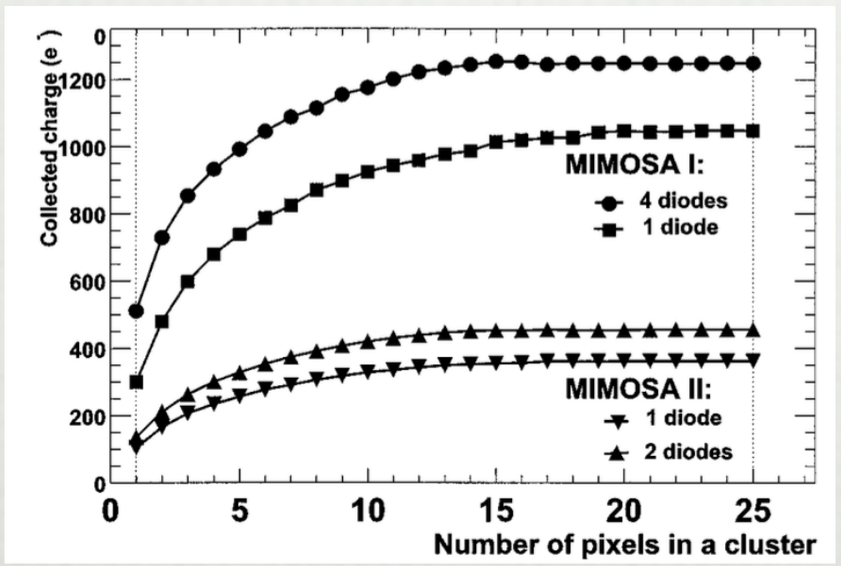
High Resistivity epitaxial layer, 4 wells (e.g. Tower Jazz 180 nm)

Some of the advantages of this technology:

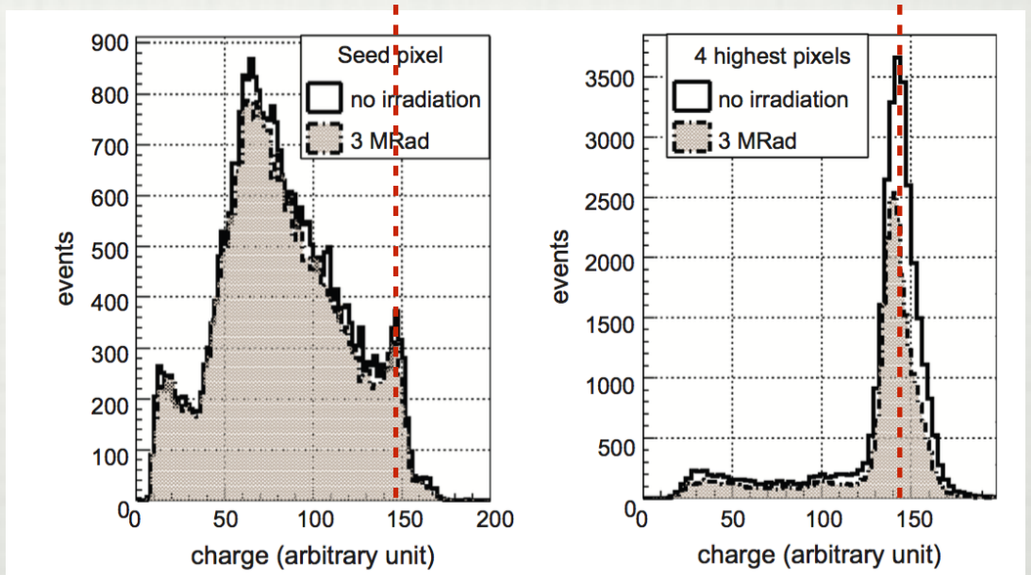
- 6 metal layers for dense interconnections
- quadruple well
- 18 μm thick epitaxial layer of 1-5 kΩ cm resistivity ⇢ collection by drift

3 good reasons for having high resistivity substrates:

a. smaller charge spread & clustering size



AMS 0.6 μm technology - 14 μm epitaxial layer - 20 μm pixel pitch



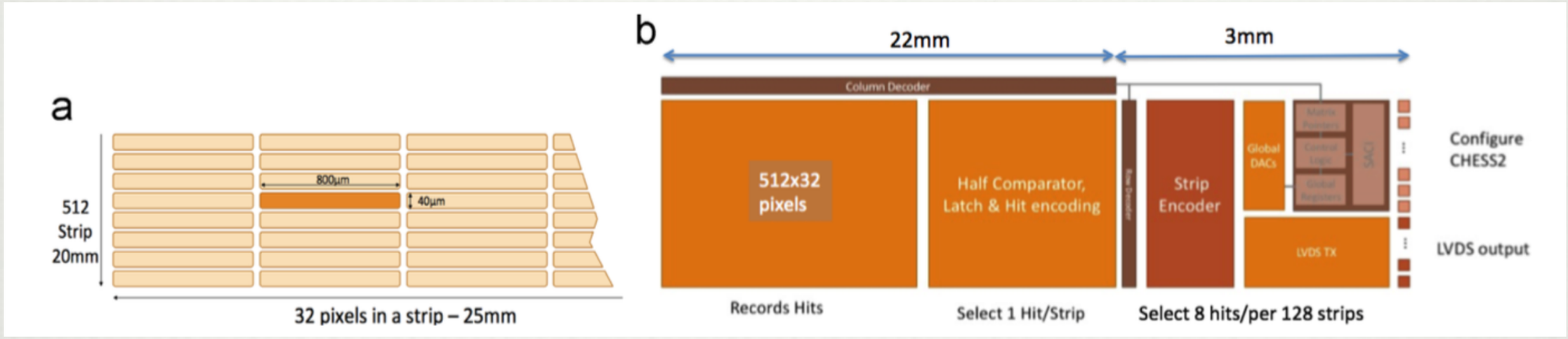
TJ 0.18 μm technology - 18 μm epitaxial layer - 20 μm pixel pitch, illuminated by an 55fe source (5.9 keV X ray, 1640 eh pairs

G. Deptuch at al, IEEE-TNS 49 (2002) 601

G. Baudot at al, NIM A732 (2013) 480

b.shorter collection time ⇢ reduced trapping probability ⇢ increased radiation tolerance (possibly from 10^{12} n_{eq}/cm^2 to 10^{15} n_{eq}/cm^2 [W. Snoeys, NIM A731 (2013) 125]

c. possibility to design pixels with unusual aspect ratio ⇢ SHORT STRIPS



Z. Liang et al., NIM A (2016) http://dx.doi.org/10.1016/j. nima.2016.05.007

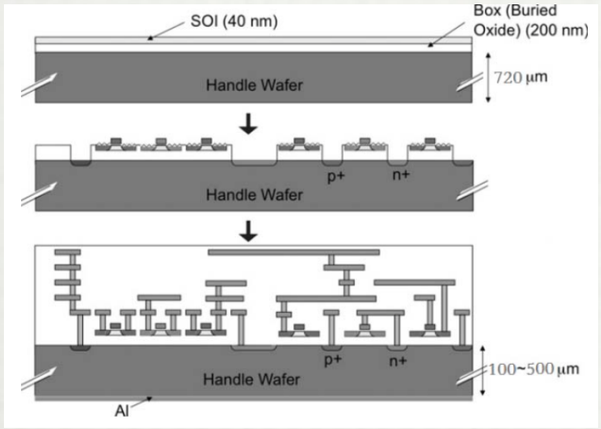
There's a lot of ongoing activity relying on these technologies. Among them, it is worth mentioning:

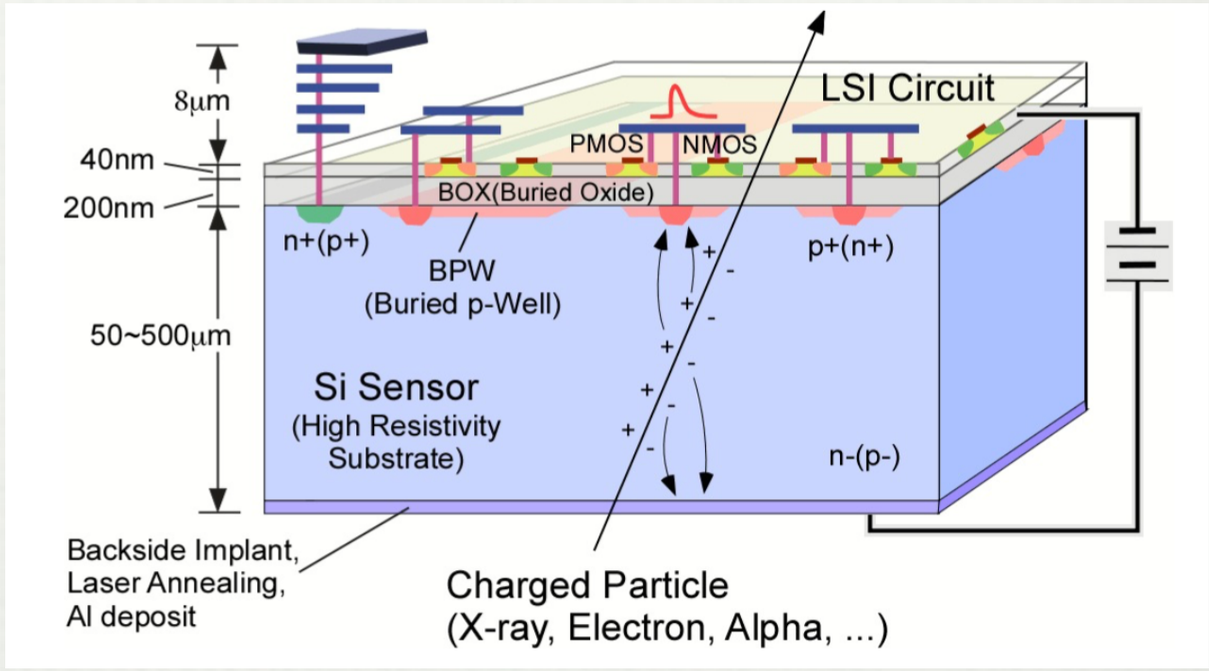
- the papers by Ivan Peric & coworkers (U. Heidelberg), driven by ATLAS
- the activity by A. Andreazza & co. (Uni.Milano) on pixels integrating a first stage amplification capacitively coupled to an LHC compliant RO chip (see poster @IWORID2016 and the oral at the next IEEE-NSS)
- notably the activity on ALPIDE, the sensor for the ALICE ITS system (see below)

Technology

- SOI on High resistivity Substrate (LAPIS, formerly OKI bu TJ seems to be on the track!)
  - H. Lan et al. IEEE sensors journals 15 (2015) 2732 a Review!
  - J. Marczewski, M. Caccia et al., *IEEE Trans. Nucl. Sci.*, 51 (2004)1025
  - M. Jastrzab, M. Caccia et al, NIM A560 (2006) 31

simplified process flow



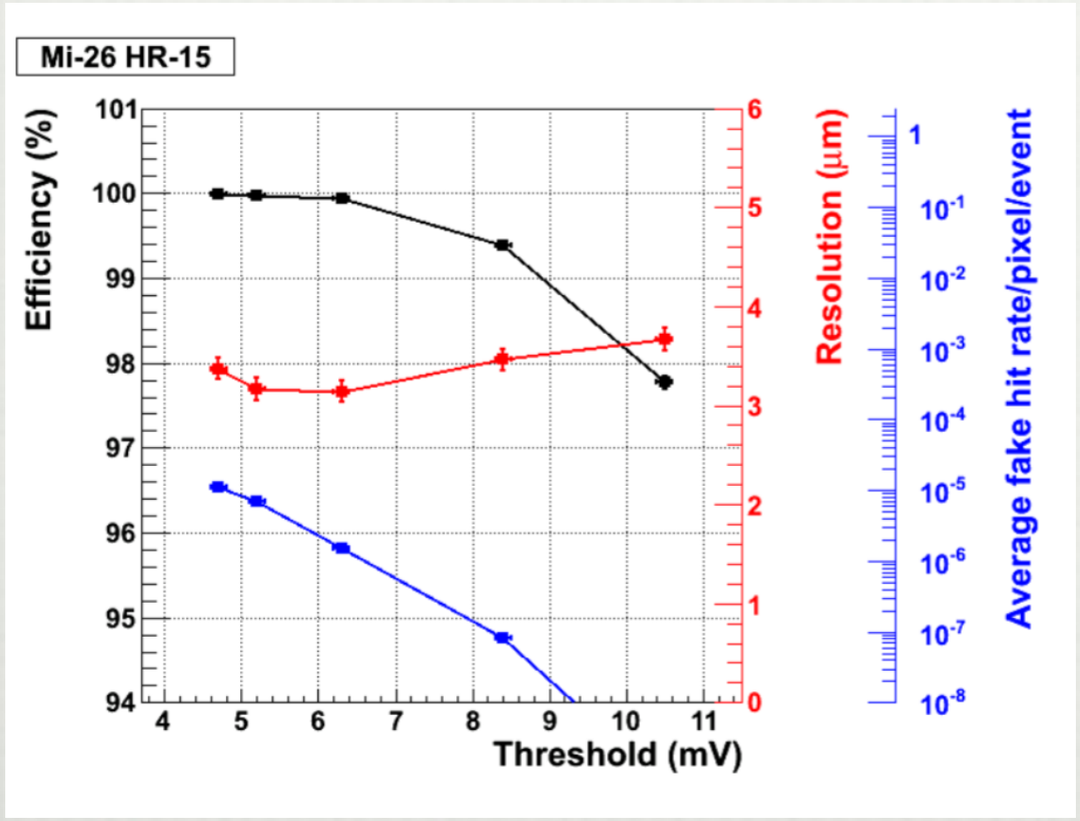


- main advantages:
  - a genuine monolithic approach
  - more flexible wrt CMOS maps (nmos & pmos naturally integrated in the SOI layer)
  - electronics "isolated" from the bulk (fast switching, reduced single event upset) [the motivation for the industrial development of SOI - partially true here]
  - the active layer is a very standard and comfortable high resistivity, fully depleted detector
- main disadvantages:
  - not easy to get SOI wafers on a high resistivity substrate
  - mind the effect of the depletion voltage (back-gate effect)
  - custom process

Architectures

☑ Analog or binary pixels?

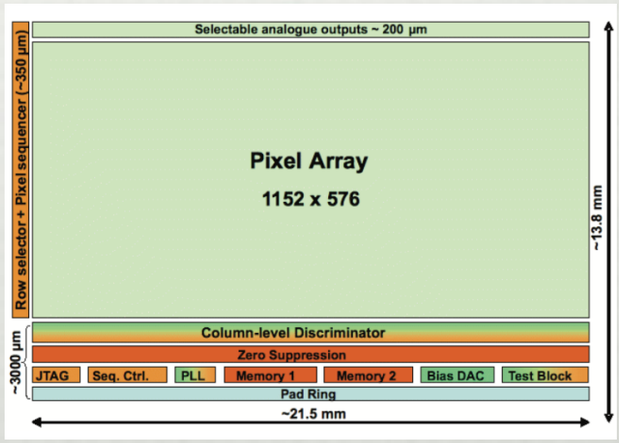
The pitch/√12 rule has been violated in MAPS:



M. Winter et al., arXiv: 1203.3750v1 (2012)

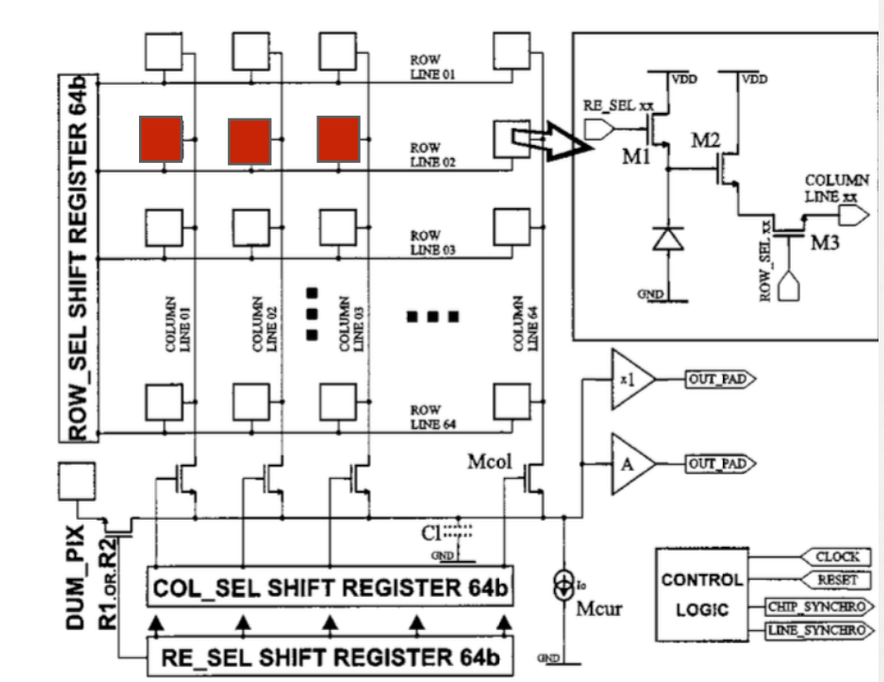
Test beam results for the MIMOSA-26 sensor:

- 18.4 μm pitch (5.3 μm binary resolution)
- rolling shutter & end-of-column zero suppression (200 ns/pixel r.o. time)
- 250 mW/cm^2 power consumption



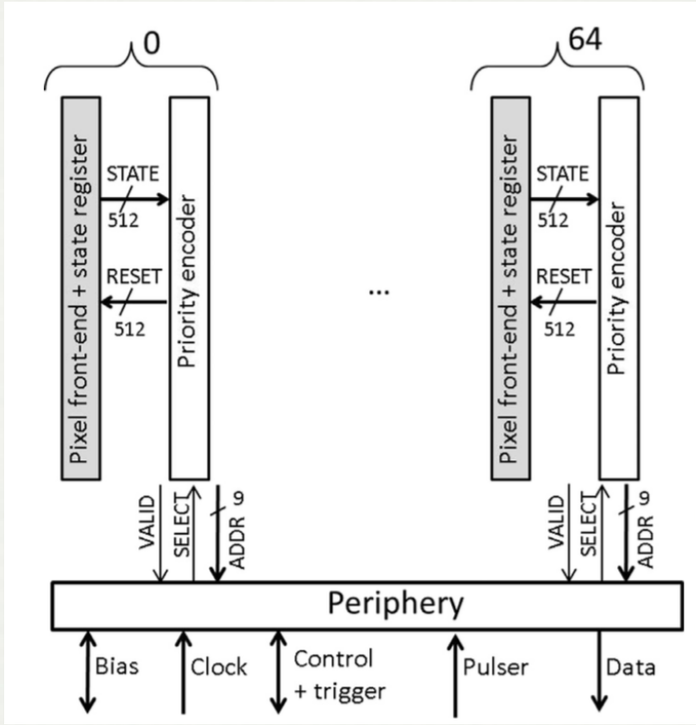
☑ Rolling shutter + end of column zero suppression or on-pixel sparsification?

Rolling Shutter



- 1 discriminator/column
  ⇢ analog info travels to the end-of-column logic
- the integration time is determined by the read-out (r.o.) time
- the r.o. time is independent from the pixel occupancy
- current power consumption at the level of 150 mW/cm^2 (MIMOSA -28)

On-pixel sparsification



- 1 discriminator/pixel + 1bit memory cell
  ⇢ analog info locally processed
- the integration time is independent from read-out (r.o.) time
- the r.o. time is dependent from the pixel occupancy
- current power consumption at the level of 50 mW/cm^2 (ALPIDE)

-NIM A 765 (2014) 177 + A 785 (2015) 61
-pixel 2014 proceedings published on JINST (doi:10.1088/1748-0221/10/03/C03030)

made possible by the quadruple well tech.

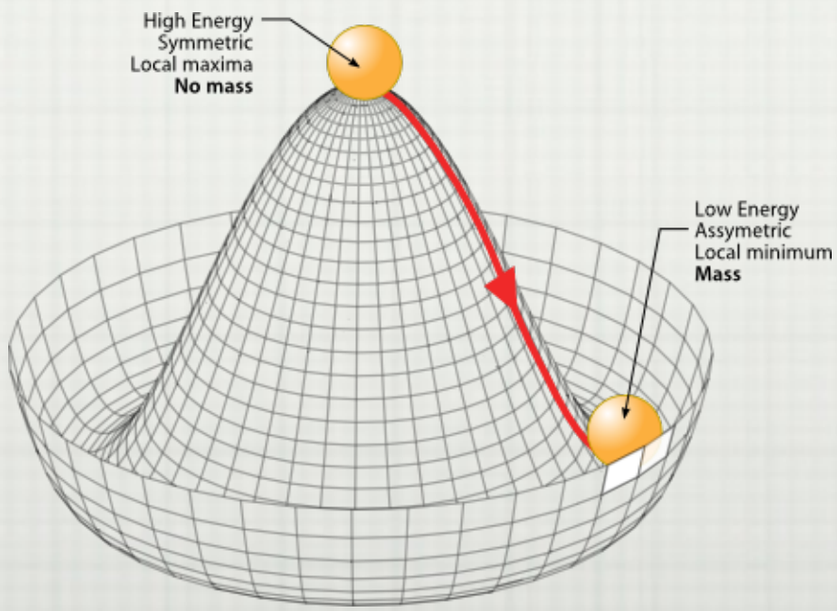
Conclusions:

- The new technologies certainly offer unprecedented opportunities

- I believe the running conditions at the new electron-positron machines are such that detectors fully compliant with the boundary conditions (and more!) can be designed and engineered, so:
  - we have to be BRAVE
  - we have to stay HUNGRY & FOOLISH
  - BUT WE DO NOT HAVE TO BE INSANE!

The optimal sensor will always result by an equilibrium (possibly NOT a COMPROMISE) of the different specs and among the different proposals (and people connected to them).

But we know there are 2 different kind of equilibria:



Thank you very much!