A new ADC chip Vulcan for PMT readout

Next Generation Nucleon Decay and Neutrino Detectors (NNN'16)

2-Nov-16 | Christian Grewing
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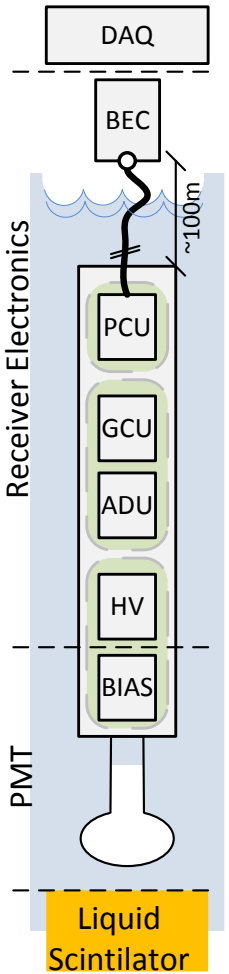
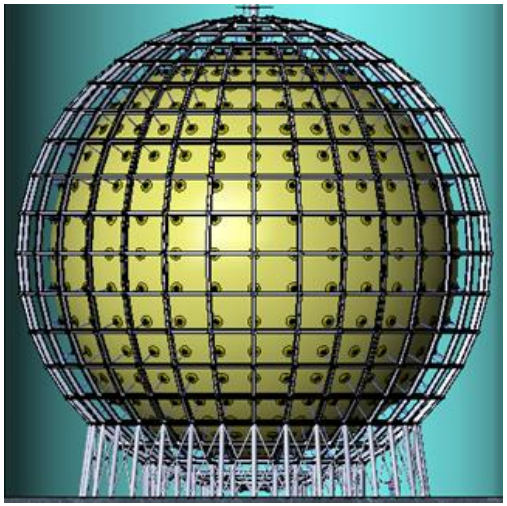
Central Institute of Engineering, Electronics and Analytics - Electronic Systems (ZEA-2)
on behalf of the JUNO Cooperation

Juno Detector Introduction

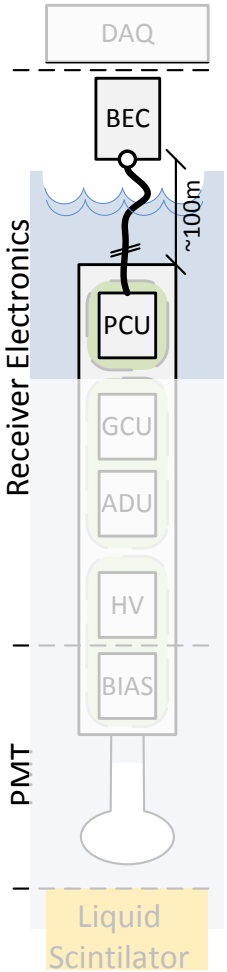


Jiangmen Underground Neutrino Observatory

- 20kton Liquid Scintillator in an acrylic sphere with a stainless steel structure
- Detector is in a water filled cavity with ca 720m overburden (1900m w.e.)
- Including: 18,000 20 “ and 36,000 3” PMT
- 100m Cable attached to data concentrators (BEC) on top of the detector
- The receiver electronics are attached to the PMT underwater for:
  - Lower data bandwidth on the cable
  - Programmable signal threshold modes
  - Local data storage (RAM) for supernova events
  - Programmable digital signal pre-processing to further reduce data bandwidth
- Intelligent PMT developed together with several groups in Asia and Europe



Receiver Chain Details



BackEnd Electronics (BEC):
Université Libre de Bruxelles

- Connection between ca 32 receivers to the DAQ and Trigger system
- Highspeed data transfer
- Reference clocks
- Power over Ethernet to supply the PCU

Cables:
Institute of High Energy Physics

- 100m CAT5 Ethernet cable

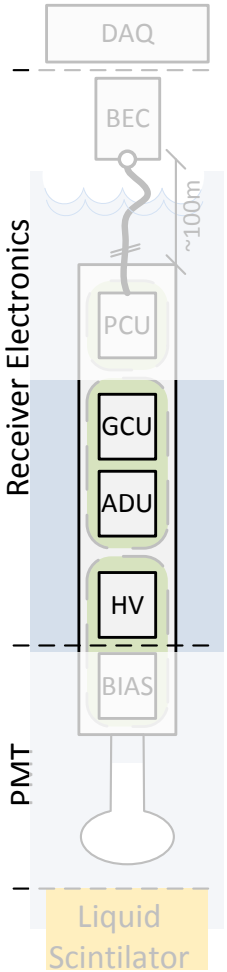
Power Control Unit (PCU):
RWTH Aachen Experimentalphysik III

- Supplying all local electronics
- Separating the clock from the powerfeed

Trigger system:
Tsinghua University

- Global trigger generation

Receiver Chain Details cont'd



General Control Unit (GCU):

Instituto Nazionale di Fisica Nucleare, Università di Padova

- Connection to the BEC and control of the HV and ADU
- LVDS signal interface to the ADU
- Dedicated fast memory (2GB) for local signal storage (supernova)
- Configurable digital processing of the signal and signal over threshold generation

Analog to Digital conversion Unit (ADU), Vulcan System on Chip:

Forschungszentrum Jülich, ZEA-2

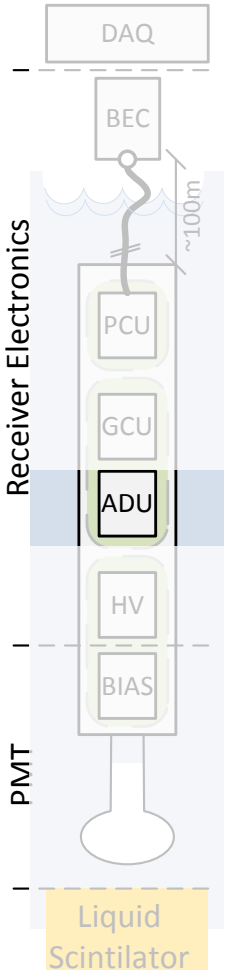
- Highly linear, low noise receiver
- 3 - 8bit, 1Gb/s Flash ADC with programmable characteristics
- Programmable data reduction and low jitter clock generation
- Configurable trigger schemes, overshoot compensation
- All integrated regulators w/o external capacitors for all internal supplies

High Voltage Unit (HV)

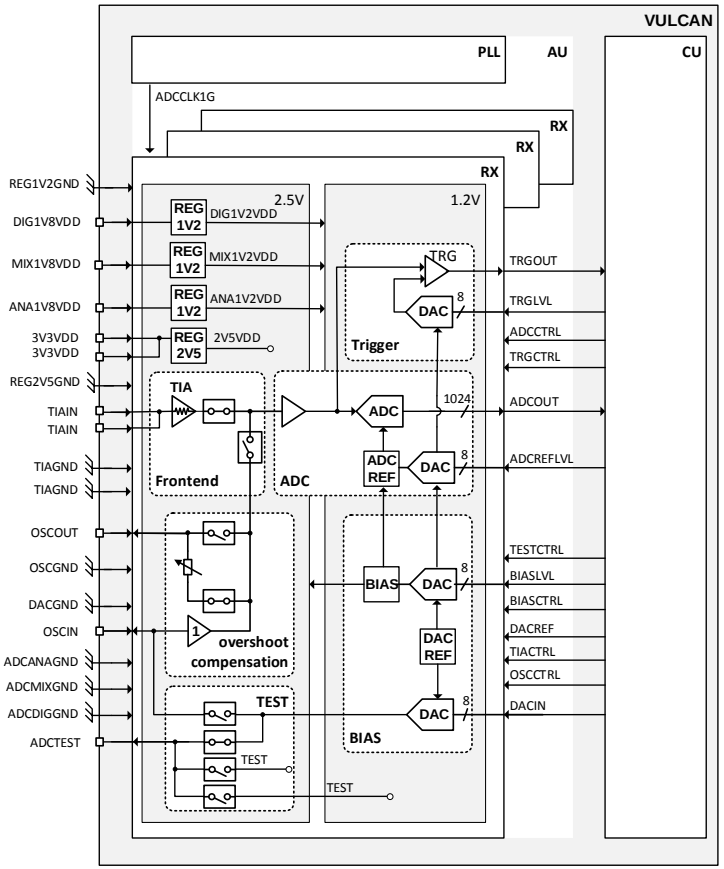
Joint Institute For Nuclear Research

- 2kV Bias Voltage for the bias circuitry of the PMT

System Architecture of Vulcan SoC

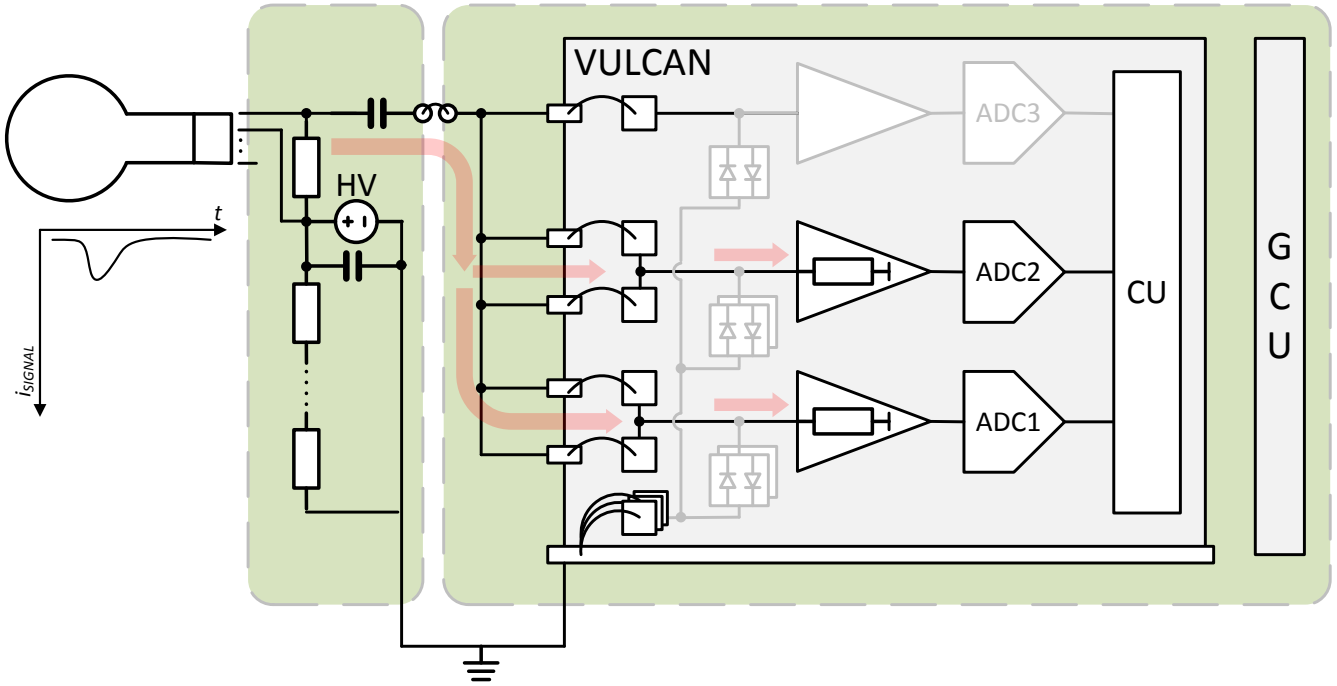


1. Approx. 80dB linearity by using 3 signal chains for 3 different signal ranges
2. Control loop to suppress DC variations for increased dynamic range and reduced noise
3. On chip clock generation from reference clock
4. No analog delay line, reducing noise and distortions
5. Flexible solution for different applications
6. Overshoot compensation
7. No external components needed

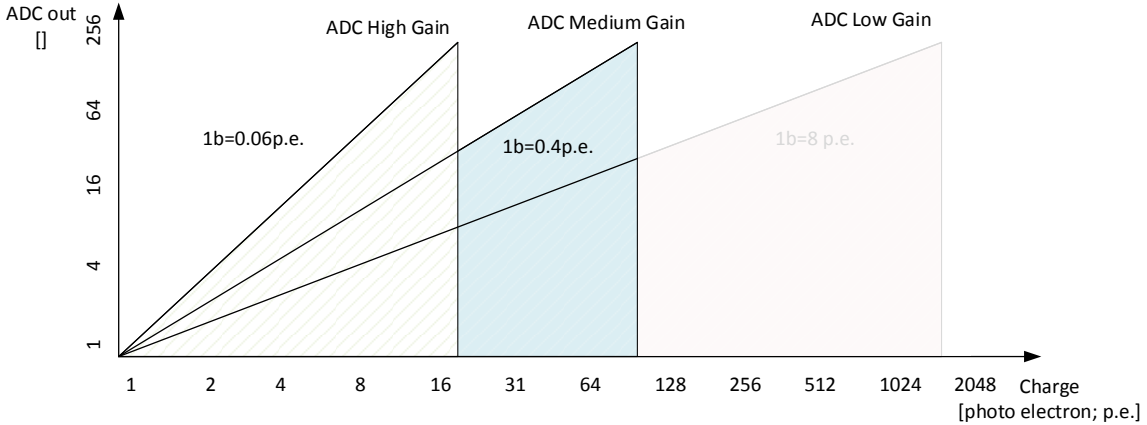


SoC is named after Vulcan, the son of Juno in ancient Greek mythology

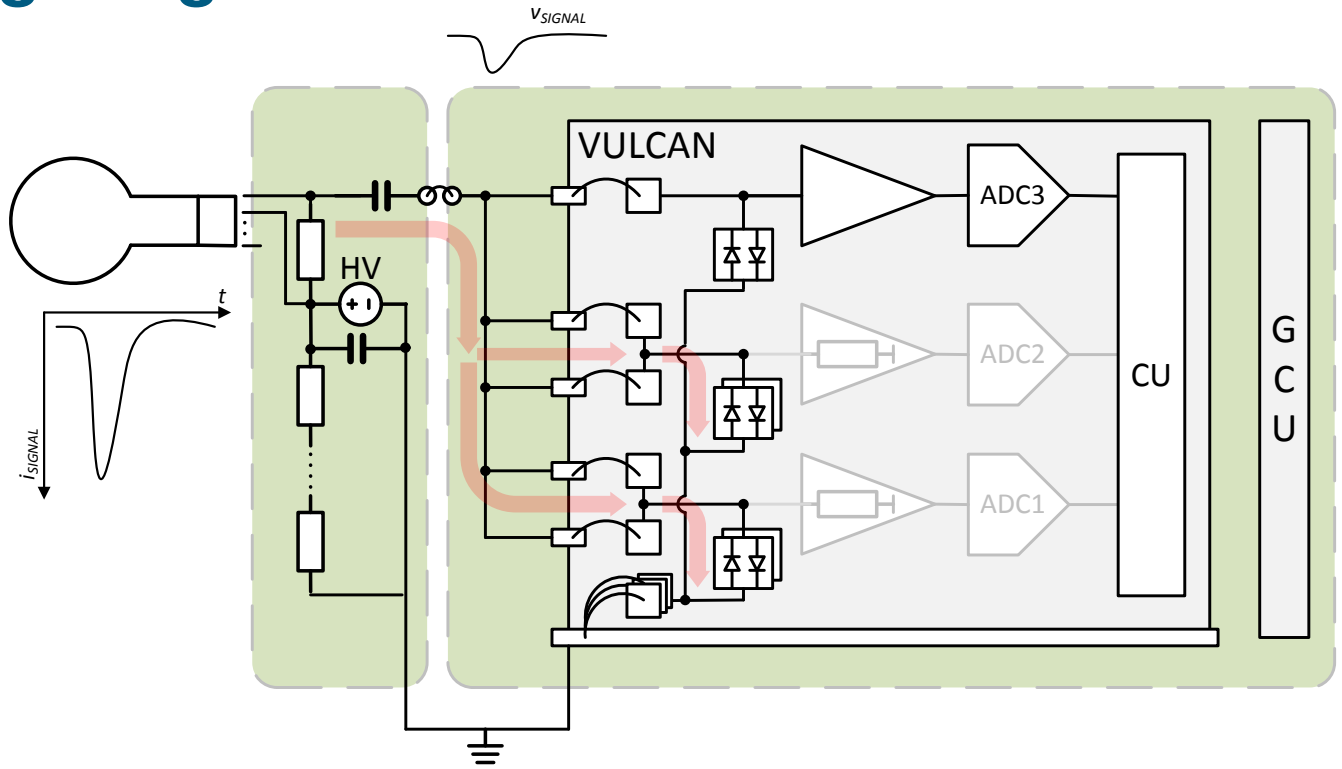
Small Signal Mode



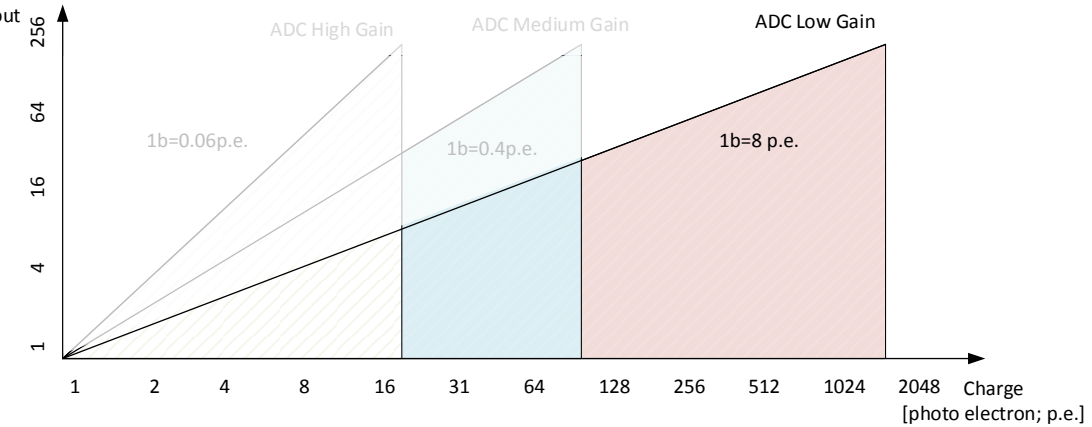
Two signal chains with programmable gains and parallel TIA inputs, combined input resistance R ≈ 5Ω



Large Signal Mode



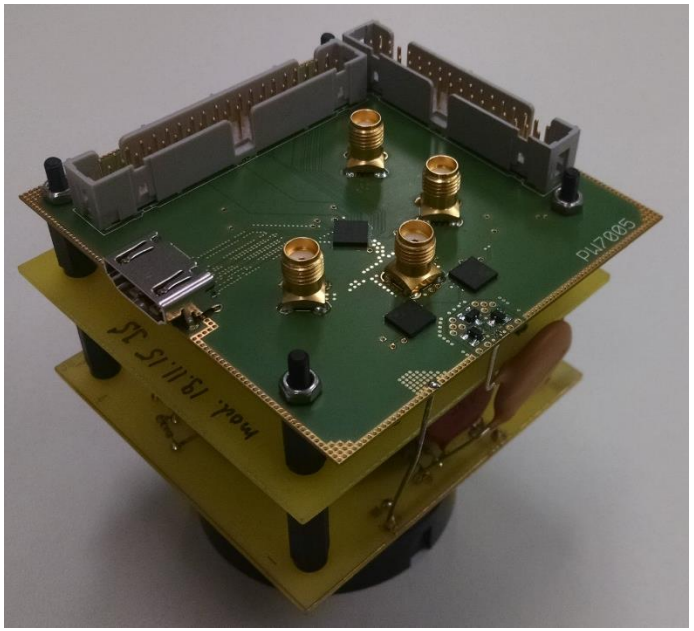
With larger input currents >20mA the TIA inputs saturate, the ESD diodes open with a combined resistance R ≈ 5Ω, The voltage over the diodes is measured with the third signal chain



Concept Verification by FE-Prototype

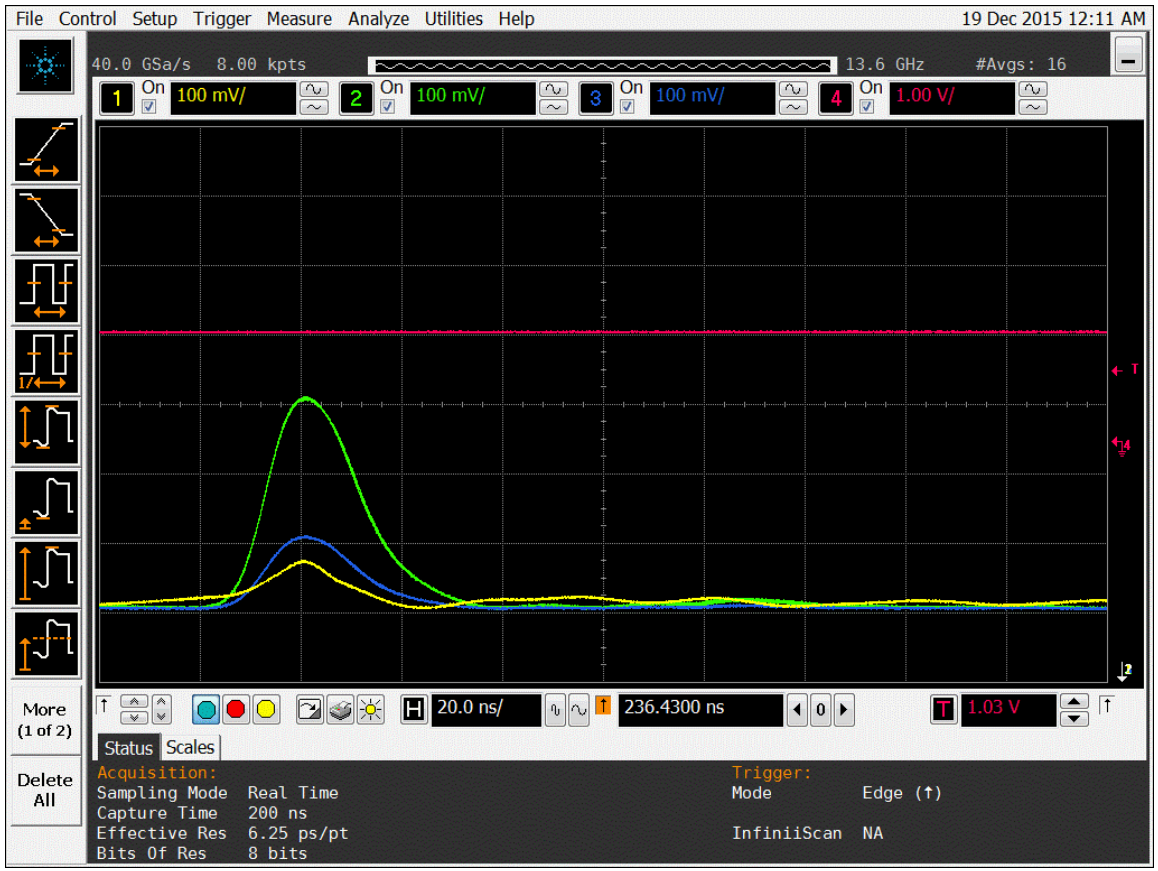
Hamamatsu R12860, dark box, HV and function generator provided by Physics Institute III B, RWTH Aachen

Demonstrator board containing two TIAs, voltage buffer, ADC and diodes attached to Aachen base



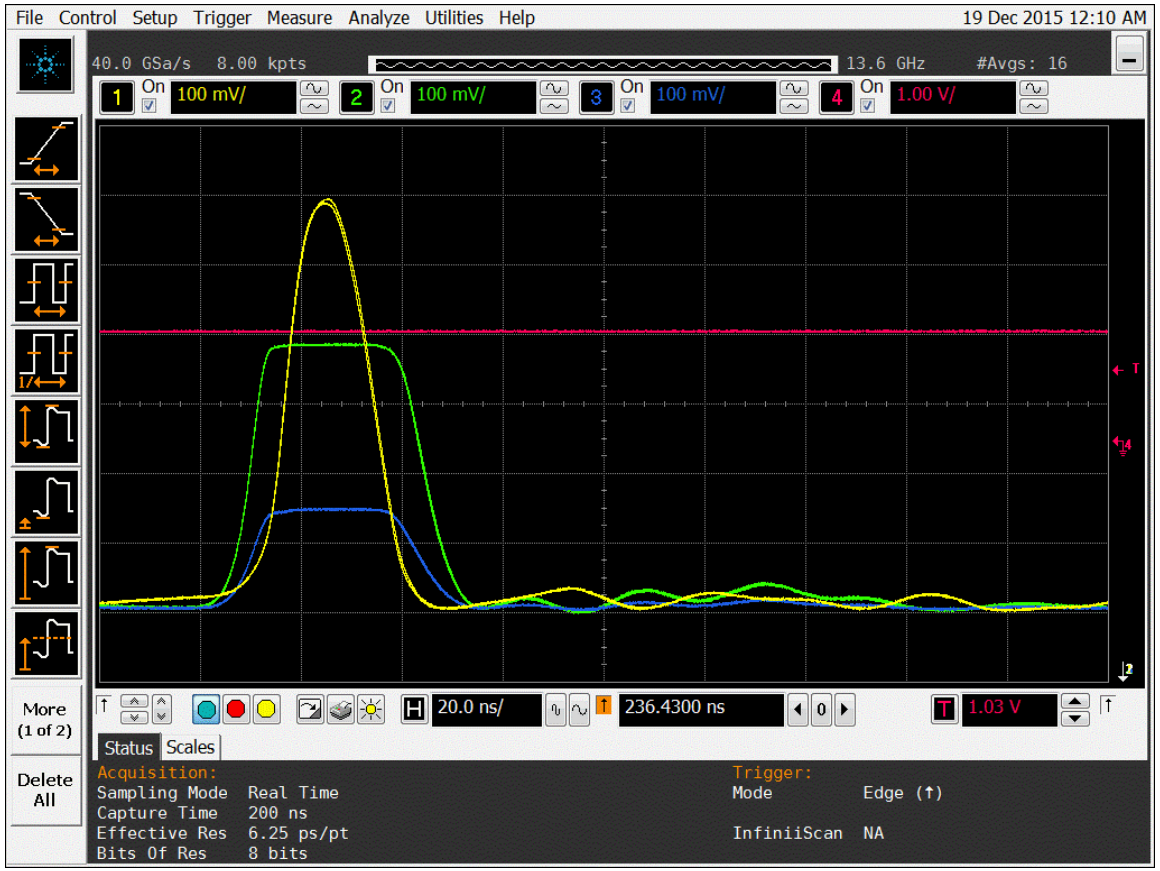
FE-Prototype:
Output Signals @ Low Occupancy

- Best result by high gain amplifier (green)
- Low gain amplifier (blue) and buffer (yellow) provide similar signals at low amplitudes



FE-Prototype:
Output Signals @ High Occupancy

- High gain amplifier (green) and low gain amplifier (blue) clip
- Buffer (yellow) still provides useful output signal



Noise Requirements

From the Conceptual Design Report (CDR):

- Noise level should be below $0.1\ \mathrm{pe}$ for single photoelectron detection.

Vulcan: $8\ \mathrm{bit}$ for $16\ \mathrm{pe}$ – equivalent input noise of the TIA is much smaller than one LSB: $I_{noise} \ll LSB$.

ENOB	pe	Resolution [1/pe]
8	16	0.0625
7,33	16	0.1
7	16	0.125
7	14	0.109

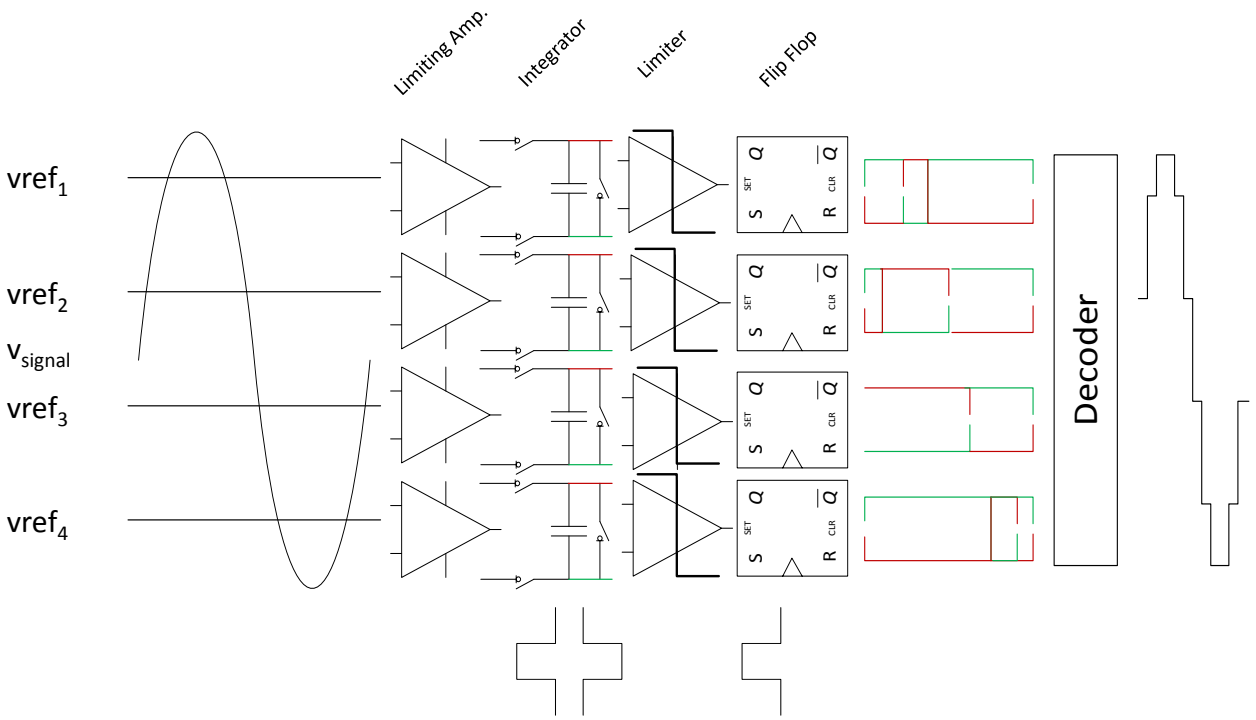
Time Resolution Requirements

From the Conceptual Design Report (CDR):

- Waveform sampling should be available over the whole energy range with a sampling rate of $1\ GS/s$.
- Arrival time resolution, e.g. by fitting of the signal leading edge, should be $\sigma_t \approx 100\ \mathrm{ps}$.

Vulcan: ADC Sampling Clock 500 MHz using both edges

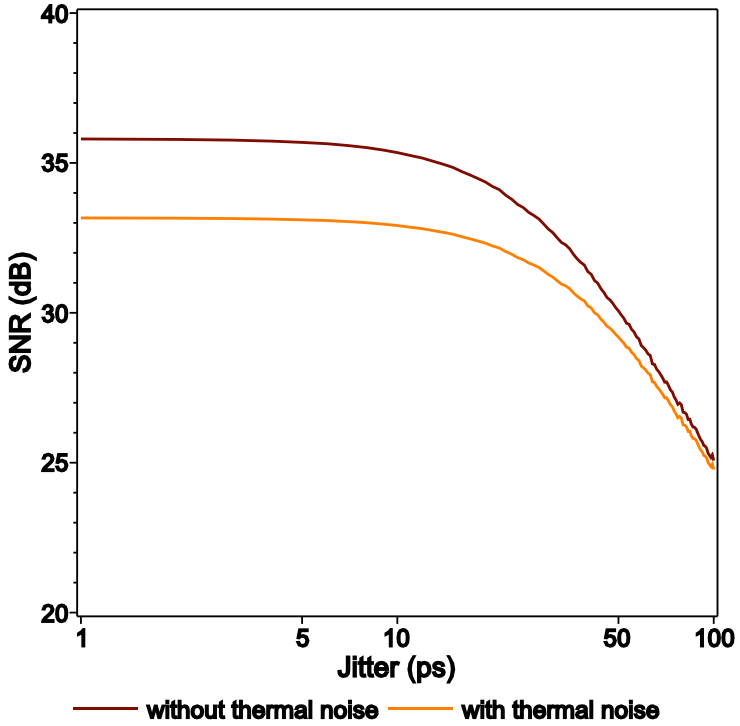
Integration after sub-ranging with respect to 4 voltage references



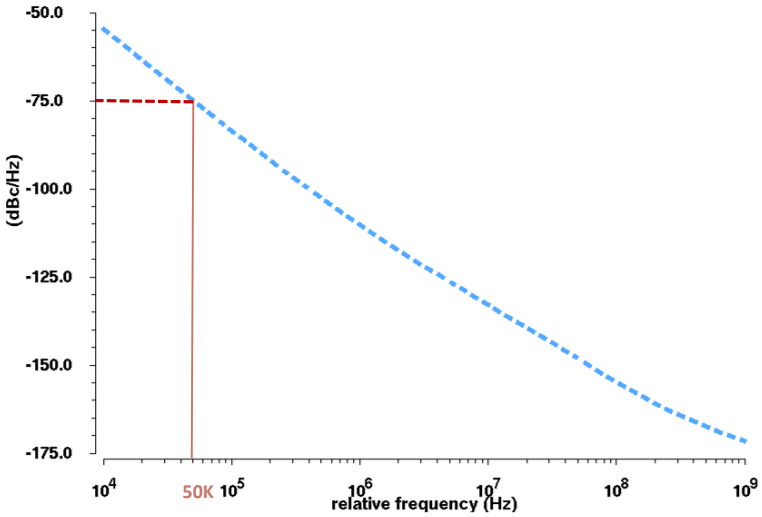
Concept Verification by Test-Chip: PLL

Initial jitter requirement: $t_j < 100\text{fs}$

Requirement (sim. results)



PN spectrum (test-chip)



RMS JITTER ≈ 0.58ps

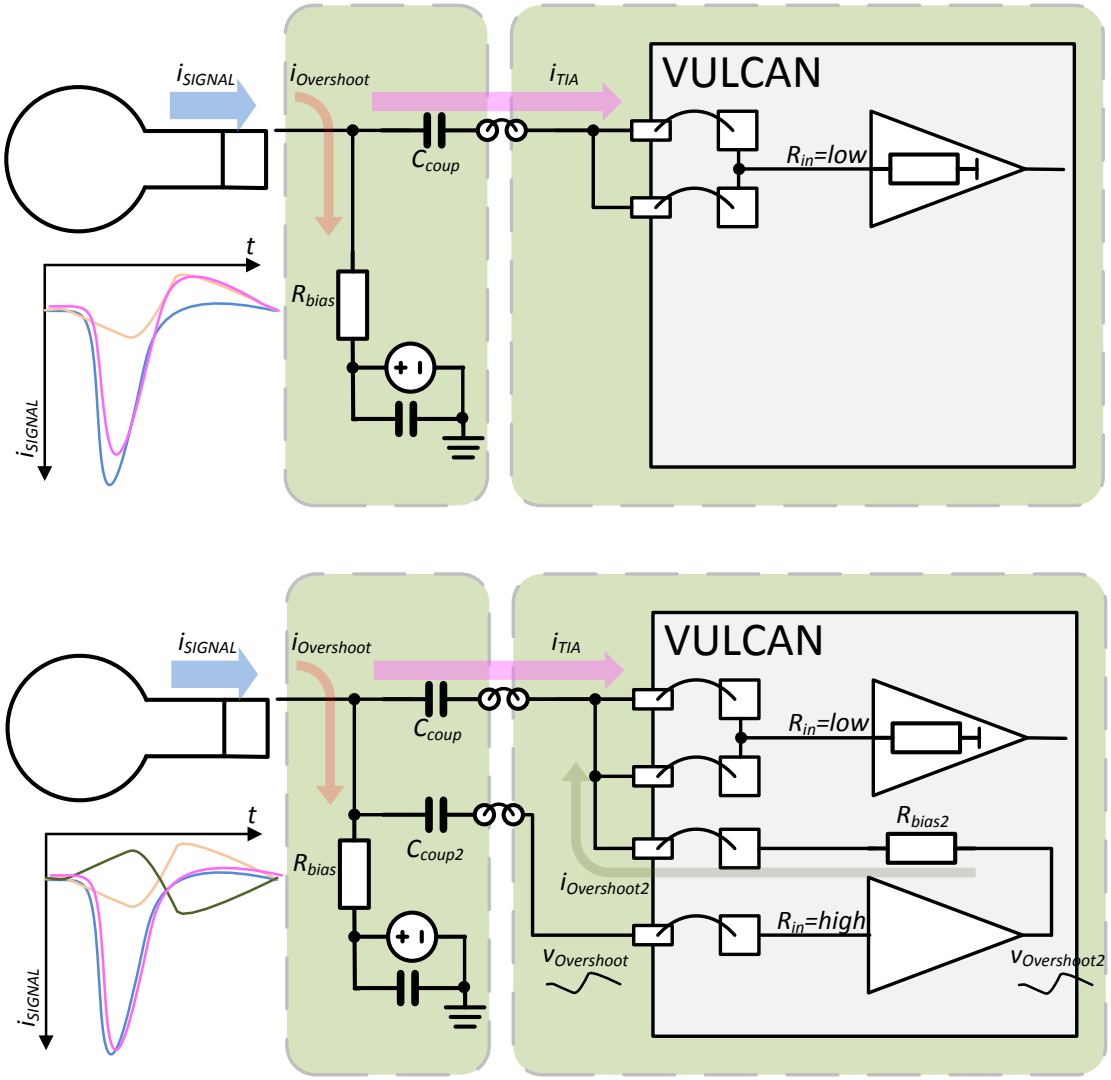
Overshoot Compensation

The signal is distorted by the AC coupling at the PMT, causing inter symbol interferences and reducing the signal to noise ratio (Signal Overshoot).

Vulcan features an integrated compensation for the Signal Overshoot:

- Sensing the voltage over the bias resistor
- Compensation current is generated on a copy of the bias resistor
- Needs additional coupling capacitance at the bias resistor

(patented)

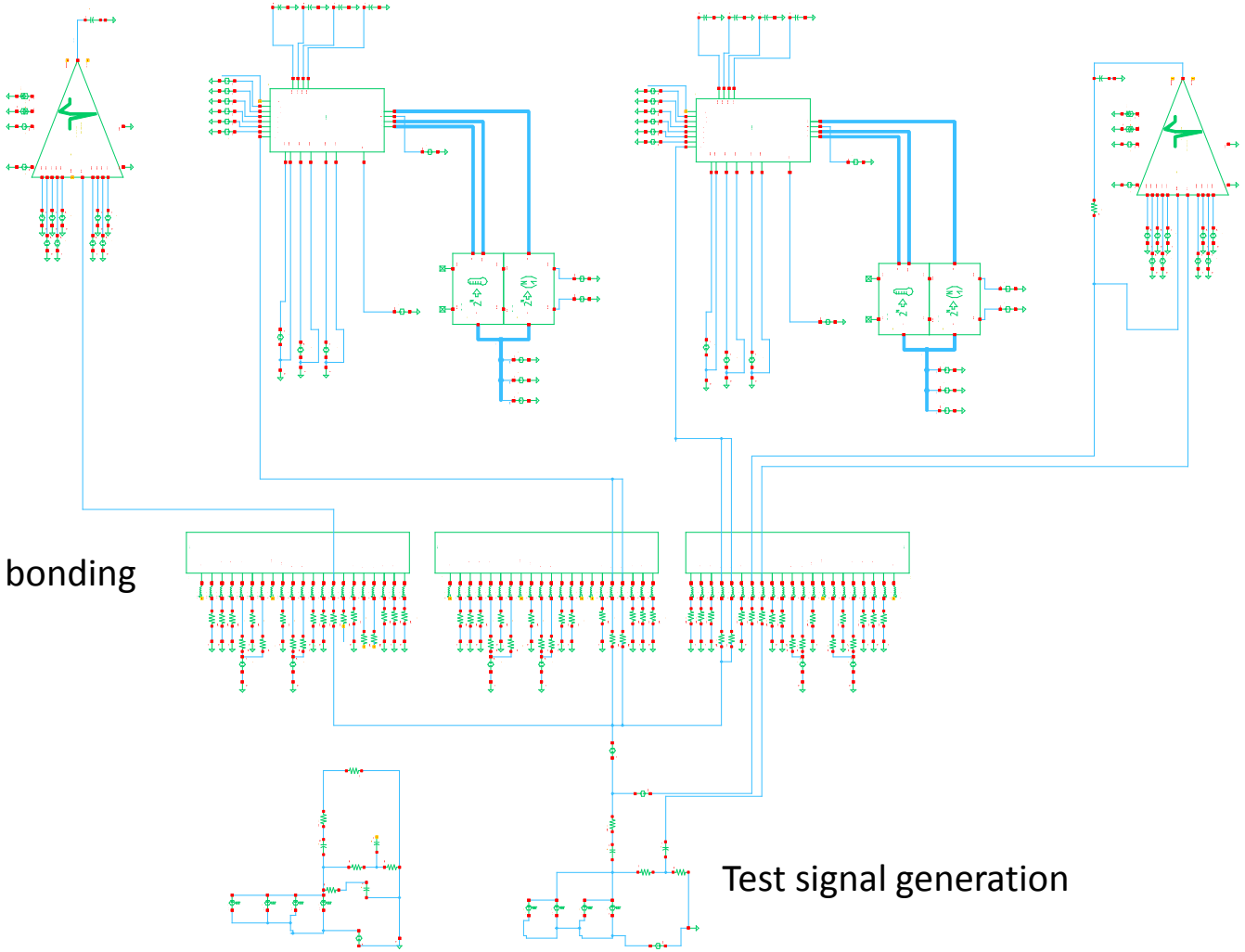


OSC Implementation VULCAN

Low gain voltage buffer

Medium and high gain TIA

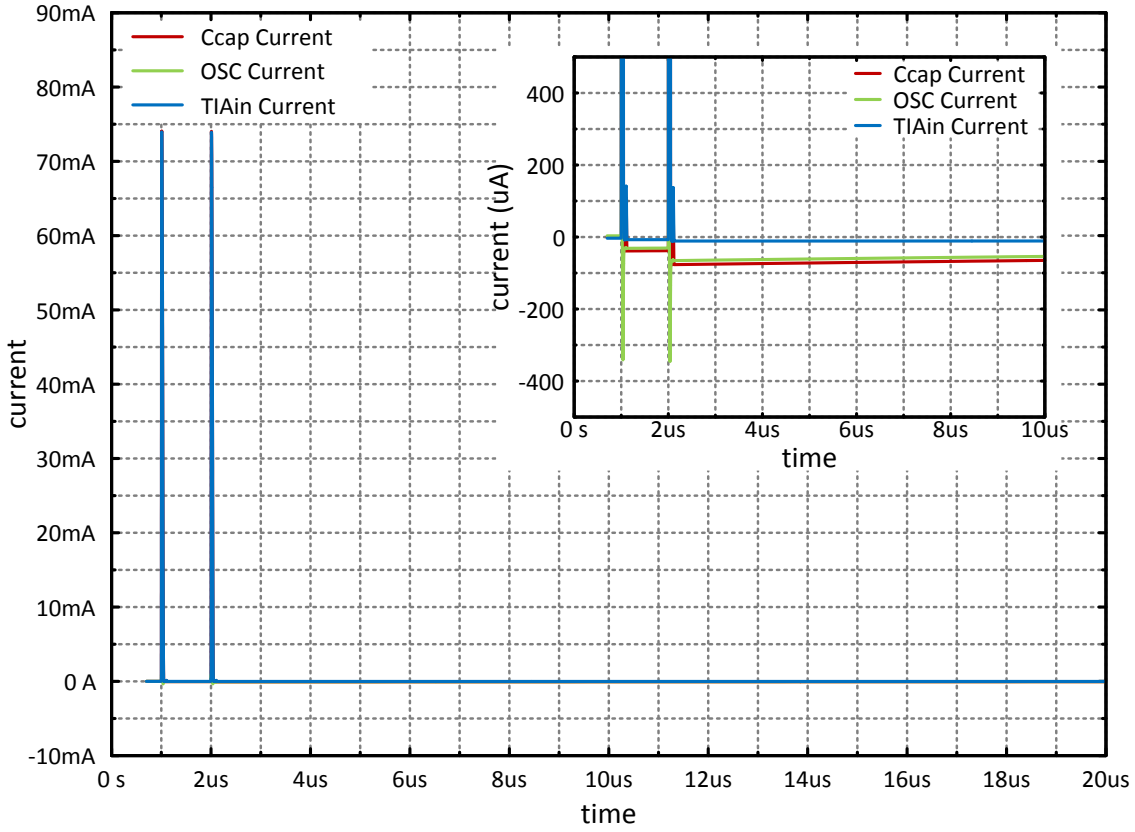
Overshoot compensation buffer



Package and bonding modell

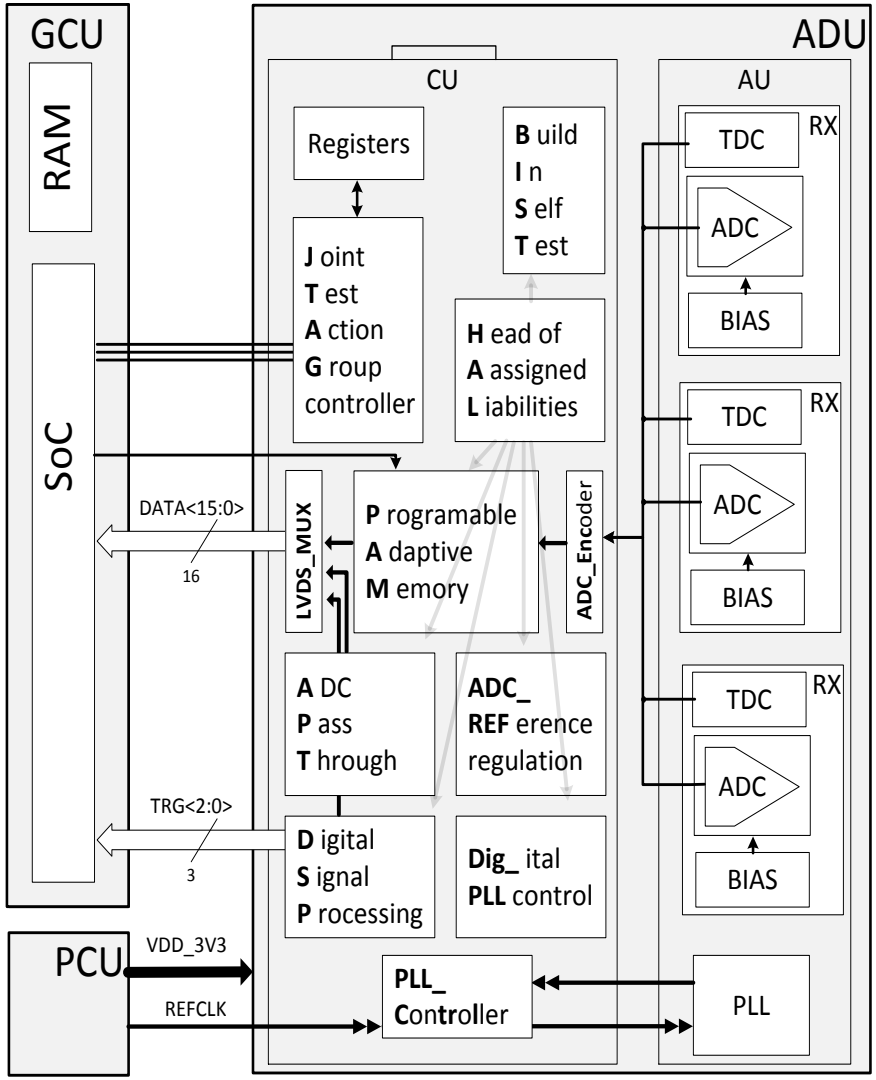
Test signal generation

Special Feature: OSC Sim Results VULCAN

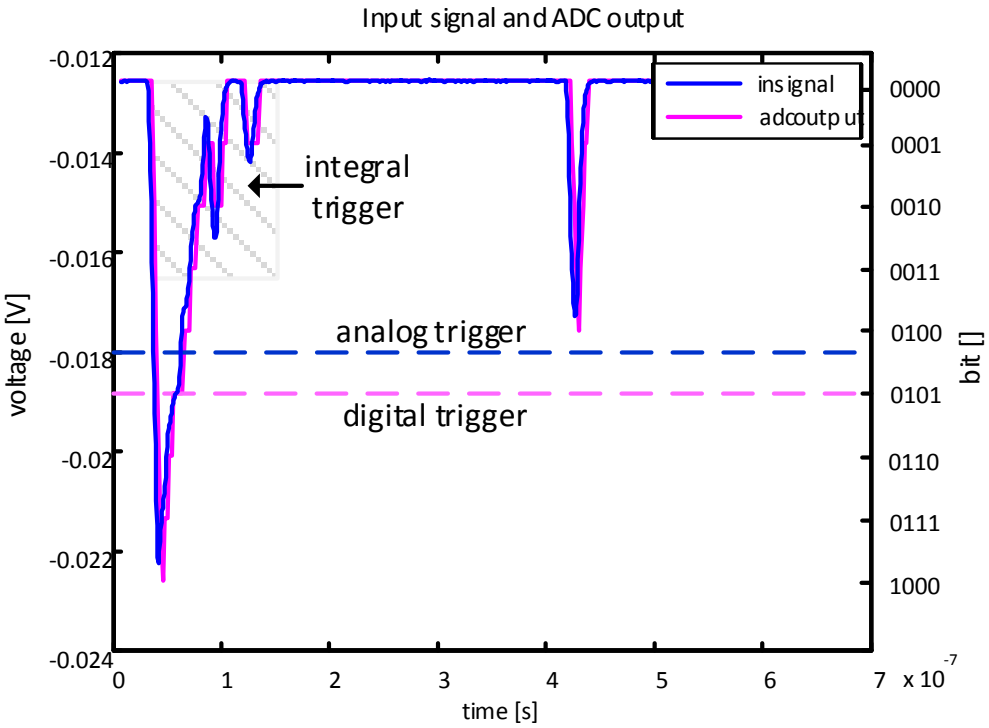


Features of the Digital Part (CU)

- Start-Up Controller (HAL)
- ADC Regulator (ADC_REF)
- Digital PLL Controller (DIG_PLL)
- Build-In Self Test (BIST)
- ADC Encoder (ADC_ENC)
- Main Data Processing (PAM)
- Trigger Generation (DSP)
- LVDS Multiplexer (LVDS)



Configurable Approach: Signal over Threshhold



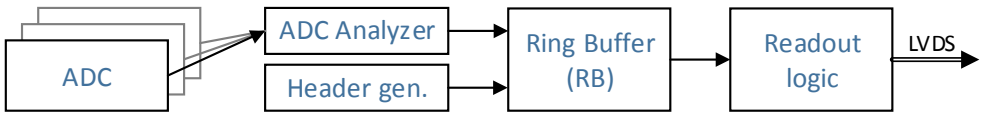
3 LVDS trigger lines are available one for each of the 3 ADC
Configurable trigger modes:

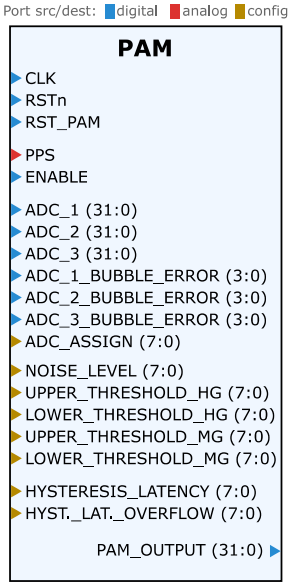
- Analog voltage comparator for fastest trigger
- Digital threshold value
- Integrating the last 8/16/32 values and compare with digital threshold

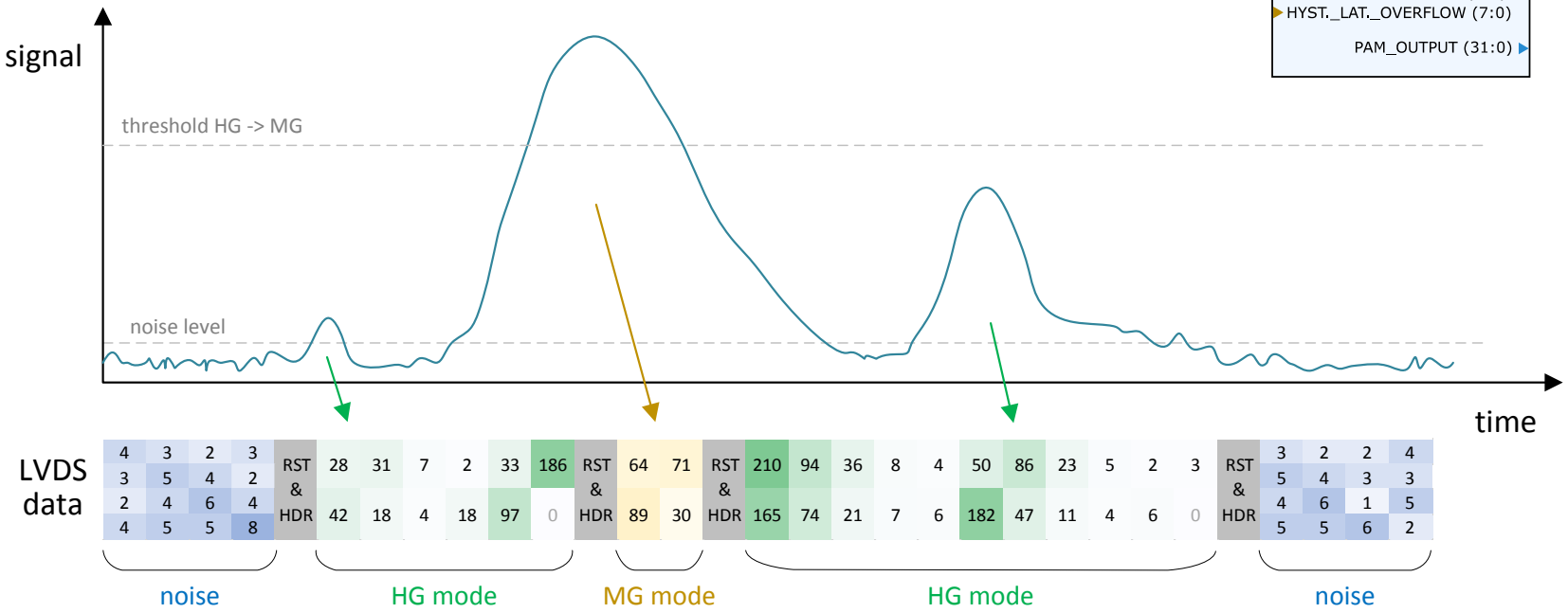
Main Data Processing (PAM)

- Purpose:
  - Select ADC gain mode and buffer data
  - Generate meta information (timing, modes, etc.)
  - Minimize output data by selecting relevant information

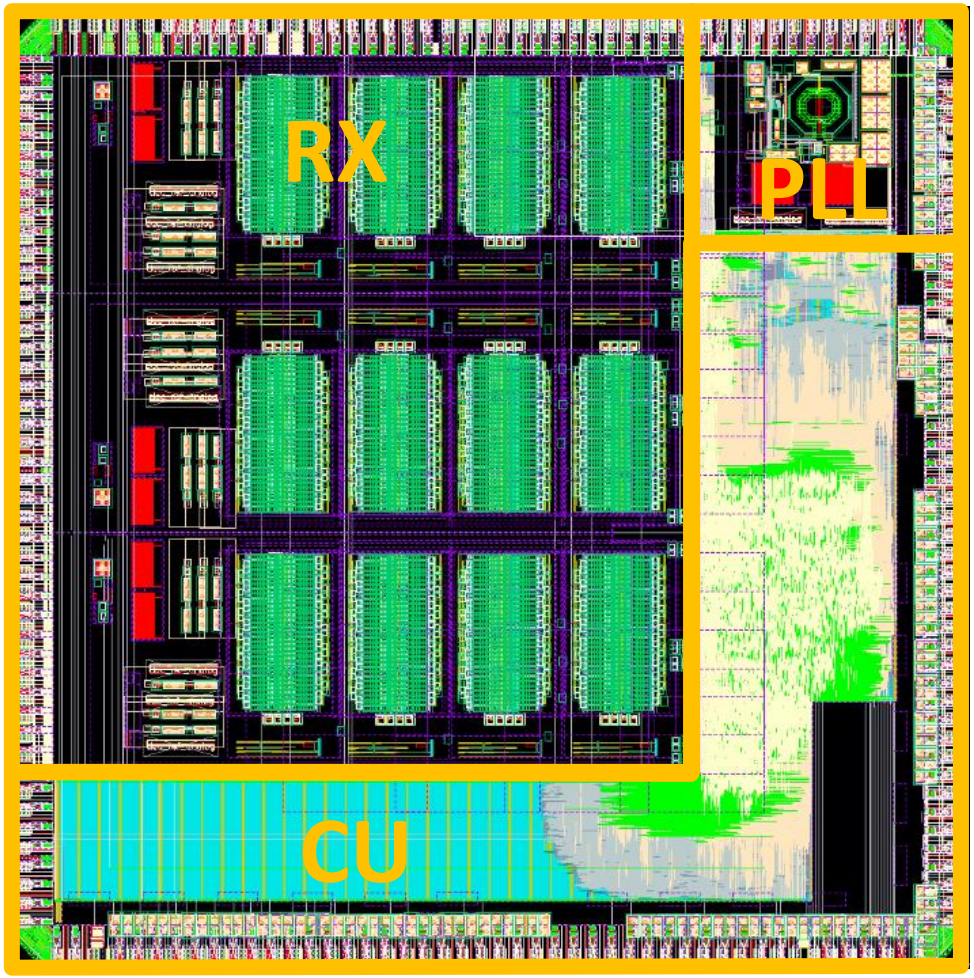
  Basic PAM structure:

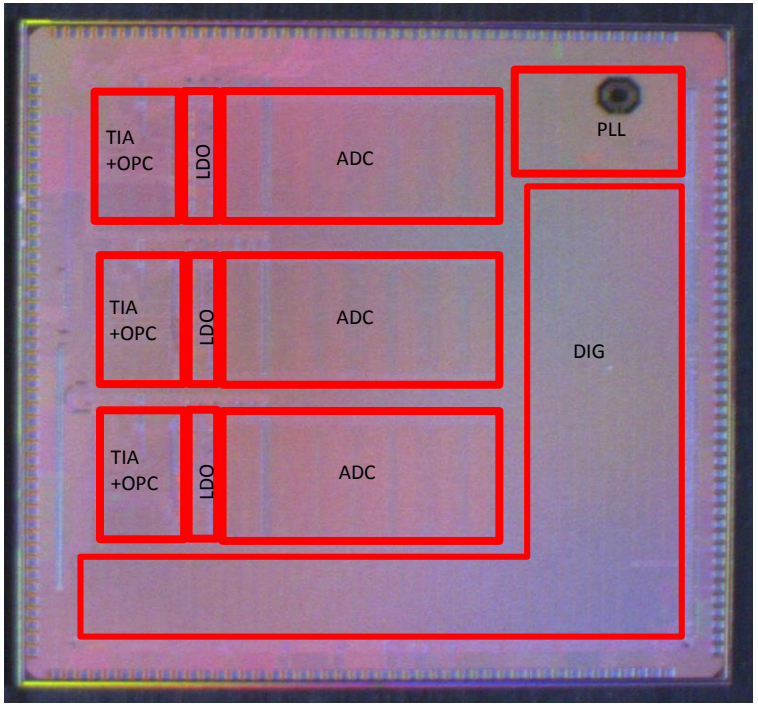






Chip Layout and Photo

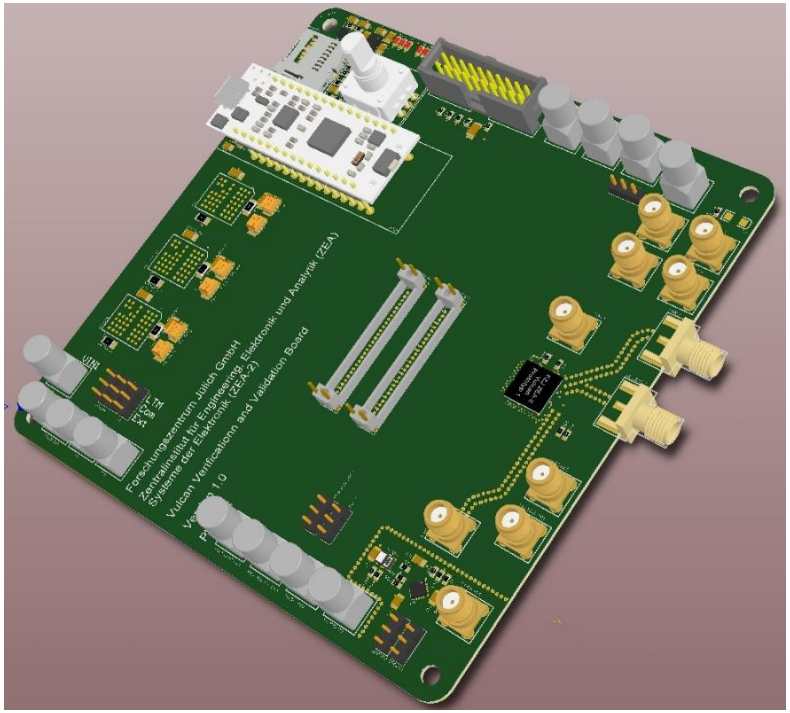




Area = 4.5mm * 4.5mm
Technology = 65nm TSMC

Current Work and Outlook

- Application Engineering
- Definition of measurements and verification support
- Examination of redesign potential / future circuitry
- Review of measurement and application boards
- Model preparation of digital part to be used in firmware development
- Silicon Back estimated mid of November
- Prove of concept measurements (Receiver chain and PMT) in Q1 2017



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