Development of Electronics for the Hyper-Kamiokande Experiment

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For
Hyper-Kamiokande Proto-Collaboration

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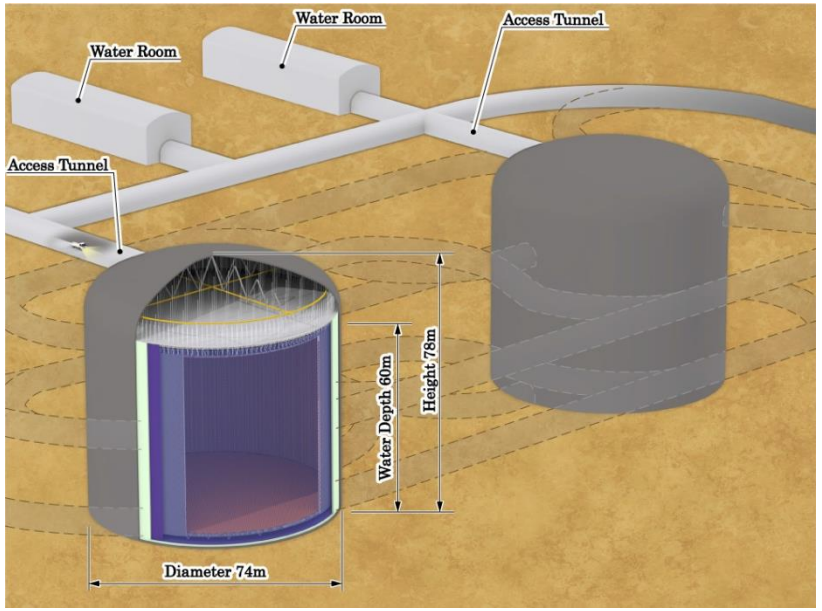
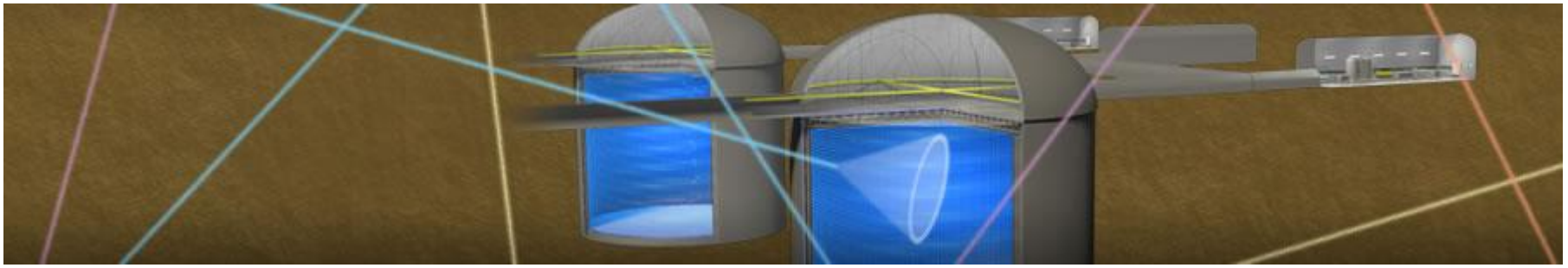
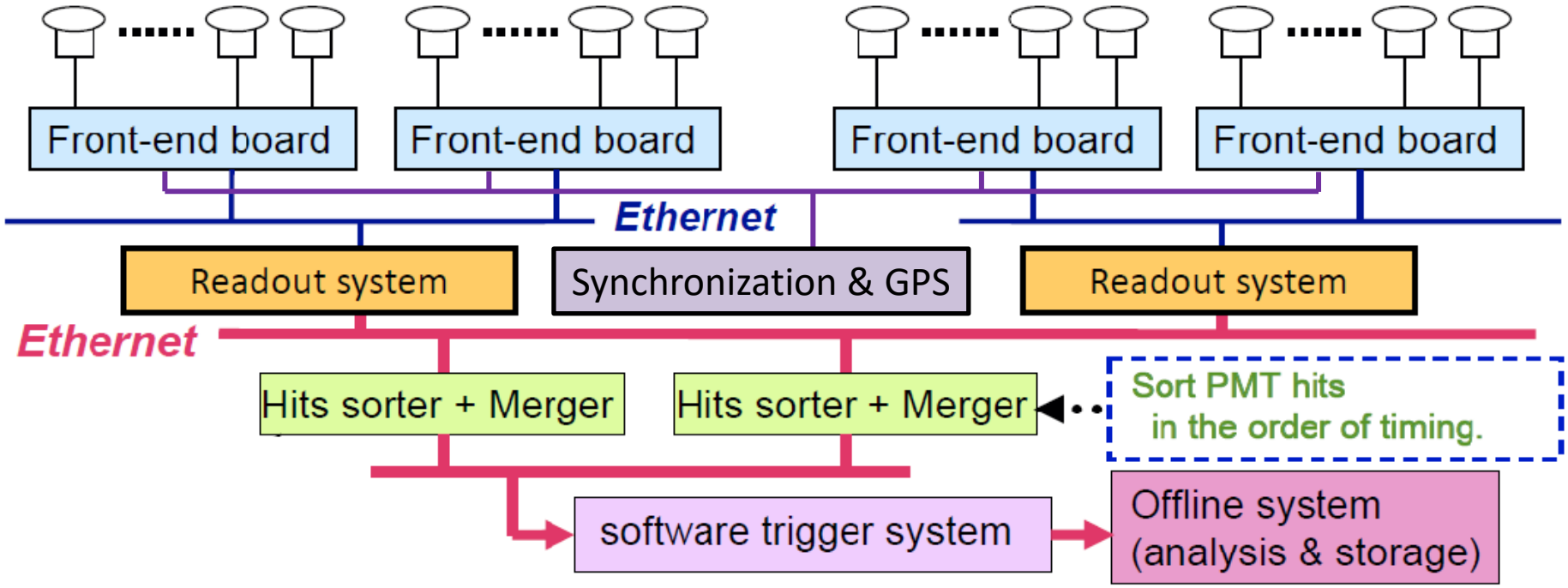
Introduction – Hyper Kamiokande

- Giant underground water Cherenkov Detector
  - Two tanks, ∅=74m, H=60m
  - ≈520kt of ultrapure water
  - 93,400 photo-sensors (80,000 ID + 13,400 OD)
- Role of photo-sensors and electronics:
  - Measure charge and timing of pulses coming from Cherenkov photons.





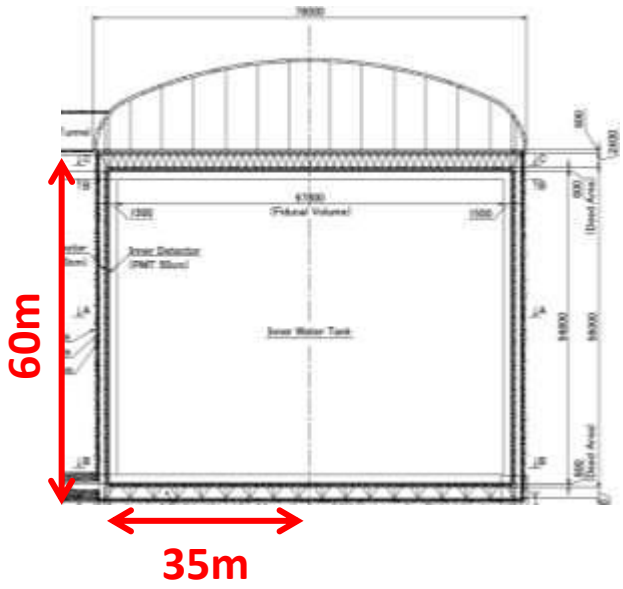
Overview of the System



- Self-triggering system
  - Digitize all photo-sensor signals above discriminator threshold
  - Send hit information to readout computers
  - Use software trigger for event selection & send them to offline system for storage
- Accurate clock synchronization and GPS
- Stable power supplies (photo-sensors, other systems)

Location of Frontend Electronics

Option 1 – detector's roof



ADVANTAGES:

- Serviceability
- More options for accommodating power-hungry electronics

DISADVANTAGES:

- Length of cables:
  - 40 m (bottom) + 65 m (wall) + 40 m (surface) ≈ 150 m
  - Expect degradation of the signal
  - Different length of cables may make calibrations difficult
- Weight of cables
  - 100~200 g/m → 150 m ≅ 15~30 kg → **675~1350 tons!**
  - Non-negligible weight
  - Affects design & cost of the structure

Location of Frontend Electronics

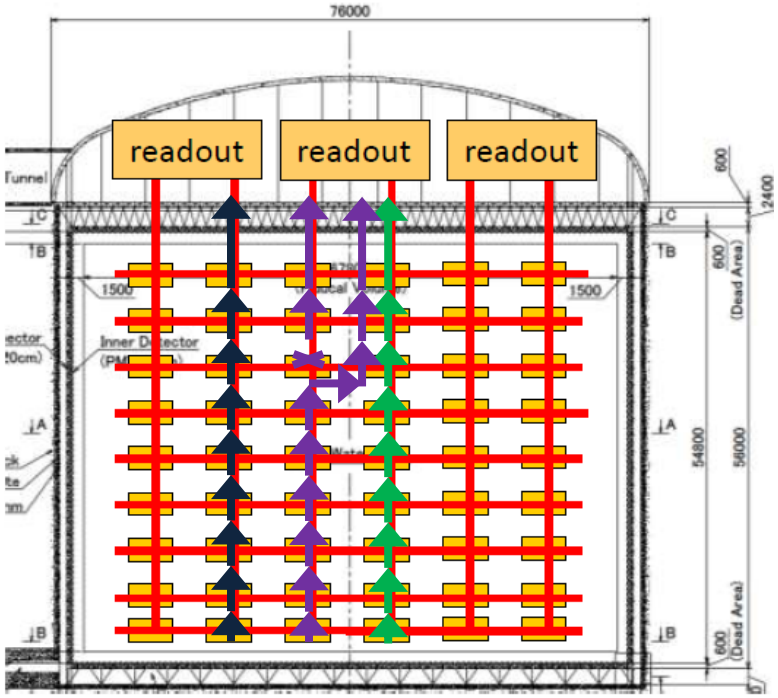
Option 2 – water (current baseline design)

ADVANTAGES:

- Shorter cables
  - Better signal quality
- Smaller number of cables
  - Savings on weight and structure costs

DISADVANTAGES:

- Hydrostatic pressure at the bottom of the tank (~6 atm)
- Poor to none serviceability
  - Extreme reliability is a must!
- Limits for power consumption
  - Heat dissipation affects water circulation



Mesh-type connection

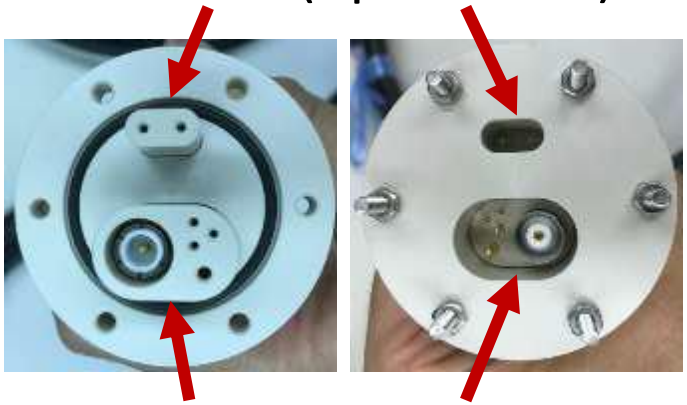
- Avoid single point of failure
- Lower module transmits data to upper module; if unable, then to its neighbors
- On-going R&D on protocol and expected data rates

Cables and Connectors

R&D on water-tight connector

- HV lines (up to 10kV)
- LV, GND & signal lines

HV lines (up to 10kV)

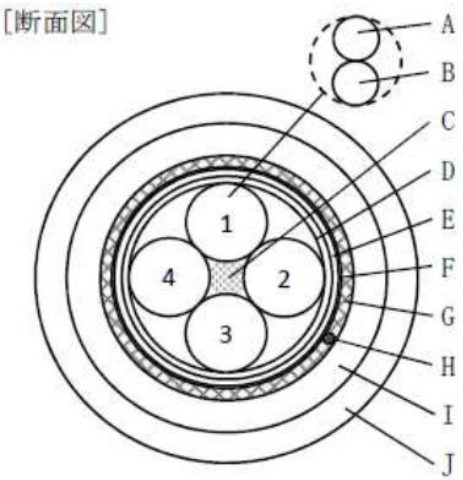


LV, GND and signal lines

Design of the outer shell is universal and can accommodate various connectors, e.g. Ethernet, optical fibers, power lines.

Pressure tolerant Ethernet cable

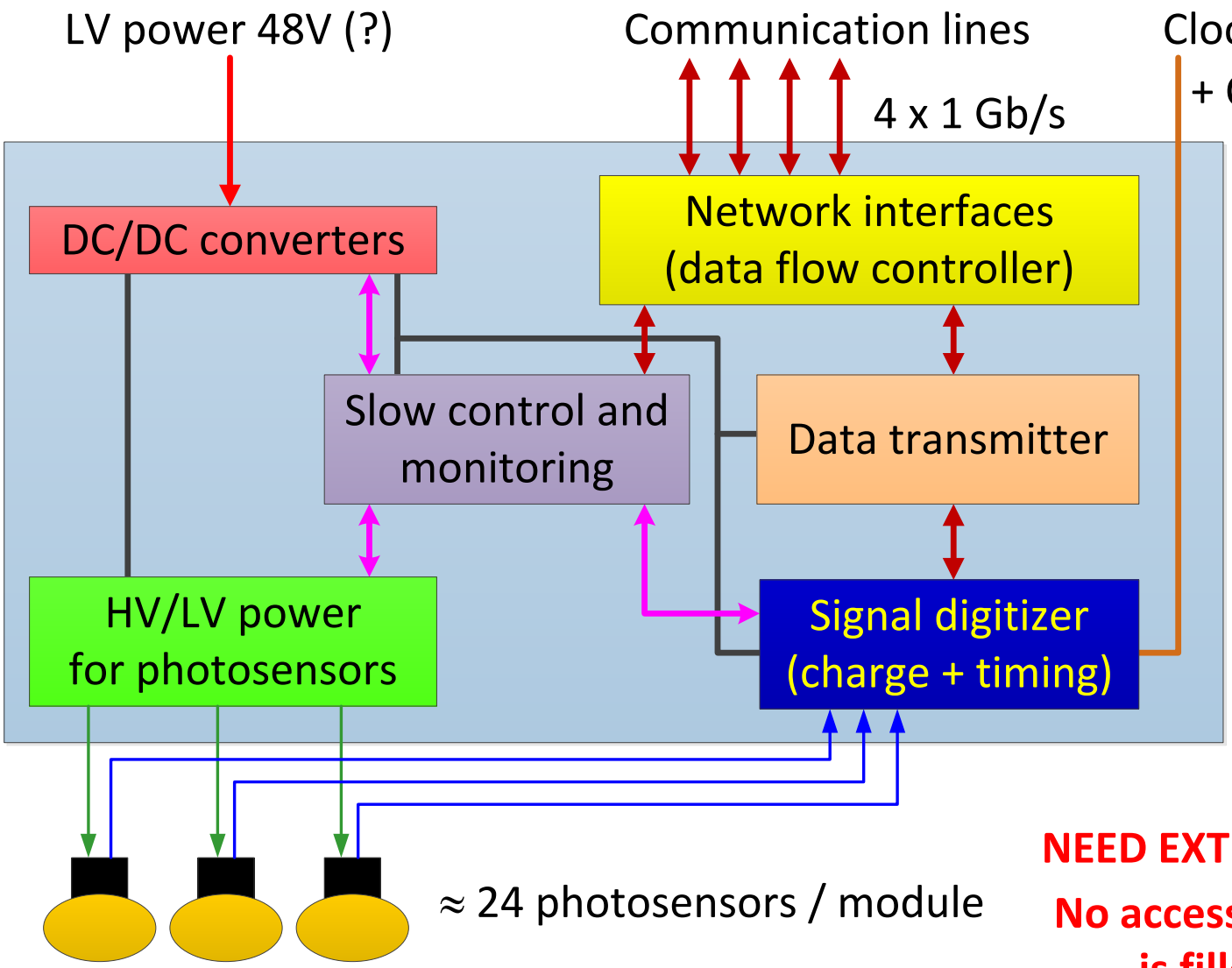
Prototype ordered, tests are on-going!



4 pairs, ~90 g/m

Standard Ethernet cable is unsuitable, because it gets compressed and does not transmit differential signal properly.

Frontends – Module



≈ 24 photosensors / module

All in water-tight chassis

Entire chassis probably filled with silicon or other material

Estimated weight of chassis + filler + board (size ≈9U VME) is ≈ **43 kg**

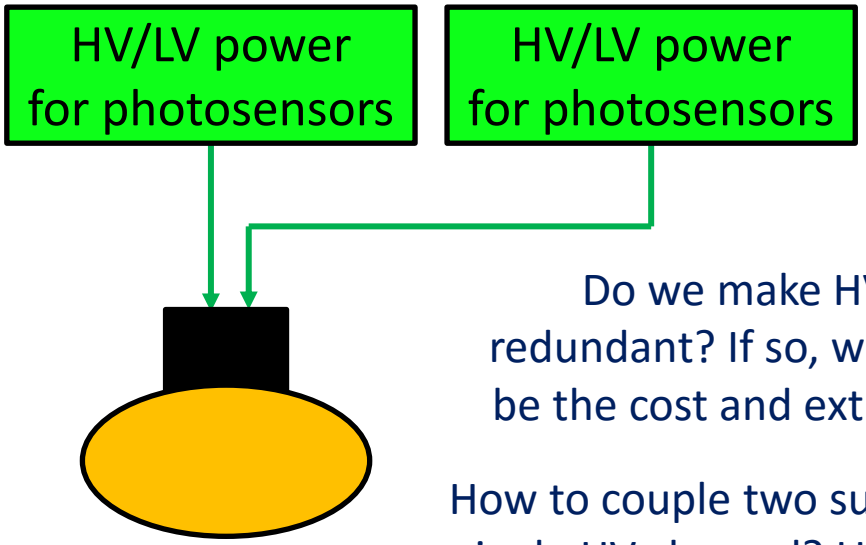
NEED EXTREME RELIABILITY!

No access once the detector is filled with water!

Frontends – Reliability

- Need reliable operation for approx. 20 years
- Extensive R&D foreseen to identify most risky components
  - What is the risk of failure?
  - Should certain elements be redundant?
  - How to provide redundancy and at what cost?

HV SUPPLY

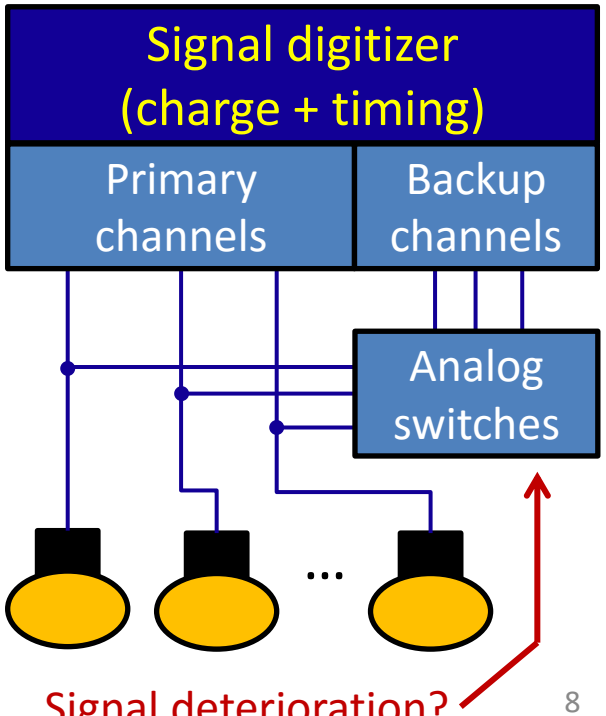


Do we make HV supplies redundant? If so, what would be the cost and extra power?

How to couple two supplies into a single HV channel? Use Diodes? Is it at all possible for HPD (8kV)?

Will we actually increase reliability?

SIGNAL ACQUISITION



Digitization Requirements

- Performance determined by photo-sensors and not by readout
  - σ(time) < 10% of photo-sensor TTS; σ(charge) < 0.05 pC.
- No dead time (or at least minimized dead time)
- Self triggering

$$BW \cong \frac{0.35}{t_r}$$

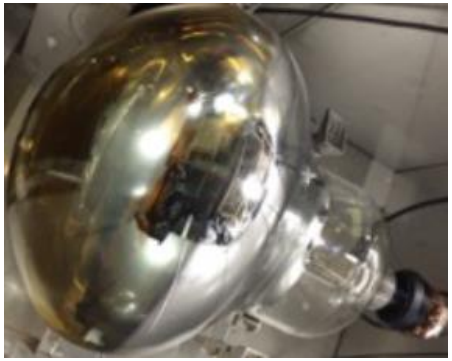
t_r = 10%–90% rise time

→ *Talk by Nakayama-san*

20” High QE Box&Line PMT

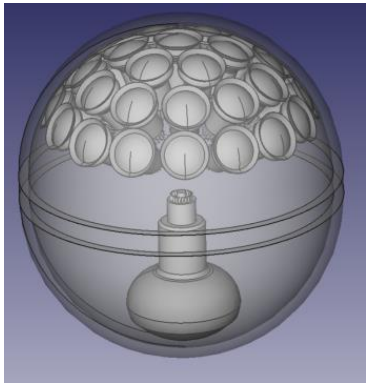
t_r = 6.8 ns
BW ≅ 52 MHz
TTS 1 p.e. (σ) = 1.7 ns

20” High QE HPD with ∅20mm AD



(*) t_r = 16 ns
BW ≅ 22 MHz
TTS 1 p.e. (σ) = 1.6 ns

multi-PMT (specs. for 3” PMTs)



t_r = ~2.5 ns
BW ≅ 140 MHz
TTS 1 p.e. (σ) < 1 ns (?)

(*) Rise time and TTS are limited by a pre-amplifier. Intrinsic TTS is ~1ns.

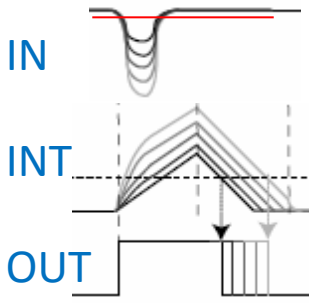
Digitization Options

Option 1
QTC + TDC

Signal from PMT

Option 2
Waveform sampling

QTC



Discriminate to get a trigger. Start the output pulse

Integrate the pulse.

Start discharging. Stop the output pulse once discharged.

Use TDC to record beginning and end of the square pulse.

Shape the pulse.

Optional

Sample the pulse.

Digitally filter the pulse.

Optional

Use digital signal processing for triggering and estimation of time of arrival & pulse charge.

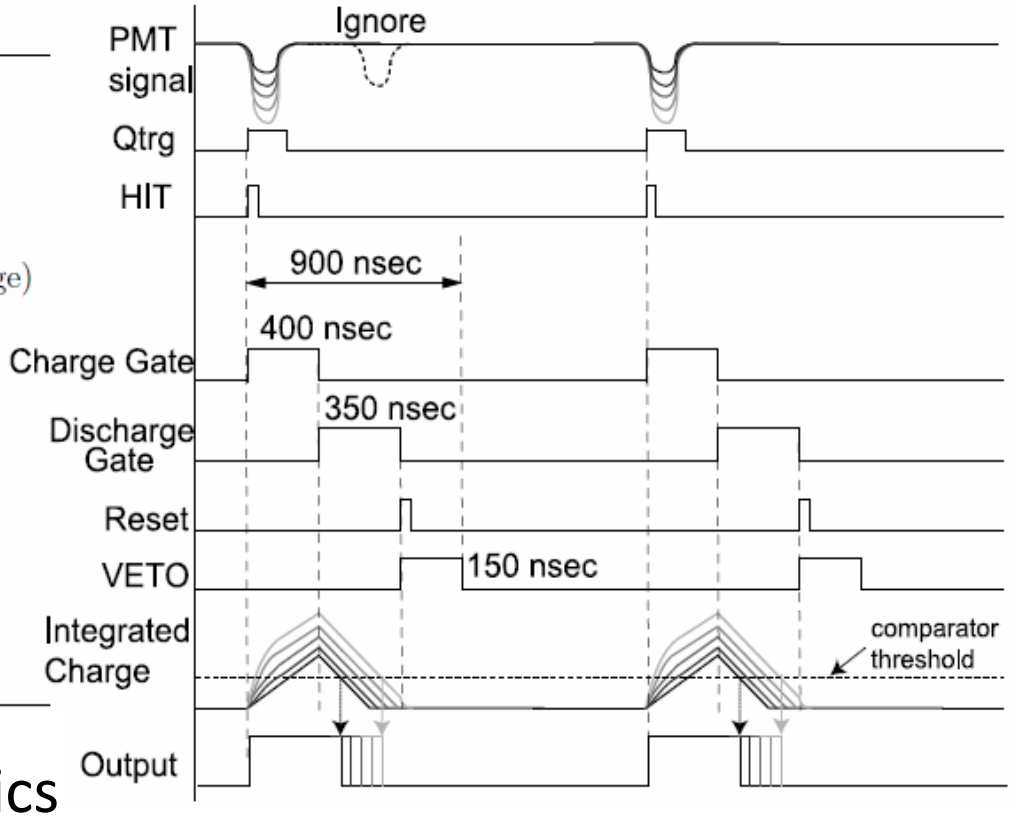
Time & Charge

TDC = Time to Digital Converter
QTC = Charge to Time Converter

Digitization – QTC + TDC

Table 1: Specification of the QTC

Type of trigger	self trigger by discriminator
Number of Input Channels	3
Processing Speed	$\sim$ 900 ns/cycle
Charge Integration Gate	400 ns
Number of Gains	3 (Ratio 1 : $\frac{1}{7}$: $\frac{1}{49}$)
Discriminator Threshold	$-0.3 \sim -14$ mV (small range)
Charge Dynamic Range	$0.2 \sim 51$ pC (small)
	$1 \sim 357$ pC (medium)
	$5 \sim 2500$ pC (large)
Charge Resolution	~ 0.2 pC (small)
Integral (Non-)Linearity	$< \pm 1\%$
Timing Resolution	0.3 ns (2 pC, -3 mV)
	< 0.1 ns (> 100 pC)
Power Dissipation	< 100 mW/ch
Process	0.35 μm CMOS
Package	100 pin CQFP

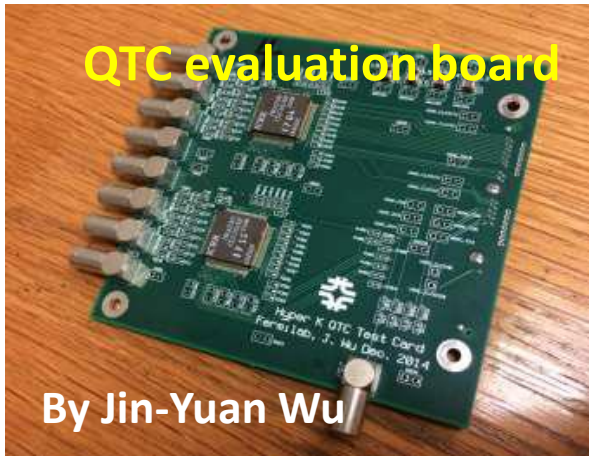


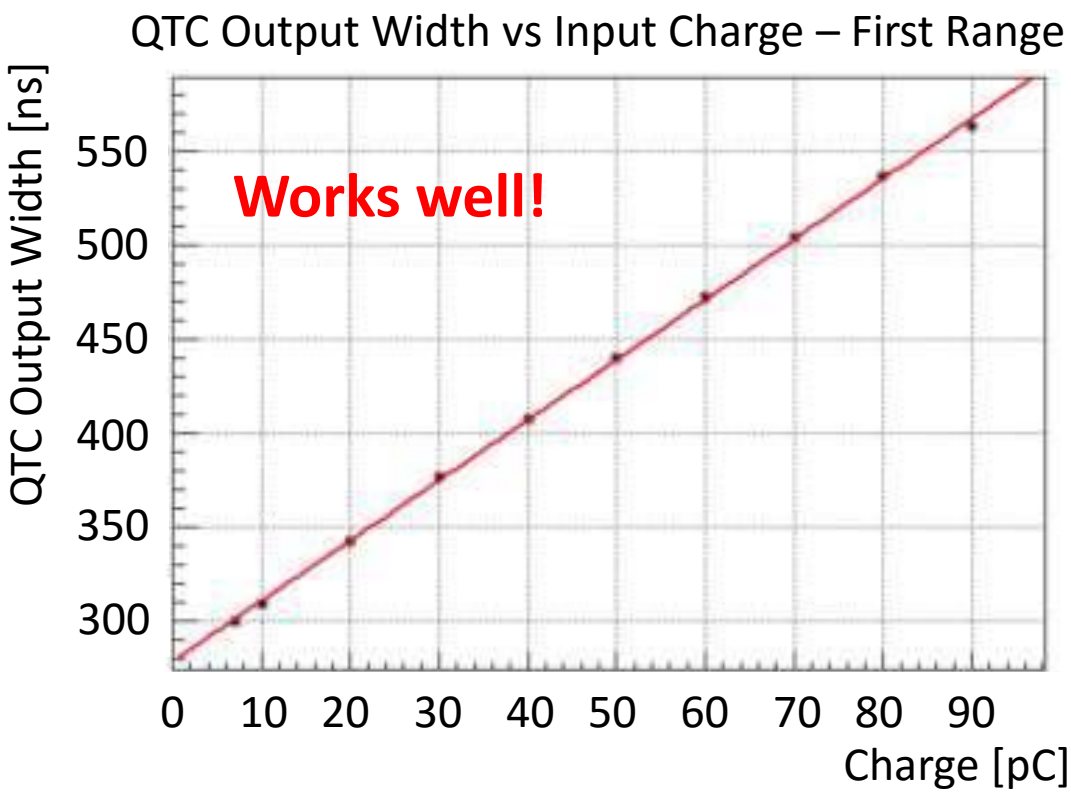
- Similar to SK-type electronics
  - Uses custom built QTC ASIC and external TDC
- 3 QTC channels per one PMT channel
  - Necessary to cover wide dynamic range
- Process rule is CMOS 0.35 μm – still possible to manufacture the same chip. However, TDC chip is no longer available.

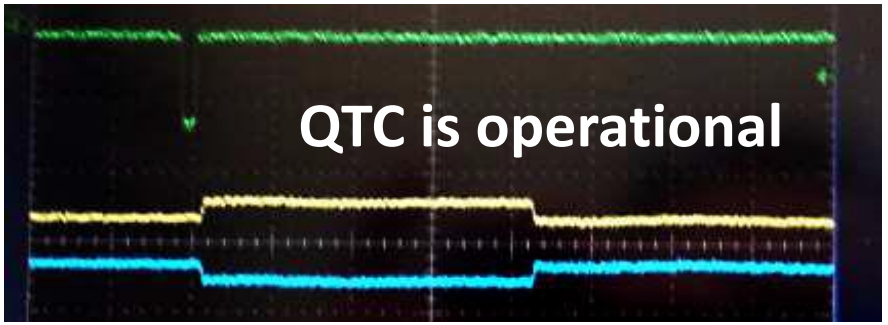
Works well in SK!
(QBEE board)

Digitization – QTC + TDC

- Considering to use FPGA-based TDC
  - FPGA-based "Wave Union" TDC by Jin-Yuan Wu, Fermilab
- QTC test board was designed and fabricated at FNAL/BU
  - Works with FPGA

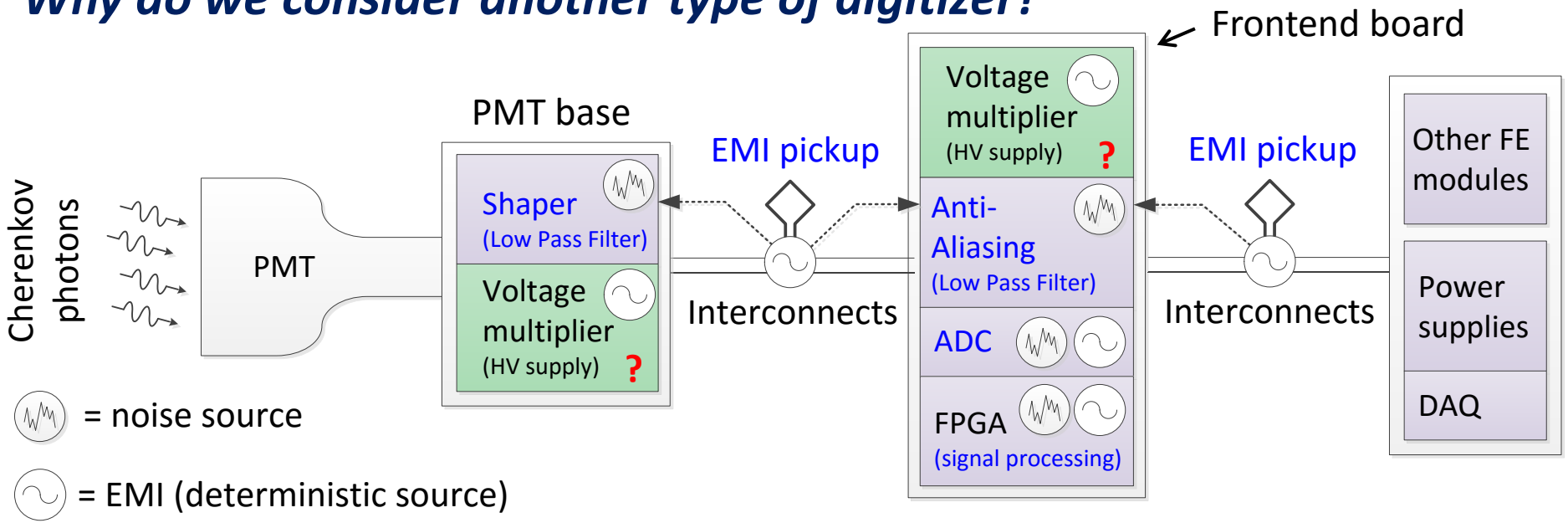






Digitization – Waveform Sampling

Why do we consider another type of digitizer?



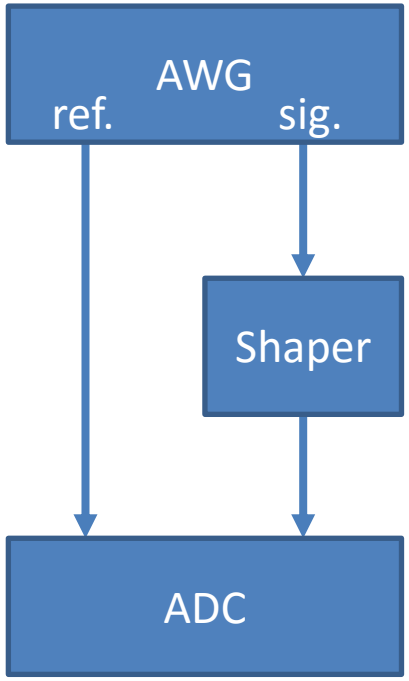
- Possibility to implement completely dead-time free system.
  - Better ability to tag decay electrons that occur at short decay times and high muon energies.
- Can subtract off periodic EMI by digital filters implemented in FPGA firmware.
- There is a price to pay: power consumption and cost (?).

Timing Resolution of Sampling Digitizers

PURPOSE OF THE STUDY:

Determine how fast and how precise does a system needs to be to achieve given performance specs?

- Use AWG instead of PMT.
- Use large reference pulse (timing accuracy $\sigma \approx 10$ ps) and small, shaped signal pulse (1 mV ~ 100 mV).
- Apply signal processing methods and calculate time difference Δt between ref. and sig. channels.
- Repeat multiple times and compute RMS of Δt values.
- Two shapers:
  - 15 ns and 30 ns rise time (10% to 90%), 5-th order Bessel-type low-pass filters.



Agilent 33600A (1 GSPS/80 MHz)

Custom shapers

Commercial ADCs (CAEN)

DT5724 (100 MSPS/14b)

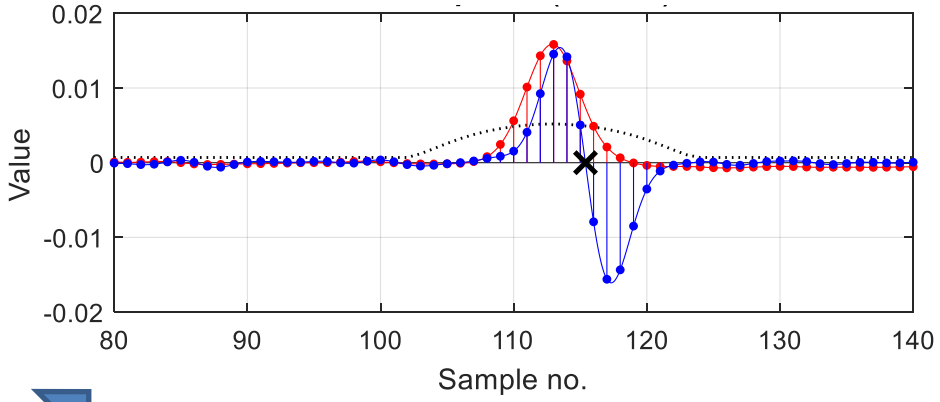
V1720 (250 MSPS/12b)

V1730 (500 MSPS/14b)

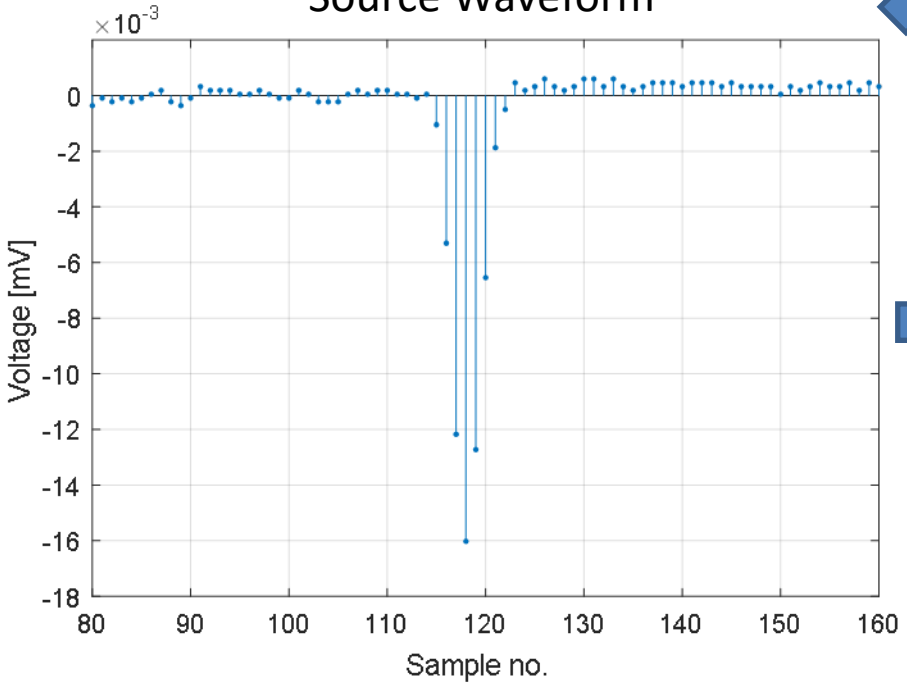
Signal Processing Methods

- Tested four methods of time estimation:
  - Digital Constant Fraction Discriminator
  - Optimal Zero-Average FIR Filter
  - Matched Filter + Cross-correlation
  - Fits *(off-line processing only)*
- Charge resolution is not a problem

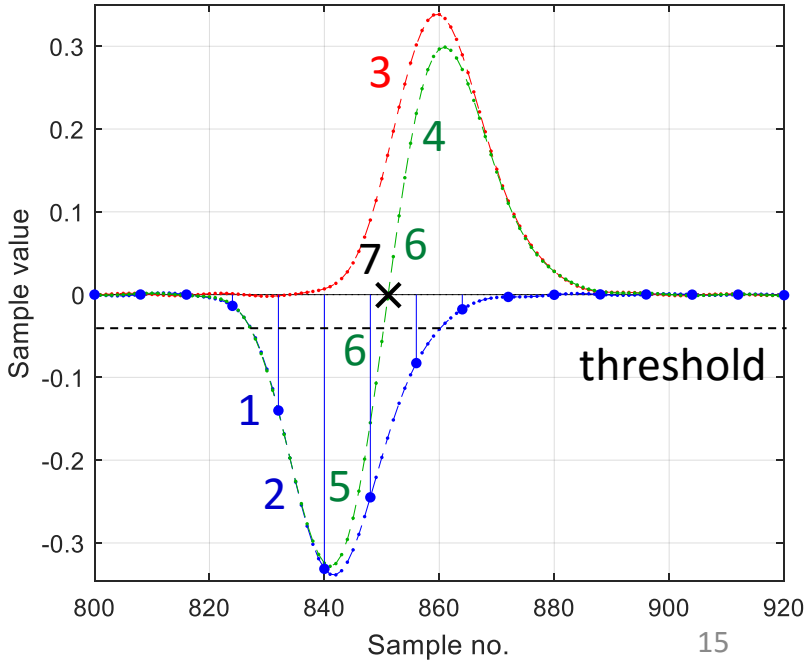
Optimal Zero-Average FIR Filter



Source Waveform

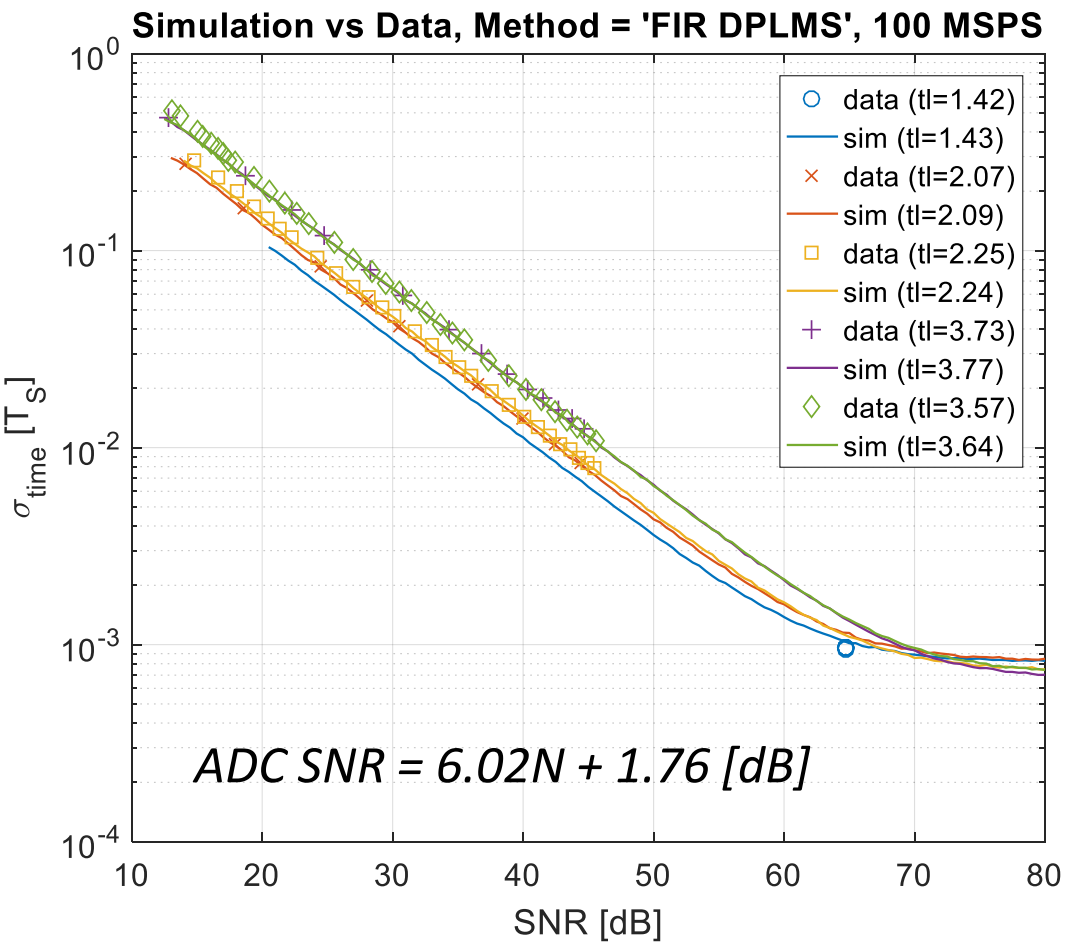


Digital CF Discriminator



Results of Timing Resolution Study

- We can easily determine time with precision well below the sampling period
- Determining factors are :
  - System bandwidth (limits sharpness of pulse edge)
  - Signal-to-noise ratio
  - Signal processing methods
- Can improve SNR with oversampling and proper filtering

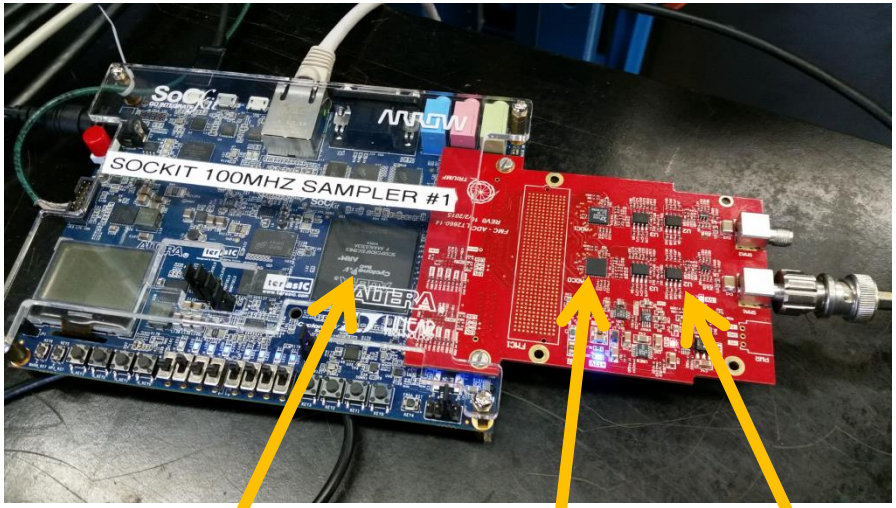


Extensive effort has been put into developing electronics models.

They match data well, so we now have tools to easily try more shaper & ADC variants.

FADC Prototype

- First prototype designed and built
  - 100 MSPS FADC + 15 ns shaper
- Low power Flash-ADC for 20” photo-sensors
  - 0.55W per channel (excluding FPGA), but possible to get down to 0.4W/channel.
  - Can get further reduction of power consumption if an 80 MSPS ADC is chosen.
- Will start analysis of the data soon.

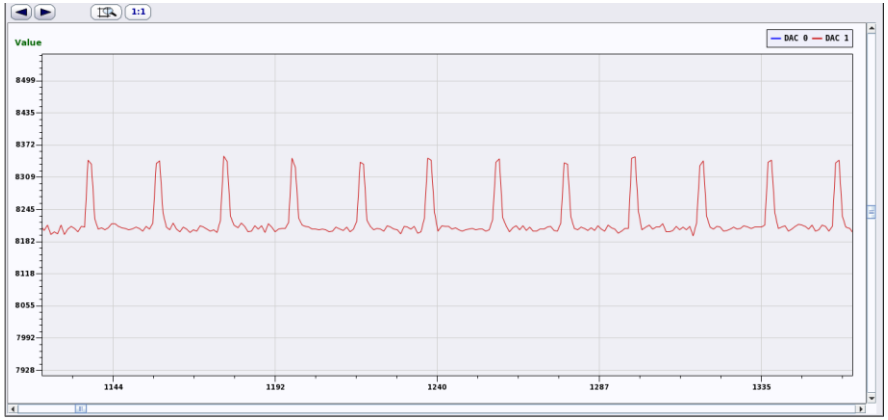


ALTERA Cyclone V SoC evaluation card

ADC LT2260

Shaper

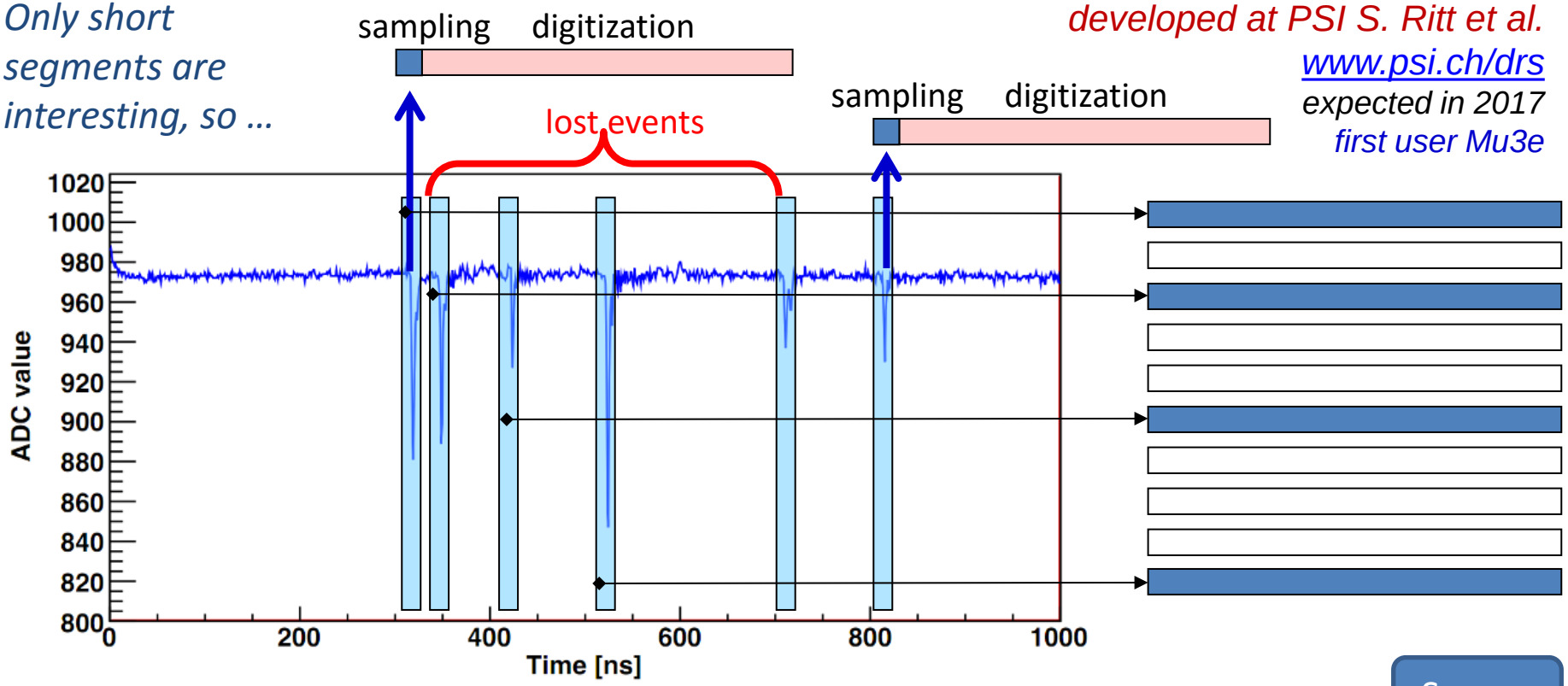
Sample waveform with periodic pulses



Cyclone V SoC = Cyclone V FPGA + Cortex-A9 ARM processor

Switched Capacitor Arrays

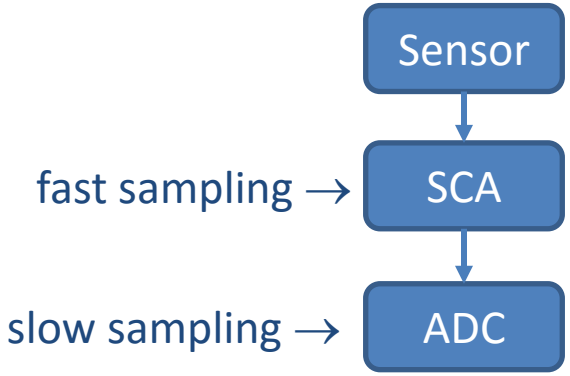
Only short segments are interesting, so …



developed at PSI S. Ritt et al.
www.psi.ch/drs
expected in 2017
first user Mu3e

DRS5 solution:

- Store continuously sampled waveform in a 2D array
- Digitize only interesting segments ($f_s \sim$ 1GHz)
- Sampling and digitization asynchronous
- Virtually dead-time less up to
  average rate = f_{ADC} / window size



Summary

- Experience from Super-Kamiokande is useful in designing new system
- On-going R&D on individual components to maximize detector performance and reliability while minimizing the cost
  - Water-tight connectors
  - Pressure-tolerant cables compatible with ultra-pure water
  - High voltage supplies
  - Digitization options
  - Reliability of all the components
  - And many, many more…

LET US KNOW IF YOU WOULD LIKE TO JOIN THE EFFORT!

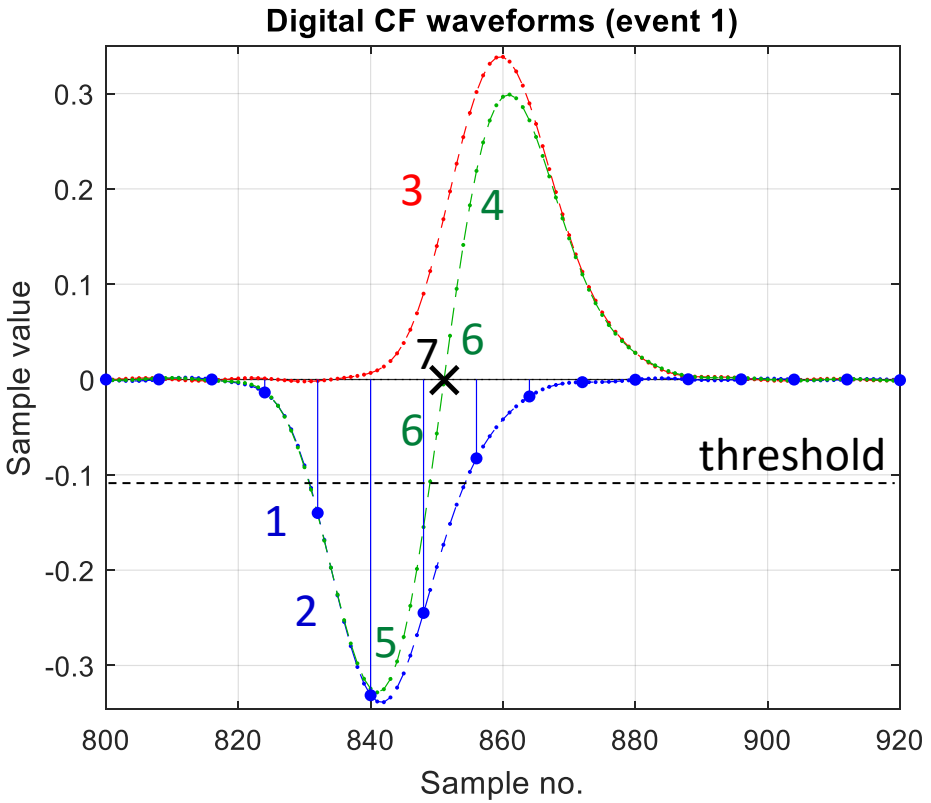
YOU ARE VERY WELCOME!

BACKUP

Signal Processing Methods

Digital Constant Fraction Discriminator:

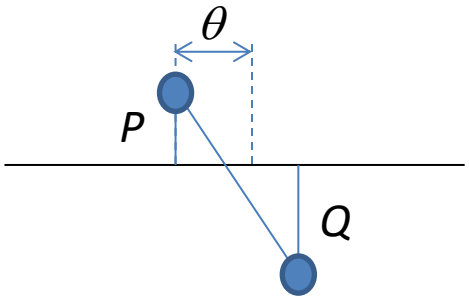
- Simple processing → needs little FPGA resources
- Does not make any assumption as to the pulse shape
- Favors high sampling rate, but some improvements are possible for low sampling rates if pulse shape is invariant
- Poor performance in low SNR conditions



Time errors and possible correction

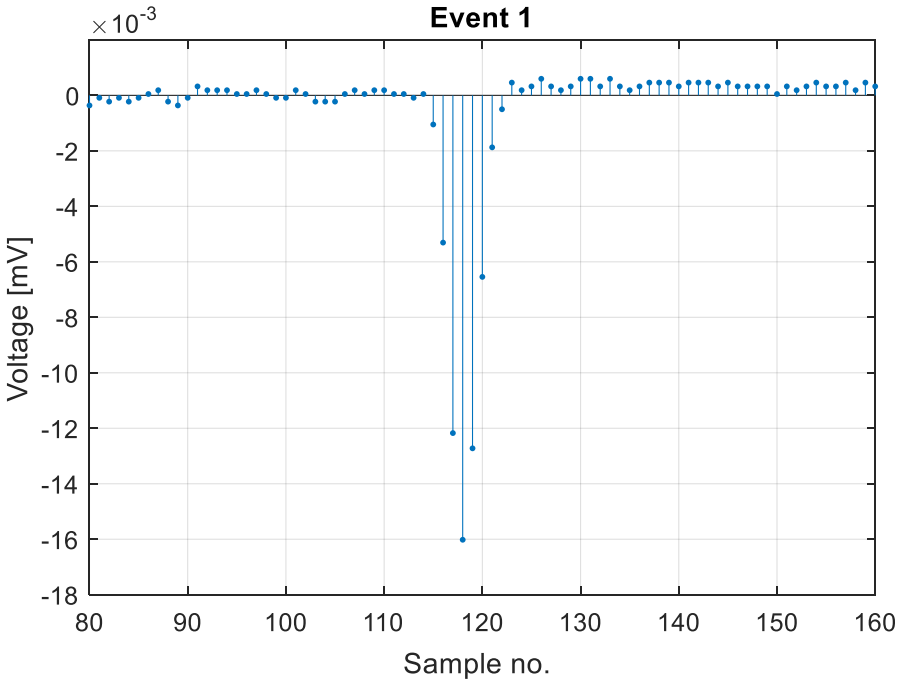
θ - actual sub-sample shift

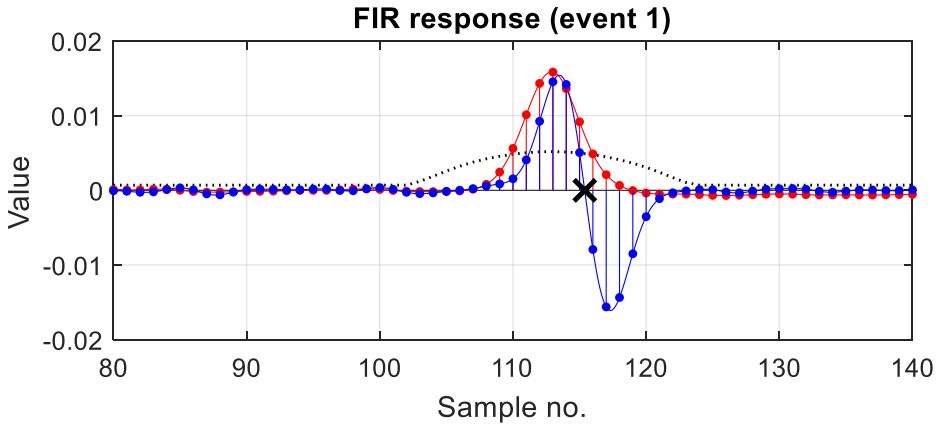
$$CR = \frac{P}{P - Q}$$

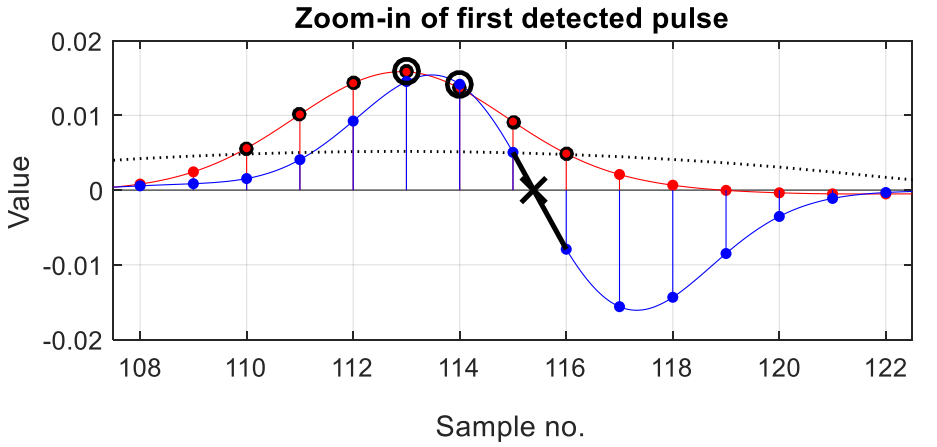


Signal Processing Methods II

Zero-Average Optimal FIR Filter:







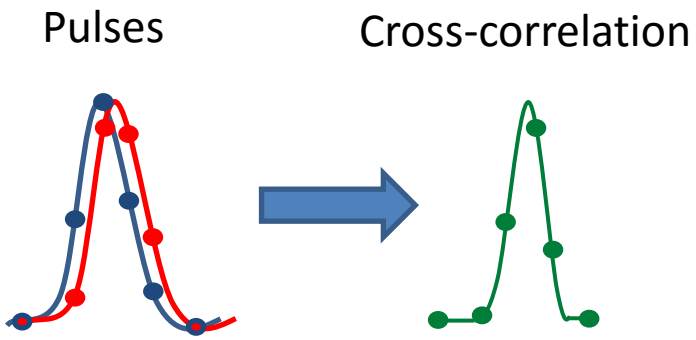
- More complex processing
  - Works well with filter orders of 9-12
- Assumes that shape is invariant
- Better behavior at low SNR

Signal Processing Methods III

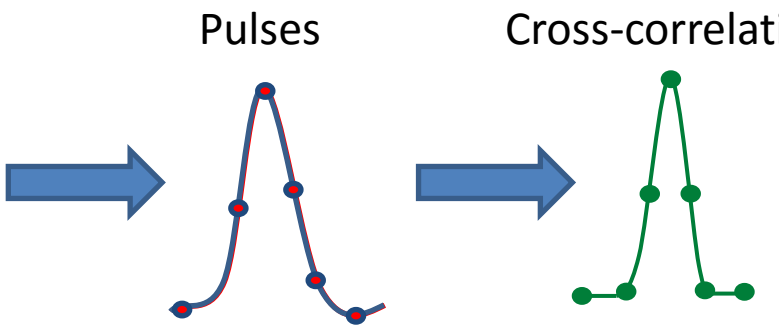
Matched FIR Filter and Cross-Correlation Processing:

- Much more complex processing
  - Works well with filter orders of 9-12
- Assumes that shape is invariant
- Similar timing performance to zero-average FIR filter
- Relatively easy to disentangle piled-up pulses

Misaligned pulses



Aligned pulses



Sub-sample shifts done using windowed sinc interpolation (Blackman window). FFT interpolation also possible if shifting impulse response.