Cold Electronics for ProtoDUNE-SP LAr TPC

SHANSHAN GAO ON BEHALF OF THE LARTPC FEE TEAM
BROOKHAVEN NATIONAL LABORATORY
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BROOKHAVEN NATIONAL LABORATORY
a passion for discovery

INTERNATIONAL WORKSHOP ON NEXT GENERATION NUCLEON DECAY AND NEUTRINO DETECTORS (NNN16)

Office of Science
U.S. DEPARTMENT OF ENERGY

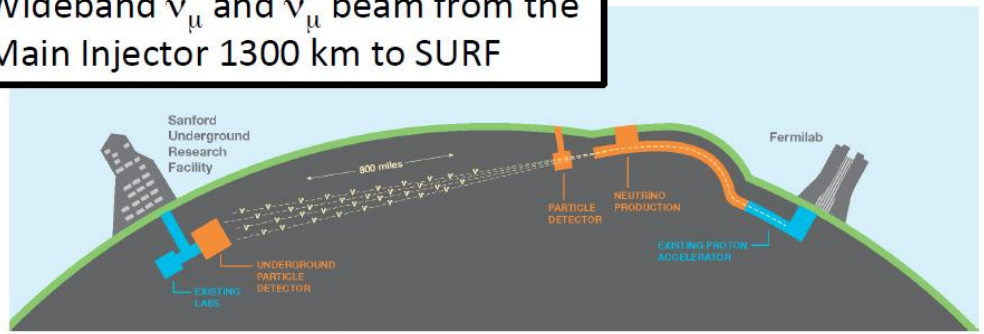
Outline

- Overview of ProtoDUNE-SP
- Cold Electronics (CE) Development
  - A Brief History of CE
  - Advantages of CE
  - Key CMOS Devices in CE for ProtoDUNE-SP
- Cold Electronics System in ProtoDUNE LAr TPC
  - ProtoDUNE-SP TPC Readout Electronics
  - Front End Mother Board Assembly
  - Warm Interface Electronics
  - Integral APA and CE Concept
- Summary
-

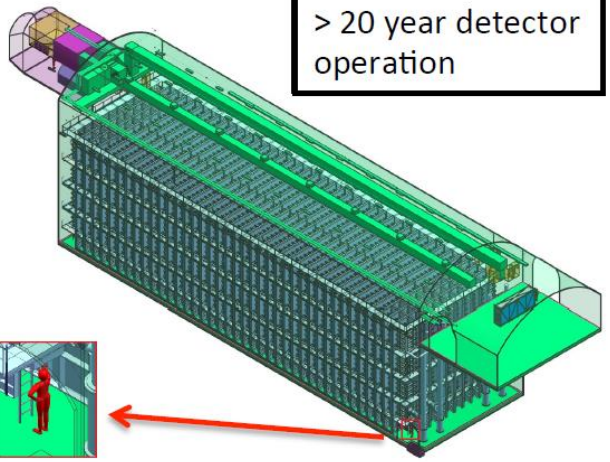
Overview of ProtoDUNE-SP

- Deep Underground Neutrino Detector (DUNE)
  - DUNE will take neutrino beam data from Fermilab in the Long Baseline Neutrino Facility (LBNF) starting in 2026

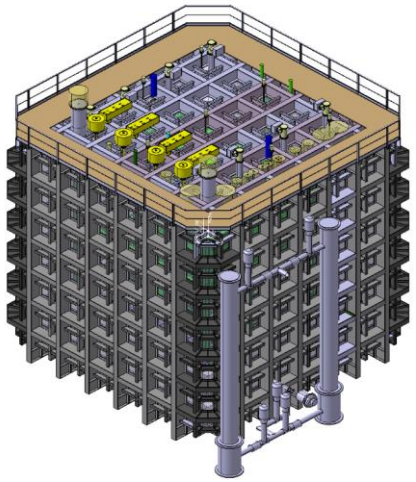
Wideband ν_μ and $\overline{\nu}_\mu$ beam from the Main Injector 1300 km to SURF



> 20 year detector operation



DUNE single phase far detector module
10 kton fiducial volume LArTPC at 4850L



ProtoDUNE-SP

- ProtoDUNE-SP
  - 700 ton LAr TPC
  - Full scale components of DUNE far detector module
  - Will sit in H4 beam line @CERN
- Goals
  - Measure detector response to known particles
  - Confirm modeling and simulation
  - Validate mechanical and electrical design and interfaces

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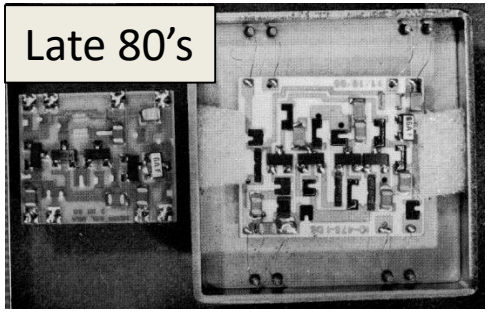
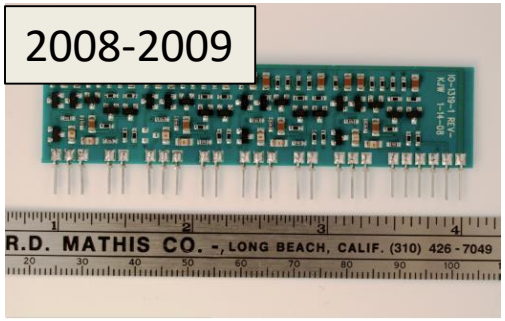
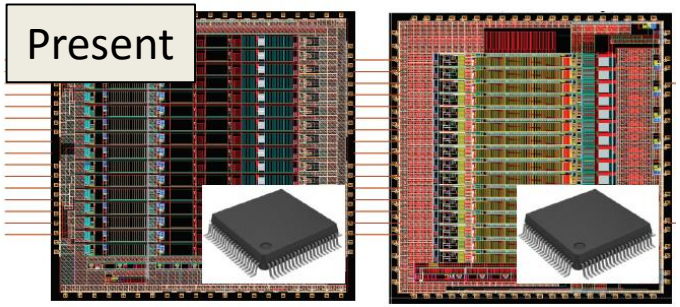
A Brief History of Cold Electronics

- Motivation of CE
  - Cold electronics decouples the electrode and cryostat design from the readout design. With electronics integral with detector electrodes, the noise is independent of the fiducial volume (signal cable lengths), and much lower than with warm electronics
- Late 80's, Cryogenics Front-End based on JFET
  - Liquid Argon calorimeter, 576 preamplifiers
- 2008-2009, MicroBooNE front-end design started from JFET
- Present, cryogenic CMOS ASIC for SBND and ProtoDUNE-SP
  - MicroBooNE has adopted the cryogenic CMOS analog front end ASIC developed for LBNF/DUNE LAr TPC program in 2010

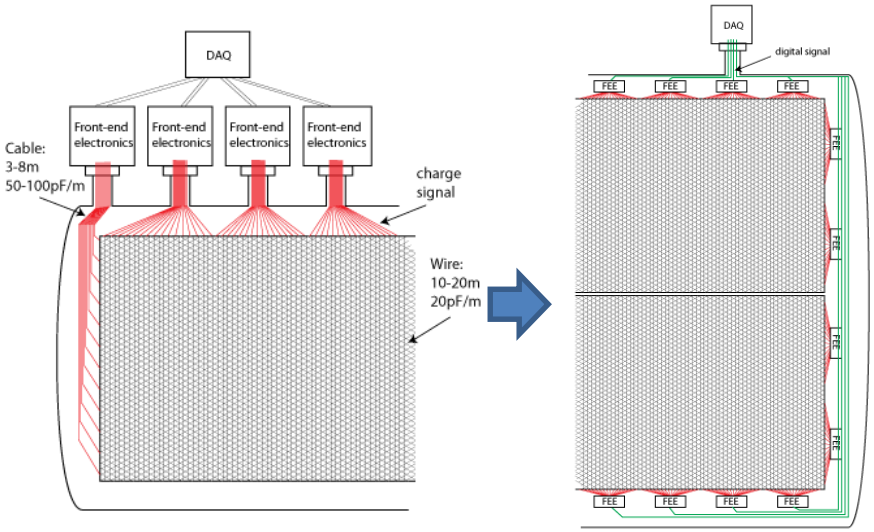




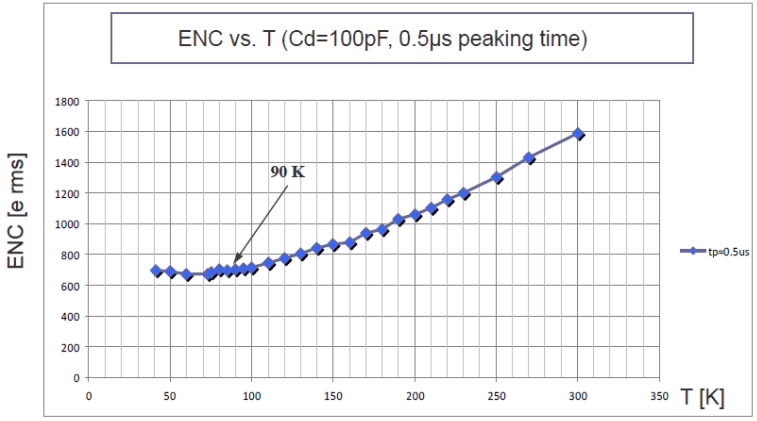


Advantages of CE

- Having front-end electronics in the cryostat close to the wire electrodes
  - Yields the best SNR
- Highly multiplexed circuits with fewer digital output
  - Greatly reduce the number of cryostat penetrations
  - Give the designers of both the TPC and the cryostat the freedom to choose the optimum configurations
- CMOS in LAr has less than half the noise as that at room temperature, higher mobility and higher transconductance /current ratio



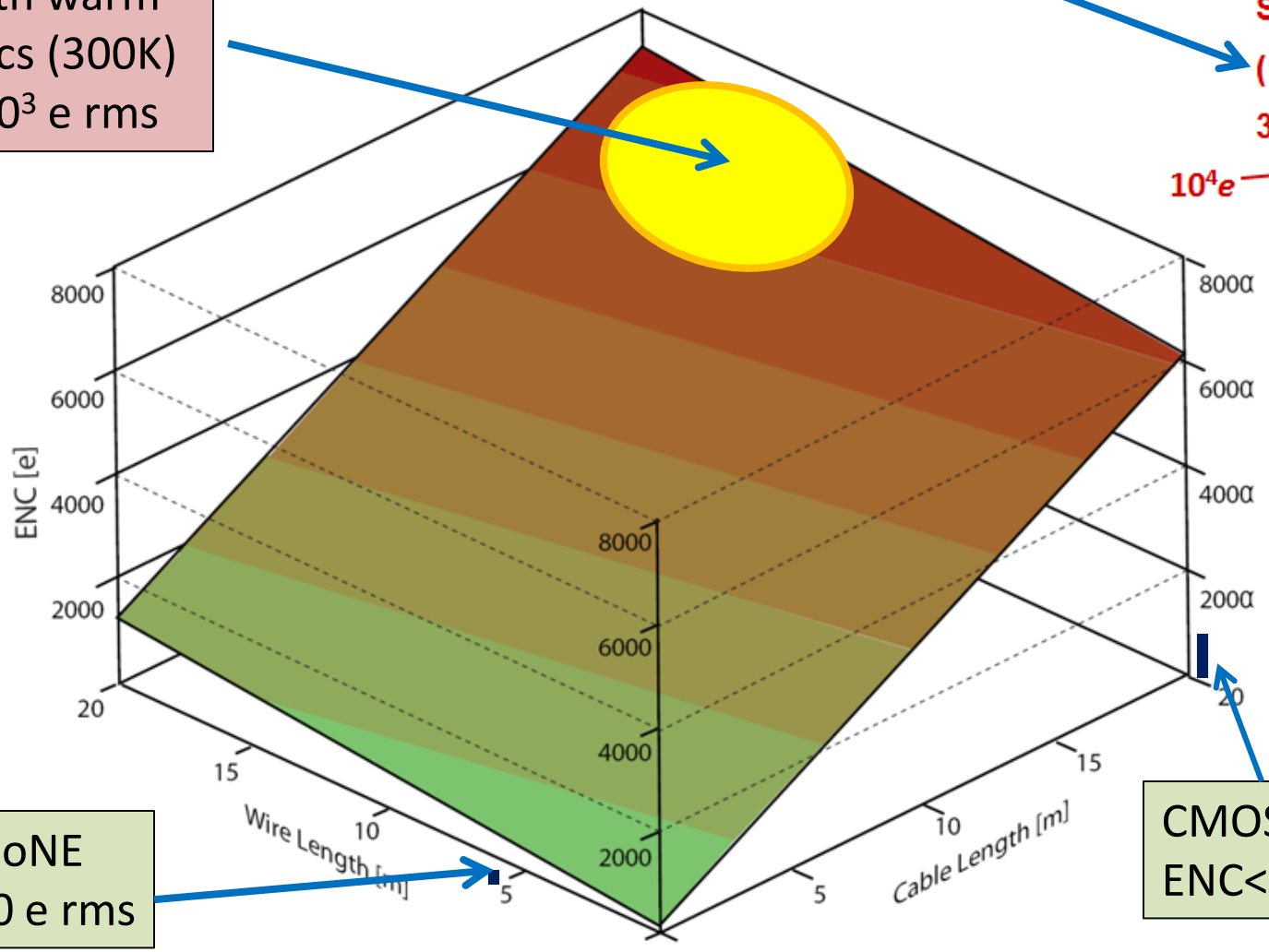
Warm readout to cold readout



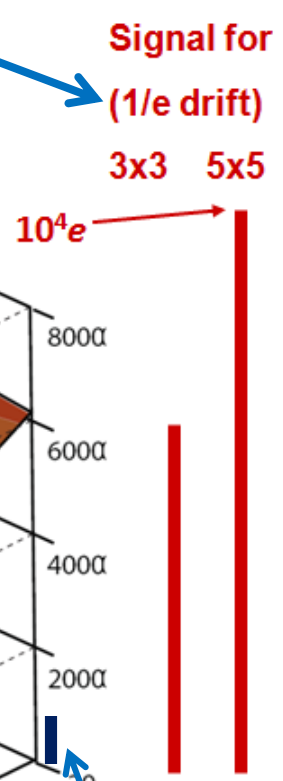
Test result of ASIC in 0.25 μm

Noise (ENC) *vs* TPC Sense Wire and Signal Cable Length for CMOS at 300K and 89K

DUNE with warm electronics (300K) ENC~$6x10^3$ e rms



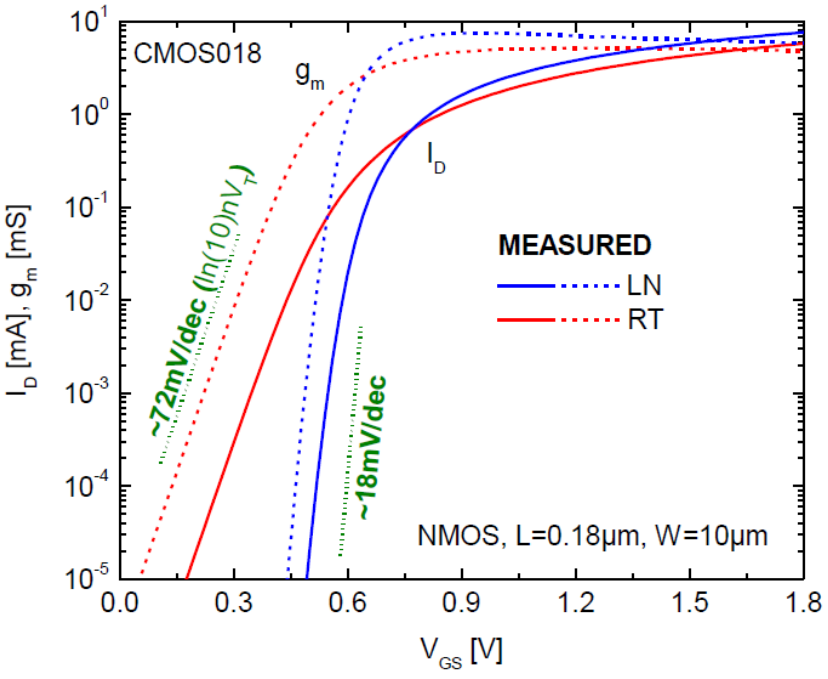
MIP Signal for 3x3 and 5x5 mm

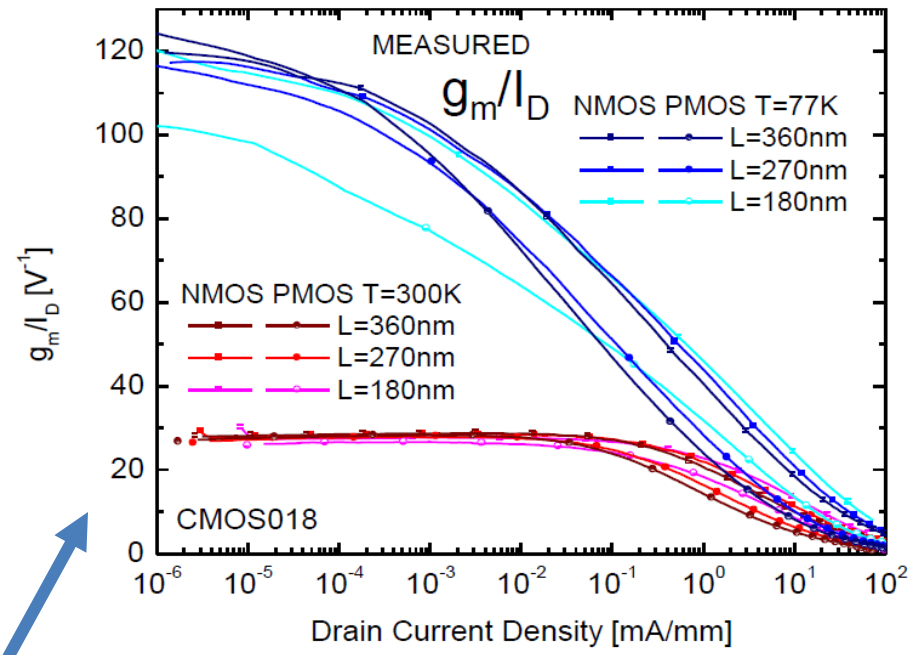


MicroBooNE ENC~400 e rms

CMOS at 77K: ENC< 10^3 e rms

CMOS Characteristics in Cryostat





Transconductance / drain current

$$\frac{g_m}{I_D} \rightarrow \frac{q}{nk_BT} = \begin{cases} \sim 30 \ \ at \ \ T = 300K \\ \sim 116 \ \ at \ \ T = 77K \end{cases}$$

At 77-89K, charge carrier mobility in silicon increases and thermal fluctuations decrease with kT/e, resulting **in a higher gain, higher g_m/ID, higher speed and lower noise**.

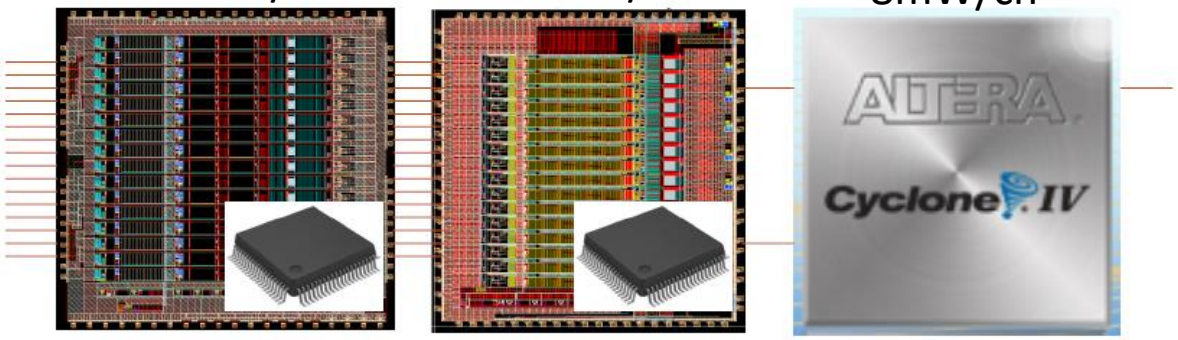
Key CMOS Devices of Cold Electronics for ProtoDUNE-SP

Voltage Regulator (COTS)
(< 100mV dropout)

Front end ASIC
~ 5mW/ch

ADC ASIC
~ 5mW/ch

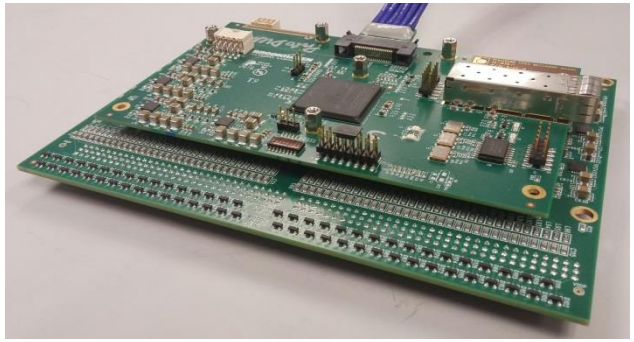
FPGA (COTS)
~ 8mW/ch



8 x

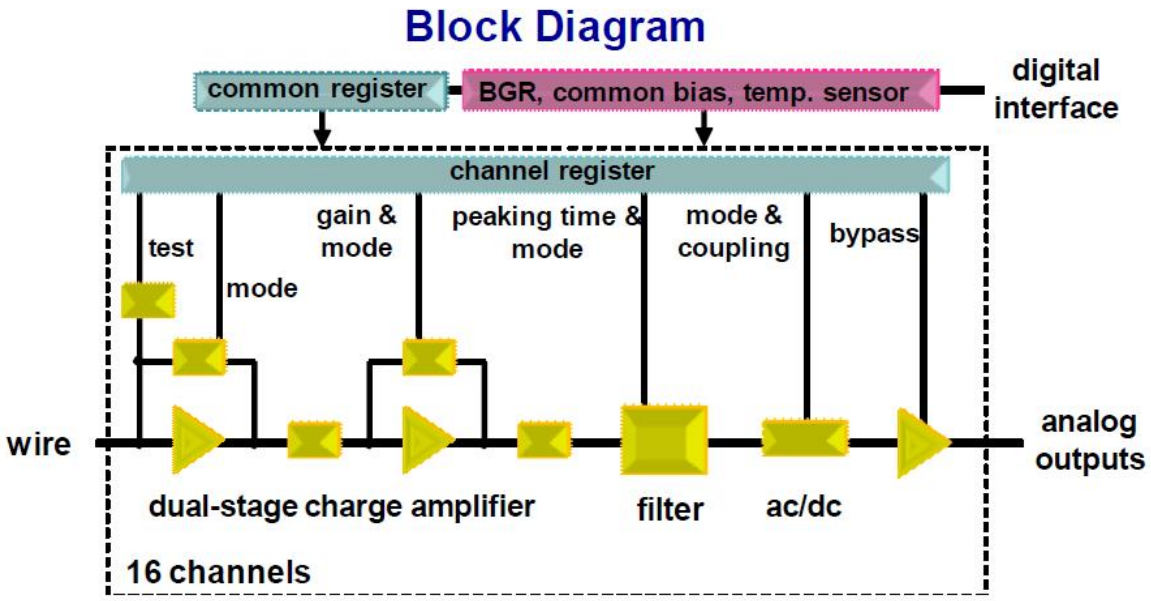
1 x

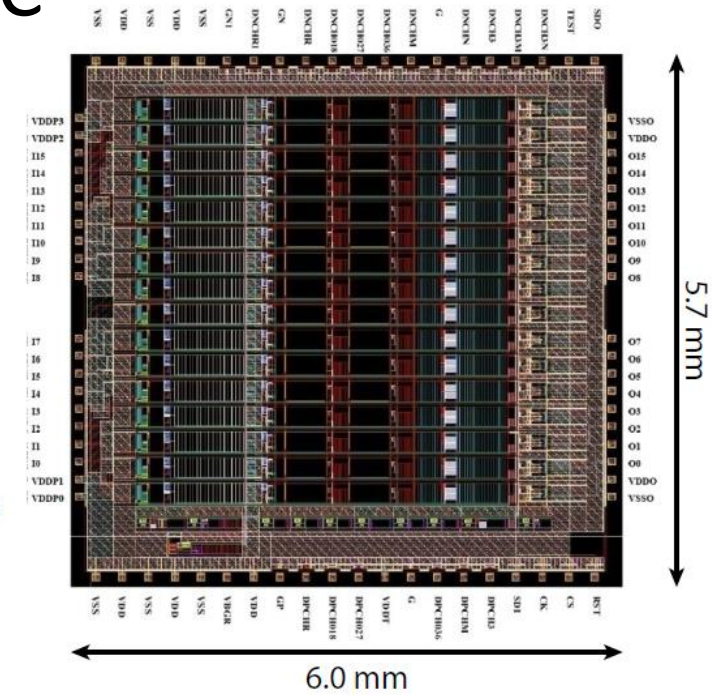
A complete front end readout chain for ProtoDUNE-SP LAr TPC



Front End Mother Board assembly serving 128 wires ~ 2.4 W + LDO inefficiency

Front End ASIC

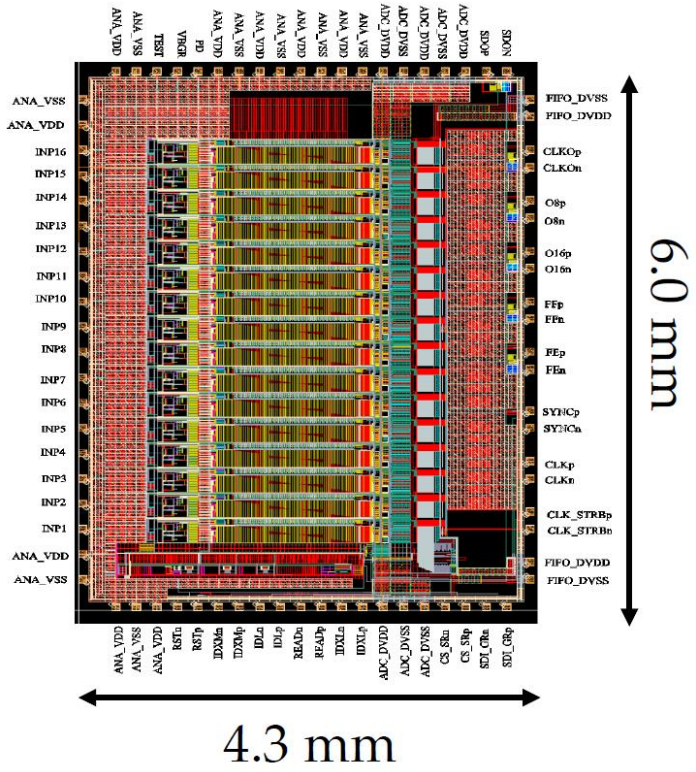




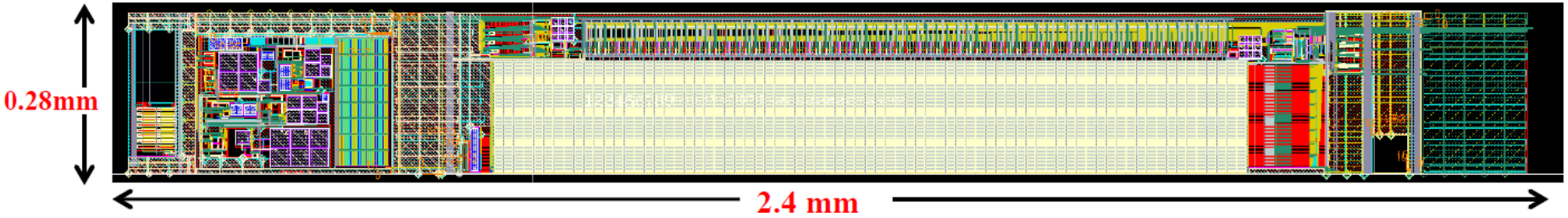
- 16 channels, programmable
- Charge amplifier, high-order filter
- Adjustable gain: 4.7, 7.8, 14, 25mV/fC
- Adjustable filter time constant
  - (peaking time 0.5, 1, 2, 3µs)
- Selectable collection/non-collection mode
  - (baseline 200, 900mV)
- Selectable DC/AC coupling (100µs)
- Build in pulse generator with 6-bit DAC

- Rail-to-rail analog signal processing
- Band-gap referenced biasing
- Temperature sensor (~3mV/°C)
- 144 registers with digital interface
- Single MOSFET test structures
- ~ 16,000 MOSFETs
- Designed for 77K-300K operation
- Designed for long lifetime
- Tech. CMOS 180 nm, 1.8 V, 6M, MIM, SBRES

Cold ADC ASIC



- 16 channels, programmable
- Sample/hold
- 12-bit ADC at 2MS/s sampling rate
- Current-mode domino architecture
- FIFO 192s bit wide x 32 bits deep
- Multiplexer 8:1 or 16:1
- Serializer 12:1
- Adjustable offsets
- Power-down modes
- ~320,000 MOSFETs
- Designed for 77-300K operation
- Designed for long lifetime
- Tech. CMOS 180nm, 1.8 V, 6M, MIM, SBRES



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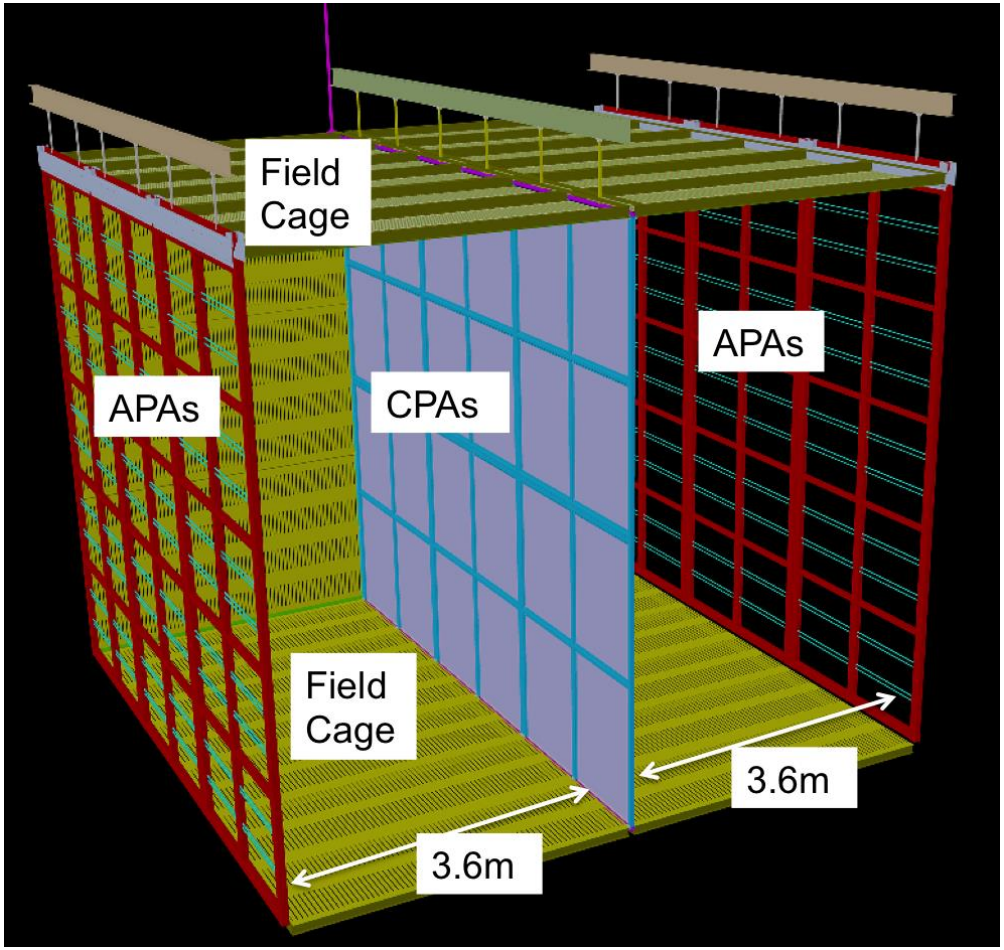
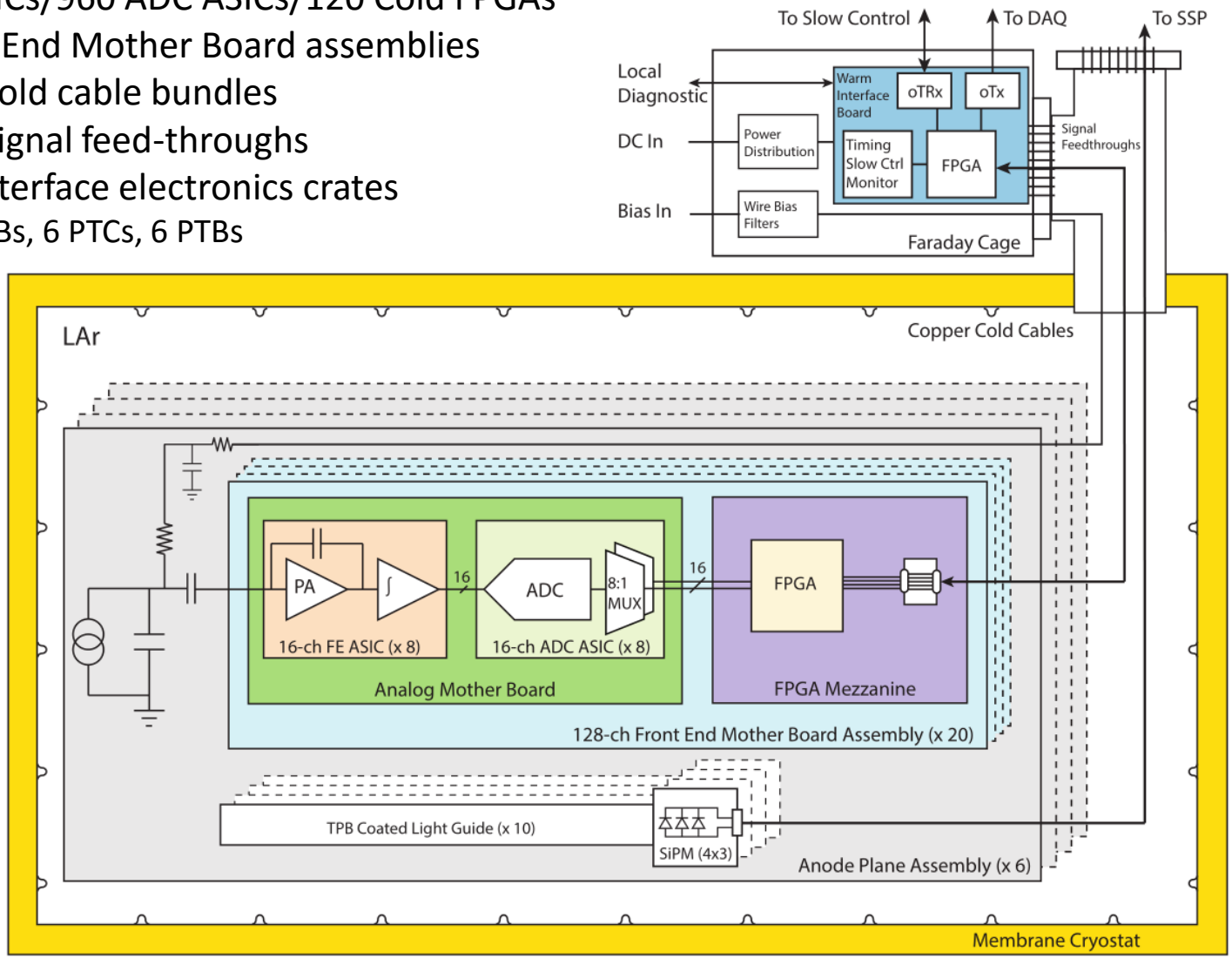
ProtoDUNE-SP



- Single-phase TPC prototype
  - Consisting of 6 full-size APAs plus 2 CPAs → 2 x 3.6m drift regions
  - Total 15,360 TPC channels
  - Will install photon detectors of different fabrication methods
  - Plan for operation in 2018
- Will be a key test of:
  - Components
  - Construction methods
  - Installation procedures
  - Commissioning
  - Detector response to particles

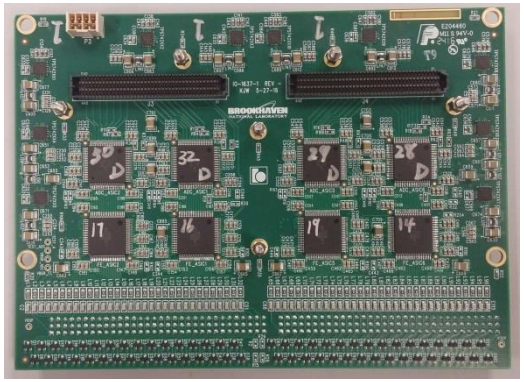
ProtoDUNE-SP TPC Readout Electronics

- Front End Electronics System
  - 960 FE ASICs/960 ADC ASICs/120 Cold FPGAs
  - 120 Front End Mother Board assemblies
  - 6 sets of cold cable bundles
  - 6 sets of signal feed-throughs
  - 6 warm interface electronics crates
    - 30 WIBs, 6 PTCs, 6 PTBs



Front End Mother Board Assembly

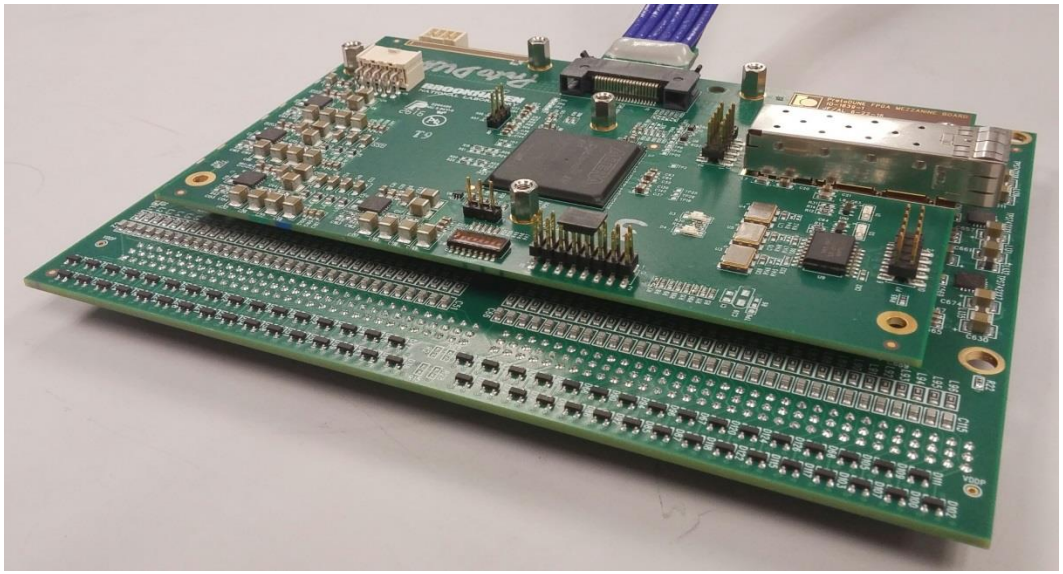
- 128 channels of digitized TPC wire readout
  - Analog Mother Board
    - 8 FE ASICs/8 ADC ASICs
  - FPGA Mezzanine
    - multiplexing and readout of digitized detector signals



Analog Motherboard

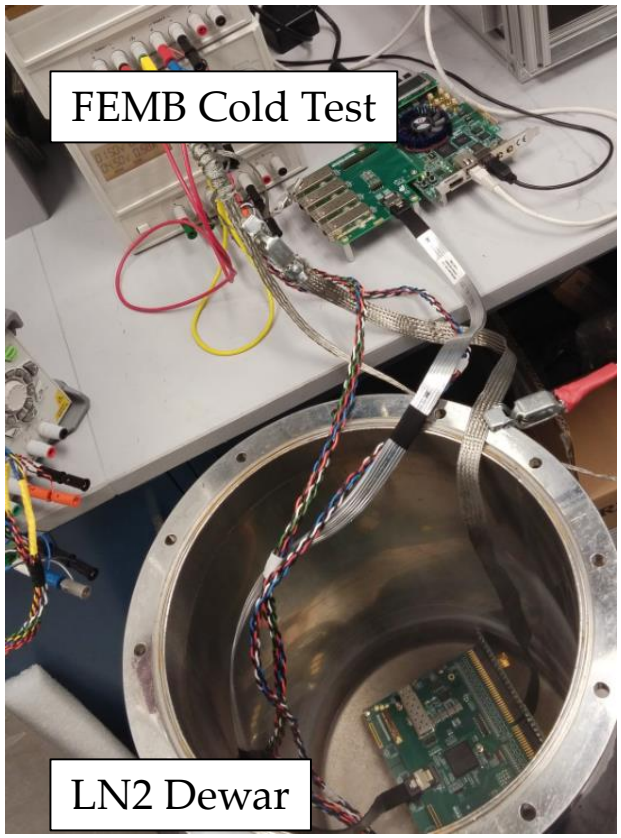
FPGA Mezzanine

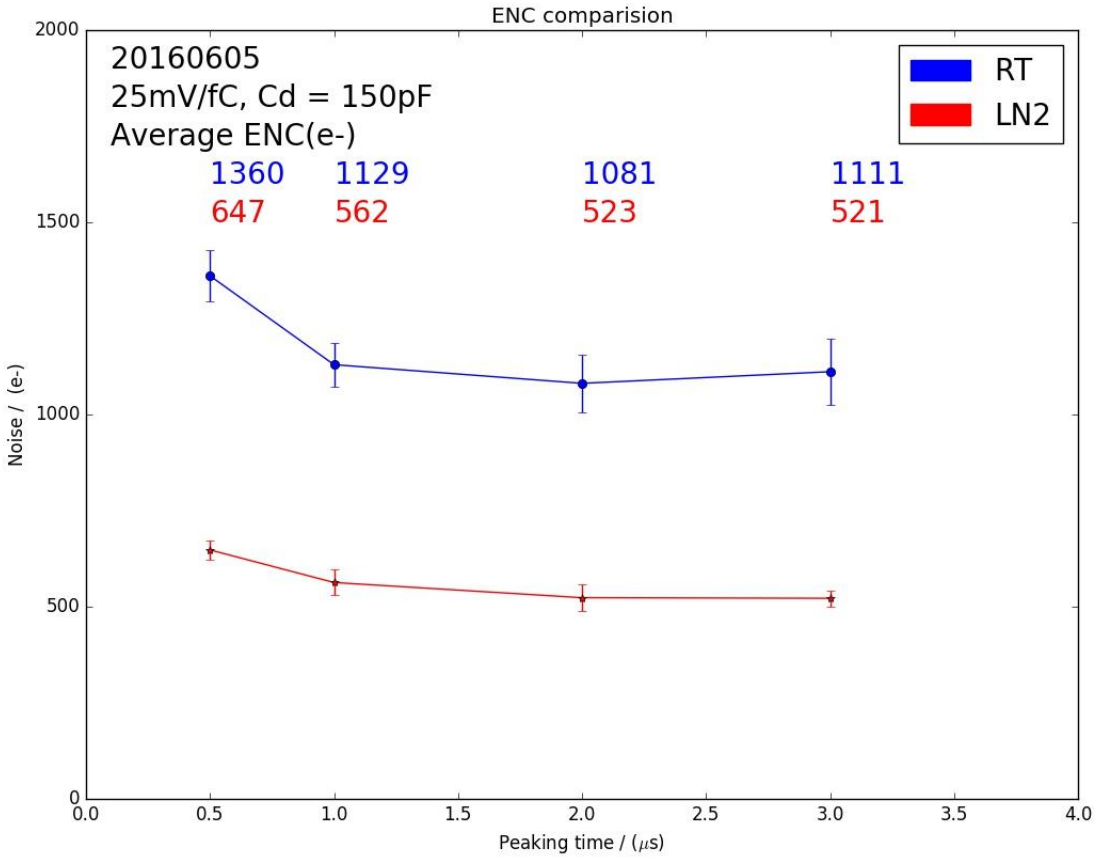
4 1Gb/s serial links to transmit 128 FE channels of data



Front End Mother Board Assembly

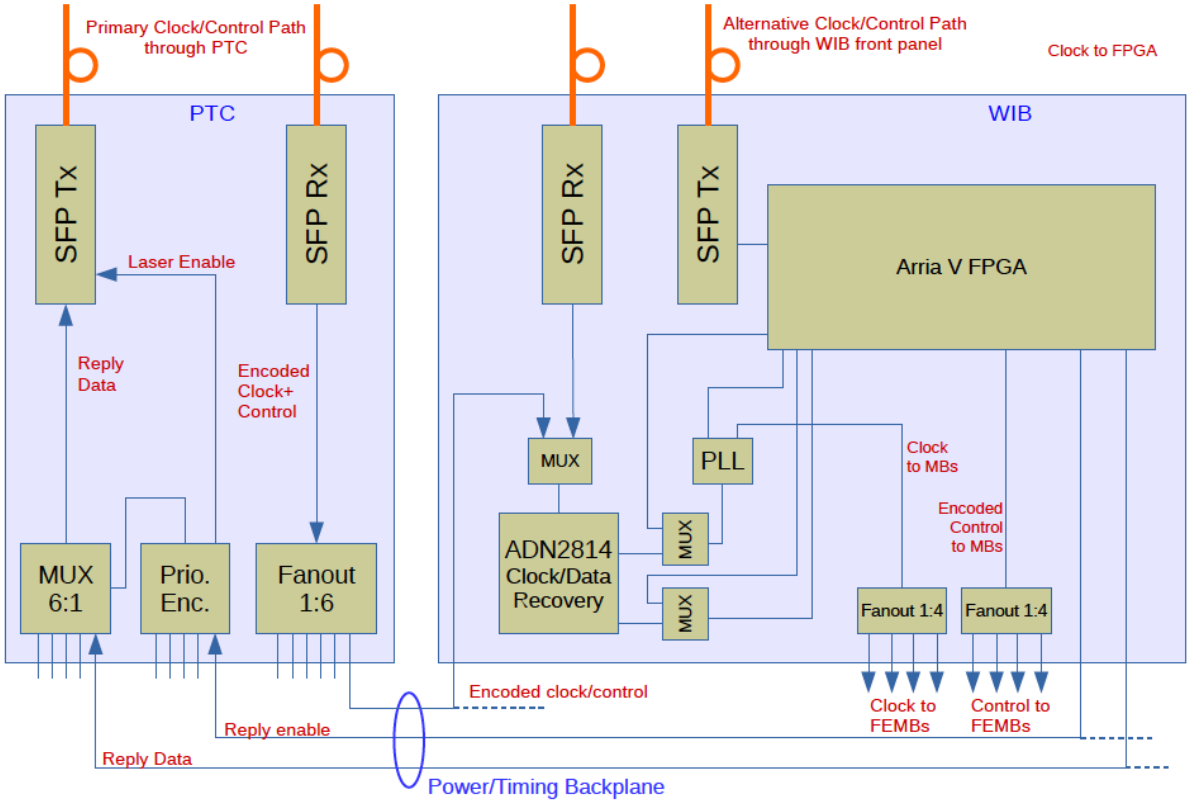
FEMB Noise Measurement





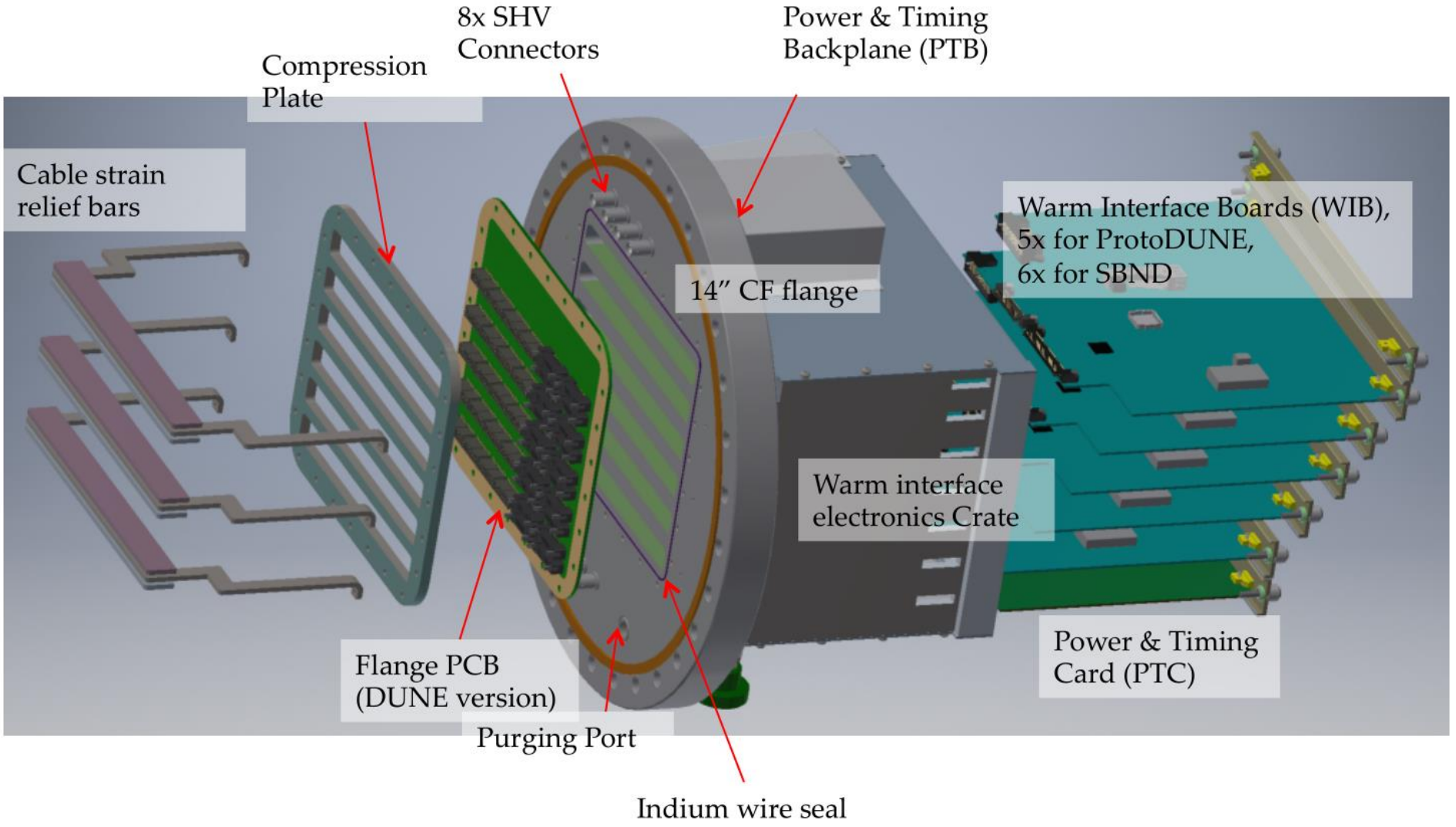
1129e- at RT and 562e- at LN2 @ 1us peaking time

Warm Interface Electronics

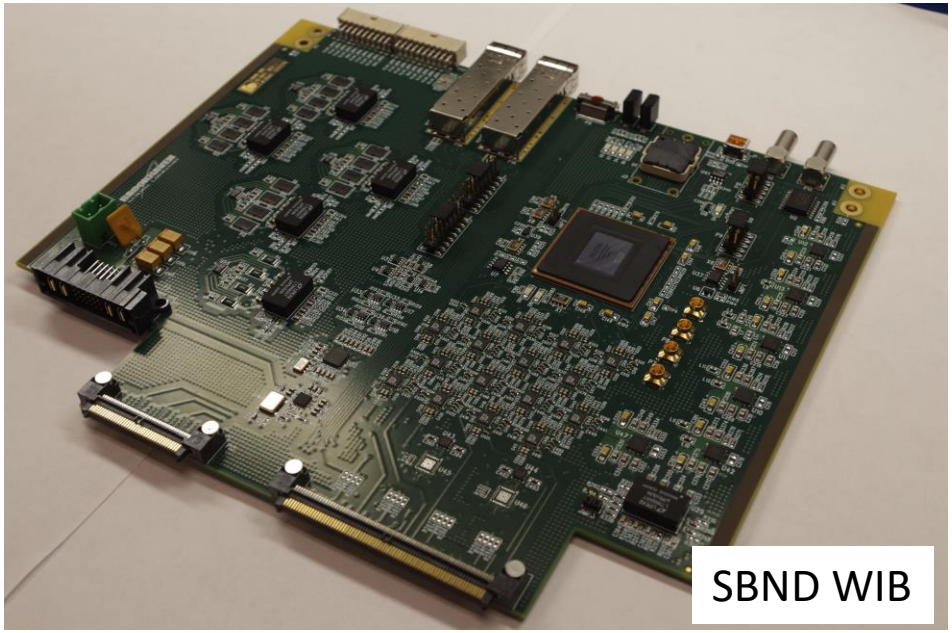


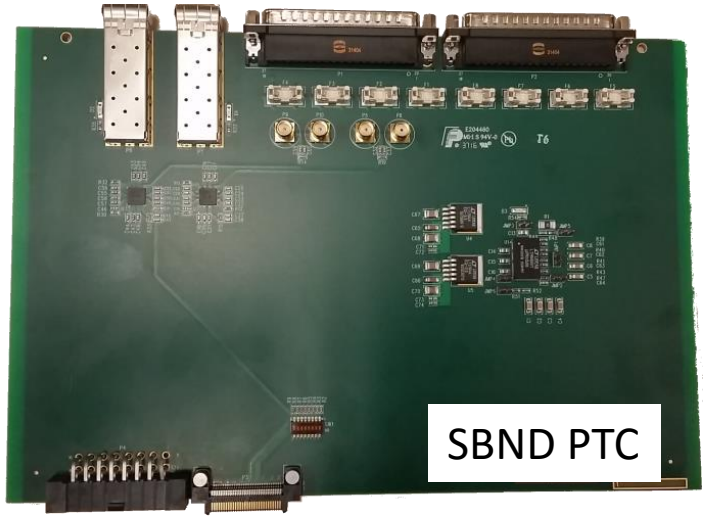
- Warm interface electronics is installed on top of the warm flange board
- Each Warm Interface Electronics Crate (WIEC) contains the following
  - 5 Warm Interface Boards (WIB), each WIB controls up to four 128-ch FEMBs
  - One Power and Timing Backplane (PTB) and one Power and Timing Card (PTC)
  - WIEC is a faraday cage with only power and optical signals going in and out

Signal Feed-through and Warm Interface Boards



Warm Interface Electronics


SBND WIB

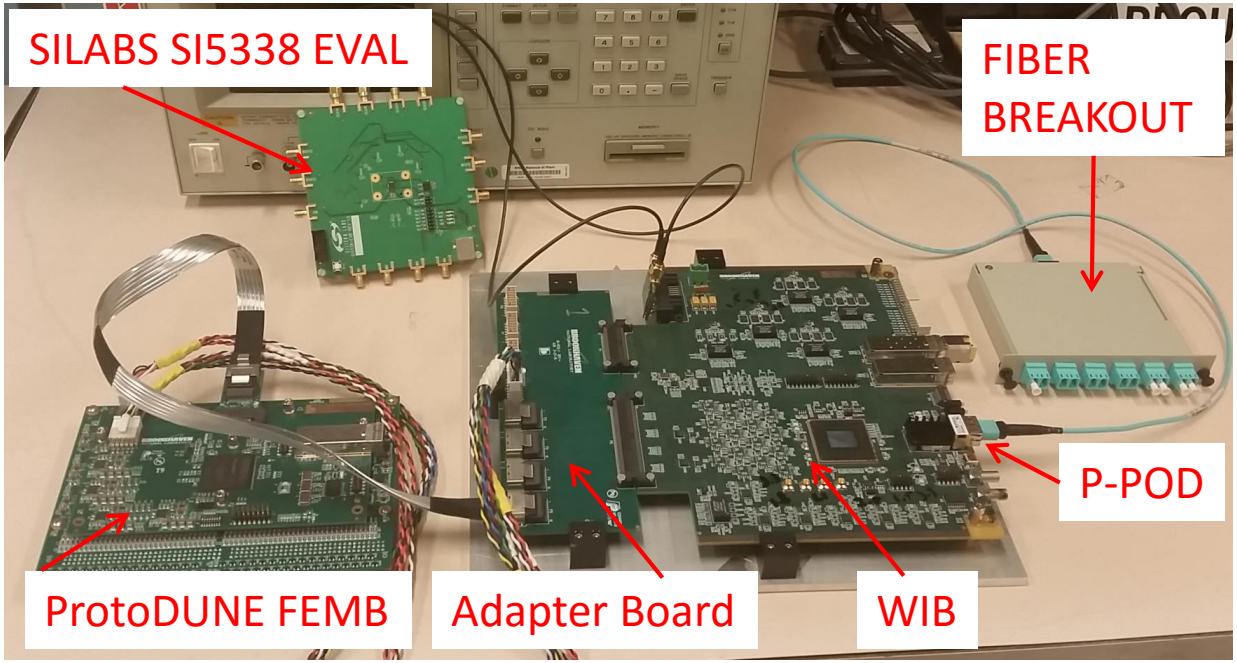

SBND PTC

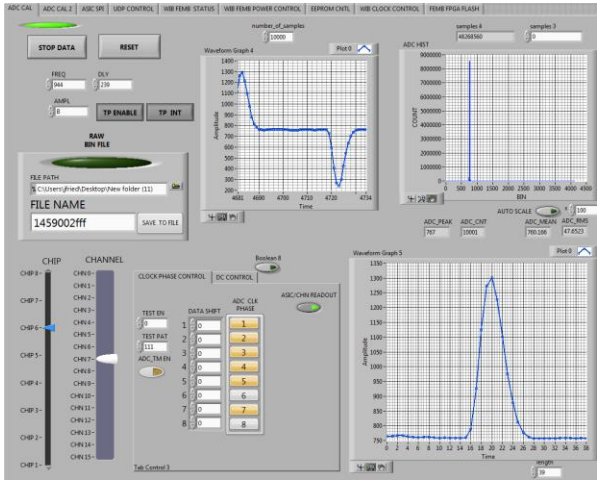
- WIB
  - ProtoDUNE-SP WIB design is being finalized
  - SBND WIB is being used for ProtoDUNE-SP firmware development currently
- PTB
  - Distributes system clock and Sync/Cntrl signals to each WIB
- PTC
  - ProtoDUNE-SP design is being finalized by UC Davis


PTB

SBND WIB + ProtoDUNE FEMB

- Test platform can be set up without signal feed-through

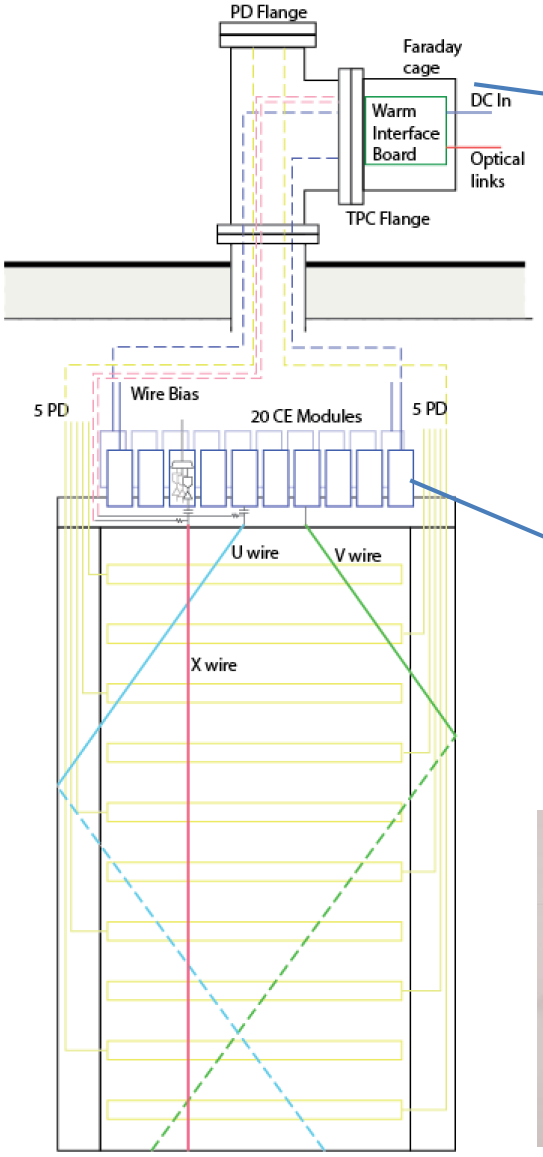


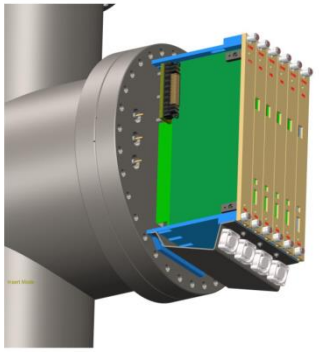


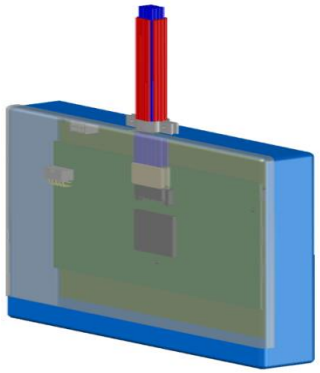
Real-time channel data

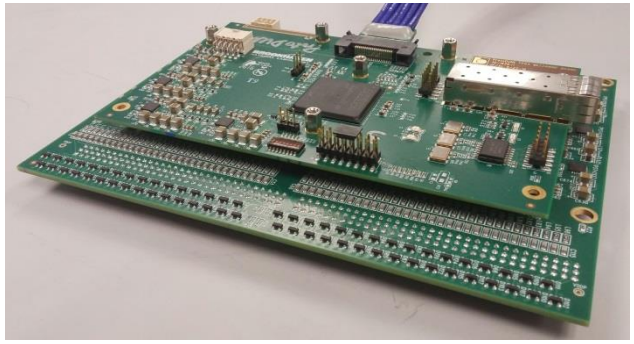
- Utilize engineering development tools used at BNL
  - Can be used simultaneously with DAQ system
  - Will simplify debugging of entire system

Integral APA + CE Concept



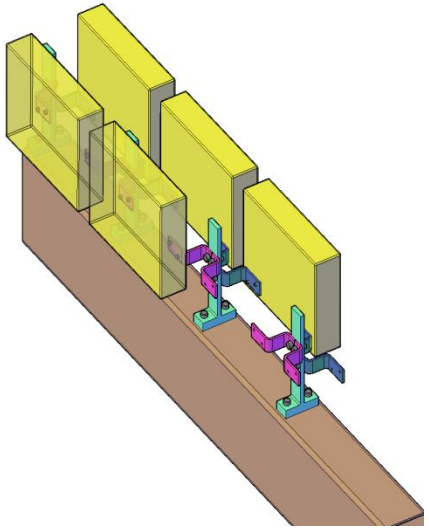






To have a chance at achieving a good performance, **the integral design concept** of APA + CE + Feed-through, plus Warm Interface Electronics with local diagnostic and strict isolation and **grounding rules** will have to be Followed. Therefore,

A 40% APA integration test stand is being built at BNL



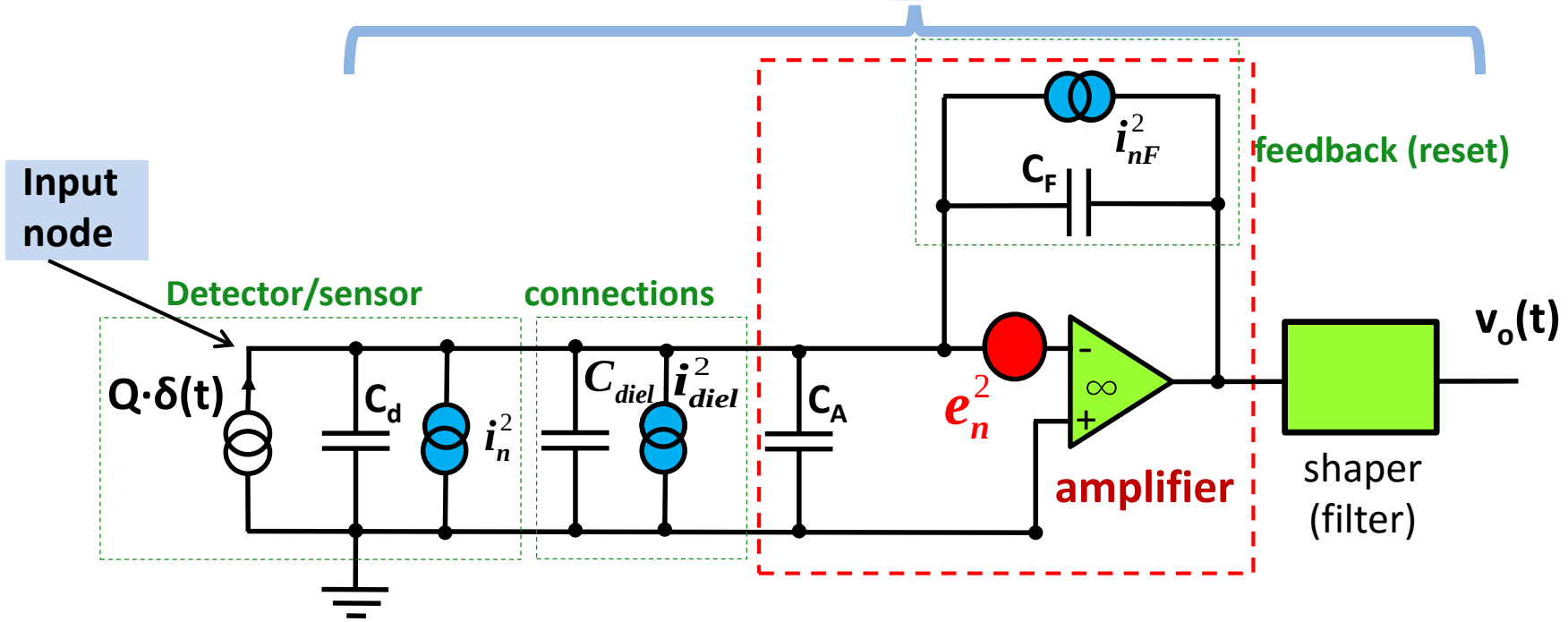
Summary

- Readout electronics developed for low temperatures (77K-300K) is an ***enabling*** technology for noble liquid detectors for neutrino experiments
  - Front end ASICs are integrated with the TPC electrodes in noble liquid to minimize the capacitance and **noise**
  - On chip **digitization** to convert to digital signals inside detector cryostat
  - **Multiplexing** to high speed serial link, to reduce cable plants, minimize outgassing, make possible the scalability to larger detector volumes
- Cold Electronics Development for ProtoDUNE-SP
  - Cold electronics ***successfully*** achieved by MicroBooNE experiment
  - It has high impact, but not risk free and needs continuous advancement
  - **Integration test** and QA/QC test will start soon to ensure the success of experiment
- Instrument ProtoDUNE-SP in 2017
  - Cold electronics will continue to be optimized to meet requirements of various experiments, with final goal to instrument the first 10 kt far detector

Backup Slides

Noise Sources in Detector-Amplifier

Overall system processing function: $h(t); w(t); H(j\omega)$



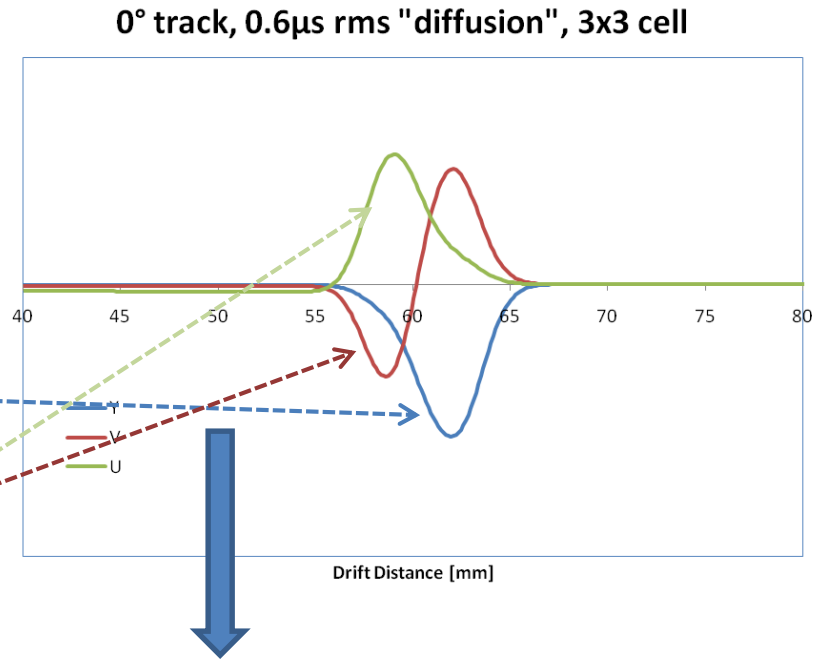
Dominant noise sources are from the components and circuits **directly connected to the input node**. Noise sources from the rest of the signal processing chain should be made negligible.

- i_n^2 arises in the sensor, e.g., from the leakage (dark) current; i_{nF}^2 may arise in feedback circuit
- i_{diel}^2 thermal fluctuations in dielectrics (dielectric loss noise)
- e_n^2 **noise associated with the input transistor:**
  MOSFET gain: "*series white noise*"
  trapping-detrapping: *1/f* eq. noise voltage generator in series

Signals in LAr TPC

- Charge signal
  - A 3mm MIP track should create 210keV/mm x 3mm /23.6eV/e = 4.3fC
  - After a 1/3 initial recombination loss: ~2.8fC
  - Assume the drift path to equal the charge life time, reducing the signal to 1/e≈0.368
  - The expected signal for 3mm wire spacing is then ≈1fC=6250 e, … and for 5mm, ≈10^4 e, for **the "collection signal"**
  - The induction signals are smaller
  - The time scale of TPC signals is determined by the **wire plane spacing** and **electron drift velocity**, (~1.5 mm/μs at 500 V/cm)

Induced Current Waveforms on 3 Sense Wire Planes



Sampling rate **≤ 2 Ms/s**

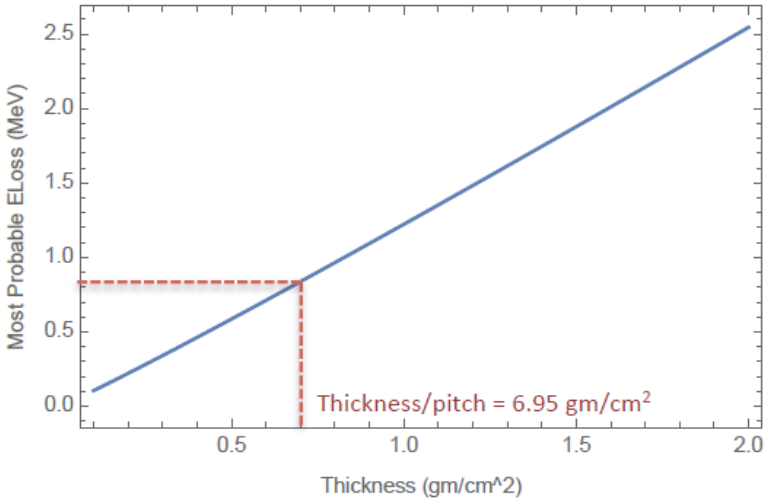
Signal to Noise

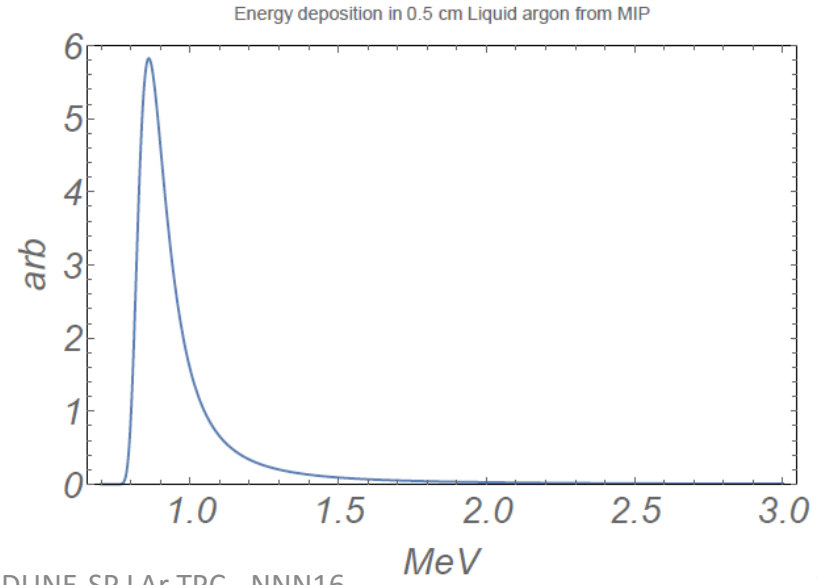
Total equivalent noise charge (ENC) shall be less than 1/9 of the expected worse case instantaneous charge arriving at the APA from a MIP.

- Driven by far detector S:N requirement to "distinguish a Minimum Ionizing Particle (MIP) track cleanly from electronic noise everywhere within the drift volume."
- Simple calculation of charge from a MIP track at the cathode parallel to the wire spacing:

$$\frac{E_{loss}\ (0.5\ cm)}{LAr\ E_{ee}} \times \frac{Recombination}{(500\ V/cm)} \times e^{-\frac{DL/velocity}{e^- lifetime}} = \frac{0.83\ MeV}{23.6\ eV} \times 0.7 \times e^{-\frac{3.6m/1.6\ m/ms}{3\ ms}} = 11{,}629\ e^-$$

- Sets the collection wire noise parameter at ENC < 1300 e^-
- Equivalent charge on the induction wires is expected to be 0.5 x collection wire charge
- Induction wire noise parameter ENC < 650 e^-





Dynamic Range

The requirement to measure a MIP-size charge from the cathode with a precision of 1% in the collection plane determines the lower end of the dynamic range. The need to collect charge deposited at the vertex of a neutrino event (mainly by protons) without suffering satura0on sets the upper end.

- Lower end calculation
  - To obtain 1% charge resolution requires 1% of 11.6k e^-: ~116 e^- per ADC count
- Upper end calculation
  - Proton energy distribution is isotropic in the range 10-100 MeV
  - Worst case assumption: all energy deposited in one 0.5cm voxel
  - Proton at wire plane: no drift losses, instantaneous deposition

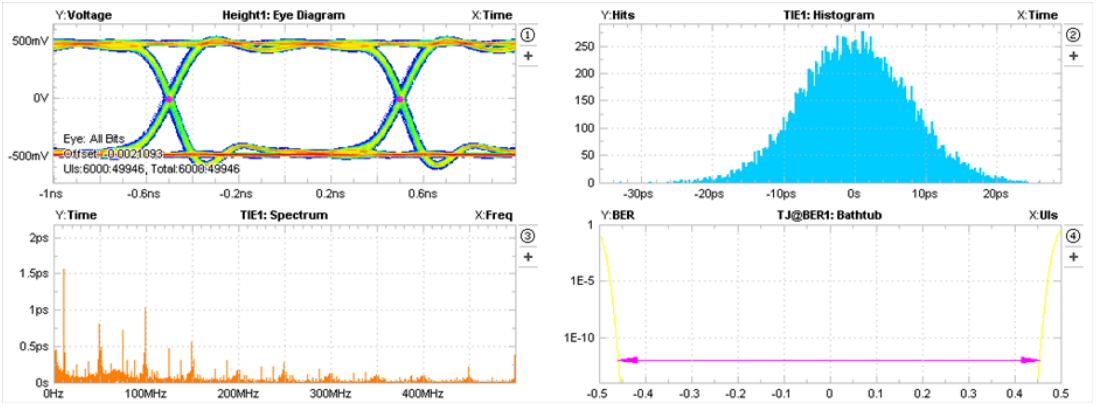
$$\frac{E_{loss}\ (0.5\ cm)}{LAr\ E_{ee}} \times \frac{Recombination}{(500\ V/cm)} = \frac{21\ MeV}{23.6\ eV} \times 0.25 = 222.5k\ e^-$$

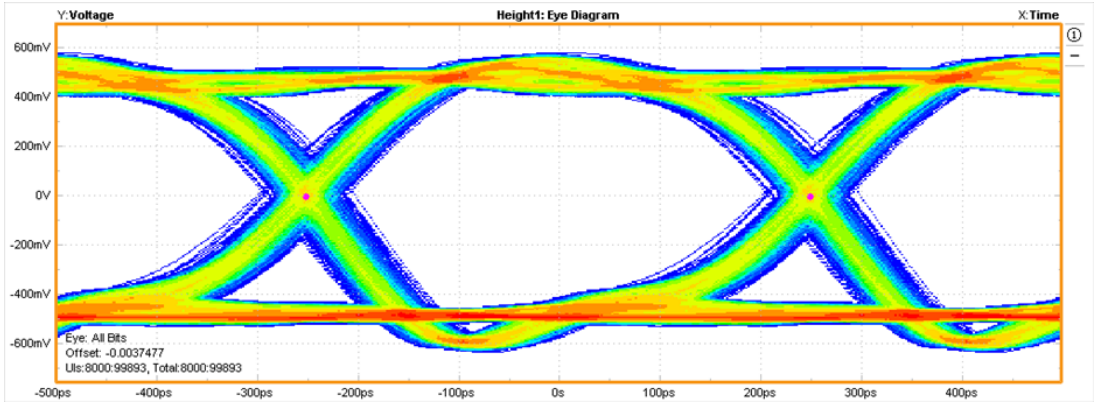
  - For CC ν_e - Ar interactions assume a mean of 2 protons/vertex
  - 445k e^- maximum charge ÷ 116 e^- /count = 3,836 counts

12-bit ADC is sufficient for digitization

Cold FPGA (COTS)

- Many commercial FPGA were tested by BNL
  - Altera Cyclone IV FPGA GX is qualified FPGA for cold operation



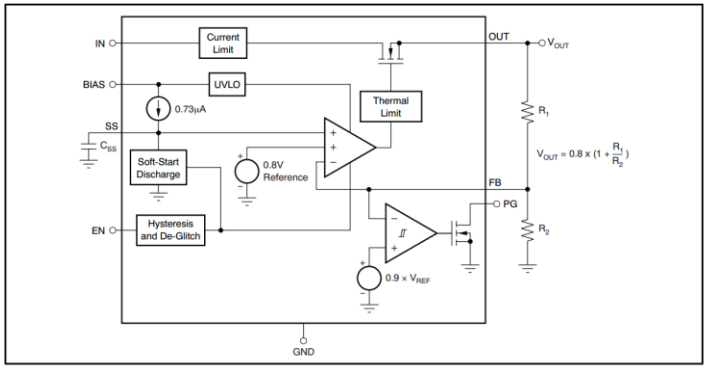


Test of Cyclone IV GX Transceiver Starter Board in LN2

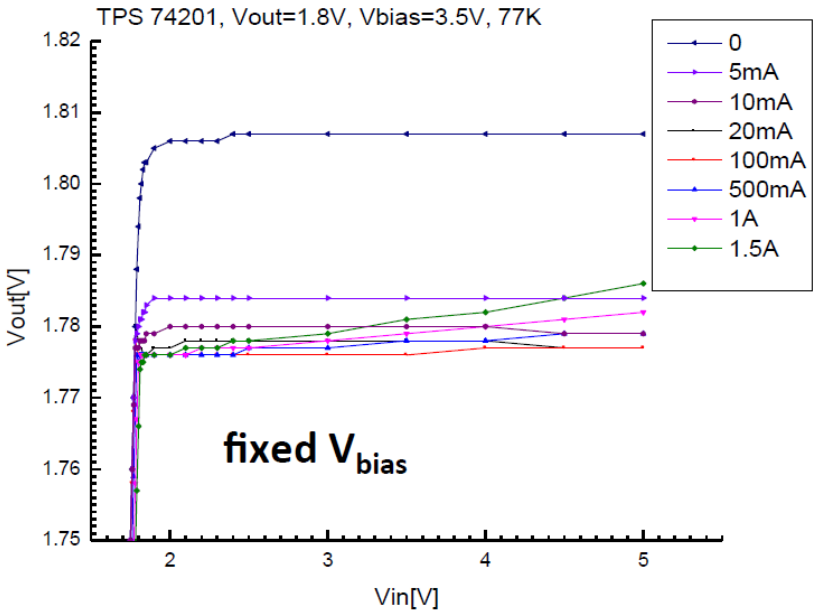
- Transceiver works well at both 1Gbit/s and 2Gbit/s
- Height
  - 839mV @ 1Gbit/s
  - 823mV @ 2Gbit/s
- Eye Width
  - 914ps @ 1Gbit/s
  - 357ps @ 2Gbit/s
- On board SRAM works with BIST
  - 18-Mb SRAM from ISSI IS61VPS102418A-250TQL
  - Cyclone IV GX is running with Nios II processor and utilization of ~80% fabric resources

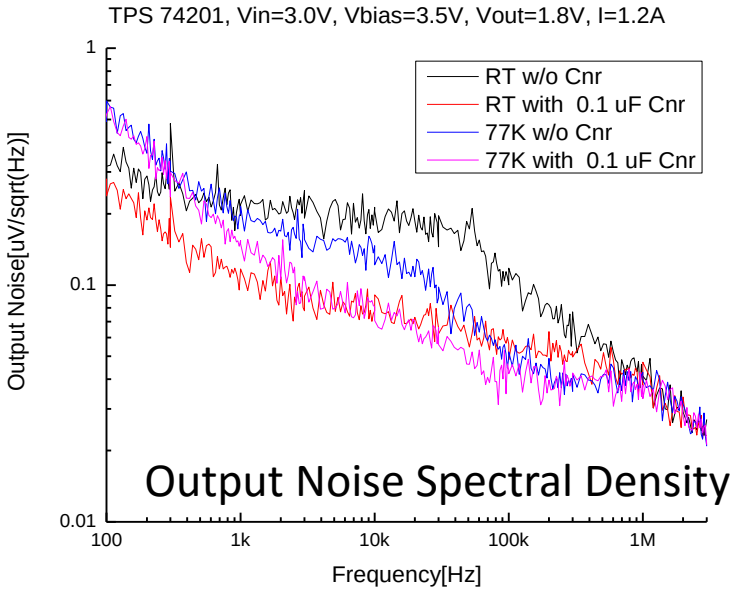
Cold Voltage Regulator (COTS)

- TI TPS742xx voltage regulator family has been identified working well at cryogenic temperature by BNL

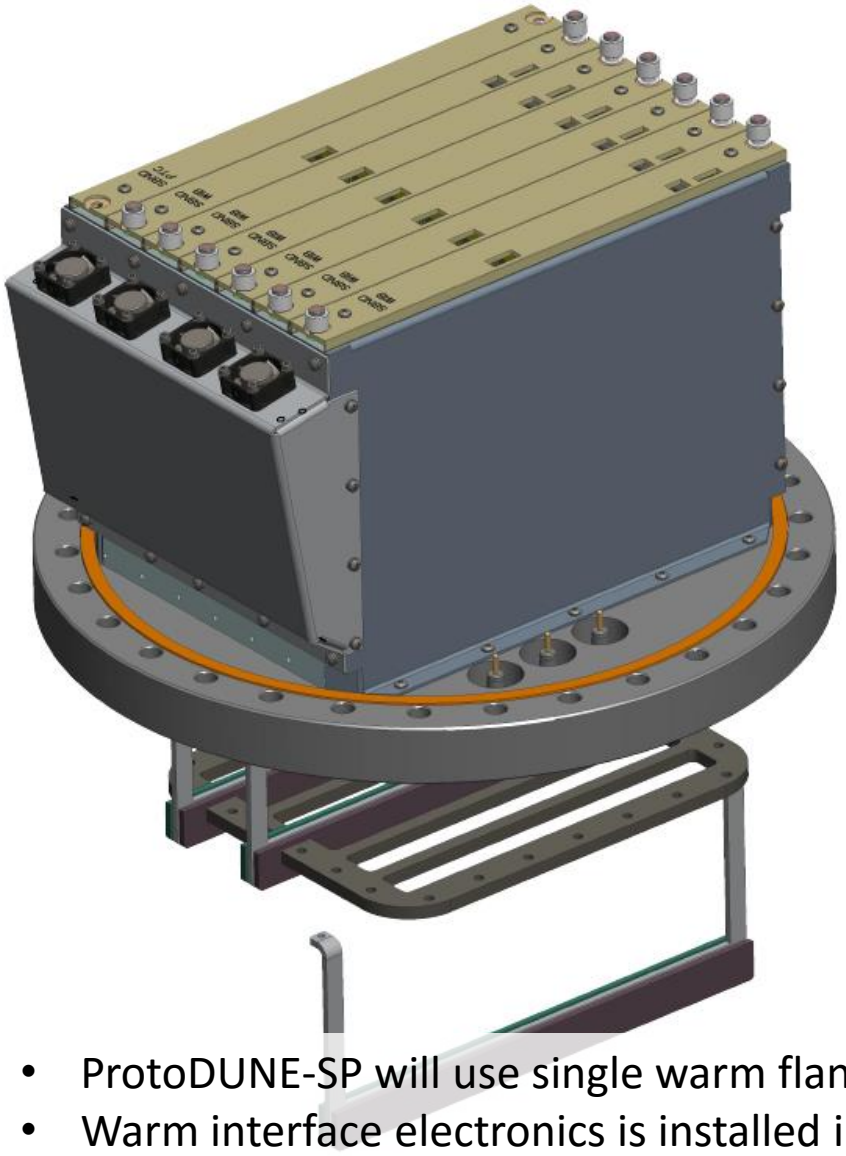


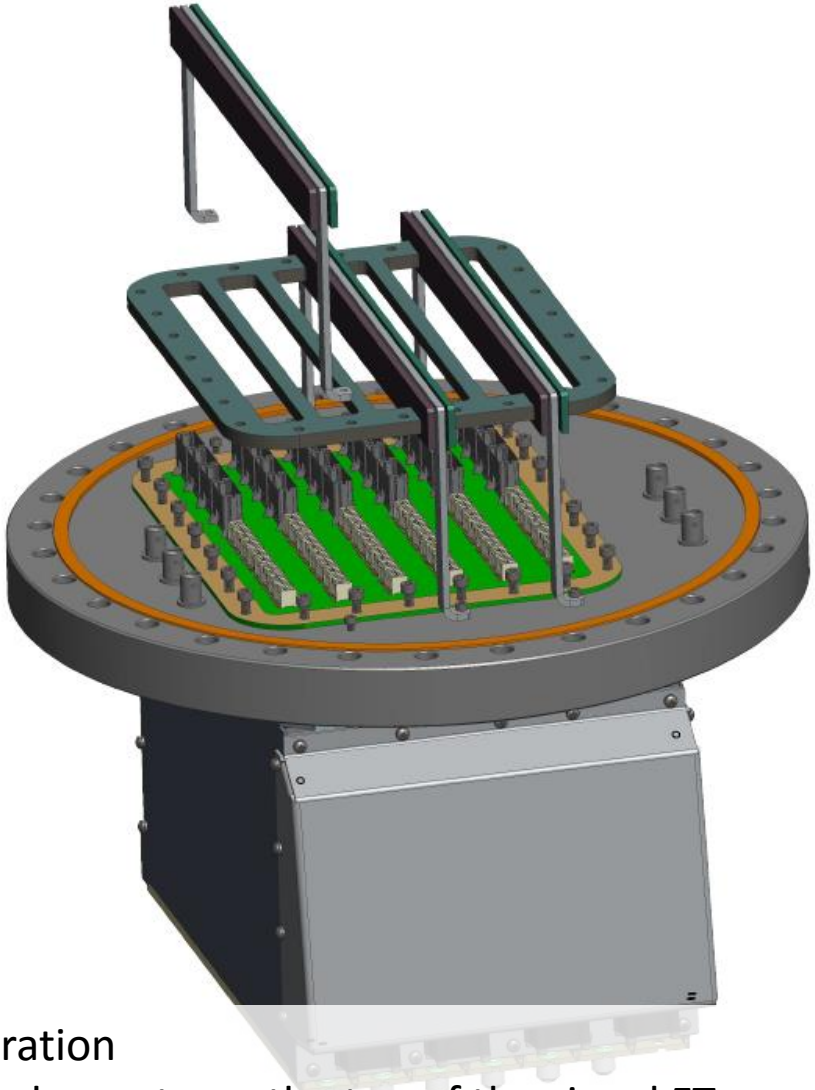
- 1.5A max I_{out}, 0.8V-3.6V adjustable V_{out}, and 55mV drop-out (typical @1.5A) makes it an ideal candidate for all of the cold electronics chain
- Low frequency noise will need to be filtered out properly to achieve optimum noise performance of cold electronics





Warm Interface Electronics on Signal Feed Through



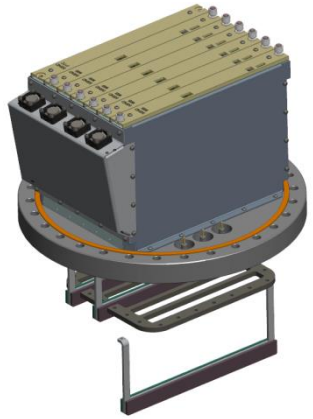


- ProtoDUNE-SP will use single warm flange configuration
- Warm interface electronics is installed inside a faraday crate on the top of the signal FT

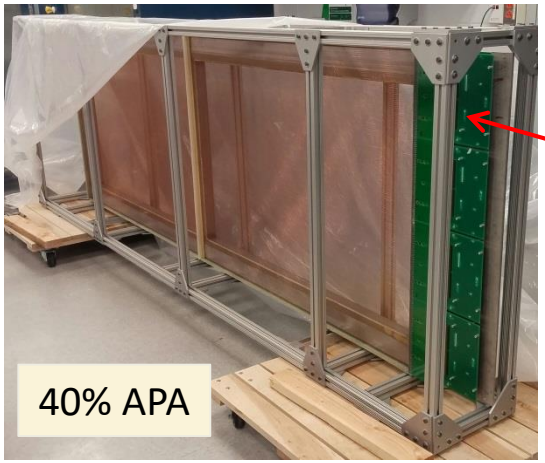
Integration Test Stand

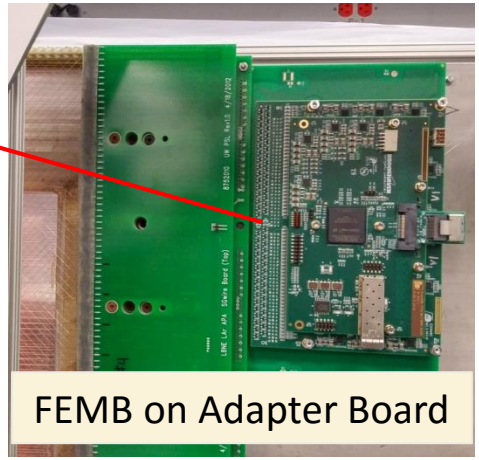
- Integration test stand is an important step to study the detector and readout electronics integration and performance
  - Test stands are being prepared at BNL, Fermilab and CERN with different focus
  - BNL: APA and FEE integration at both RT and LN2
- The TPC APA + Cold Readout + Feed-through + Faraday Cage with Warm Interface and Local Diagnostics should be treated as an integrated whole
  - BNL integration test stand will test the full readout chain from APA to WIB
  - Cold box will house the 40% APA from DUNE prototype, plus cold electronics and cold cable
  - Signal feed-through assembly and warm interface electronics housed in the crate will be installed
- Integration test will start in mid-November

Integration Test stand



Cold box will house APA+CE, plus cold LV and data cable.
Cold box can be tilted to submerge FEMB+cable in LN2





7m Cold Data Cable and Power Cable