Performance of ICARUS T600 electronics at LNGS and its upgrade for operation on SBN at FNAL.

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ICARUS-WA104 Collaboration

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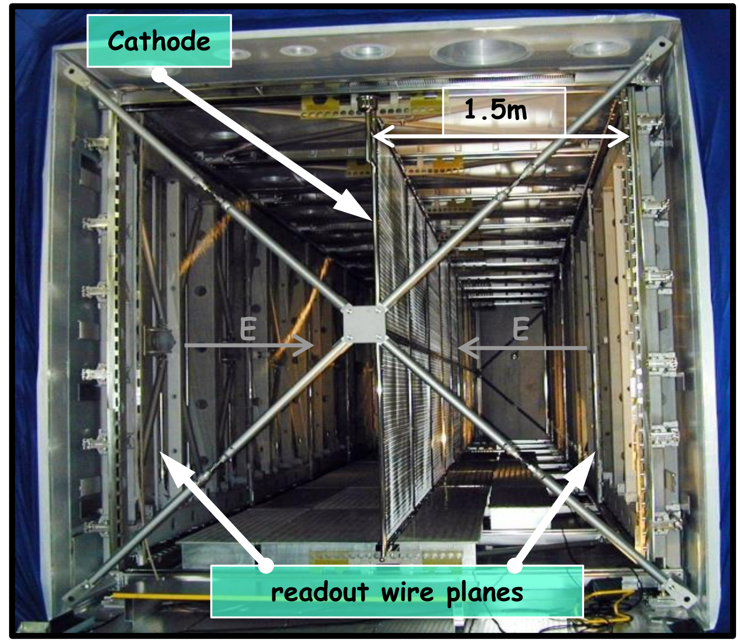
Outline

- ICARUS T600 TPC
- ICARUS T600 electronics and DAQ
- Upgrading for SBN operation at FNAL
- Cosmic rays test results
- Conclusions

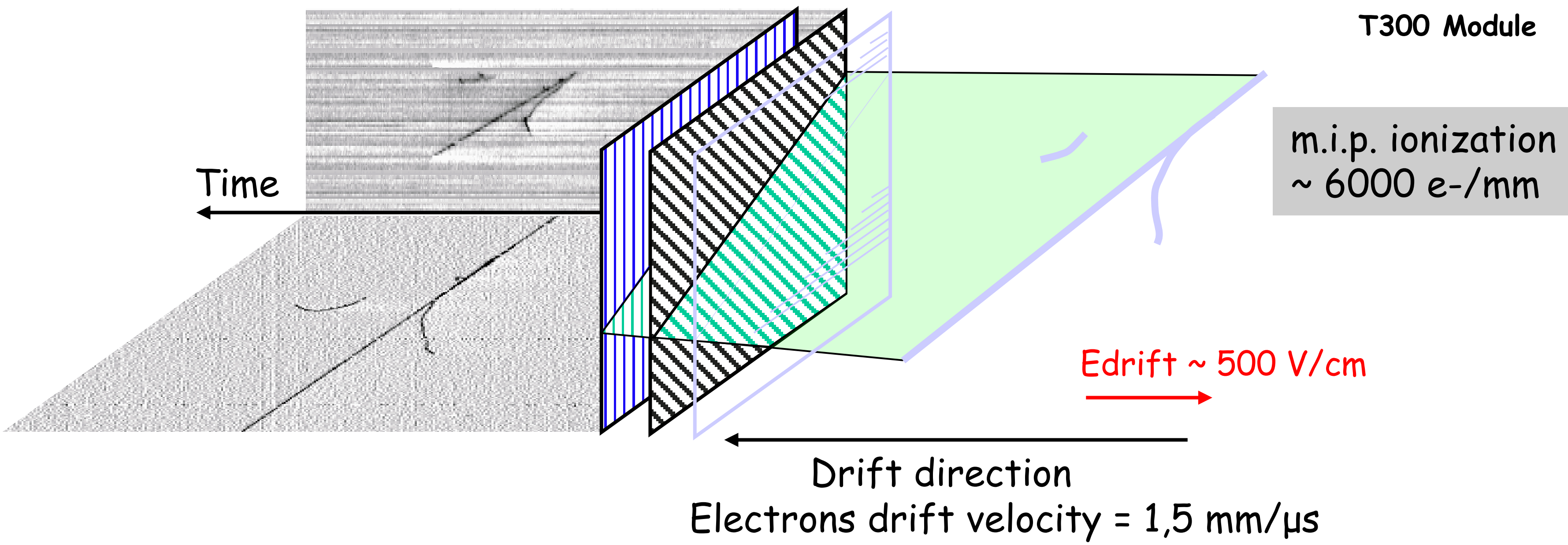
ICARUS T600 TPC

ICARUS T600 is the *unique* example of very large mass liquid argon (LAr) Time Projection Chamber (TPC). It provides 3D imaging of any ionizing event (like an electronic bubble chamber). A major feature is the continuous sensitivity, self triggering capability, and calorimetric measurement.

- 2 identical T300 modules adjacent (3.6m x 3.9m x 19.6m each)
- 2 chambers per module, 1.5 m drift length each
- 3 readout wire planes per chamber wires at 0, ±60° (ind1, ind2, coll view)
- 53248 wires, 3 mm pitch and plane spacing



T300 Module



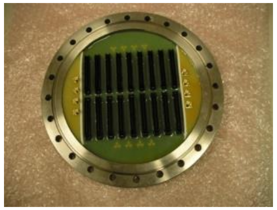
ICARUS front-end electronics racks

96 racks on the top of detector:

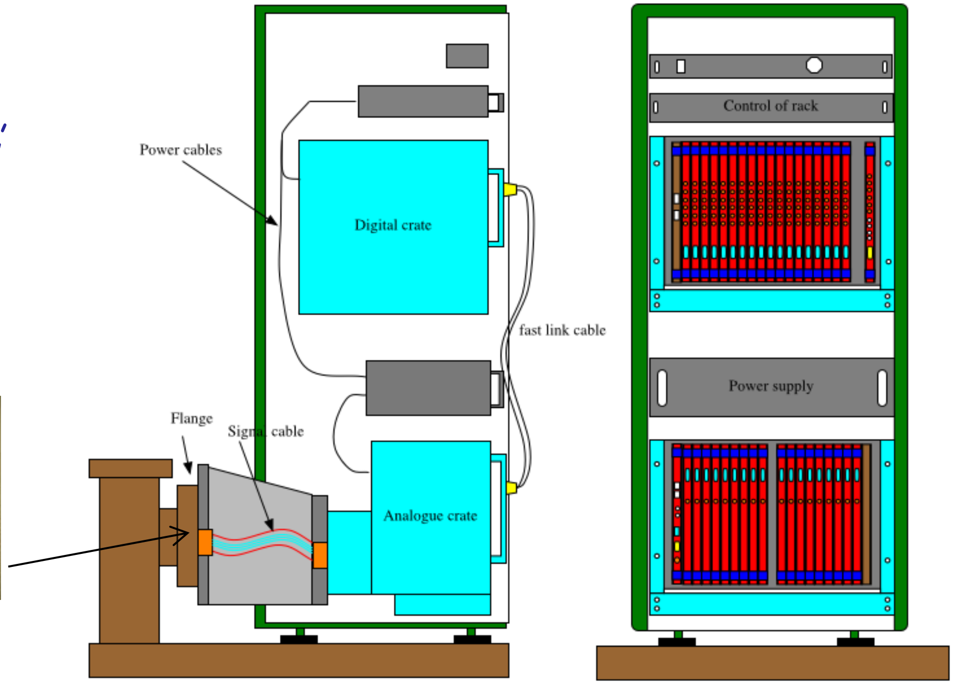
- 16 racks for the horizontal wires of Induction-1 plane (528 ch per rack).
- 72 racks for the wires at $\pm 60^0$ of Induction-2 and collection plane (576 ch per rack, except of four racks, first and last of each row, with 448 ch each).
- 8 racks for the wires of decreasing length at $\pm 60^0$ from the corners of the wire frame (544 ch per rack).

Each single rack, in front of each feedthrough flange, houses 576 readout channels (32 ch modularity) and contains:

- One VME-like analogue crate with 18 analog boards, 18 decoupling boards in the backplane, and one slow control Mod.
- One digital VME crate with 18 digital boards, one CPU, and one clock/trigger distributor Mod.
- Power supplies and their control and monitor.

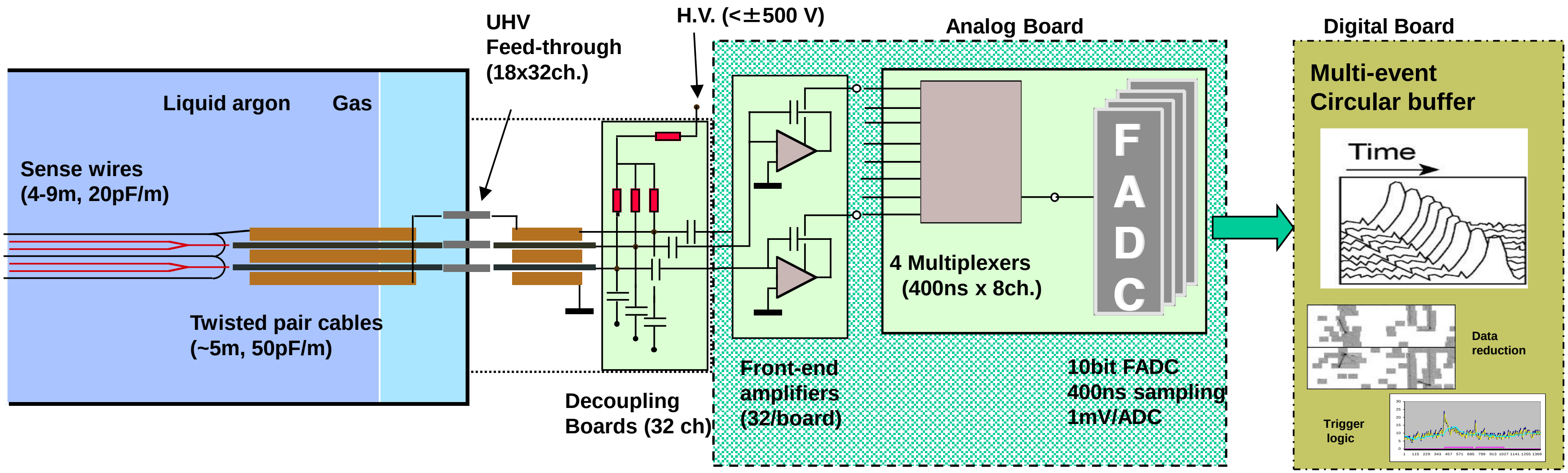


UHV Feed-through (18 x 32ch.)



ICARUS front-end electronics

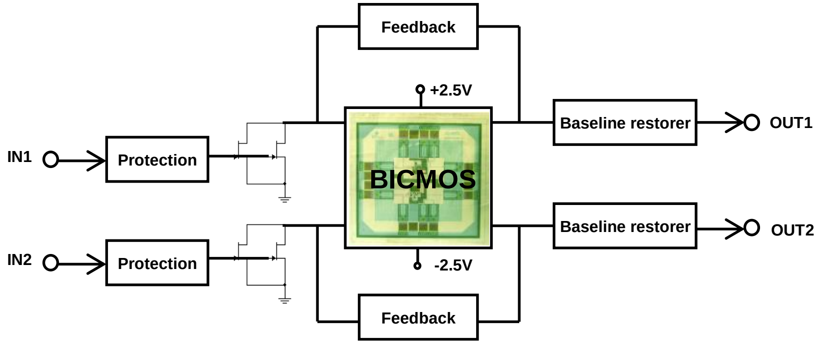
- The ICARUS T600 read-out electronics was designed to provide continuous digitization and waveform recording of the signals from each wire of the TPC.
- **Decoupling Board**: it receives 32 analogue signals from the chamber and passes them to the analogue board via decoupling capacitors; it also provides wire biasing voltage and distribution of the test signals.
- **Analog Board**: it hosts 32 front-end low noise charge sensitive pre-amplifiers, performs data multiplexing and data conversion ADC (10 bit). The sampling period for each channel is 400 ns.
- **Digital Board**: it provides multi event buffer memory for 32 channels, data compression, and trigger logic.



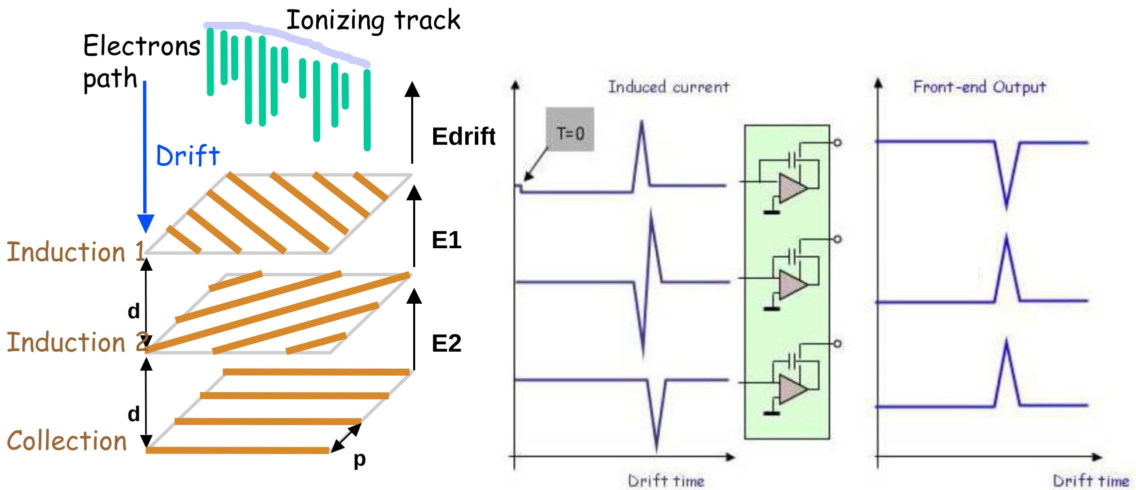
- Signal to noise ratio (S/N) better than 10 and a ~ 0.6 mm single point resolution were obtained during the LNGS run, resulting in precise spatial reconstruction of events, allowing for measuring muon momentum by multiple scattering (MS) with $\Delta p/p$ ~16% in the 0.4-4 GeV/c range.

ICARUS preamplifier and signals

- Input stage: two jFet are connected in parallel.
- Custom IC in BiCMOS technology
  - Two channels unfolded Radeka integrator
  - External feedback network
- Baseline restorer circuit
- Two versions
  - "quasi-current" mode: $R_f C_f \approx 3\mu s$ (collection + first induction);
  - "quasi-charge" mode: $R_f C_f \approx 100\mu s$ (mid induction);



Sensitivity ≈ 6 mV/fC
Dynamic range > 200 fC
Linearity < 0.5% @ full scale
Gain uniformity < 3%
E.N.C. ≈ (350 + 2.5 x C_D) el
≈ 1200 el. @350pF
Power consumption ≈ 40 mW/channel



Shaping time at output:

- Current mode (Induction 1, Collection): ~ $3\mu s$. Signal proportional to induced current. Integral of collection signal area proportional to charge.
- Charge mode (Induction 2): ~ $3\mu s$. Signal amplitude proportional to charge.

Lossless data compression

Online lossless data compression

- In data collected with T600 LAr-TPC, the difference between one sample and the previous one is within ± 7 ADC counts in more than about 98% of the cases.
- This allows for storing the differences instead of the full 10 bit data, using fewer bits.

Compression scheme

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
4-bit Difference of channel N				4-bit Difference of channel N+1				4-bit Difference of channel N+2				4-bit Difference of channel N+3			

Difference

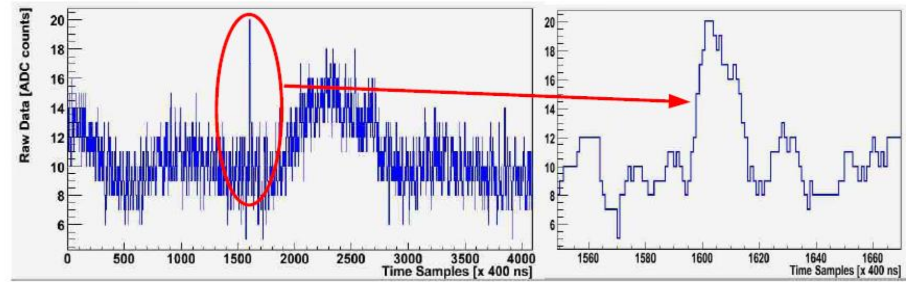
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0			10-bit full difference									

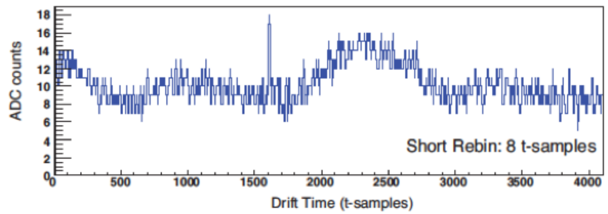
- Assuming to handle data in 2-Byte format, the choice is to pack four 4 bit difference (± 7 ADC counts) obtaining a ~4 compression factor.
- When the difference is larger than |7|, the full difference is stored in 2-Byte with a 4 bit flag (1000).
- The compression efficiency is affected by the large energy deposition from e.m showers or high dE/dx tracks.
- During LNGS run the real measured compression factor was 3.92.

Hit finding algorithm (double rebinning sliding windows)

Real time algorithm for hit finding implemented on FPGA:

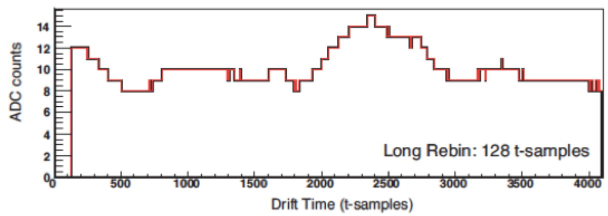
- A typical m.i.p. signal: ~15 ADC counts, 30-40 t-samples, could be affected by:
- Low frequency noise (fluctuation of the baseline): 10-15 ADC counts, 1500 t-samples;
- High frequency noise: 2-3 ADC counts, 5 t-samples.





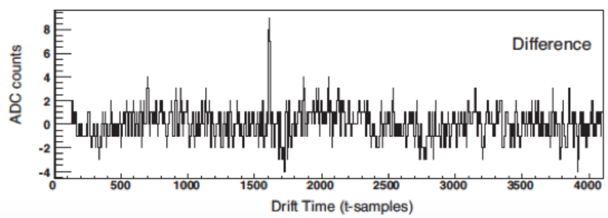
The high frequency component can be smoothed by averaging the waveform over a short time window.

$$Q_8(t) = \frac{1}{8}\sum_{i=0}^{8} Q(t-i)$$



The low frequency component can be smoothed by averaging the waveform over a long time window.

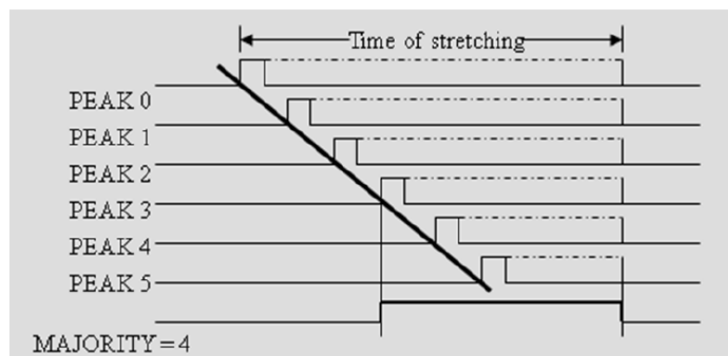
$$Q_{128}(t) = \frac{1}{128}\sum_{i=0}^{128} Q(t-i)$$



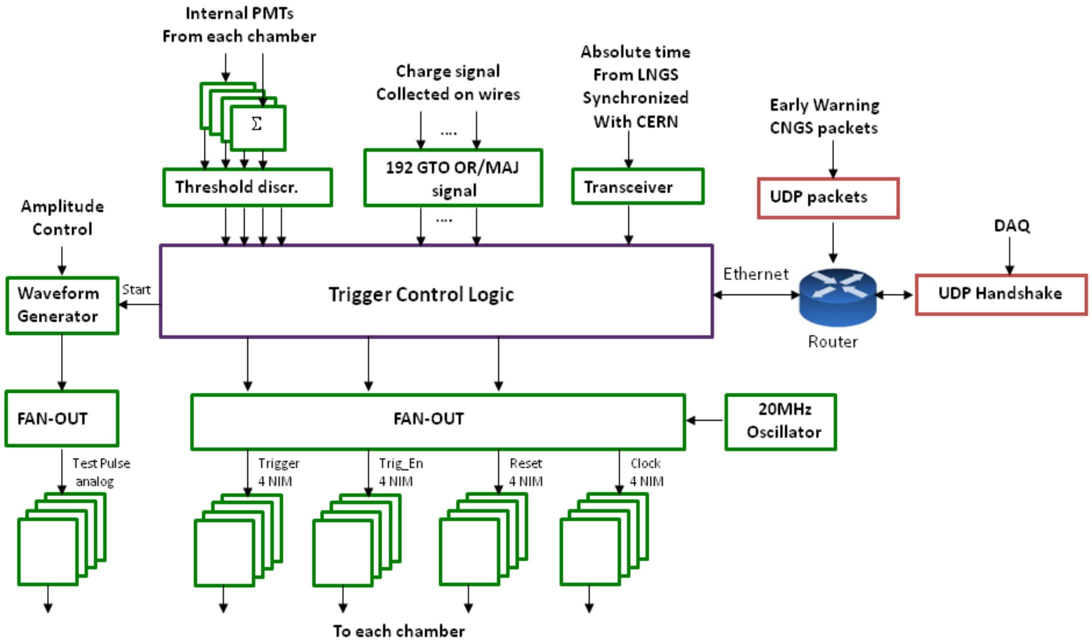
A hit signal is generated when the difference S(t) goes over threshold.

$$S(t) = Q_8(t) - Q_{128}(t)$$

- Majority over 16 consecutive wires (~5cm).
- Peak stretching (25-125 μs) to guarantee high efficiency majority selection for inclined tracks.
- A local trigger is generated by the logical OR of the two majority signal on the same board.



ICARUS global trigger scheme



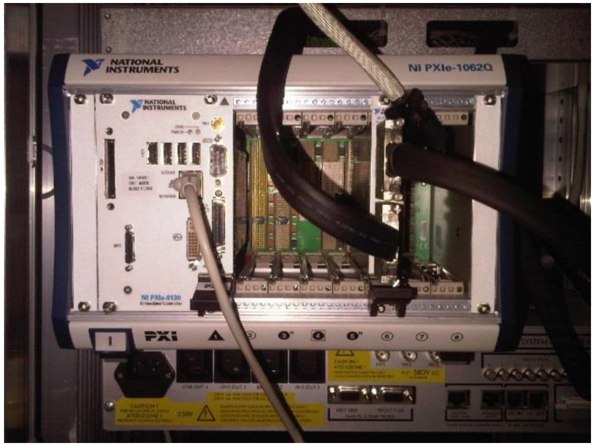
Trigger sources

- CNGS beam gate (obtained from Early warning through internet and GPS);
- Light signals collected by 74 PMTs;
- Charge signals (TPC wires).

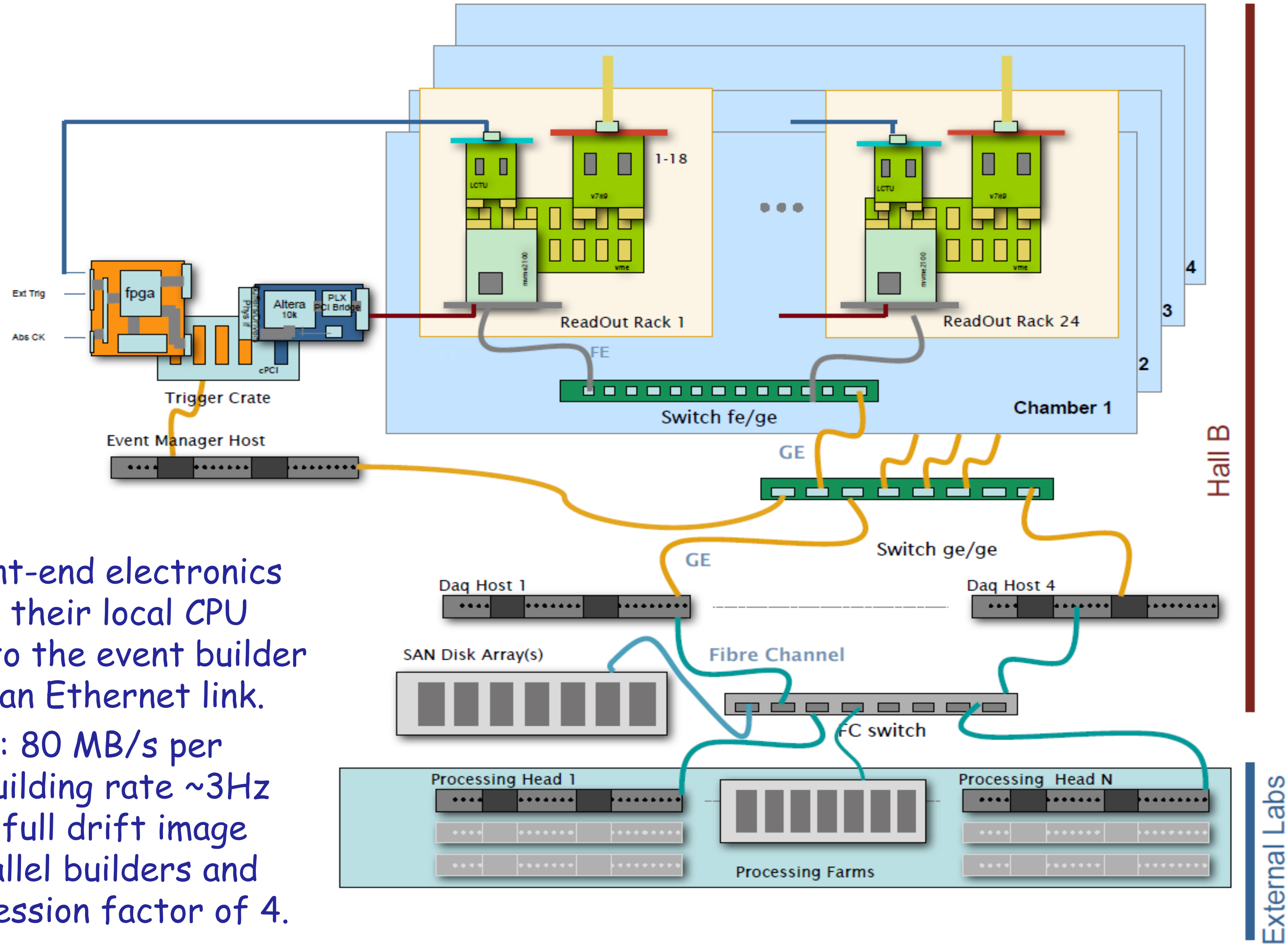
Trigger implementation

- Commercial NI PXI crate;
- Real time controller (PXIe-8130): trigger – DAQ communication;
- FPGA board (PXI-3813R, PXI-7833): signal handling, time critical processing.

- A continuous communication with DAQ, in handshake mode, prevents the generation of new triggers in the case of the detector busy, while a multi-veto configuration minimizes dead-time.

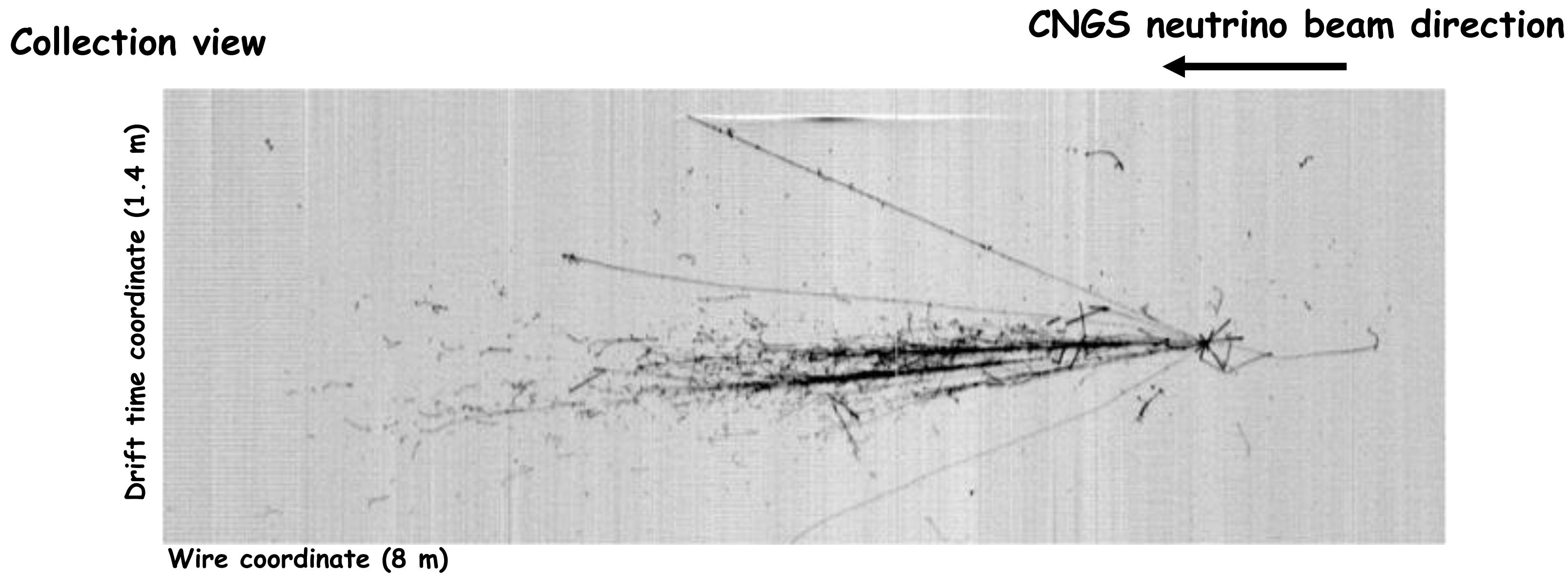


ICARUS T600 DAQ event builder



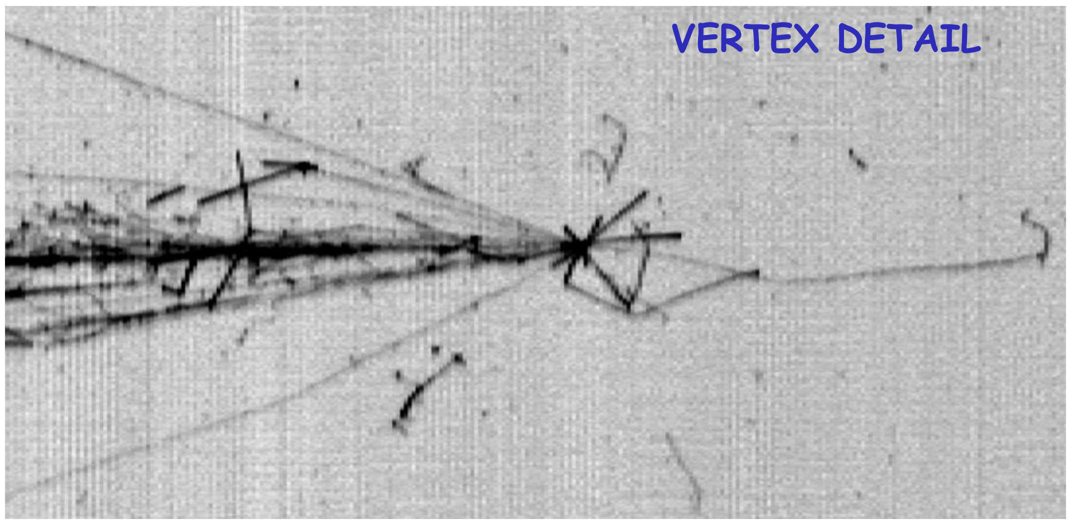
- The 96 front-end electronics crates have their local CPU connected to the event builder PC through an Ethernet link.
- Throughput: 80 MB/s per chamber, building rate ~3Hz for a 1.6ms full drift image using 4 parallel builders and data compression factor of 4.

CNGS neutrino interaction in ICARUS T600 (May 2010)



The first neutrino event!
0.6 mm spatial resolution in 8m image size.

Extremely high quality image thanks to the very high S/N of electronics (not forgetting purity, mechanical precision and stability…).



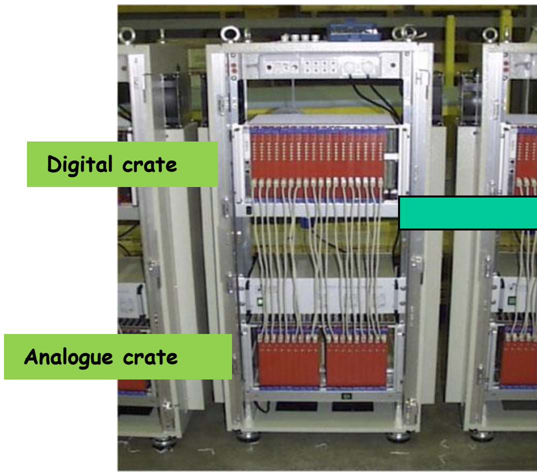
The need for an upgraded electronics

- Even though old electronics can be considered state of the art for the time it was conceived (1998) and well suited for ICARUS-T600, this electronics has some limitations:
  - poor treatment of induction signals, in case of showers or high dE/dx tracks, due to signal undershoot;
  - limited data throughput due to the choice of VME standard (8-10 MB/s), perfectly legitimate at that time.

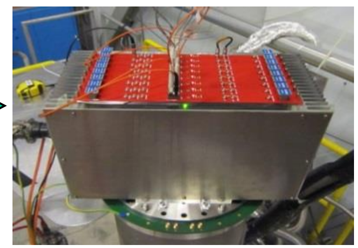
- Improvements concern:
  - short shaping peak time of the analogue signals to avoid undershoot;
  - adoption of serial ADCs and smaller packages of components to make the system much more compact;
  - adoption of a modern serial bus architecture with optical links (Gbit/s) to increase bandwidth;
  - use of the flange as electronics backplane to simplify layout and cabling.

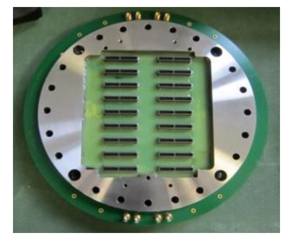
New simplified/compact design

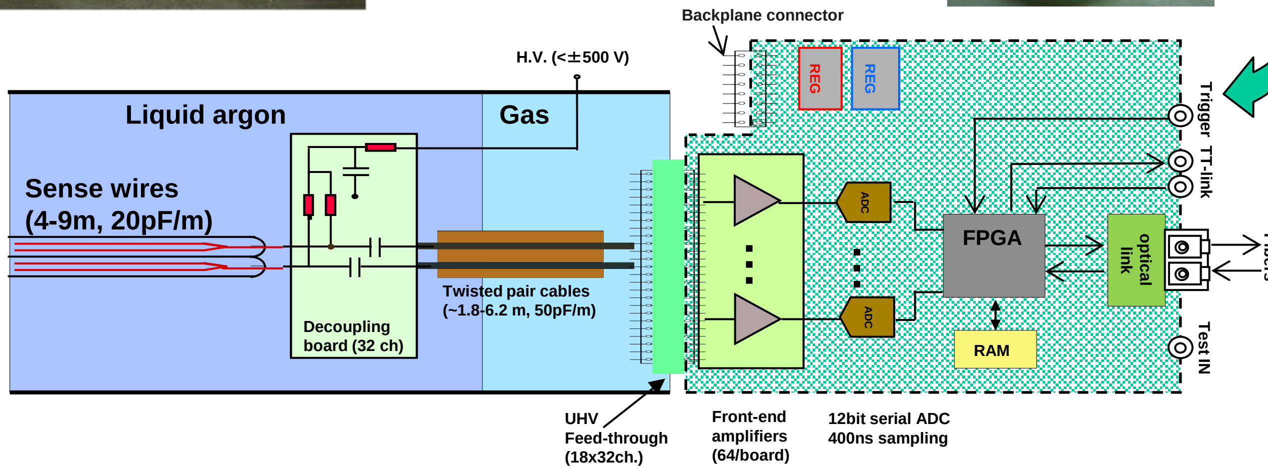
- A new, compact design, has been conceived to host both analogue and digital electronics on a single board directly connected to the proprietary flanges.
- One mini-crate, mounted on the flange, can host 9 boards for 576 channels, 64 channels each.
- The backplane of the crate distributes the power supply and local control signals.
- A single boards hosts 64 front-end low noise charge sensitive pre-amplifiers, 64 serial 12 bit ADC (2.5 MHz), FPGA, memory, optical link interface…



From 595 to 10 liters

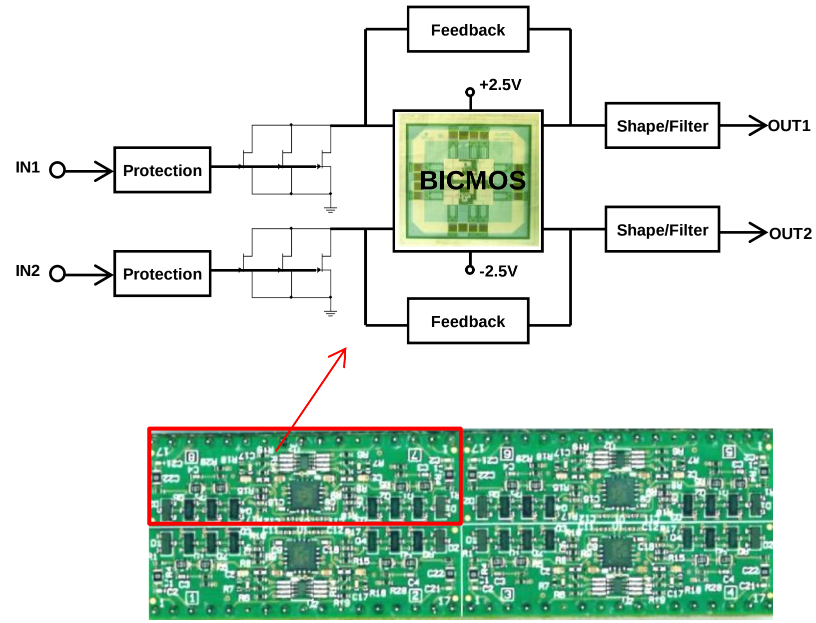




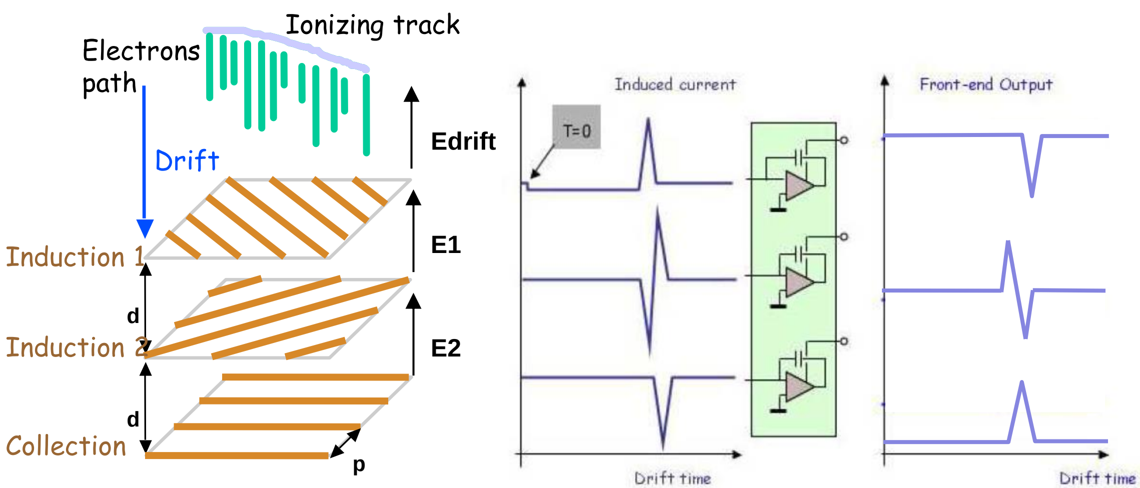


Improved preamplifier

- Three jFet are connected in parallel to increase g_m (50-60 mS).
- Same pre-amp response (shaping peak time and gain) both for collection and induction signals.
- Adoption of a smaller package for the custom BiCMOS dual channel amplifier.
- The gain of the front-end amplifier and filter is $3\ V/300\ fC$. The $12\ bit$ ADC input range is $3.3\ V$ with a least count equivalent to ~500 electrons. This value matches with the amplifier noise of ~1000 electrons with an "equivalent" detector capacitance of ~$270\ pF$ (wires plus cables).



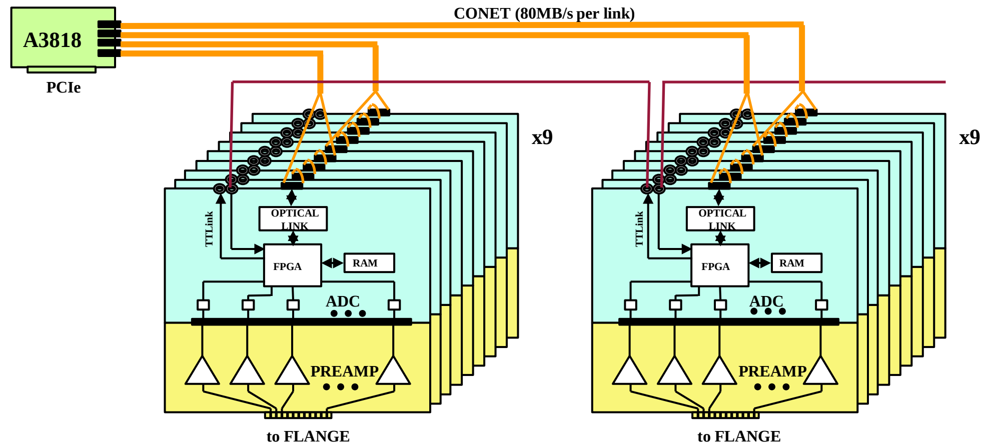
8-channel Preamplifier module

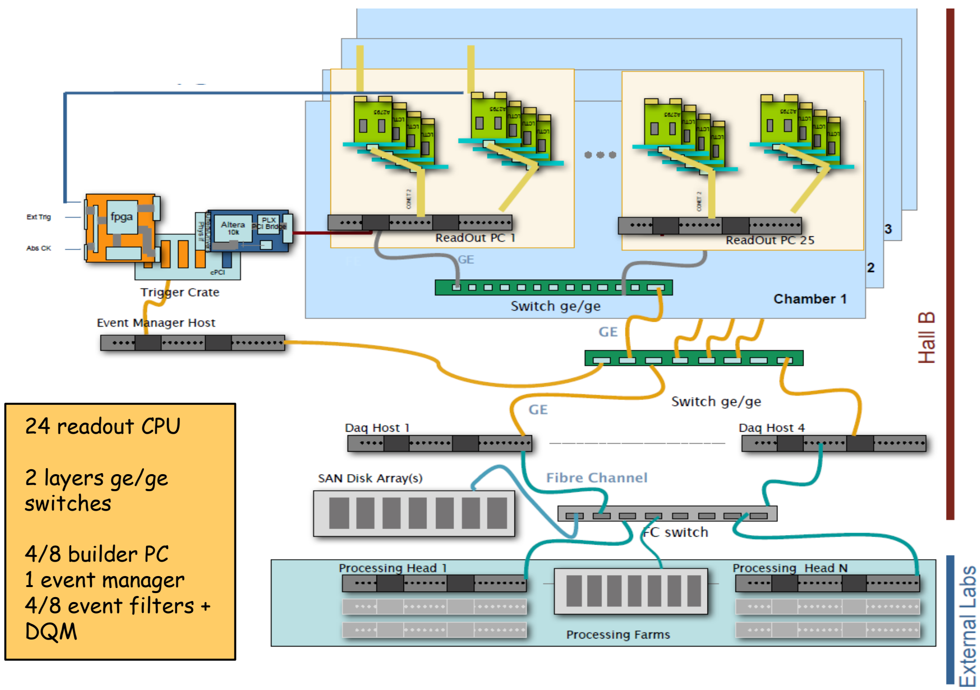


- All views (including Ind2) are read out with pole-zero cancellation circuit, shaping peak time $t = 1.5\ \mu s$.
- Short shaping peak time preserves bipolar signals allowing for numerical integration of the digitized output.

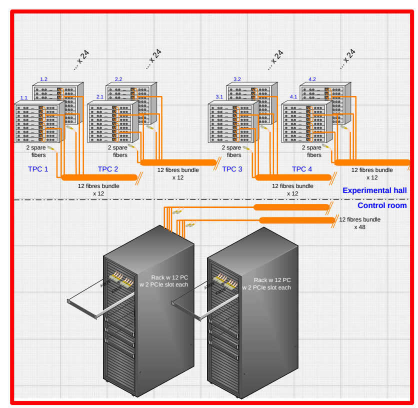
Upgrading DAQ

- The system provisionally uses the CONET transfer protocol.
- Each mini-crate (flange) will require two CONET loops.
- Each A3818 can handle 4 loops (2 flanges).
- On each PC can host 2 A3818, a total of 24 readout PC will be needed for the whole detector





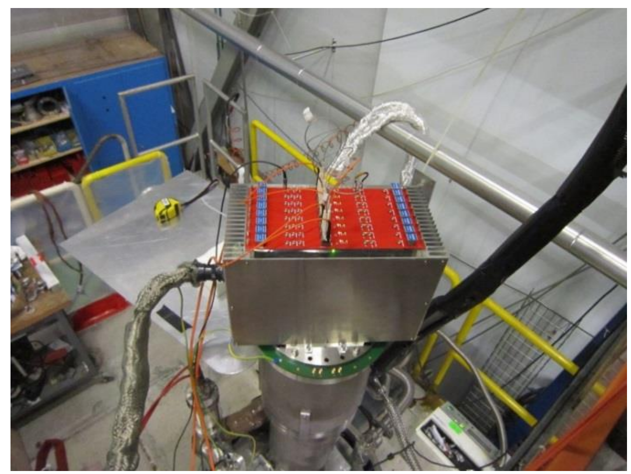
- The readout DAQ could keep the existing DAQ architecture, simply replacing the VME CPU in each readout unit with a PC equipped with a CONET interface. Expected building rate ~15Hz without data compression.



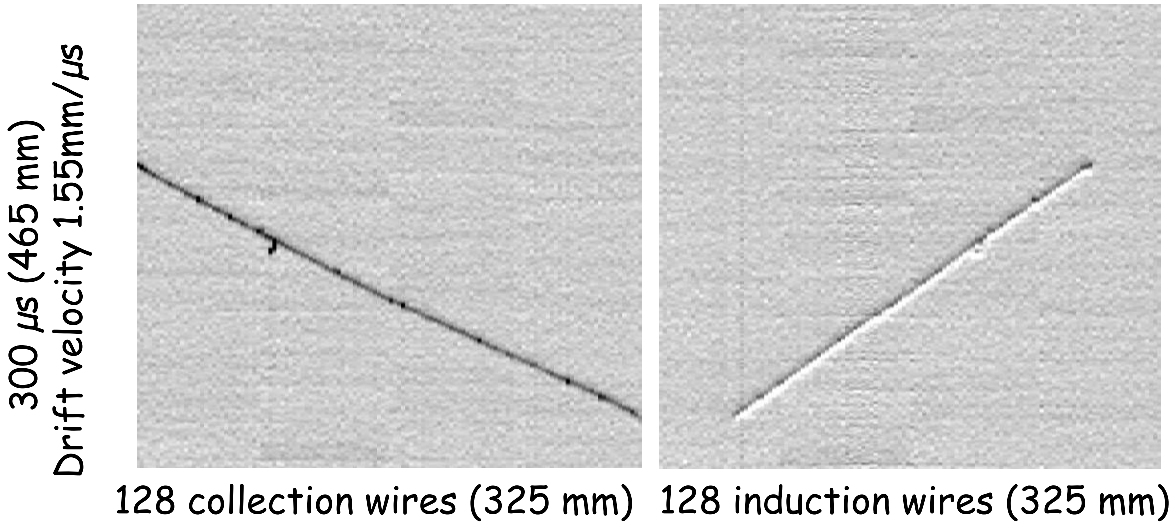
- The whole DAQ can be hosted in a 54U rack
- 4 X 24 fiber bundles (+ spares) from control room to mini crate (~50/100m)

Test facility in CERN (50 liter LAr TPC)

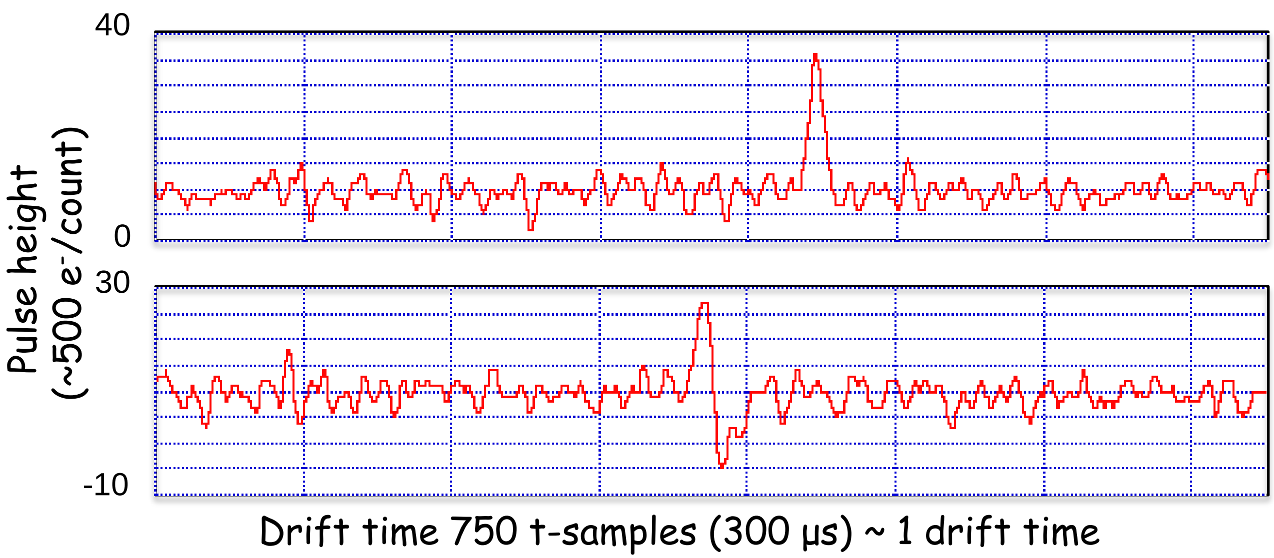
- 2 wire planes (ind, coll), 128 wires each;
- 2.54 mm wire pitch and 4 mm plane spacing
- 46.8 cm drift length, at 500V/cm.
- Cable length as in ICARUS collection plane, about 2.5m



Cosmic rays test @ 50 liter CERN LAr TPC



- A single mip track event:
  - Same ~2ADC counts (~1000 e^-) noise for both Collection & Induction;
  - unipolar collection signal: ~ 25 ADC counts;
  - Symmetric bipolar induction signal with slightly reduced amplitude as expected.
  - No filter applied to any data.

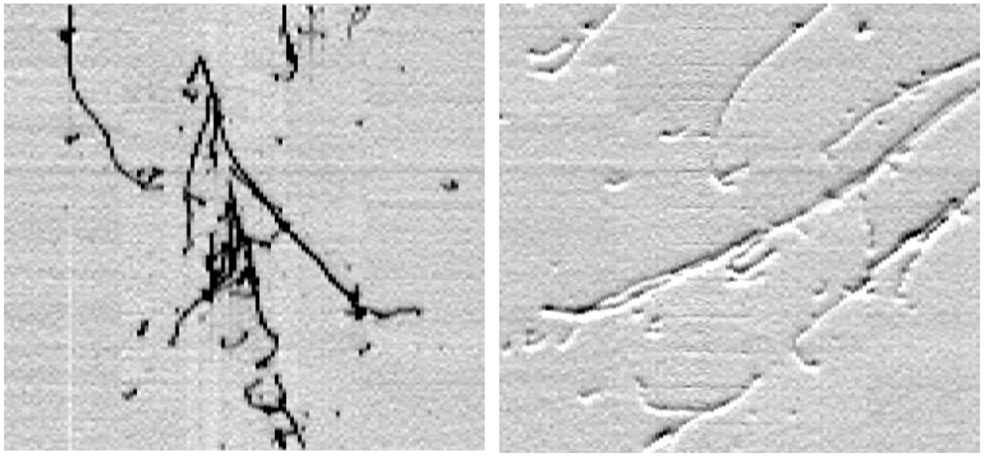


collection signal (on a single wire)

induction signal (on a single wire)

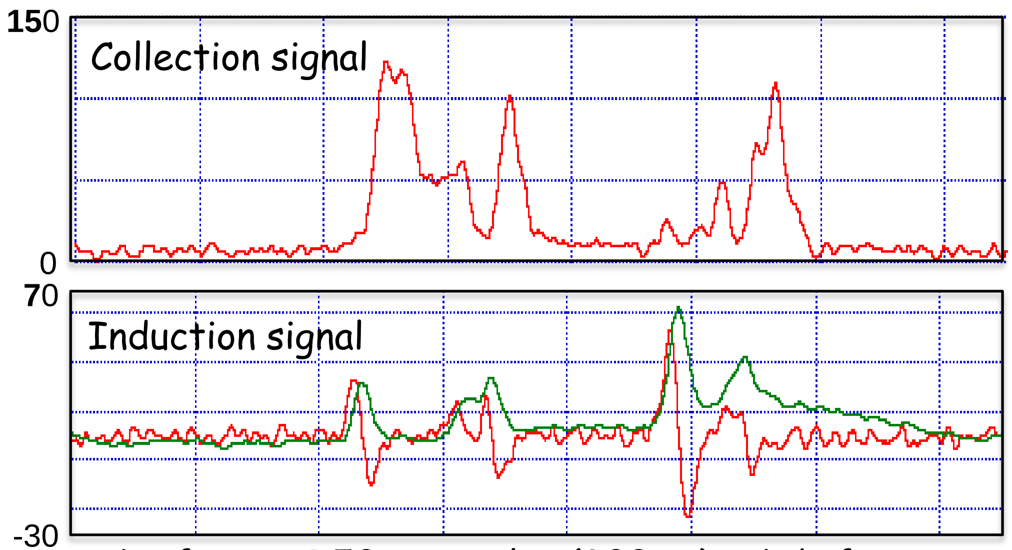
Cosmic rays test @ 50 liter CERN LAr TPC

300 μs (465 mm)
Drift velocity 1.55mm/μs



128 collection wires (325 mm) 128 induction wires (325 mm)

Pulse height
(~500 el/count)

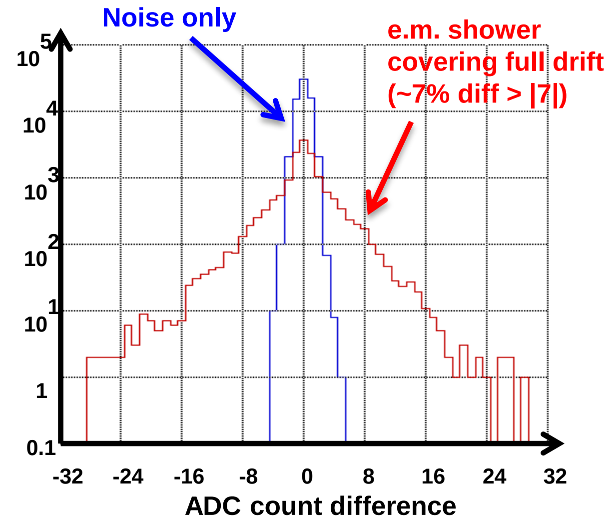


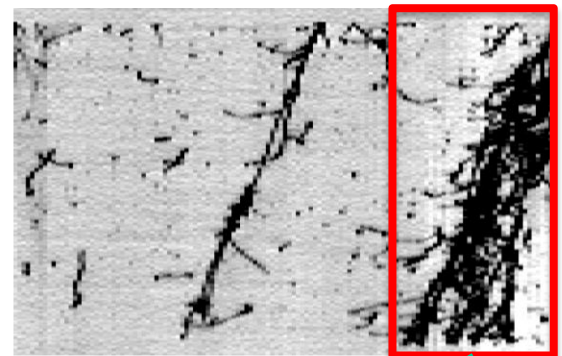
Drift time 750 t-samples (300 μs) ~ 1 drift time

- A shower event developing along the drift direction in Collection;
- The optimized preamp architecture results in:
  - no signal undershoot even after large signals;
  - a very stable baseline;
  - unprecedented image sharpness and better hit position separation due to the faster shaping peak time.
- On induction plane, energy information easily recoverable with dedicated algorithms (e.g. running sum, green curve).
- No filter applied to any data.

Lossless data compression

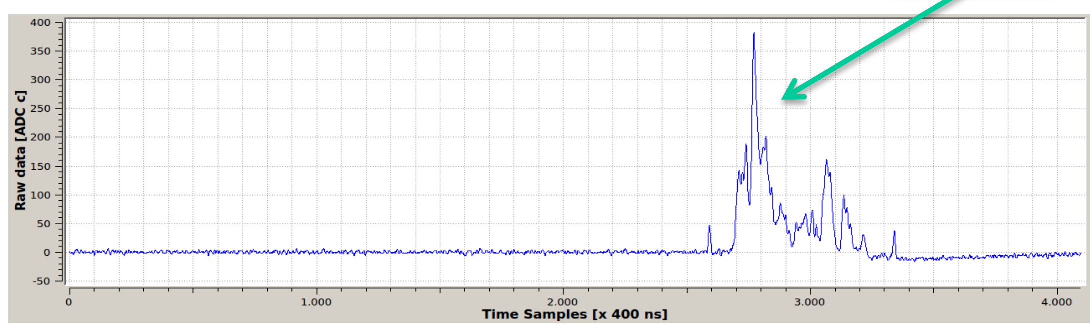
- From the test with the 50 Liter LAr-TPC, due to the low rms noise (~ 1000 electrons = 2 ADC counts), the difference between consecutive samples is within ± 7 ADC counts in 100% of the cases in absence of tracks.
- In case of an event, as shown inside the red rectangle (very high density shower), the difference distribution is as in the red curve above the event image: only 7% of the cases the difference exceeds ± 7 ADC counts.
- We can then use the same compression scheme used for the old system based on 10 bit ADC, according to the model in the figure, expecting a compression factor very similar to the previous one.





Compression scheme															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
4-bit Difference of channel N				4-bit Difference of channel N+1				4-bit Difference of channel N+2				4-bit Difference of channel N+3			

Difference															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	12-bit full difference											



Conclusions

- ICARUS T600 is a milestone being the largest LAr TPC ever operated underground. It produced some thousands high quality neutrino events thanks to its mechanical precision and stability, LAr purity, and electronics quality.
- T600 TPC overhauling is in progress at CERN in view of its transfer to FNAL on SBN beam.
- The improved electronic read out will allow for using also induction view for dE/dx measurement.
- Better S/N ratio (>12).
- The full synchronization of the sampling time in whole system will improve the muon momentum measurement by MS (reduction of $\Delta p/p$ from 16% to 13%).
- The data throughput will increase to ~15Hz.
- Embedding the signal boards onto the feedthrough flange makes the system extremely compact, without external cables between flange and electronics.
- Signal cables do not carry high voltage resulting in microphonic noise reduction.
- Fully external electronics makes the system easy to maintain and suitable for any future evolution.

Thank you !