nEXO Readout Electronics R&D Status

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NNN'16, for the nEXO electronics group

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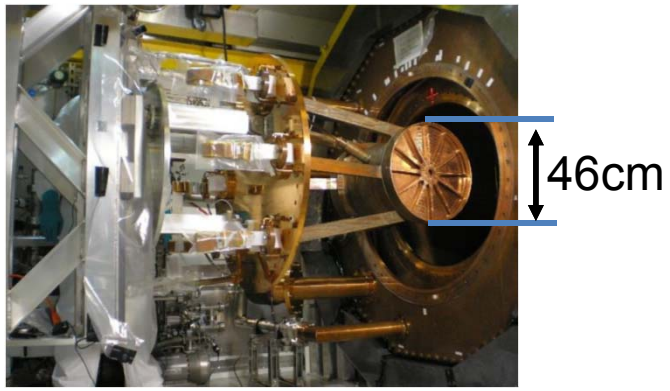
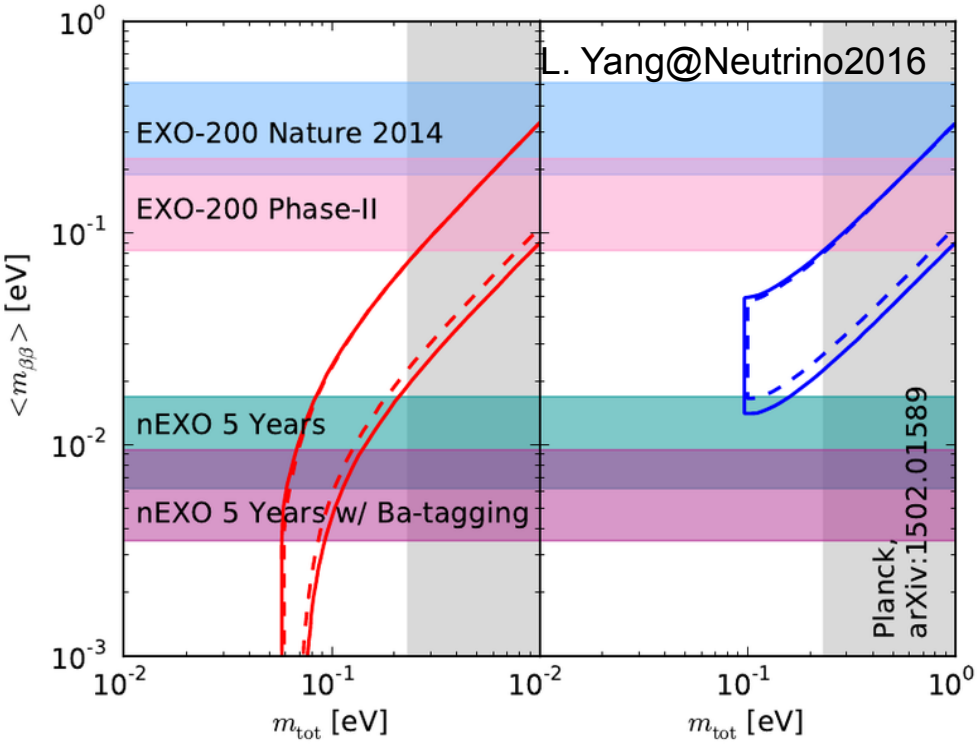
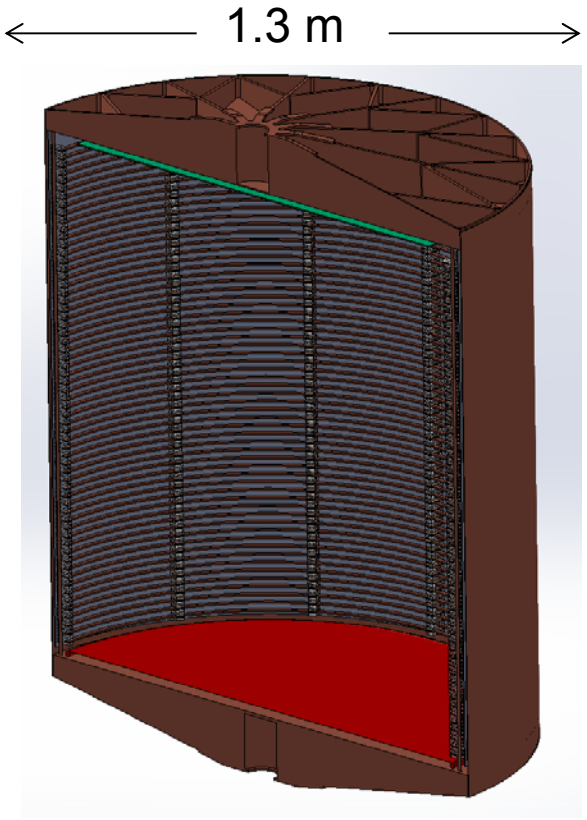
0νββ Search at EXO-200/nEXO

EXO-200: 200kg liquid-Xe TPC



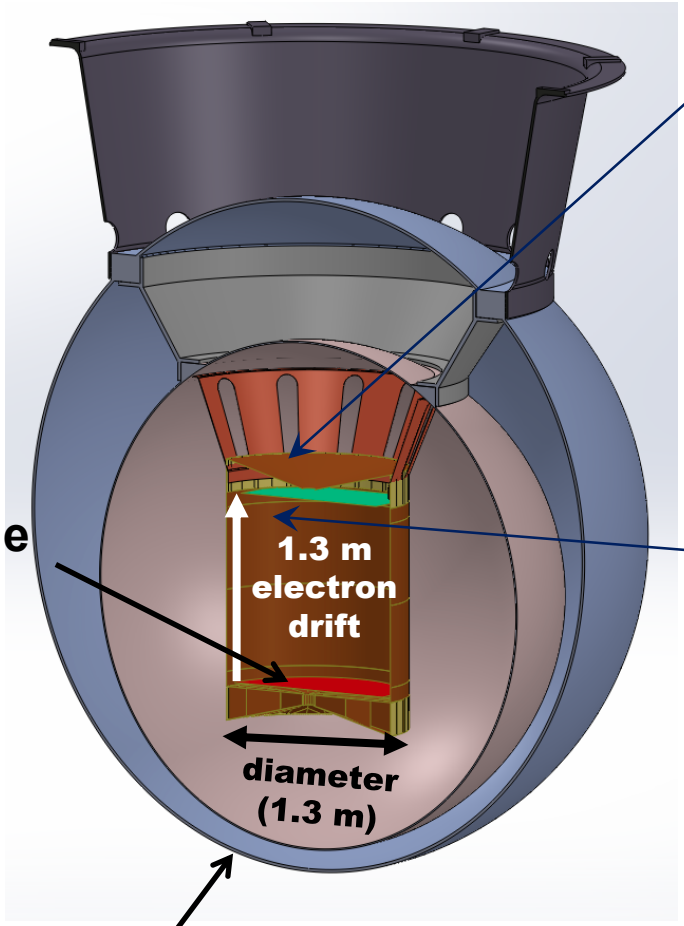




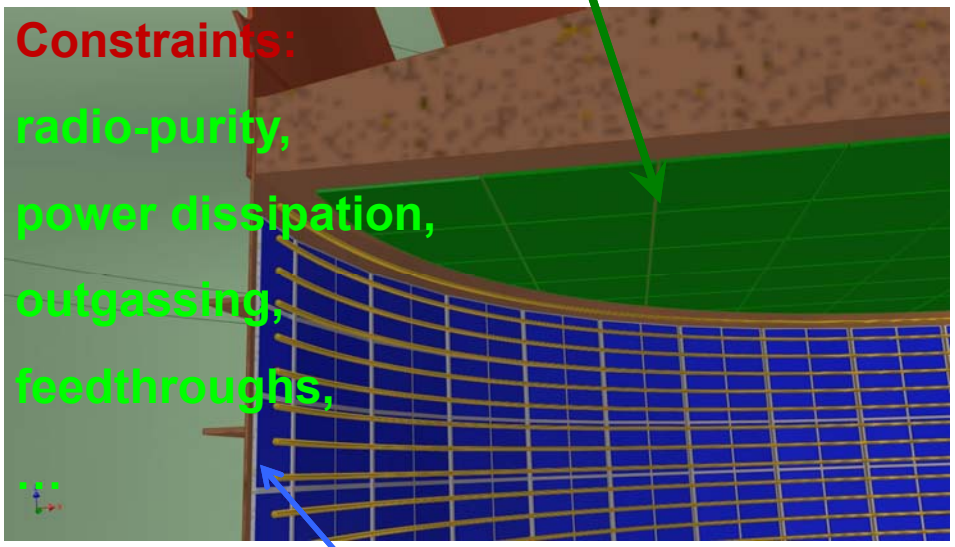
nEXO Detector

- ~ 5 tonne LXe TPC, 4.7 tonnes of active ^{enr}Xe (90% or higher)
- < 1.0% (σ/E) energy resolution

nEXO TPC Conceptual Design (artist's view)



Charge Readout Tiles + ASIC

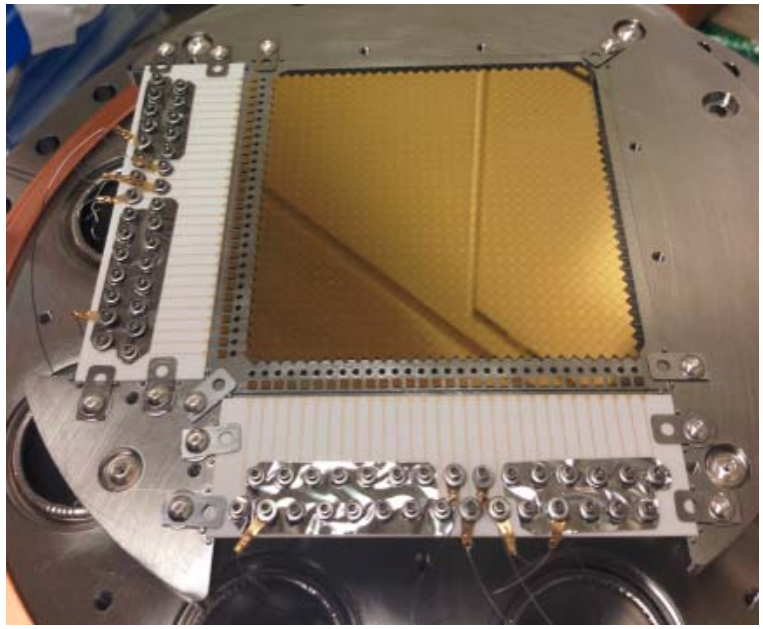


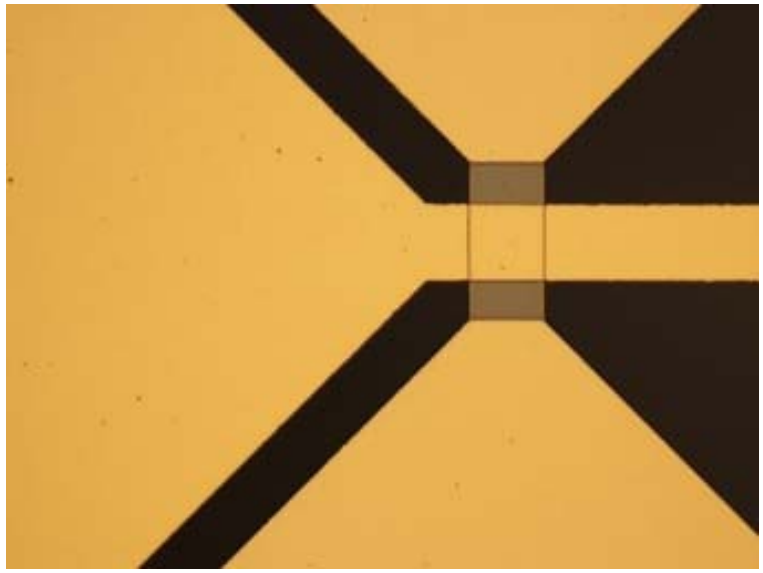
Silicon Photomultipliers (SiPMs) + ASIC

Baseline concept (Improved TPC design):

- Single drift volume
- Charge collection on the anode plane
- Light collection on the barrel behind field shaping rings

Charge Readout tile for nEXO





- Electrons are incident upon the strip (tile) plate (bottom)
- Each row and column of charge collection pixel is connected to a pad in one of the two rows of output pads

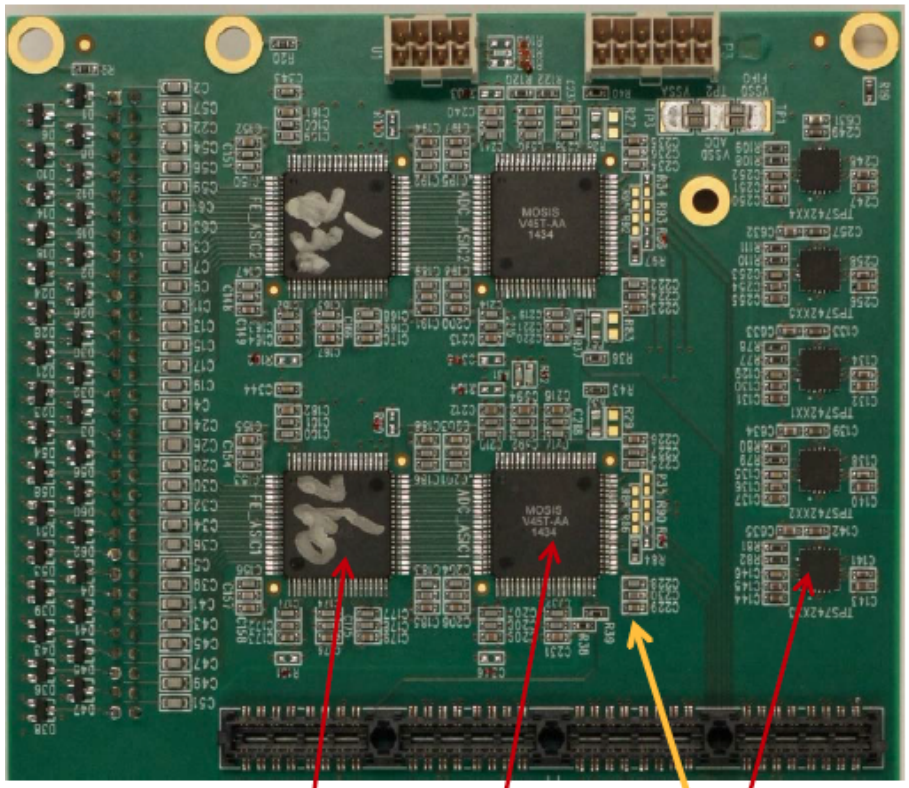
- The prototype of the tile includes 30+30 (x+y) channels
  - A tile needs two ASICs
  - Output capacitance ~20pF/ch
  - ➔ENC<200e-@20pF
  - Event rate<1Hz

Motivation for *Cold* Electronics

- **Energy resolution**
  - Need to minimize noise for charge readout channels, and achieve single photon sensitivity for the light readout
  - EXO-200 has achieved ~1.2% energy resolution at the Q value
  - nEXO will reach resolution <1%,sufficient to suppress background from 2vββ
- **Signal multiplexing**
  - nEXO detector will have thousands of charge and light readout channels. Sending signals from individual channels out will be unfeasible
  - Multiplexing can also reduce overall radioactivity

Adapting *LAr ASIC* readout for nEXO (BNL)

½ of LAR TPC FE board (=64 channels)



Details given by Shanshan

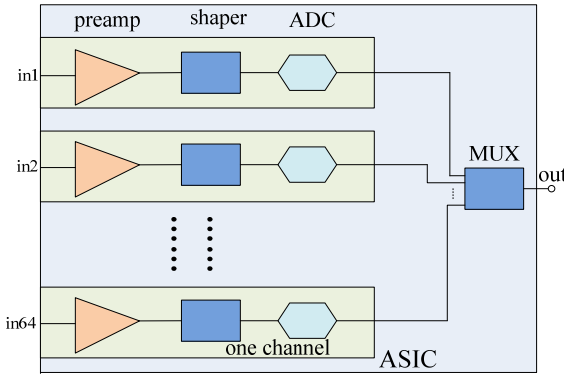
- BNL has developed ASICs for LAr detectors, similar concepts can be applied to nEXO
- The design have be optimized for LXe
- Biggest challenge is to further reduce the radioactivity in the front-end design and noise
- The plan is to develop a 64-channel board (4 front-end ASICs and 4 ADC ASICs), appropriate for a~10x10 cm² tile.
- Progressive approach:
  - Reduce board layers and use Si-Caps
  - Low background PCB and bare ASIC
  - Integrate preamp and ADC ASICs and increase channel number to 32

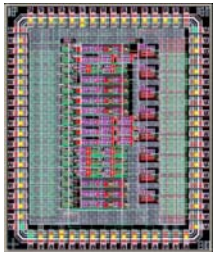
Cold ASICs for Charge readout(IHEP)

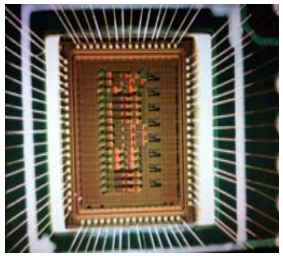
- On-going R&D at IHEP
- Critical spec.: <200 e-/ch
- Two schemes:
  - Digital multiplexing→
    - Individual ASICs designs done (pre-Amp, ADC)
    - Integration need be done
    - Tested with tile
  - Analog multiplexing→
    - Based on analog sampling technique
    - v2 has been tested

(integrated with charge tile)

Cold

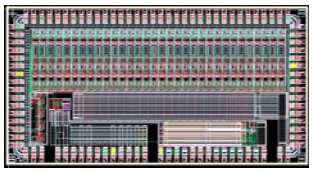


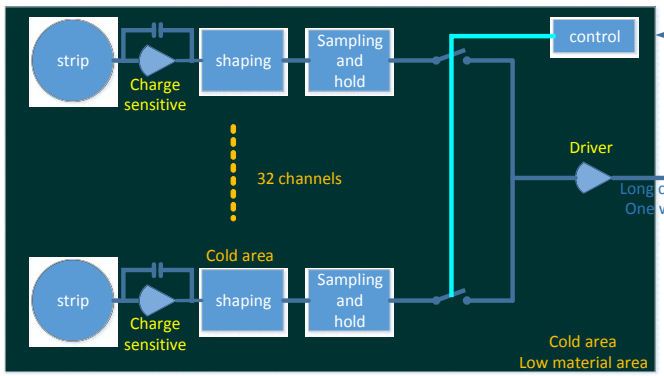


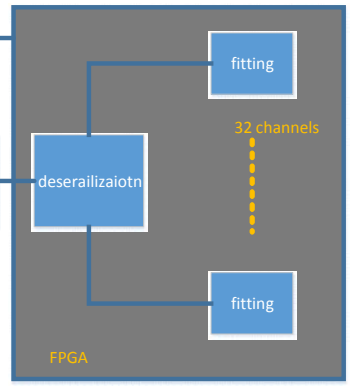


Warm

- Two chips have already designed and tested
- Need more tests (ADC's cold, noise, etc.)
- Need to be merged







Cold

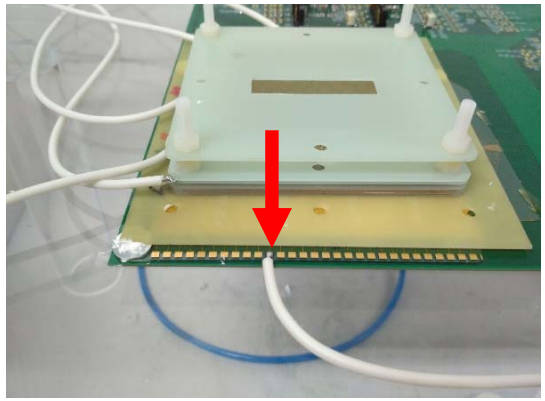
Warm

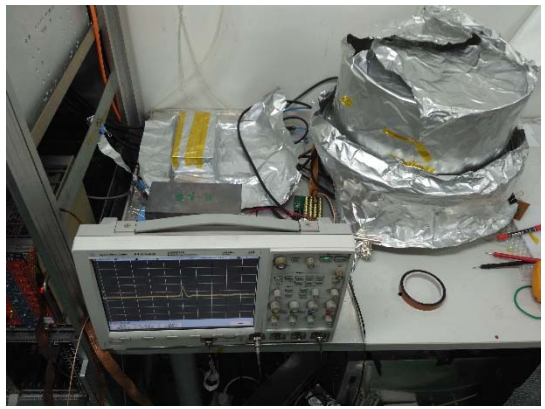
Digital multiplexing vs. Analog multiplexing

- **Advantage**
  - All digital processing
  - Simple system
- **Challenges**
  - More power
  - Analog & digital crosstalk
  - Too much data processing on chip
  - High-speed serial data transmission, may be a challenge

- **Advantage**
  - No ADCs
    - make chip's architecture as simple as possible, also the DAQ
    - Low crosstalk between analog and digital
  - Share one buffer on chip and one ADC external, power reduced greatly
  - Off chip ADC could be high sampling frequency to improve SNR
  - Minimize number of cables between cold and warm (2clk+2power+1output)
- **Challenges**
  - Shielding(P+G) become important
  - Noise performance a little worse

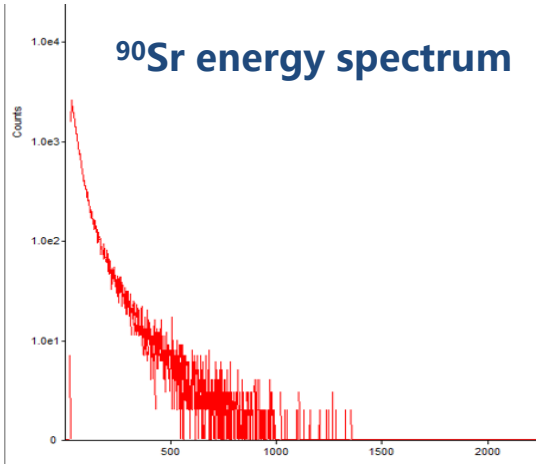
Measurement results(IHEP)

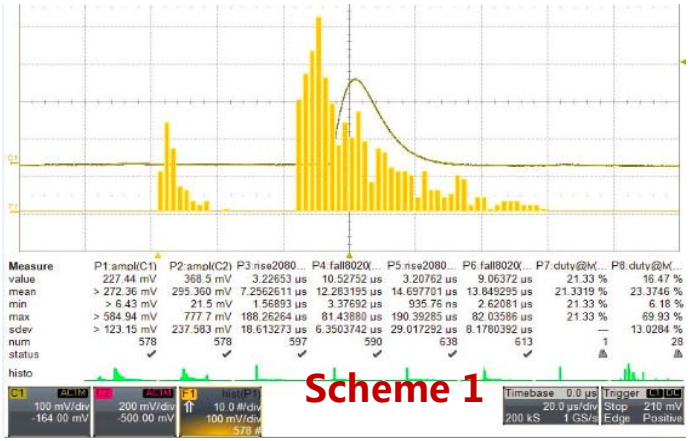




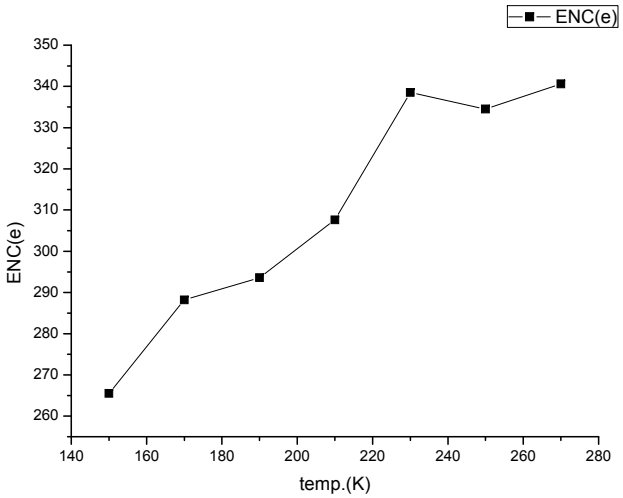
Specification	Value	Note
VDD	AVDD=1.8/DVDD=3.3	Analog power/Digital power
Peaking time	2μs /4μs	Tune switch to change
Sampling frequency	<132M	2M sampling rate/channel
ENC	~265e-	@160K
INL	<0.4%	@160K
Input signal rate	>1kHz	High rate performance
Linear range	-64fC~-0.32fC	Negative polarity
Power dissipation	<3mA@1.8V/channel	NOT include output buffer

- Radioactive Source: ^{90}Sr
- The energy spectrum fit well with ^{90}Sr's spectrum





Scheme 1

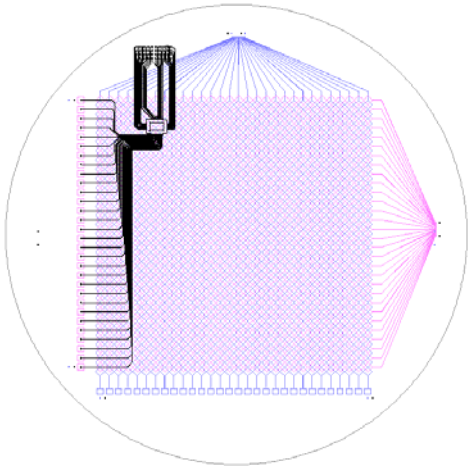


ENC decreases as T goes down

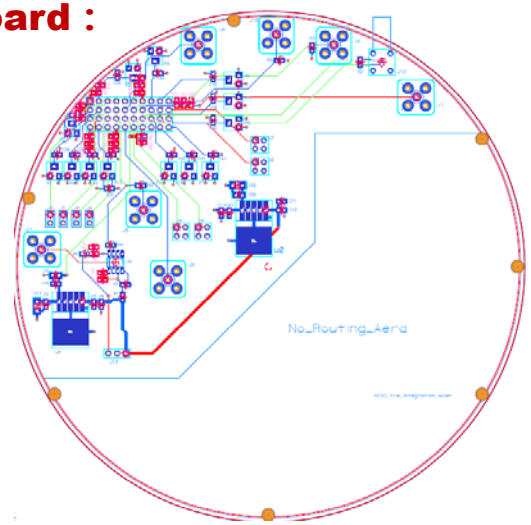
Scheme 2

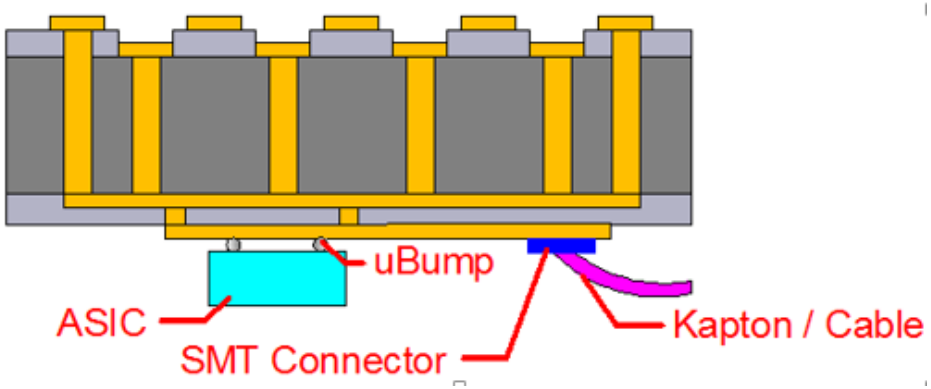
Pre-integration Test

mask :



board :





- A 3-D tile for multiplexing version
- ASIC is not final version, the chip's pins are not fixed
- The route is for wire bonding and functionality test. Not too much consideration for noise, crosstalk and other performances
- The bump-bonding option is still on the table

Some Charge Readout Design Considerations

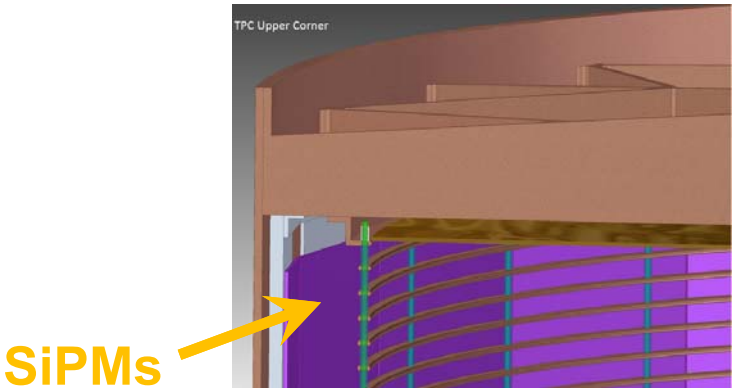
- Reading induced current can preserve the largest amount of waveform information
- Analog multiplexing can reduce the data clock speed, but need to demonstrate high analog signal transfer fidelity
- Buffered readout of trigger events only would have data rates an order of magnitude lower than continuous readout.
- Data rates (power dissipation, cable volume) out of cryostat: inversely proportional to readout tile size for a given strip pitch.

nEXO SiPM Readout Development

Challenge: How to deal with large sensor capacitance?

Need low noise (< 0.1 p.e.) and fast readout

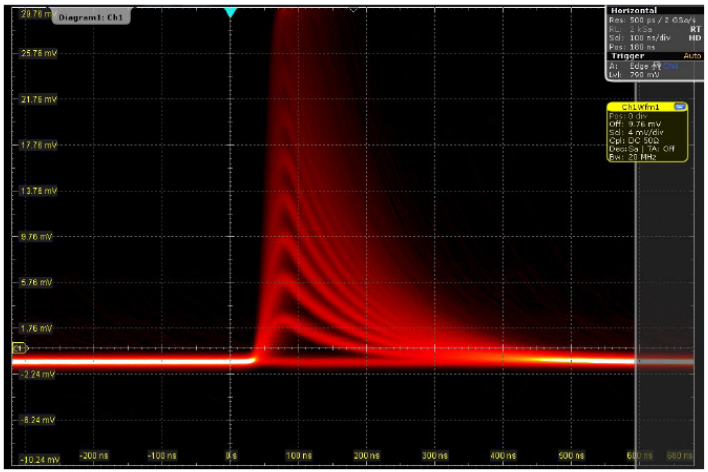
- **Very large area, up to 4 m^2**
- **Large capacitance, 3-9 nF/cm^2**

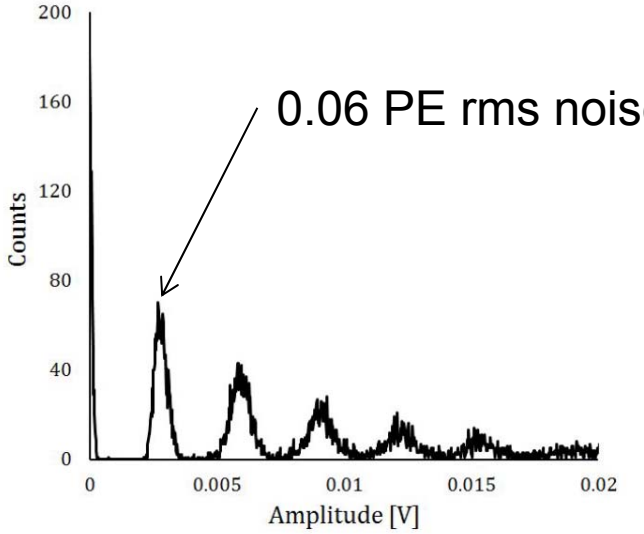


- **Demonstrate front-end readout for a single channel using discrete components (IU, ORNL)**
- **Analog SiPM ASIC readout system design (BNL)**
- **3D-SiPM readout (TRIUMF, Sherbrooke)**

SiPM Preamp Testing (ORNL, IU)

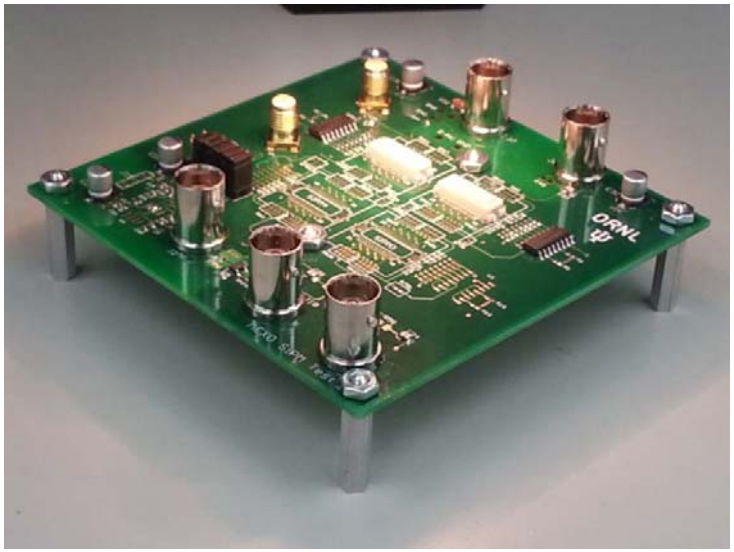
- Measurements supporting BNL's initial estimate of max area and Lorenzo's noise formula's:



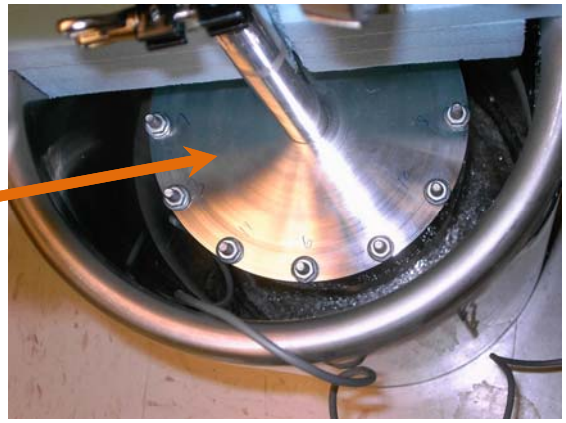


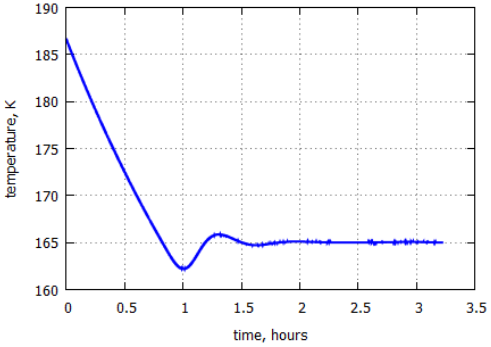
- SensL array SM-4 at LXe ~1.5 cm^2 active SiPM area at 90 pF/mm^2. Power is 20 W in FE circuits or 0.5 mW/cm^2.

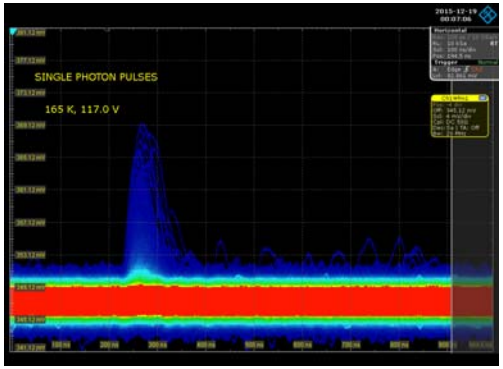
- Formulas would set 0.1 PE limit at 1.7 cm^2 when scaled, in agreement with this measurement.

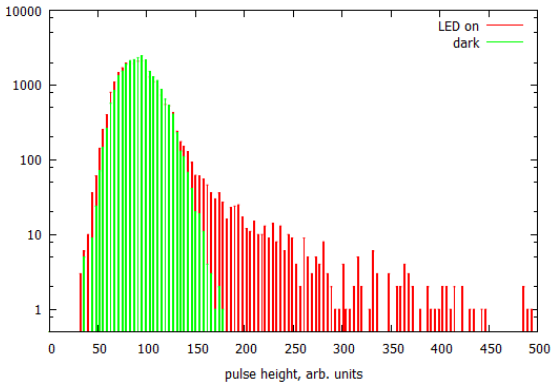


IU cold box, SiPM series test



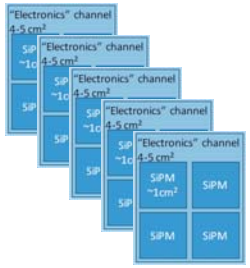




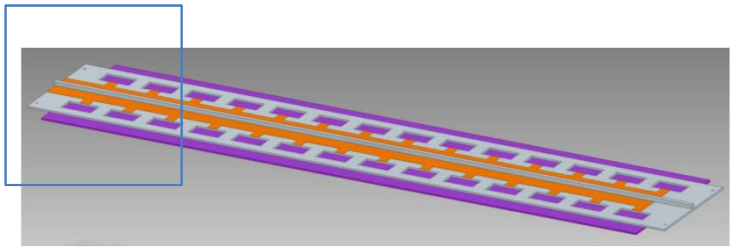


- **Cold box & SiPM/readout test setup completed**
  - **Excellent temperature stability; operation in vacuum or with LN boiloff purge**
  - **Blue LED with external pulse input, can make a few ns pulse width**
  - **ORNL/IU test board modified for external VCC & improved test output buffer; tested w/ current pulse w/o SiPM @ 165 K (and down to 150 K) – performance is excellent *with raised VCC***
- **Simple series connection of 2 MEG devices**
  - **Negative result so far for single-PE peak, but investigation will continue (one known blunder + *possible series connection gain stability issue?*)**

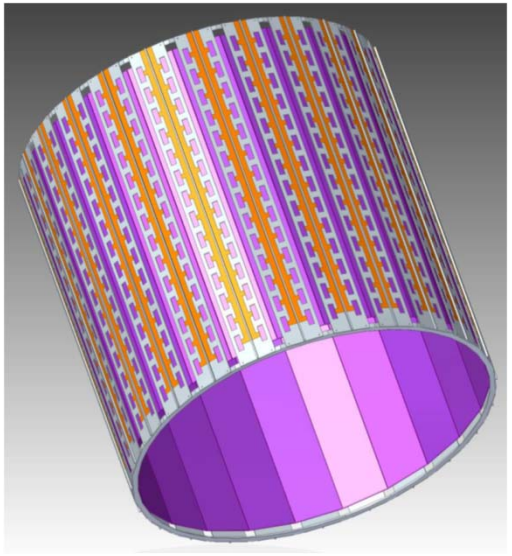
From single channels to large tiles



SiPM module



SiPM Ladder



Barrel (e.g, 24 ladders)

- In the next few months, they should be able to demonstrate a single channel readout.
- Perform an intermediate demonstration with 10 x 10 cm^2 tile?
- For analog SiPMs, approximately 20~30 channels, about the size for an ASIC based readout, also the size of proposed Si interposer.

Summary on nEXO electronic R&D

- **Demonstrate a complete readout chain for a charge readout tile. (not the final low background design)**
  - **First prototype testing has done**
  - **Integration with the tile will occur soon after(1st edition done)**
- **Prototype demonstration of an individual SiPM readout channel**
- **Develop overall Light readout concepts**
  - **Further investigation of the readout schemes**
- **Identify and test low background components for final low background constructions**
  - **Tested *Si Caps*, *cable* and *PCB* testing underway**

THANK YOU!

Electronic R&D Goals

- **Demonstrate a complete readout chain for a charge readout tile. (not the final low background design)**
- **Prototype demonstration of an individual SiPM readout channel. Develop overall readout concepts.**
- **Identify and test low background components for final low background constructions.**

Currently parallel paths are being pursued for both the charge and light readout in the R&D period.

Optimizing the design is tightly coupled to detector simulation, data analysis, radio-purity budget, etc.