Asian Module for ILD-TPC

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dP/P ~10^-5 P

10 times better resolution than that of LEP TPC





Possible solution of ILD Tracker

	posi. reso	# meas. point
Si pixel VTX	<i>δ</i> ∼5um	6
Inner Si strip	δ~20um	6
TPC main tracker	δ∼100um	220
(Si main tracker	<i>δ</i> ∼20um	5)

Momentum resolution



MS term limits # of Si layer

-> σ/\sqrt{n} is same for TPC and Si tracker (if B,L are same)





Gaseous tracker

TPC : continuous tracking = many sampling of moderate precision good tracking efficiency

degenerate Higssino case: only low Pt π/μ tracks





Si tracker

small sampling but with high precision tracking efficiency ?? good for high Pt track but not sure for low Pt track

Requirements to TPC

momentum resolution local resolution : 100um over full drift volume no distortion (E-field, B-field) B-filed: anti-DID recon. under non-uniform B-field E-field: geometrical/engineering beam related ion problem

detection efficiency

stable operation of gas amplification good 2track separation good efficiency even in high BKG

less material structure RO electronics/cooling

The way to achieve local resolution 100um

$$\sigma_{\kappa} = \delta\left(\frac{1}{P_T}\right) = \frac{\sigma_x}{0.3BL^2}\sqrt{\frac{720}{n+4}}$$

High B field 3.5 T Long lever arm 1.8 m Many hits 200 layers

good position resolution 100 um

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principle of gas detector
property of gas
principle of position measurement
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How TPC determine tracks



- 1.) Ionization by dE/dx number of electrons
- 2.) Drift of electrons motion in E,B field Lorentz force diffusion
- 3.) Gas amplification MPGD readout pad/electronics



Position information is smeared by diffusion

Position is determined by COG of charge dist. Charge distribution must be broader than RO pad.



Gas property Ar:CF4:i-C4H10 high wt

3.5T case

CD ~ 25 um@1cm drift at drift region 350 um at amp. region

> less diffusion@drift Position information is smeared by diffusion

modest diffusion@amp. COG of charge dist. Charge distribution must be broader than RO pad.

Position accuracy of single electron



Interpretation



[A] Purely geometric term (S-shape systematics from finite pad pitch): rapidly disappears as Z increases

[B] Diffusion, gas gain fluctuation & finite pad pitch term: scales as 1/N_{eff}, for delta-fun like PRF asymptotically:

 $\sigma_{\bar{x}}^2 \simeq \frac{1}{N_{eff}} \left(\frac{w^2}{12} + C_d^2 z \right)$ [C] Electronic noise term:

Z-independent, scales as $\langle 1/N^2 \rangle$

Alternative solution

Micromegas :

diff@amp. region is only 10~20 um In order to avoid hode-scope effect micromegas choose resistive anode pad



Timepix w/ micromegas : narrow pad size 55um × 55um hode-scope effect is small enough count each electron not cluster



MWPC :

cannot provide good resolution at high B field

Ion problem

Production of Ions is inevitable in gas detector.

dense ions in drift volume may deteriorate drifting electron.

Primary ions : produced by generated charged tracks



ions from gas amplification(backdrift ions) : ions (dense) discs are formed due to slow drift velocity MPGD owns inherent ability of ion absorption

Beam Structure @ ILC



s a natural ability of is, but it's not perfect.

"GATE" ing GRID



train produce back-drift ions' disk without "Gate mechanism" for ions as big difference of drift velocity between electron and ion drift velocity of ion is 10000 times slower

1st train produce prim. ion pairs in all drift volume electron drift to MPGD(endplate) and amplification produce more ions

next train produce prim. ion pairs again before ions are swept out amp. ions by 1 train form thin disc and drift slowly

Effect of ion (disc)

Primary ions are inevitable no way to recover but ions are spread over all volume effect to position measurement is acceptable O(10 um)

Ions produced by amplification form dense ion disc which deteriorate position accuracy ~60 um

not negligible to 100 um resolution

We need Ion Gate device

ILC beam structure is good for gating gate is open for 1ms collision gate is closed for 199ms between collisions



Gating for back-drift ions



R&D of GEM type Gate

F.Sauli proposed a GEM as Gating device operated at very low voltage at 2006



Realization of GEM Gate is not easy as we thought at the beginning due to the limited electron transmission at gate-open. especially for high B field !

We realized a necessity of R&D to make a large aparture GEM in order to increase electron transmission.

Ordinal chemical etching process can build a 50% aparture GEM some challenging company can make a larger aparture but not sure

FUJIKURA investigate process and QC system enable to produce GEM with more than 80% aparture using laser aviation for insulator removal at 2014

Gate GEM new vs old

New aparture 80% gate GEM

Old aparture 50% gate GEM



Electron transmission

10cmx10cm prototype(type 3) provides more than 80% transmission even for B = 1T field



module size gate will be tested under LP1 facility using beam on Nov.2016

R&D of LCTPC

EndPlate and Field cage Infrastructure of module test (LP1)

module R&D Asian module, DESY module, Micromegas module Timepix module

readout electronics/cooling

Distortions

Endplate



handling/replace --> middle size module low material : aluminum --> space frame

maximize sensitive area

-> install method, module boundary

LP1 endplate -> will be @ LP2?(1.5)



Field Cage DESY



Double layer Kapton strips are laminated on honeycomb cylinder

LP1 beam-test facility @DESY T24 beam line

facility to test various modules under the same environments

up to 5GeV/c electron

PCMAG(KEK) provide 1T B field on movable stage cryo system updated LP1 field cage fit in the magnet

Si tracker was planed to be installed _{phi(turn table)} in the magnet for precise reference point

x(slide bar)

y(hight)







Concept of Asian module

Minimize insensitive regions (module boundary, GEM frame) pointing IP no side frame



Bunch of tiny connectors (40 pins) 161 connectors

all other space for HV supply

+ Back Frame



28 pad raws (176/192 pads/raw) ~1.2(w) × 5.4(h) mm² staggered every each layer

Total 5,152 ch/module



Double GEM (100um thick) for simpler structure

GEM electrode is divided in the middle of ${\sf R}$

Gate GEM is assumed above GEM structure



local resolution as a function of drift distance





Extrapolation to the ILD-TPC



The expect performance satisfied with the

In order to achieve 100um res. all over the drift volume, we have to have more diff.@amp region or narrower pad

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Difficulties of module R&D

typical local resolution is as good as we expected

How can we extend this performance to all over the module

quality of components (GEM, gate, connector..)
mechanical/engineering (GEM /Gate stretching.....
design
procedure of study



14um Gate GEM



-> E field is distorted @ boundary



Field Shaper





Lesson

R&D study should be done in step by step: module design must be cooperated with this procedure Saving money may not save your R&D Much room is better than no room but is not proper

GEM sheet







segmentation 2
 -> observe frequent trip
gap 300um
 -> gap was too short
 one segment trip -> discharge@gap

segmentation 4

- -> improve? but many discharge
- gap 1mm
 - -> HV OK but
 - -> this gap provide another distortion

no segmentation@front/ 4 segments@back -> distortion became smaller gap 500um



GEM discharge study

Why our LCP 100um thick GEM discharge frequently ? even at reducing GEM segment area

Micro discharge is counted during long term GEM operation for 50um(CERN,Raytech, Scienergy) and 100um(Scienergy) GEM (standard 10cmx10cm size)

no clear difference was observed

RIKEN group has studied gain stability of LCP GEM and found 100% variation even in the same GEM due to thickness of insulator (LCP) LCP: uniformity of thickness is O(10%) in specification (Kapton/polyimde sheet is much better than this)

Quality control of GEM

Next step to realize real TPC

finalize module design GEM structure, Gate structure, Pad plane readout electronics the final RO electronics is postponed until ILC go sign

integration of real electronics and cooling

related to Pad plane design

Study is on going with intermediate RO electronics(s-Altro16)

Integration of PCB+RO electronics @LP1

Present front end electronics modified Alice TPC electronics

Front End Card Backplane Pad plane SALTRO16 MCM Multi Chip Module 16 ch ALTRO PCA16 Kapton cable PAD plane

reduction of size/material



All functions are integrated into one chip: sAltro16 analog-digital mixed

> sAltro16 -> sAltro64 extension prog. terminated

But we have many sAltro16 for integration test





Front End Electronics Architecture

MD,



Slide by Leif Joensson

integration of cooling system

Electronics can be small but power consumption remain same ! Cooling is another important issue





Cooling scheme is studied by Takahiro

simulation using TPG as heat conductor non-negligible temp. gradient w/o power cycling heat flow through connector

Mockup study is on going



toward the final module design



Summary

GEM Gate seems to be working (watch the result of next beam test)

We convinced Asian module has a potential to reach to LPTPC goal 100um resolution intrinsic performance of each components look OK.

But to achieve ILC requirements over the module/TPC improvement of engineering/design/QC are necessary design to minimize E distortion