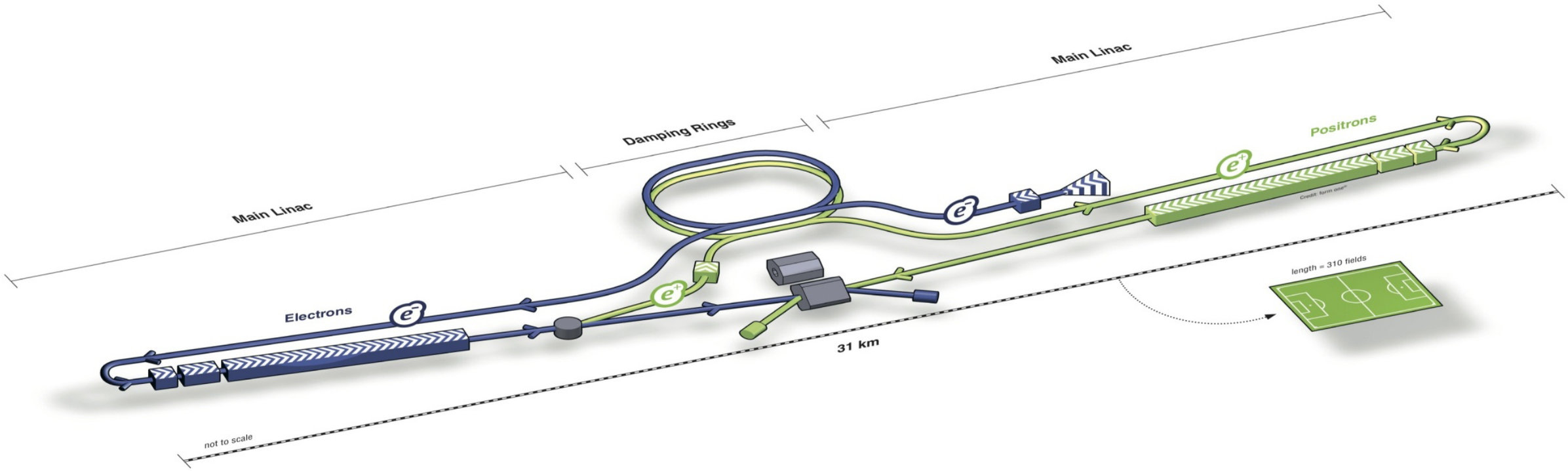
SOI pixel detector for the ILC experiment

Mini workshop on SOIPIX at IHEP 2016/7/14

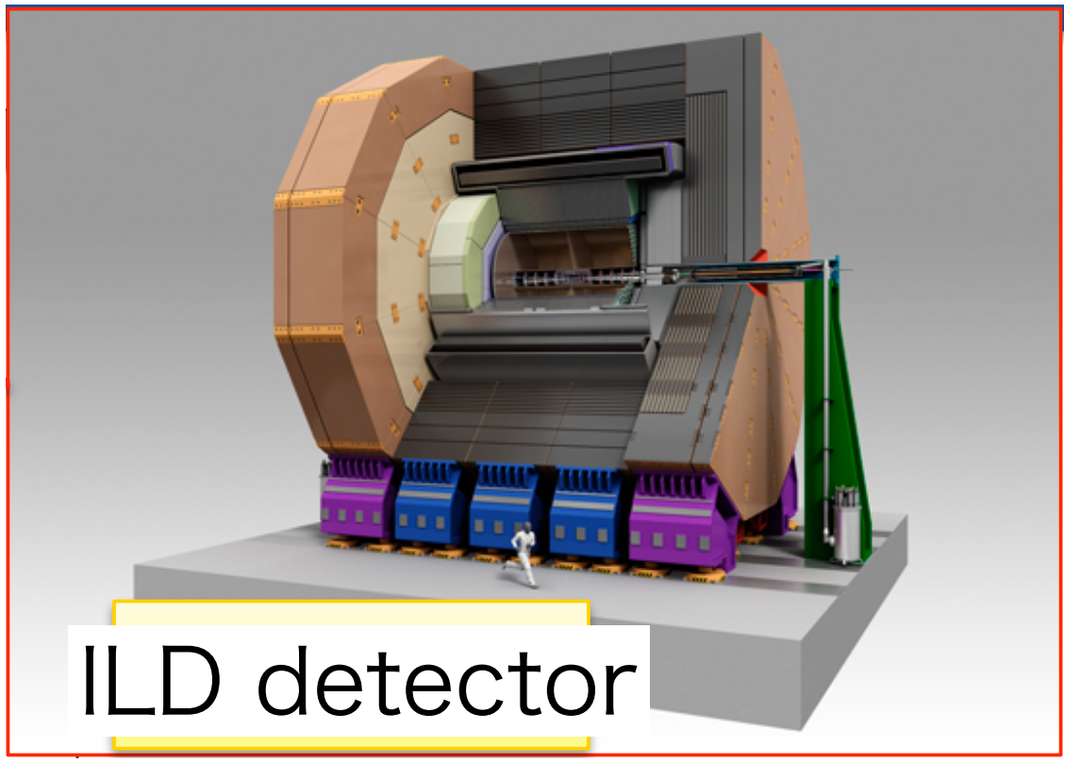
Osaka University Manabu Togawa

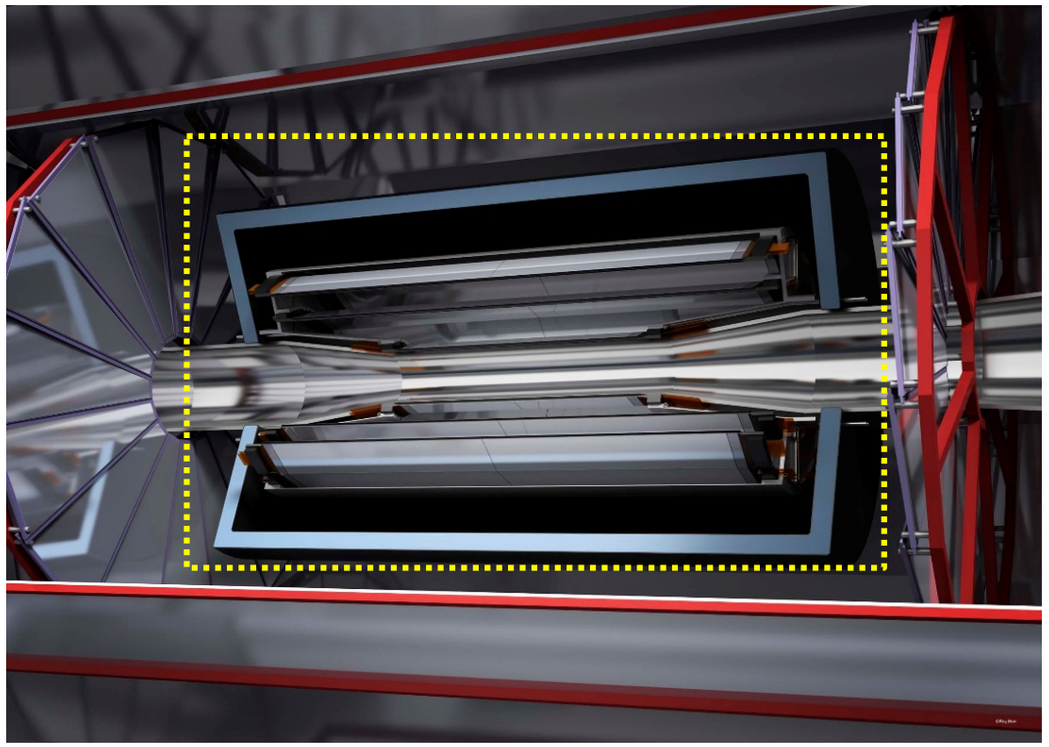
ILC experiment



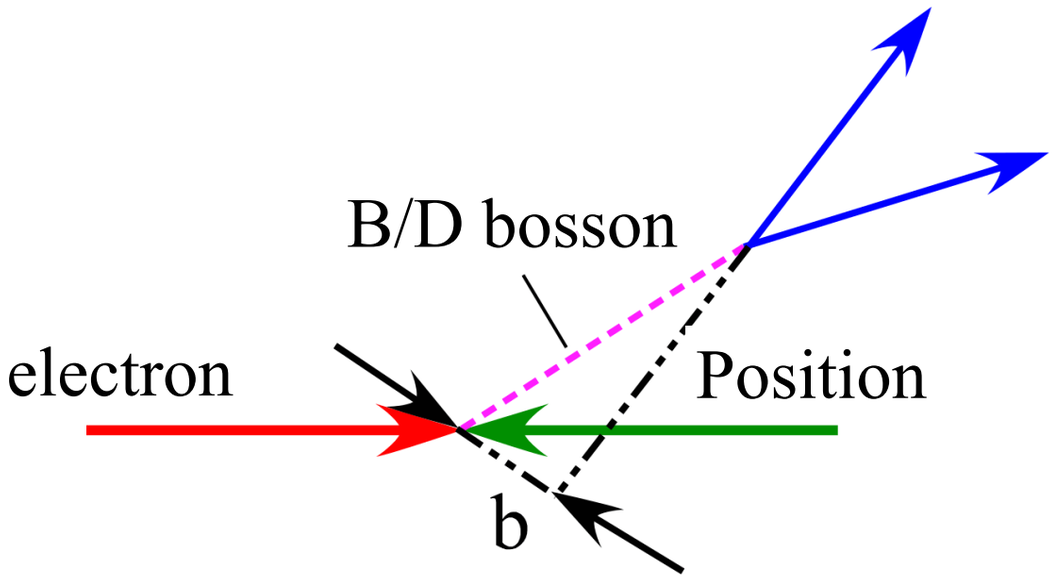
- e+ e- collider of $\sqrt{s}$ = 250 - 500 GeV
  - Precise measurement of Higgs particle
  - Discovery of new particles
    - SUSY, dark matter…

ILC vertex detector



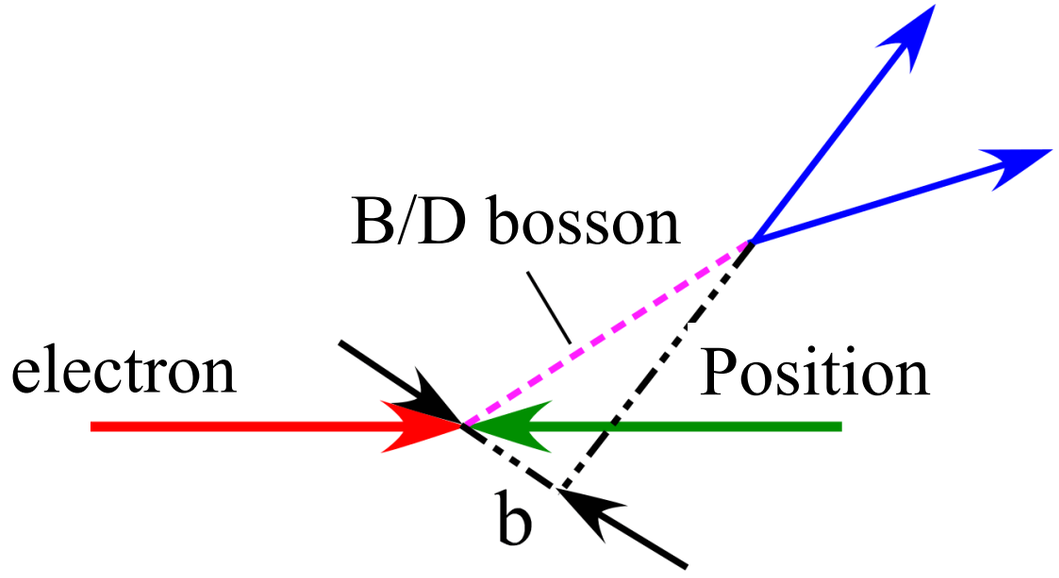


- Si pixel sensor locates around the IP point to measure the tracking of charged particles precisely.



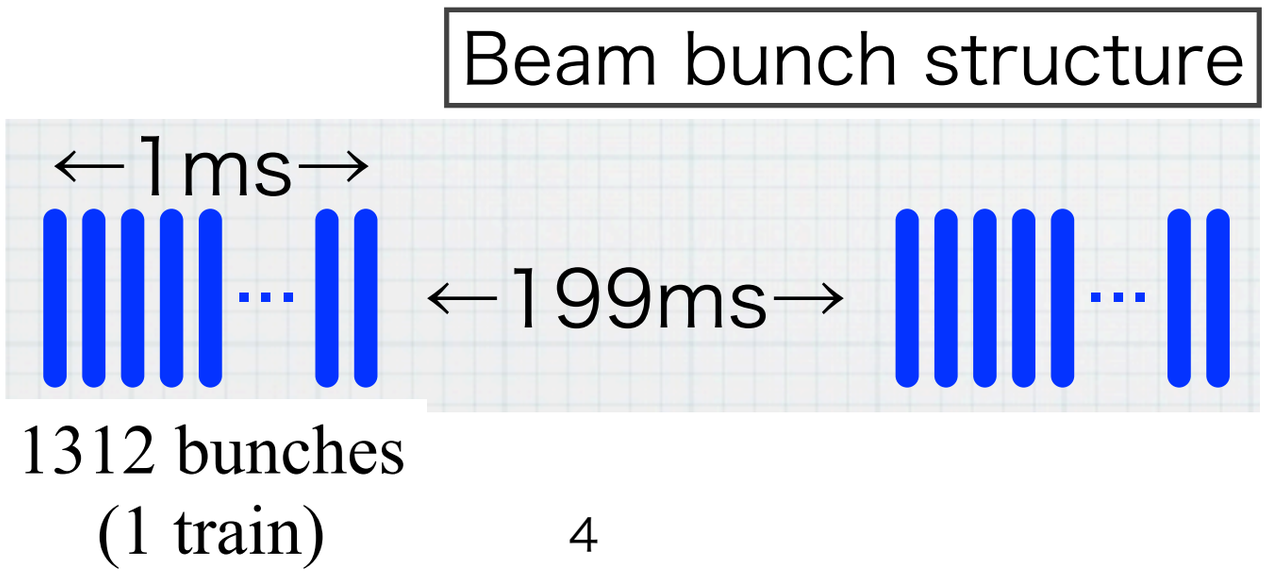
$$\sigma_{ip} = 5\mu m \oplus 10\mu m / p \sin^{3/2}\theta$$

Requirements for ILC physics and operation



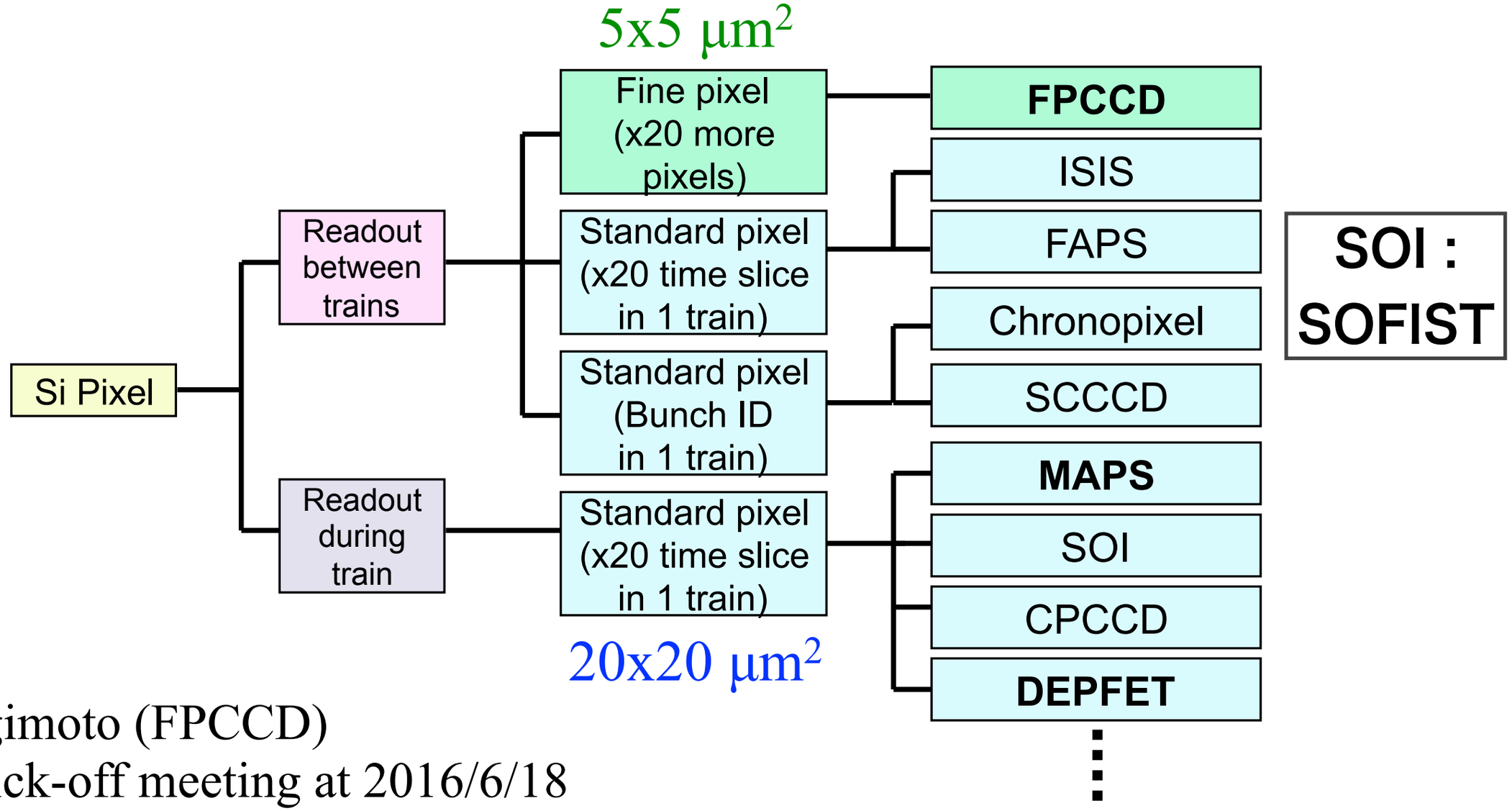
$$\sigma_{ip} = 5\mu m \oplus 10\mu m / p \sin^{3/2}\theta$$

- 1) Vertex resolution
  - Position resolution : < 3 μm
  - Low material : < 0.1% X_0 (< 100 μm thickness for silicon)
- 2) Integration during beam train
  - Detector occupancy : < 2 %

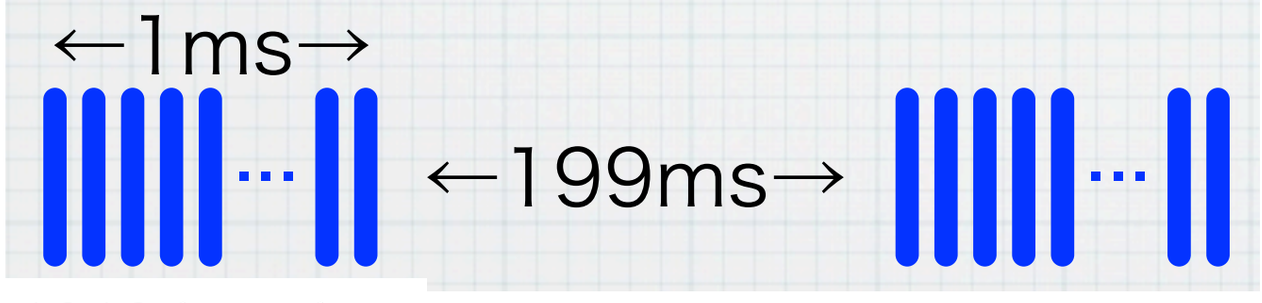


Candidates

* Hybrid type is disaster in terms of cost and amount of material



Y. Sugimoto (FPCCD)
ILC kick-off meeting at 2016/6/18



1312 bunches
(1 train)

Requirement of readout ; Occupancy < 2%

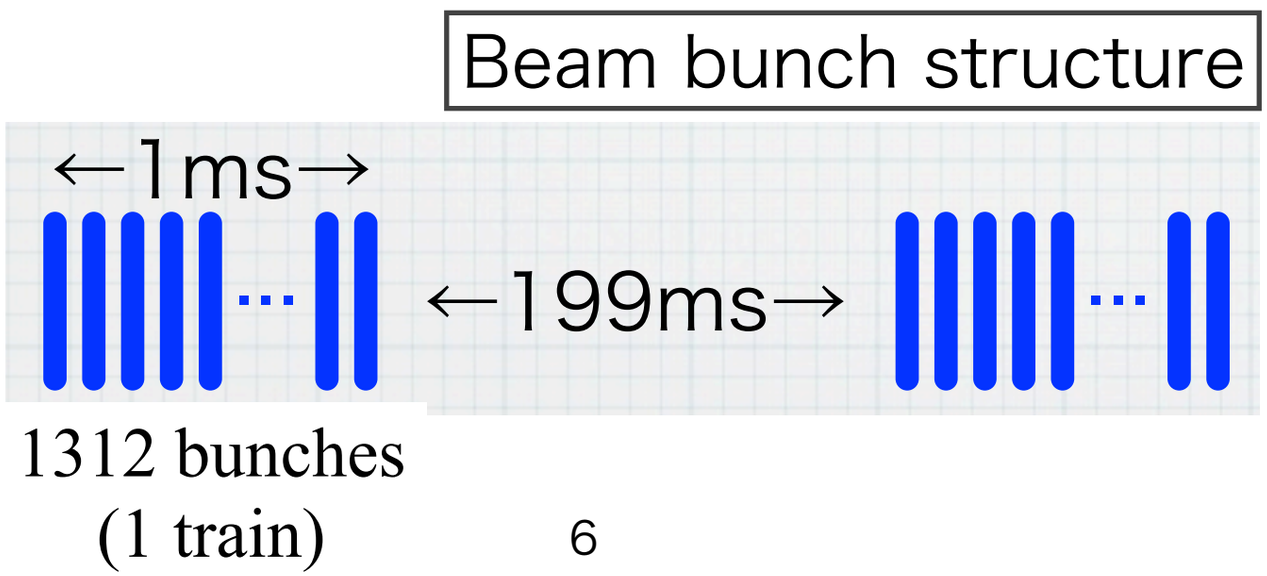
Occupancy estimation on 1 train at 500 GeV for FPCCD (5x5 μm^2)

Layer	Occupancy (%)
0	1.24
1	0.78
2	0.12
3	0.10

Scale to std. pixel (20 x 20 μm^2)

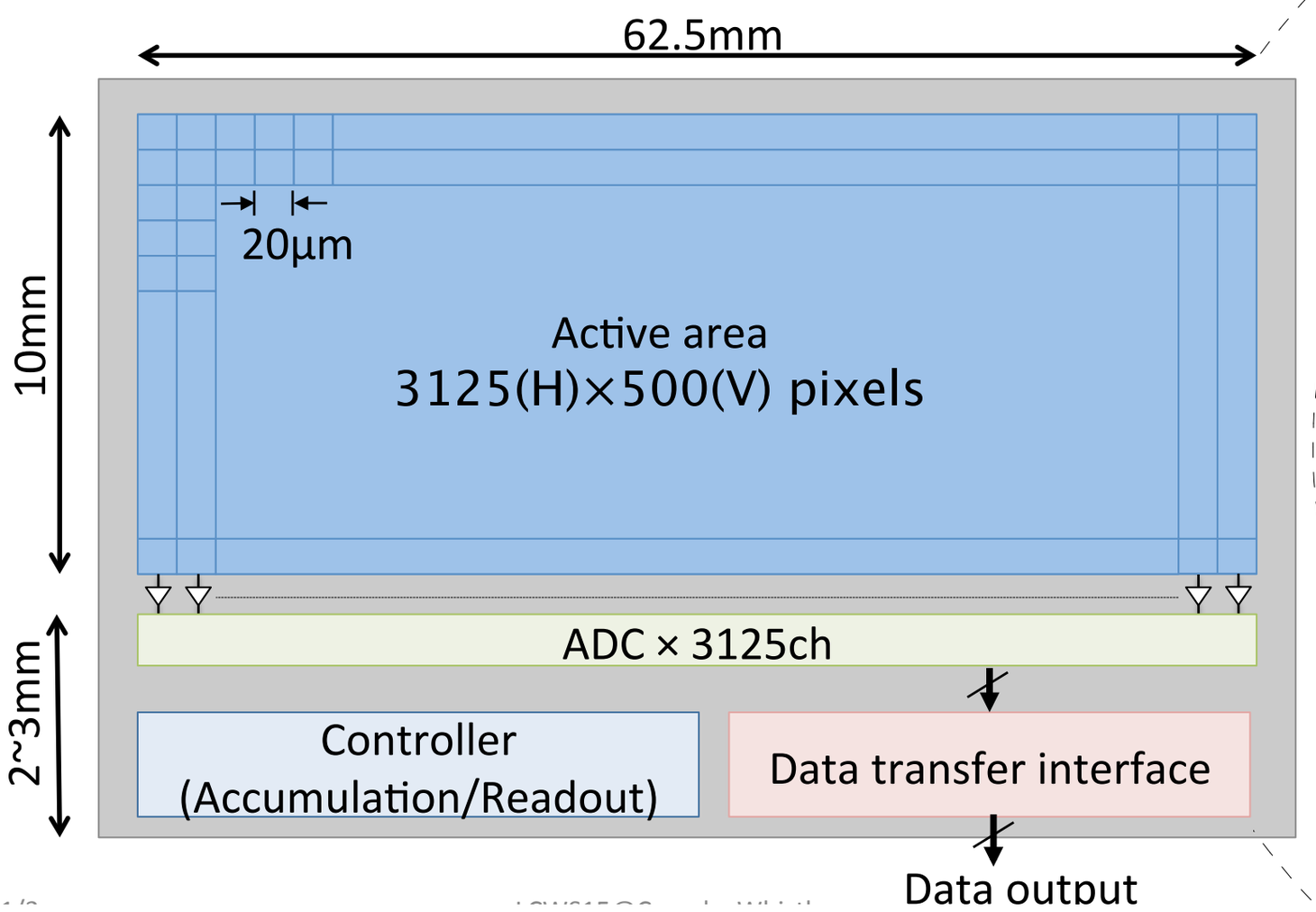
~ 20 % (x16)

Need to have
multiple readout during train or bunch identification

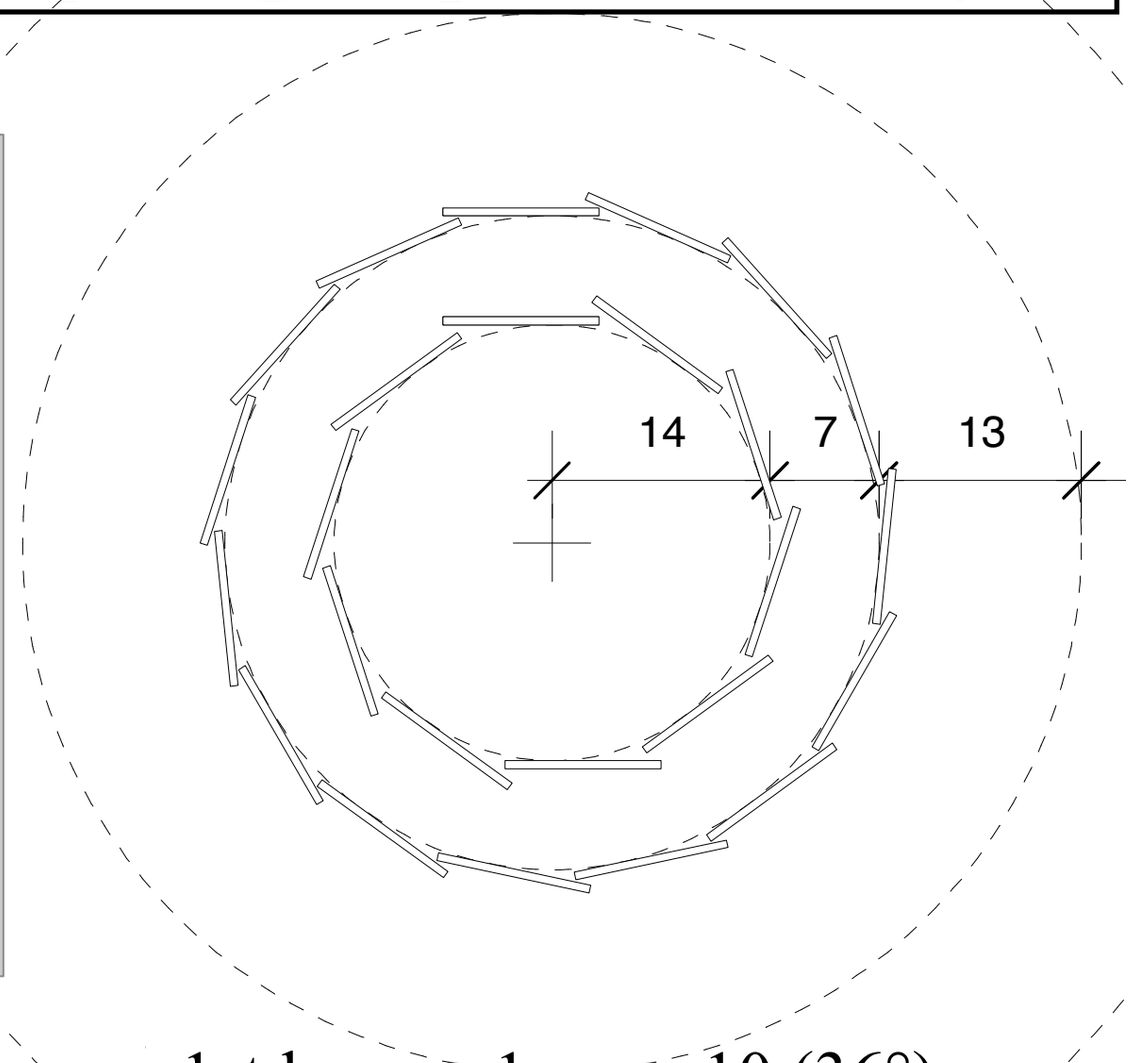


SOFIST
(SOI sensor for FIne measurements of Space and Time)

Final design



Proposing shape for inner layers

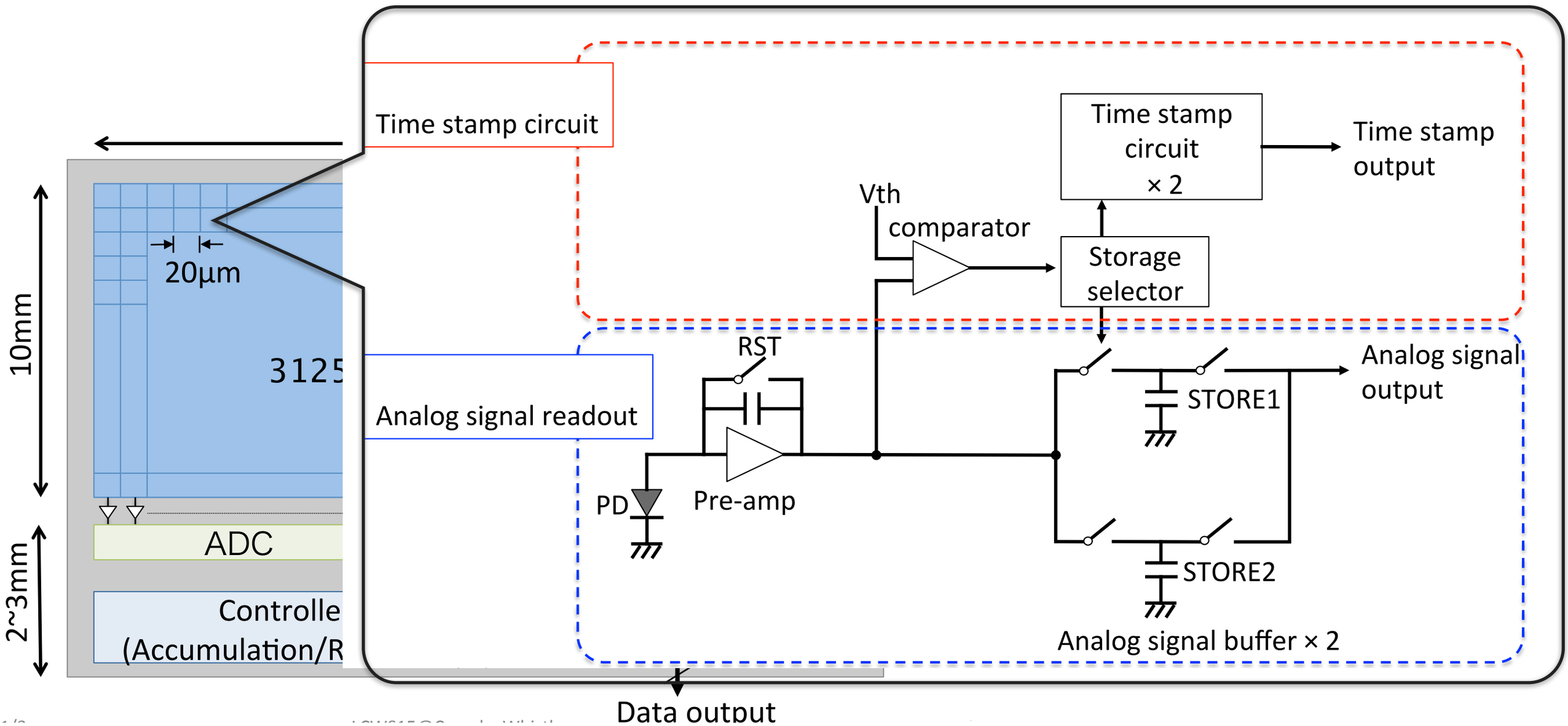


1st layer : 1 cm x 10 (36°)
2nd layer : 1 cm x 15 (24°)

Pixel size = 20 x 20 μm^2
Thickness = 50 μm

SOFIST

Circuit on 1 pixel (in design)



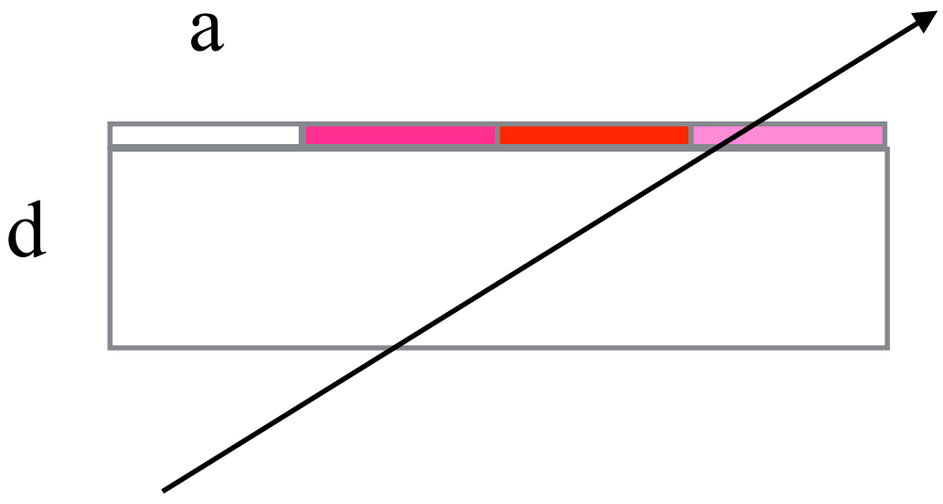
The number of buffers should be decided in terms of the occupancy

SOFIST

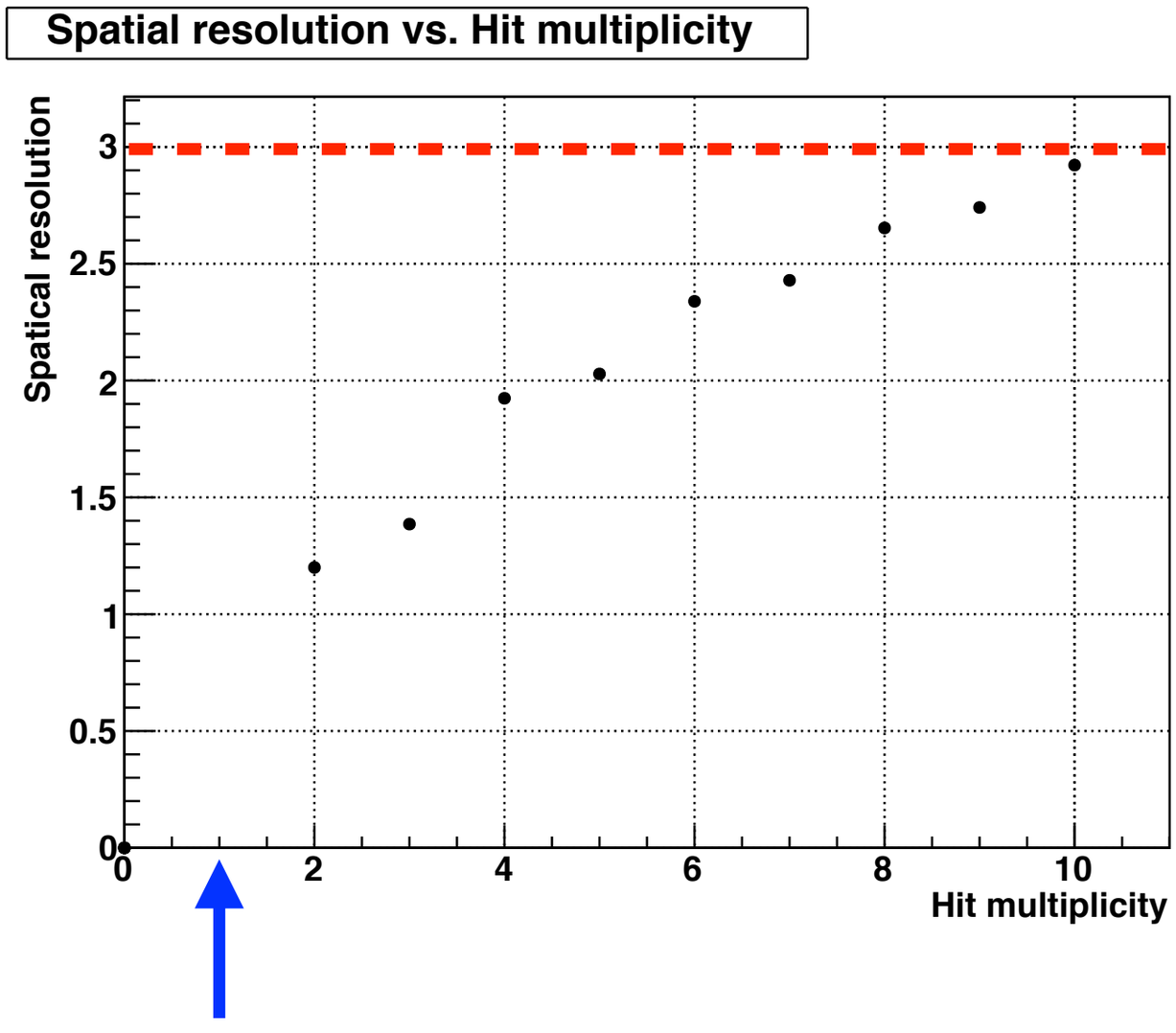
Position resolution (estimation)

- In case of 2 hits : $\delta x = N * a / S$
  - S/N = 17 is assuming.

Position is calculated by centroid-method.



a : pixel pitch = 20 um
d : thickness = 50 um
S : Total charge
N : Noise in 1 pixel
M : Hit multiplicity of pixels

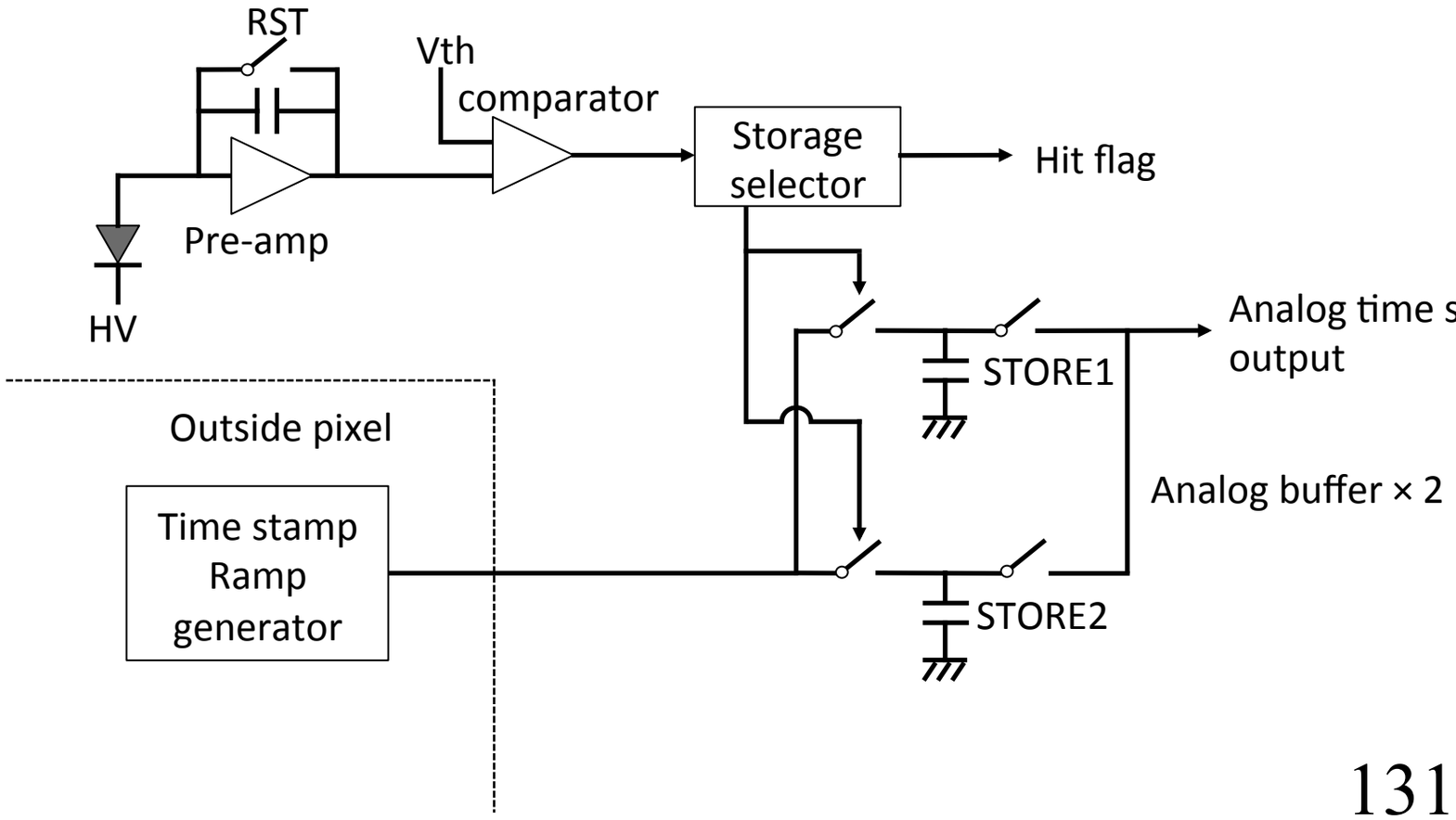


Resolution = 20/sqrt(12) ~ 5.8 μm in case of M = 1…

SOFIST

Timestamp

- 2 ways
  - Keep digitize information on pixel circuit.
  - Keep charge from ramp generator.



→ ADC

ADC can be shared w/ signal charge buffer.

1312 bunches / 256 (= 8 bits) bunch resolution in principle.

SOFIST

Summary of design

Description	Spec.	Unit	Comment
Pixel size	20 x 20	μ	
Active area size	62.5(H) x 10 (V)	mm	
N of pixels	3125(H) x 500(V)	-	
Thickness	50	μm	1 MIP ~ 3700 e
Noise level	< 200	e	S/N < 17
Readout	ADC 8 bits	-	
Timestamp for bunch	8 bits		Using analog buffer

* Zero-suppression is definitely needed.

** Readout speed and Power consumption need to be considered.

SOFIST

Development plan

- v. 1 : Test for analog circuit
  - Pre-amp
  - x2 analog buffers

Production was done.
Now evaluating performance.

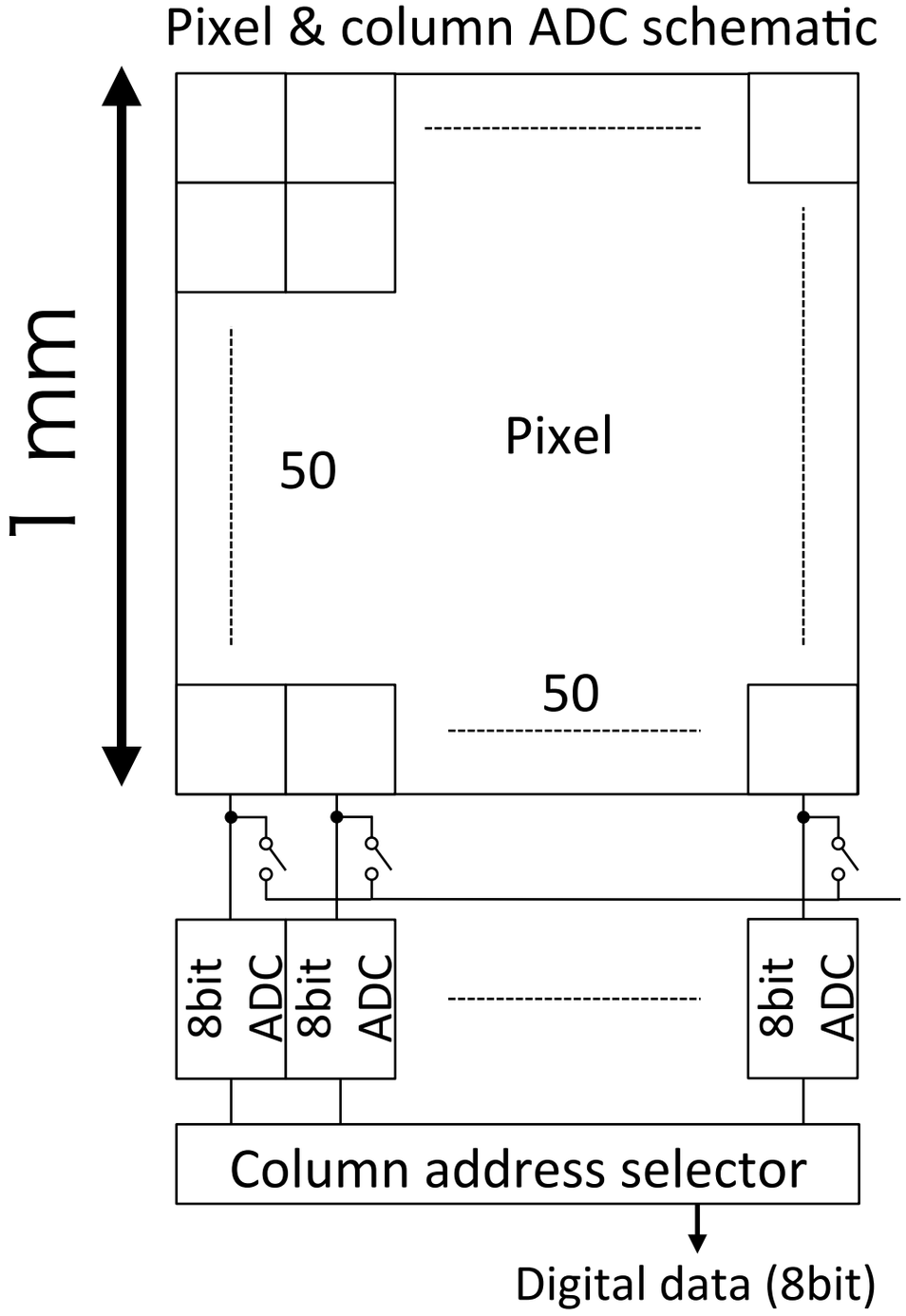
- v. 2 : Test for digital circuit
  - Time stamp circuit (x2 analog buffers)
  - Zero-suppression

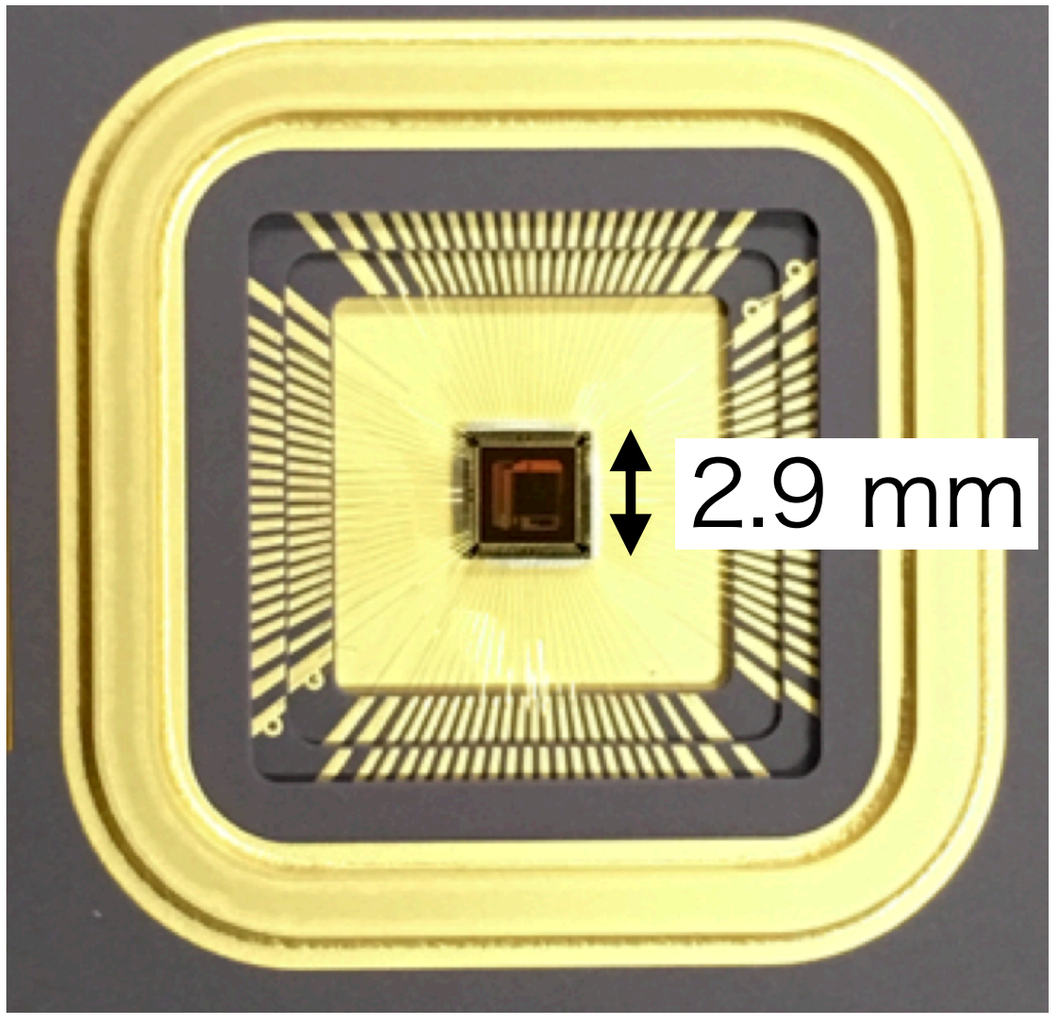
Design was done.
Submitted to production.

- v. 3 : Implementation both analog and digital circuits

- * Grown sensor size needs to be considered.
- ** Pixel size is too small to have buffers…

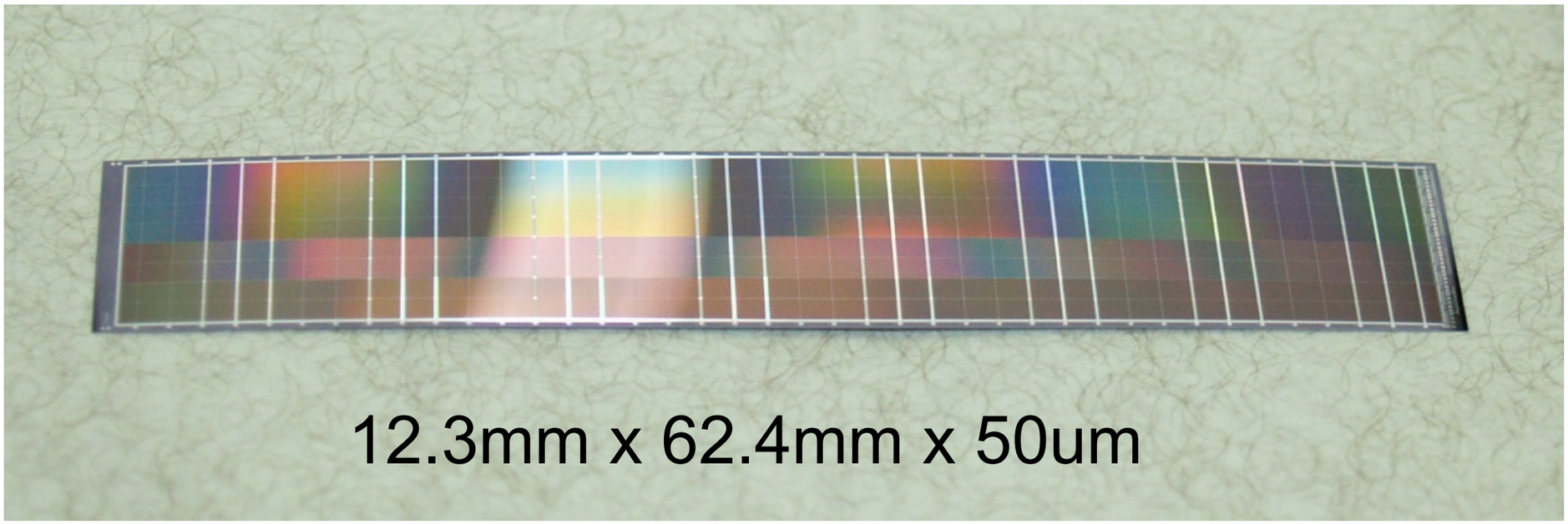
SOFIST v.1





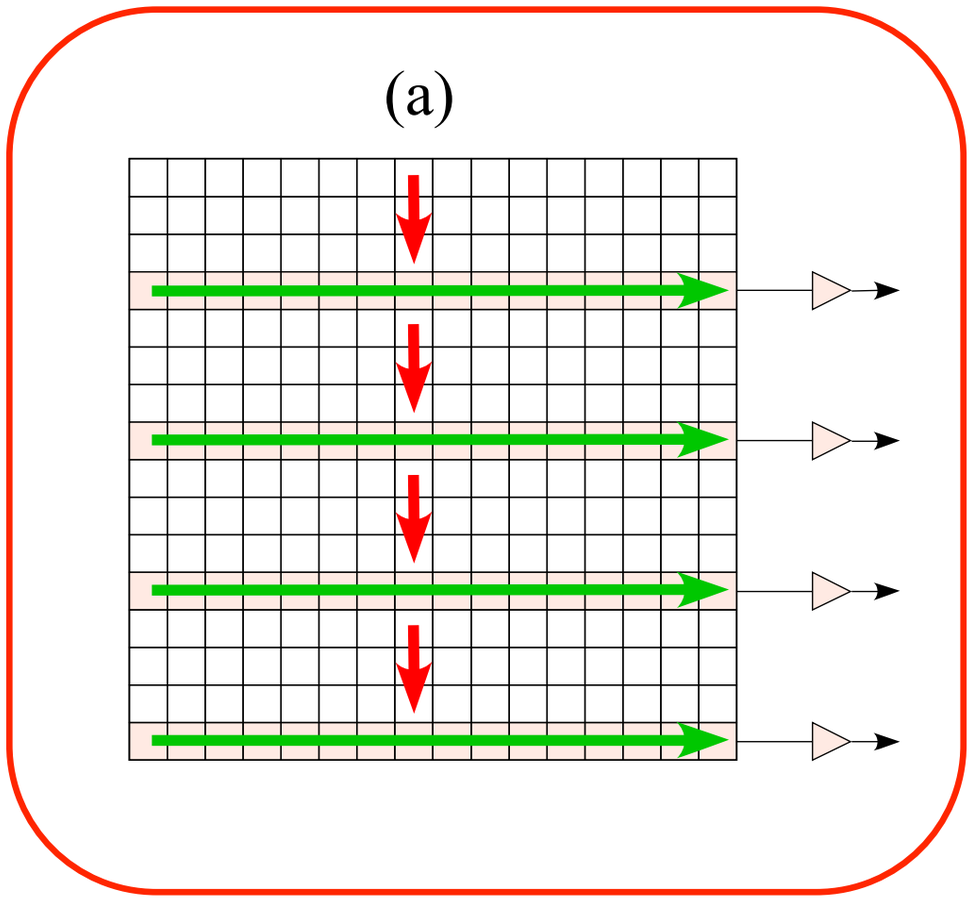
Details in S. Ono and M. Yamada talks in tomorrow

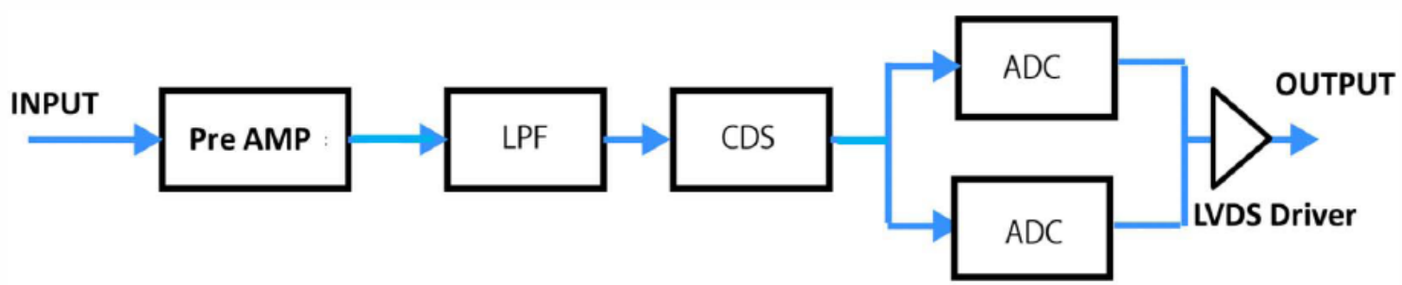
FPCCD
(Fine Pixel CCD)



- Pixel size : 5 x 5 μm^2
- Active area : ~15 μm thick epitaxial layer.
- Wafer thickness : 50 μm
- Total # of pixels : 10^{10} : needs 10 Mpix/s readout

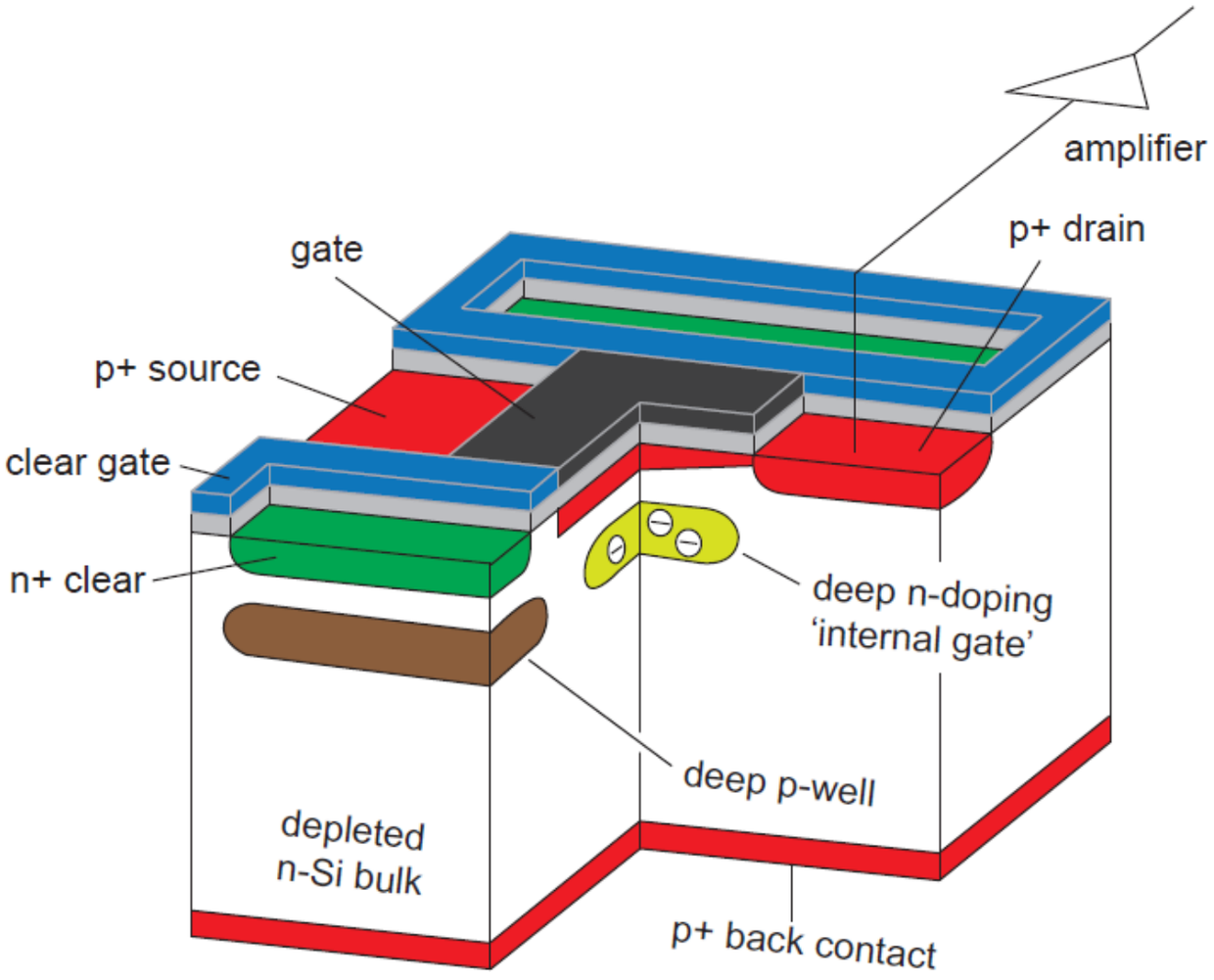
FPCCD readout





- Amplifier and ADC need to be prepared.
- Readout : 10 Mpix/s (currently achieved 2.5 Mpix/s)

DEPFET
(DEpleted P-channel FET)

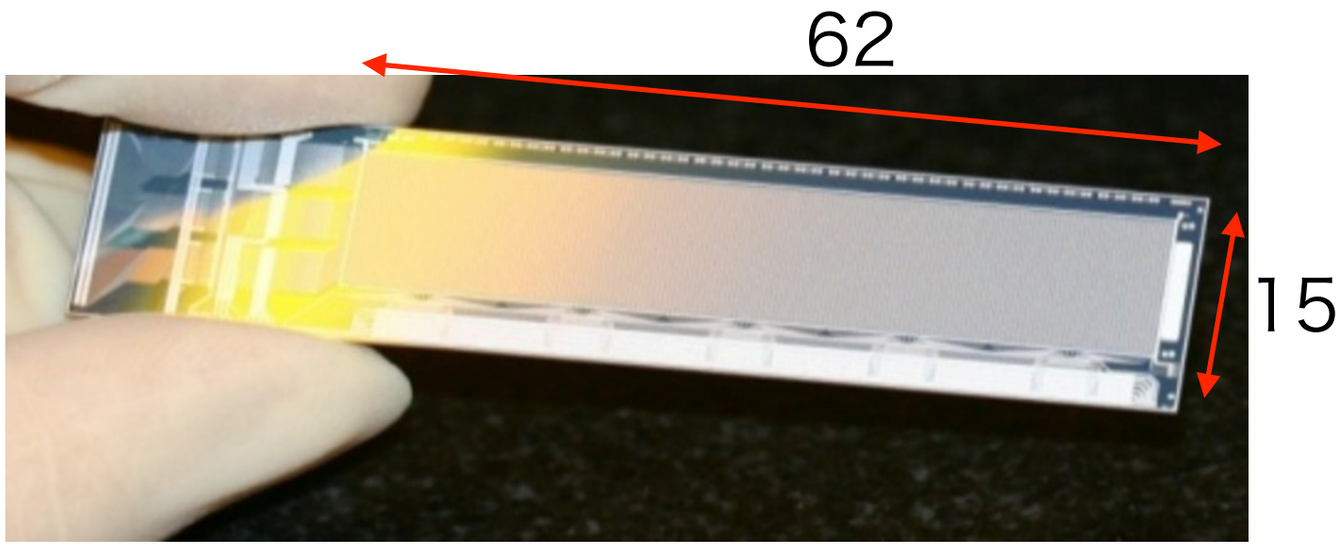


- Pixel size : 20 x 20 μm^2
- Fully depleted : ~50 μm.
- The charge stored in the internal gate.

- Will be installed at the Bell2 experiment

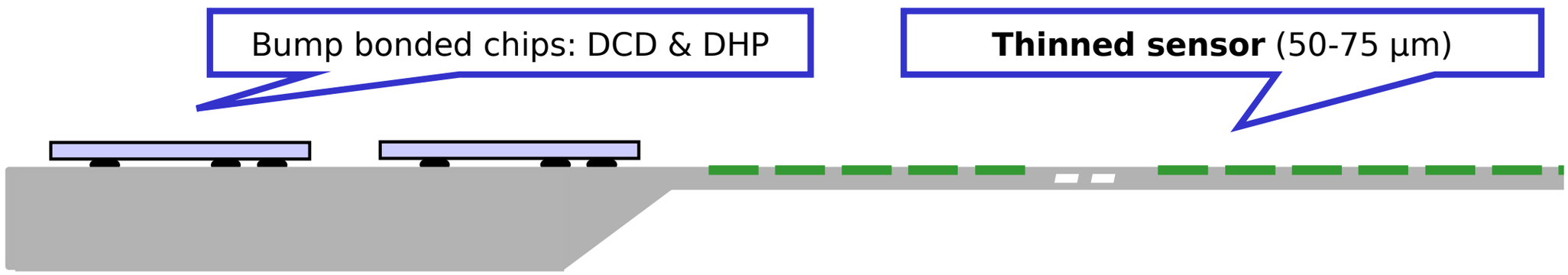
DEPFET

DEPFET spec.



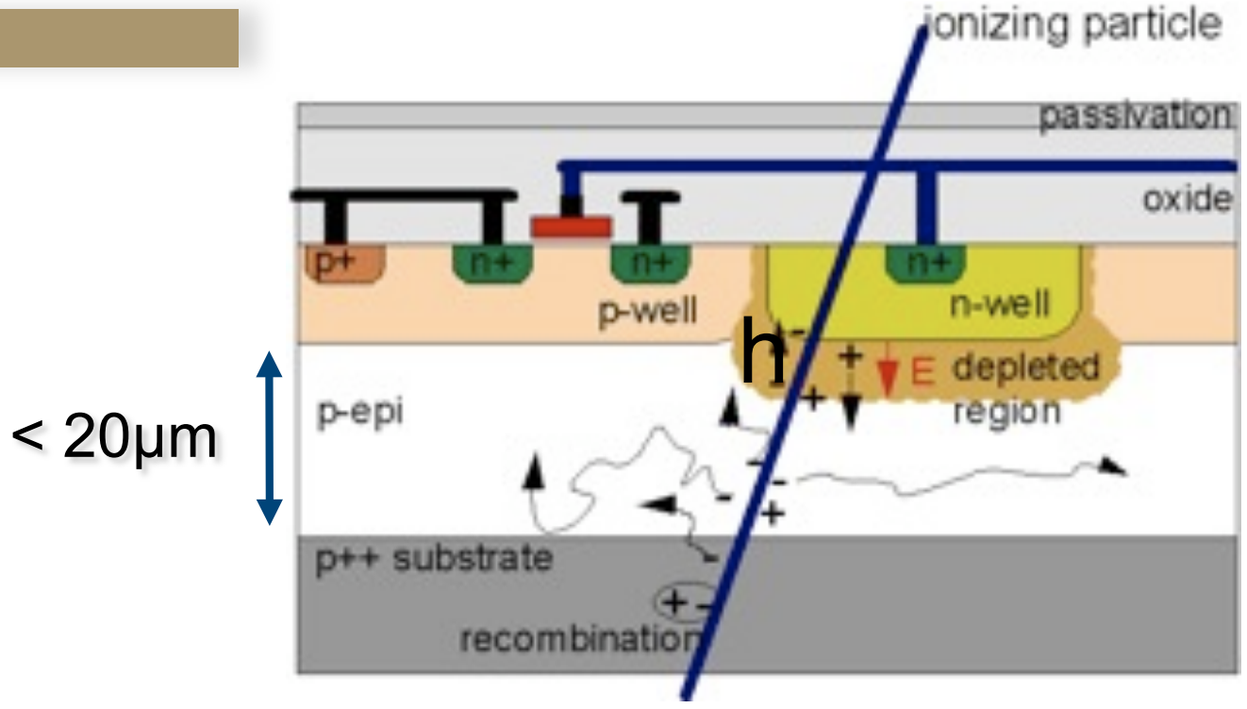
- Spatial resolution :
  - 2.3 - 3.5 μm
- Material budget :
  - 0.15 X_0 (including support frame)
- Frame rate :
  - 40 μs / frame w/ rolling shutter readout.
  - 25 times readout / train
- Micro-channel cooling

2 ASICS for digitizing and control



M. Vos (DEPFET)
LCW15

PLUME
(Pixelated Ladder with Ultra-low Material Enbeded)

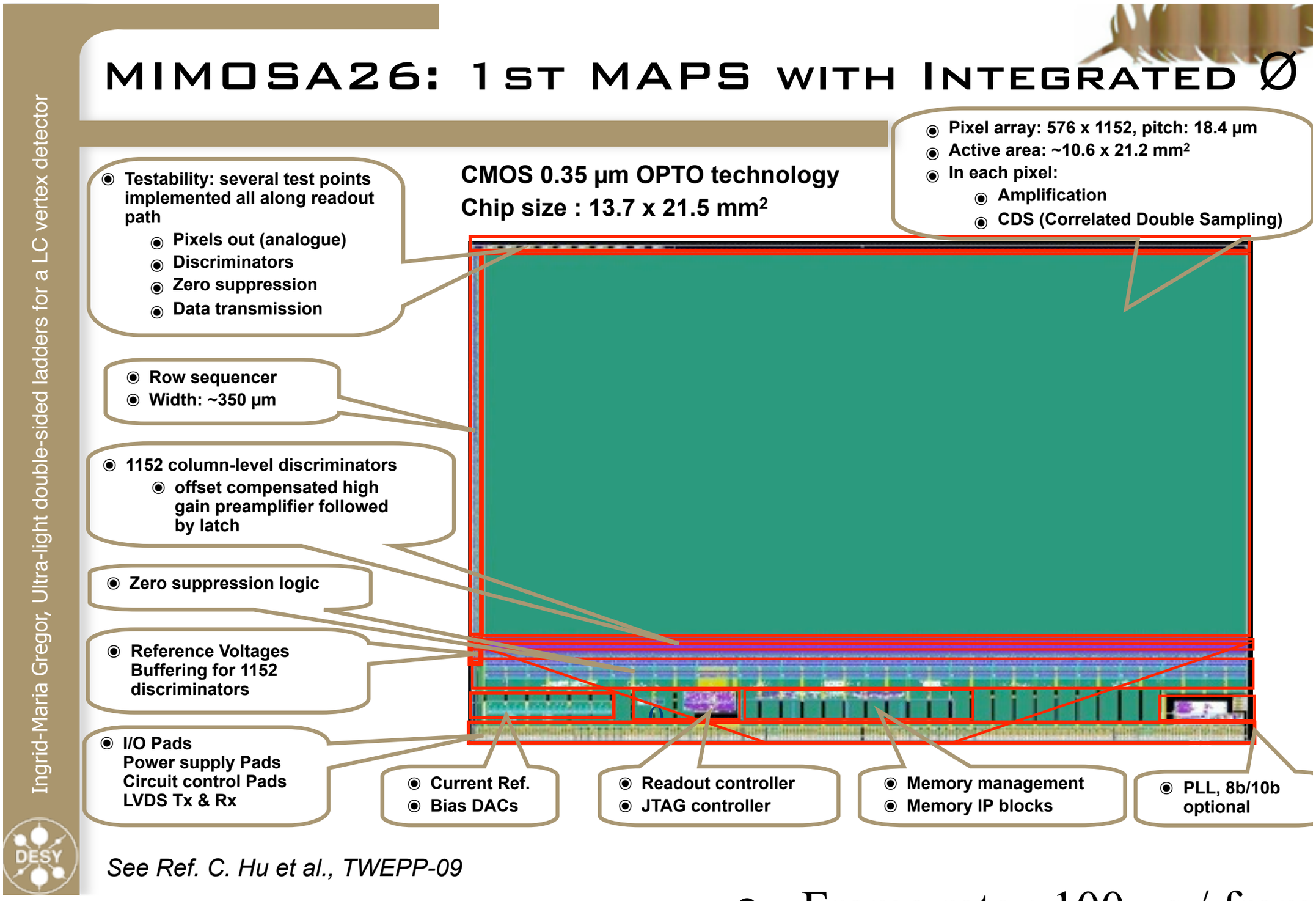


- Pixel size : 18.4 x 18.4 μm^2
- Active area is p-epitaxial layer < 20 um
- ASICS on chip
  - Based on MAPS (Monolithic Active Pixel Sensor)

- MAPS was installed and is operating at RHIC STAR experiment (2014)
  - https://www.google.co.jp/url?sa=t&rct=j&q=&esrc=s&source=web&cd=6&ved=0CEIQFjAF&url=https%3A%2F%2Findico.ific.uv.es%2Findico%2FmaterialDisplay.py%3FcontribId%3D666%26sessionId%3D29%26materialId%3Dslides%26confId%3D2025&ei=iOjiU7fRNIzl8AXm7oH4Dw&usg=AFQjCNENtD1w2gpNY5N9-zTP1QSo-LyYiA&sig2=XGv_eUsBycWJM-D-PgXHTA&bvm=bv.72676100,d.dGc
- Target to ALICE and ILC

PLUME

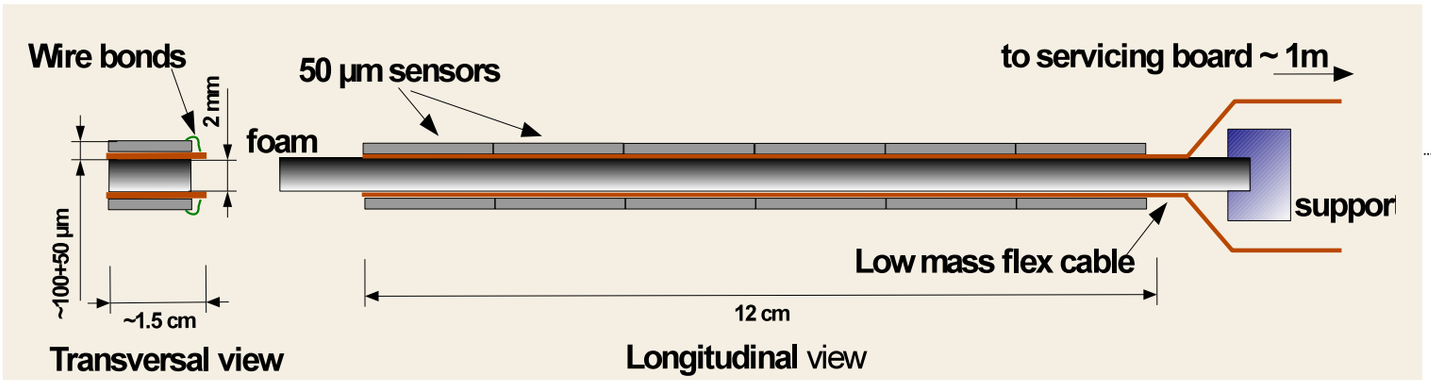
Most of all functions are on sensor

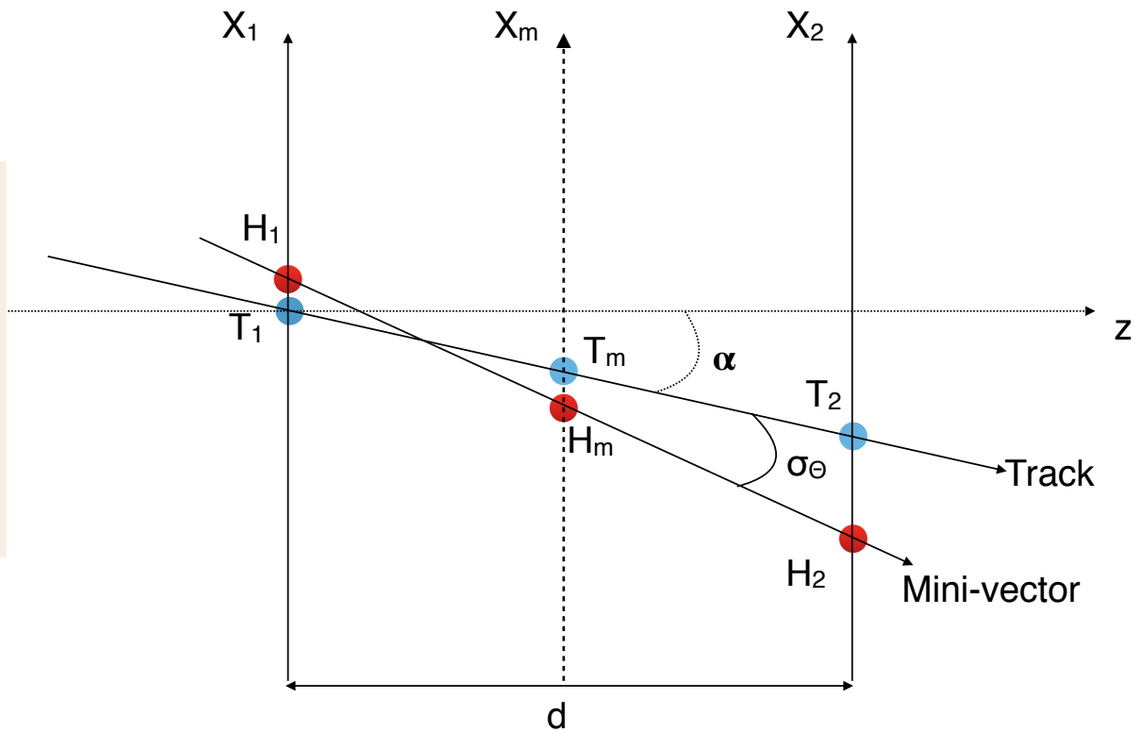


See Ref. C. Hu et al., TWEPP-09

- Frame rate : 100 µs / frame w/ rolling shutter readout.

Double sensor in 1 layer





- Special resolution is achieved ~ 3.5 µm using 2 sensors even if binary readout.

Summary

	SOFIST	FPCCD	DEPFET	PLUME
Pixel size (	20 x 20	5 x 5	20 x 20	18.4 x 18.4
positon resolution (μm)	(<3)	<1.4	2.3-3.5	3.5
Thickness (μm) [Active area]	50 [Full]	50 [~15]	50 [Full]	50 [~20]
Material budget (%X (Not final value)	0.05 + **	0.25	0.15	0.35
ASIC on chip	Yes	No	No	Yes
Row read rate [Goal]	2.5 MHz [10 MHz]	2.5 MHz [10 MHz]	10 MHz [40 MHz]	?
Frame rate [μs]	Readout btw train w/ timestamp	Readout btw train	40 us (25 / train)	~100 us (10 / train)
Frame rate [μs]	ADC on chip	ADC	ADC	Binary

Advantages of SOFIST (SOI)

- Full depleted on 50 μm thickness
  - vs. PLUME (15 μm)
- Most of functions are on chip
  - vs. DEPFET
- Best bunch identification w/ on-chip buffers
  - SOFIST : 1312/256 (using 256 bits ADC readout)
  - DEPFET : 1312/25, PLUME : 1312/10

Backup

Consideration

- Pay load is almost full at v.2
  - Actually full w/ 25μm^2 pixel.
- More buffers may need for the low occupancy operation.

Mori-san's master thesis

http://epx.phys.tohoku.ac.jp/eeweb/paper/2014_Mthesis_mori.pdf

Occupancy study by Mori-san for FPCCD

表 5.1: 各レイヤーの占有率 (250 GeV)

6.7 6.1 0.6

レイヤー	占有率 (%)	直接ペアの占有率 (%)	反跳ペアの占有率 (%)
0	0.561	0.506	0.055
1	0.353	0.319	0.034
2	0.056	0.053	0.003
3	0.045	0.043	0.002
4	0.010	0.010	0.001
5	0.009	0.008	0.001

表 5.2: 各レイヤーの占有率 (350 GeV)

8.4 7.5 0.9

レイヤー	占有率 (%)	直接ペアの占有率 (%)	反跳ペアの占有率 (%)
0	0.702	0.622	0.080
1	0.443	0.392	0.052
2	0.067	0.063	0.004
3	0.055	0.052	0.004
4	0.013	0.012	0.001
5	0.011	0.010	0.001

表 5.3: 各レイヤーの占有率 (500 GeV)

14.9 12.6 2.3

レイヤー	占有率 (%)	直接ペアの占有率 (%)	反跳ペアの占有率 (%)
0	1.244	1.053	0.191
1	0.779	0.661	0.118
2	0.122	0.113	0.009
3	0.100	0.092	0.008
4	0.023	0.021	0.002
5	0.020	0.018	0.002

表 5.4: 各レイヤーの占有率 (1 TeV)

100 40.5 100

レイヤー	占有率 (%)	直接ペアの占有率 (%)	反跳ペアの占有率 (%)
0	12.752	3.386	9.367
1	7.010	2.099	4.911
2	0.458	0.345	0.113
3	0.379	0.281	0.098
4	0.099	0.065	0.034
5	0.089	0.057	0.032

Ratio of cross size of pixel : x16

Ratio of multiple hits : x0.75 -> FPCCD x12 is occupancy of SOFIST.

2 bunches -> $0.149^2 \sim 0.02$

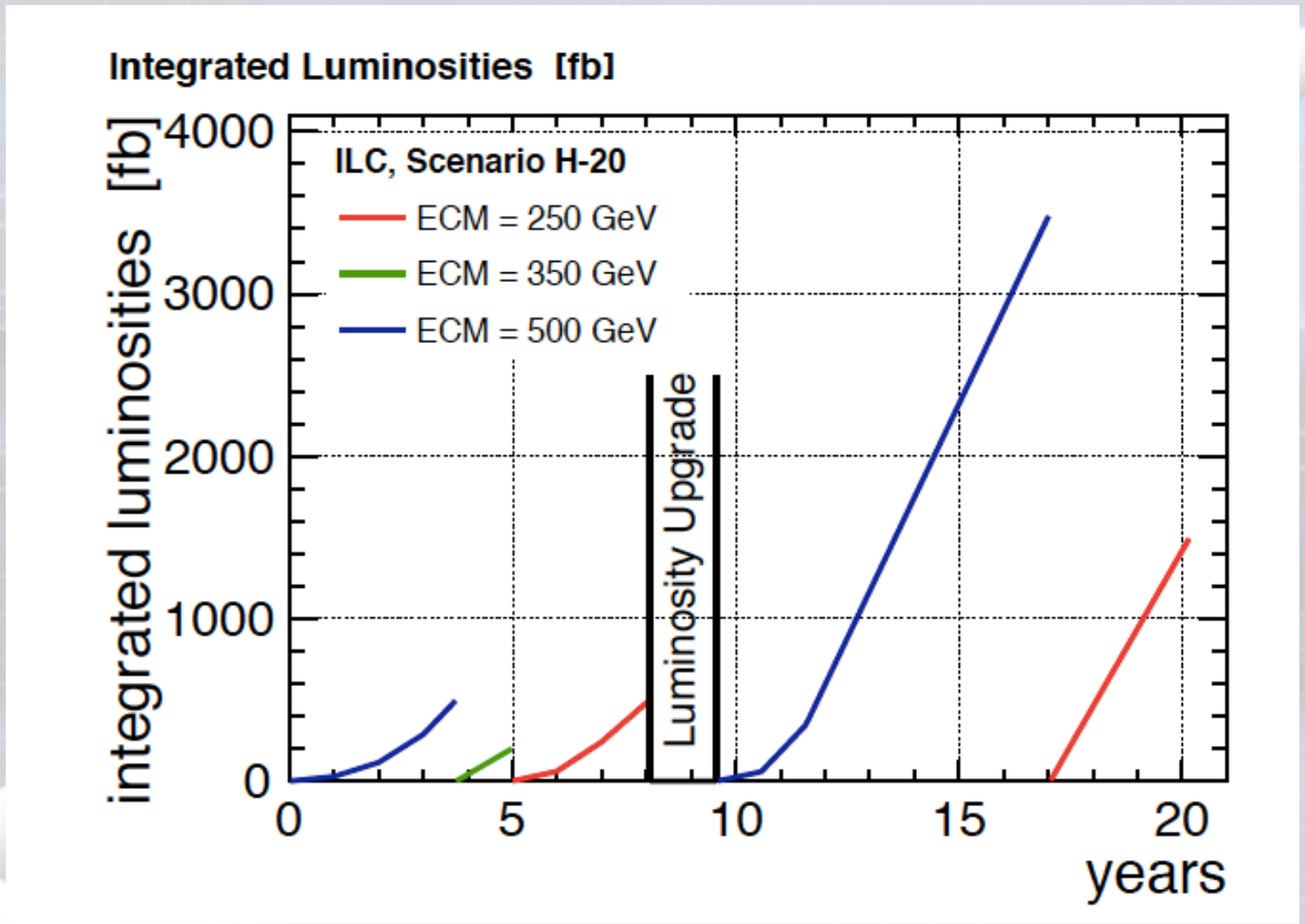
Consideration

- Pay load is almost full at v.2
  - Actually full w/ 25μm^2 pixel.
- More buffers may need for the low occupancy operation.

- Needs more circuit spacing…
  - 3D technology (CMOS layers)
    - Technology has been developing by SOI group.

Standard Sample ILC Running Scenario

- Adopted by the LCB (Linear Collider Board)
- ILC 500 GeV (1 TeV is optonal and not included here)



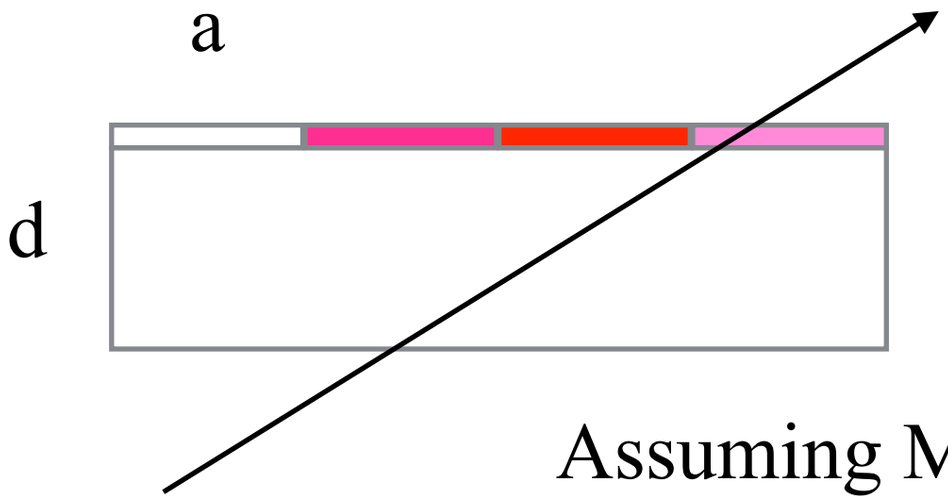
Total
250GeV 1500fb-1
350GeV 200fb-1
500GeV 4000fb-1

Luminosity upgrade :
5 Hz -> 10 Hz

Accelerator talk by K. Yokoya

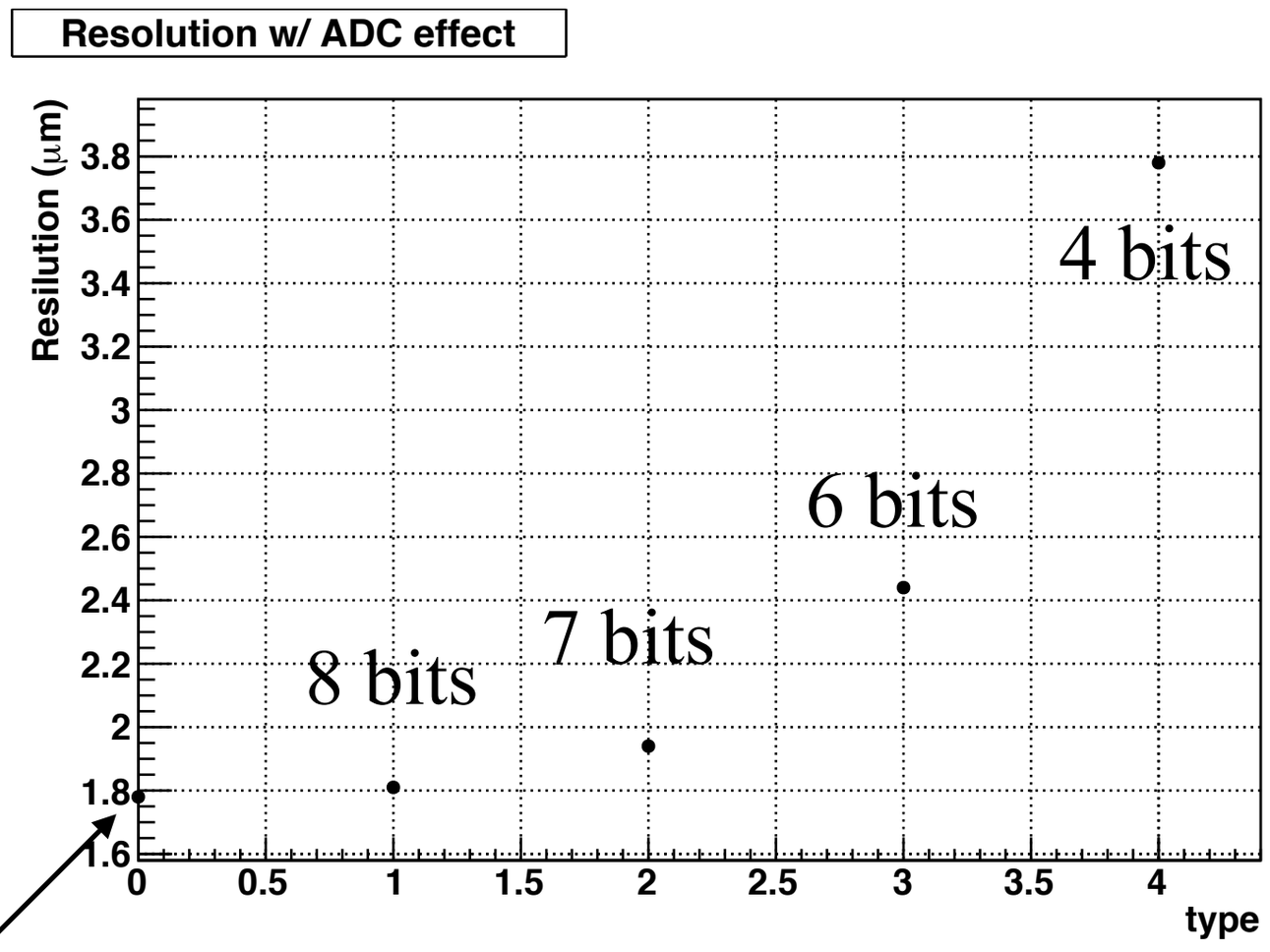
SOFIST

ADC requirement



Range requirement : 5 MIP

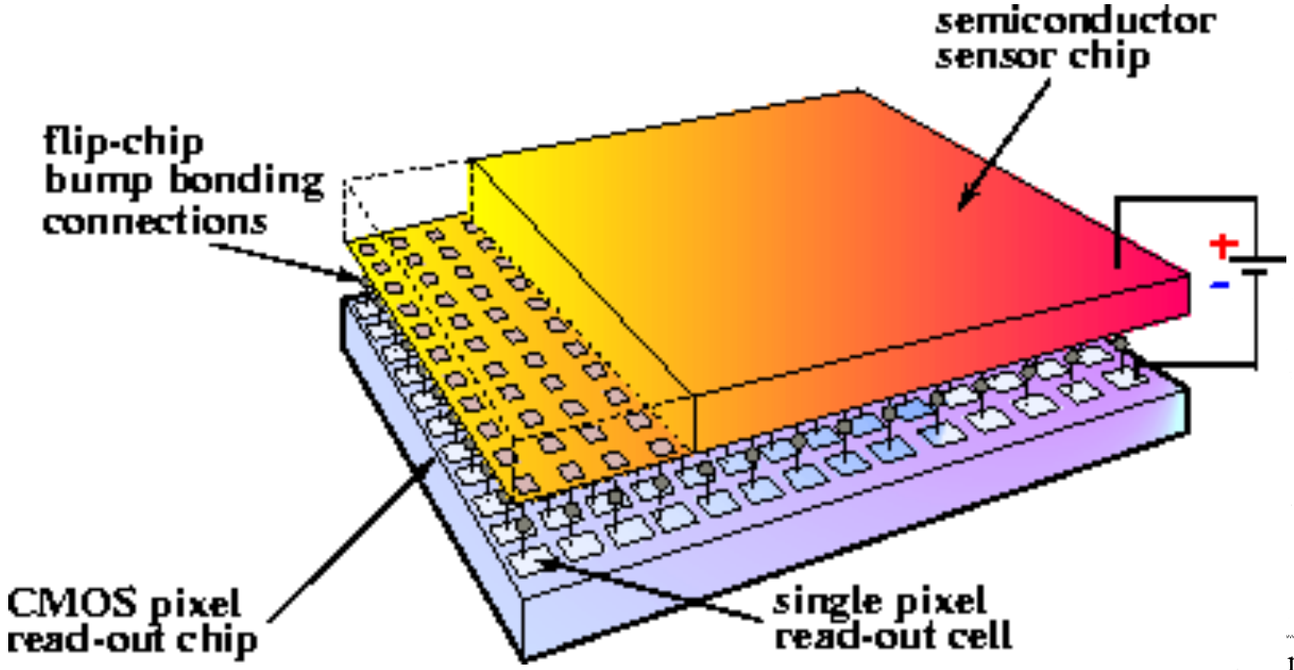
Assuming M = 3

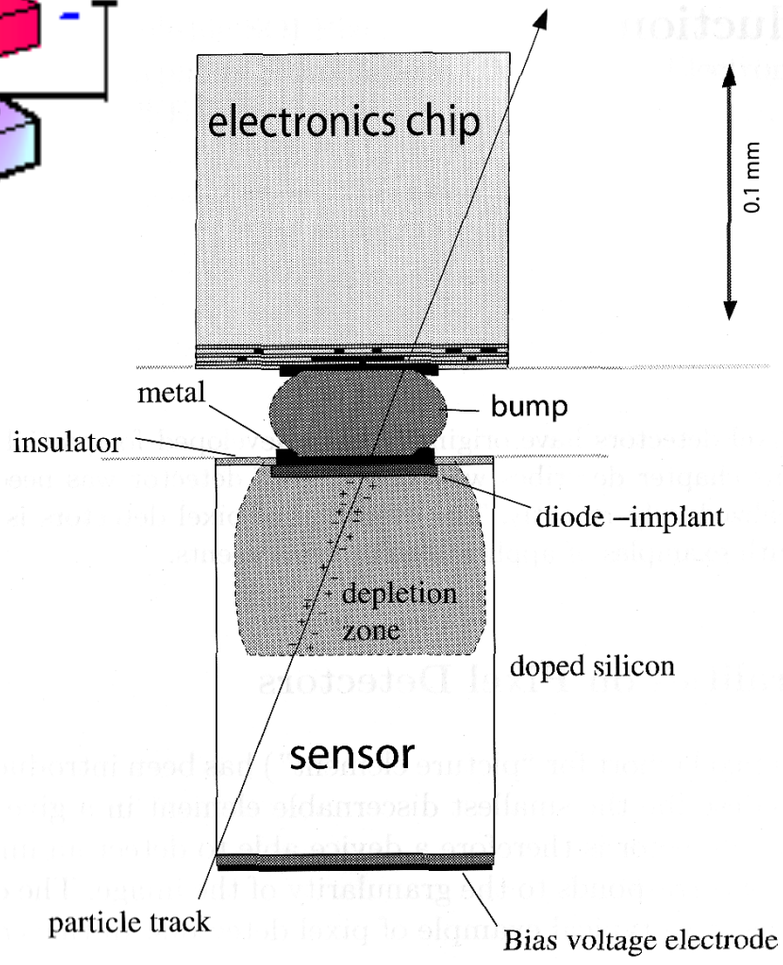


No ADC conversion

8 bits looks suitable

ピクセル検出器の現状





- 検出器と読出しエレクトロニクスを別々に作り、金属バンプにより接合する
- 位置分解能に制限
- 余分な物質が大量にある
- 寄生容量によるスピ-ドの低下

Hit multiplicity of FPCCD

Mori-san's master thesis

http://epx.phys.tohoku.ac.jp/eeweb/paper/2014_Mthesis_mori.pdf

(1) クラスター内のピクセル数

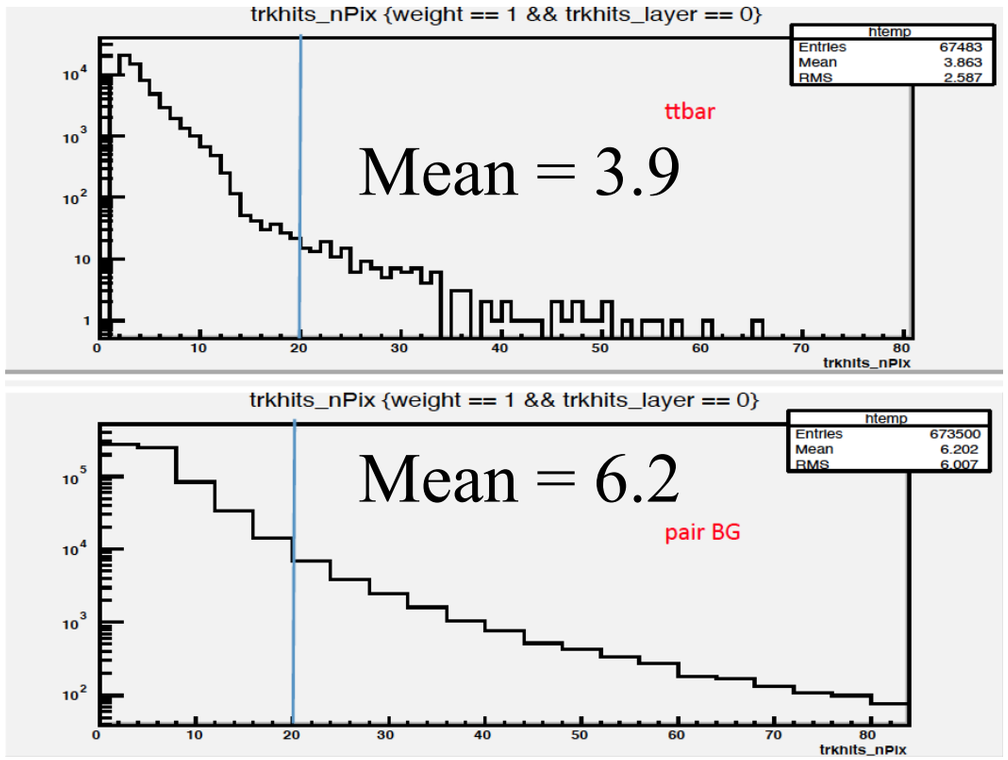
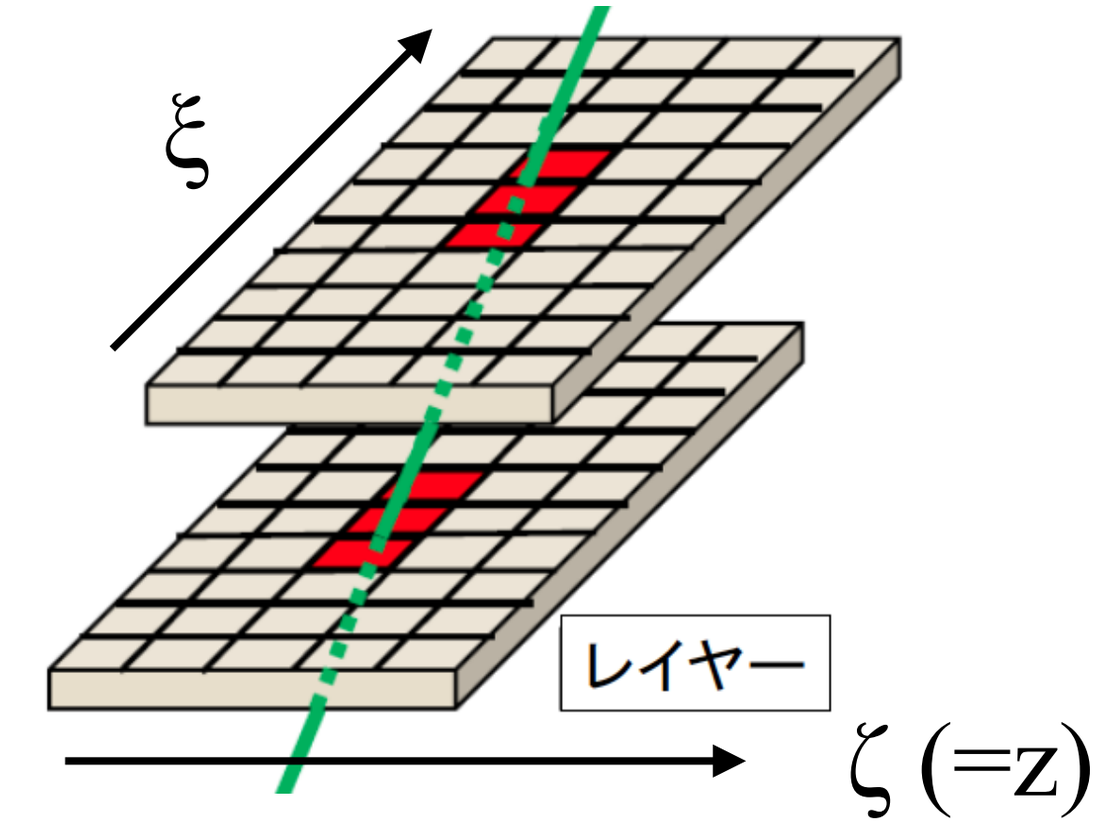


図 5.2: クラスター内のピクセル数分布



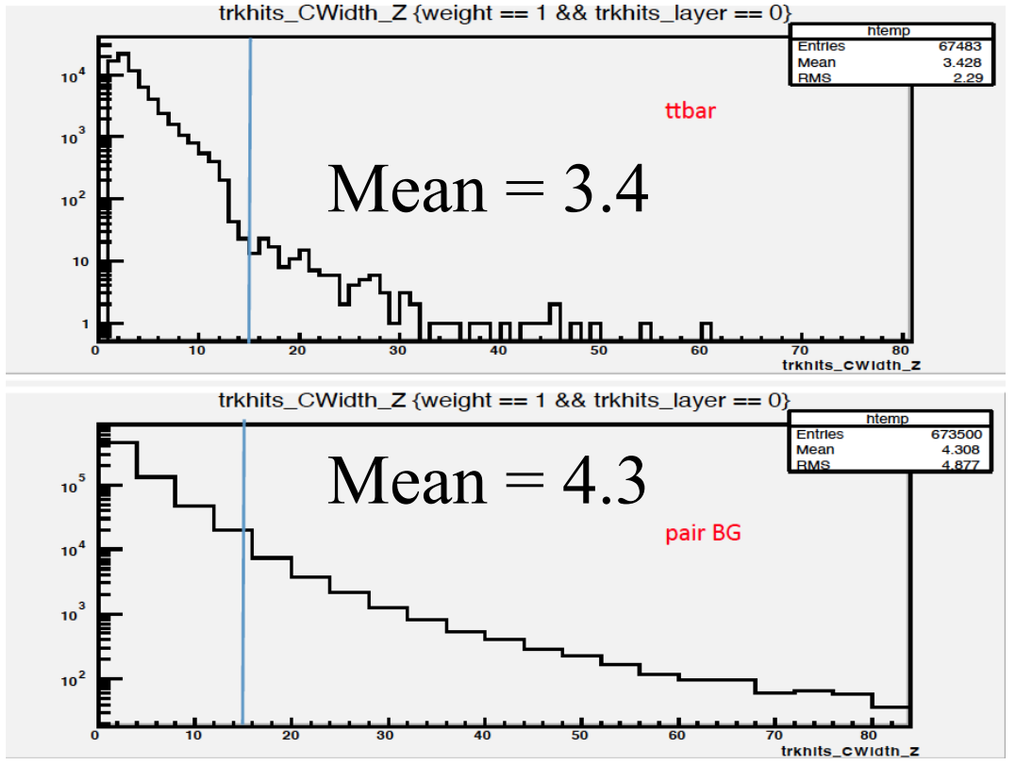


図 5.4: クラスターの ζ 方向の長さ分布

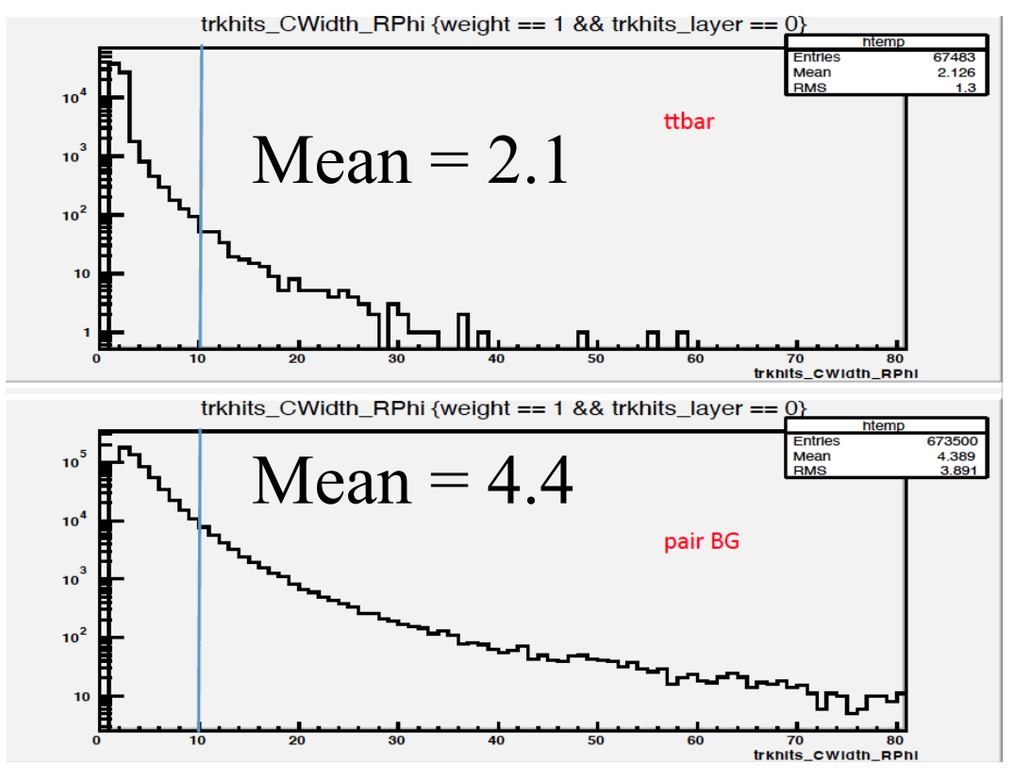


図 5.3: クラスターの ξ 方向の長さ分布

For SOI detector

- FPCCD : 5 um pitch, 15 um full depletion
- SOI : 20 um pitch, 50 um full depletion
  - -> Multiplicity will be times (5/20)*(50/15) = 0.75
- The multiplicity in case of tt->6jets looks up to M=10.

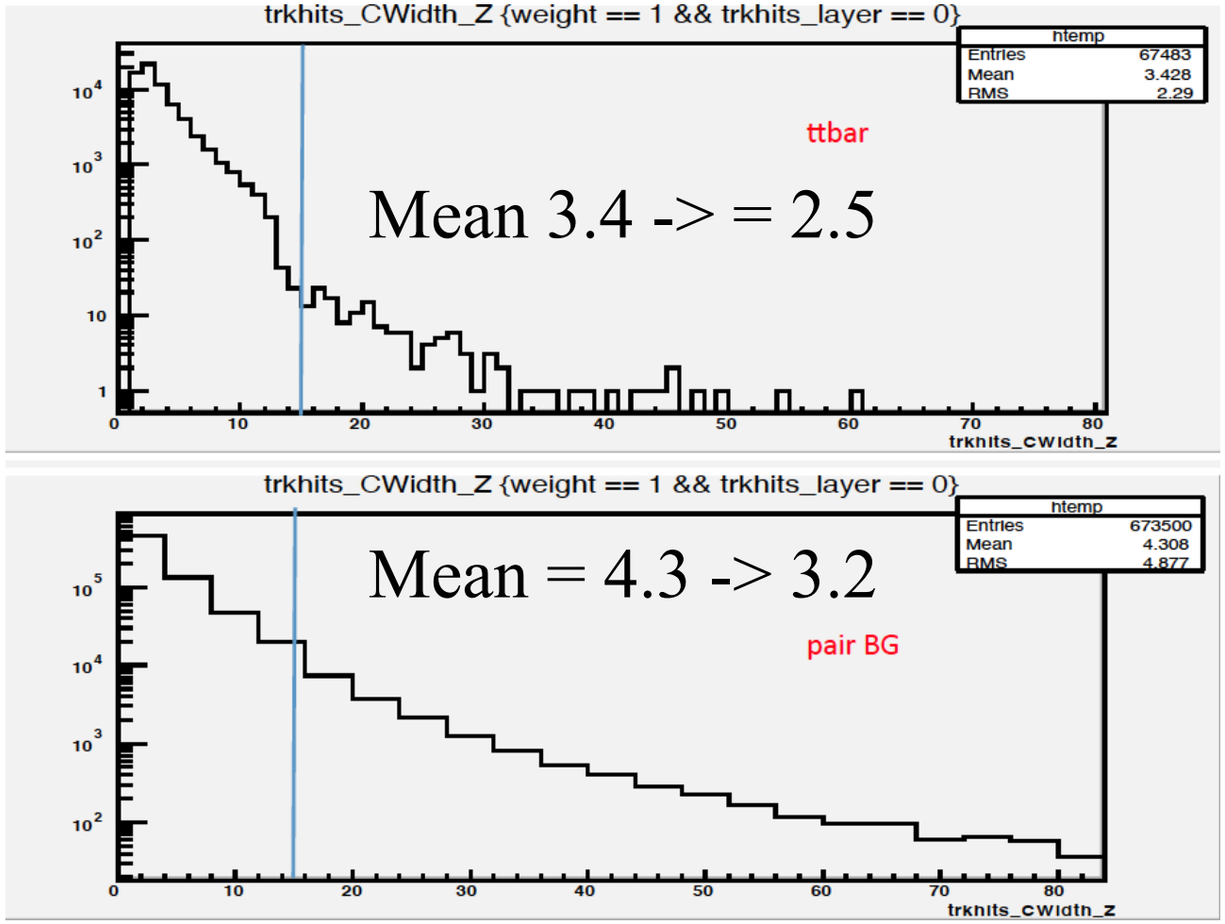


図 5.4: クラスターの ζ 方向の長さ分布

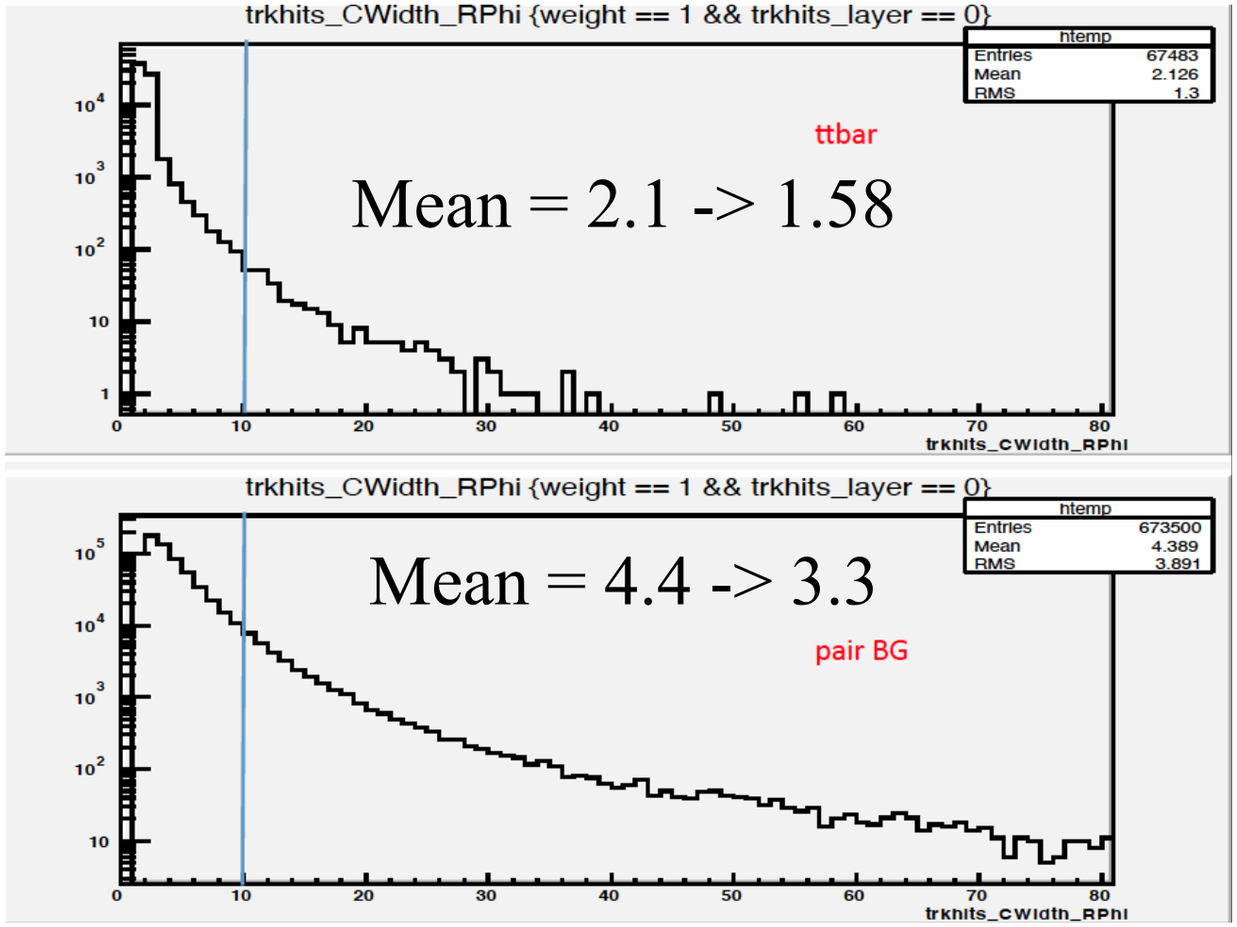
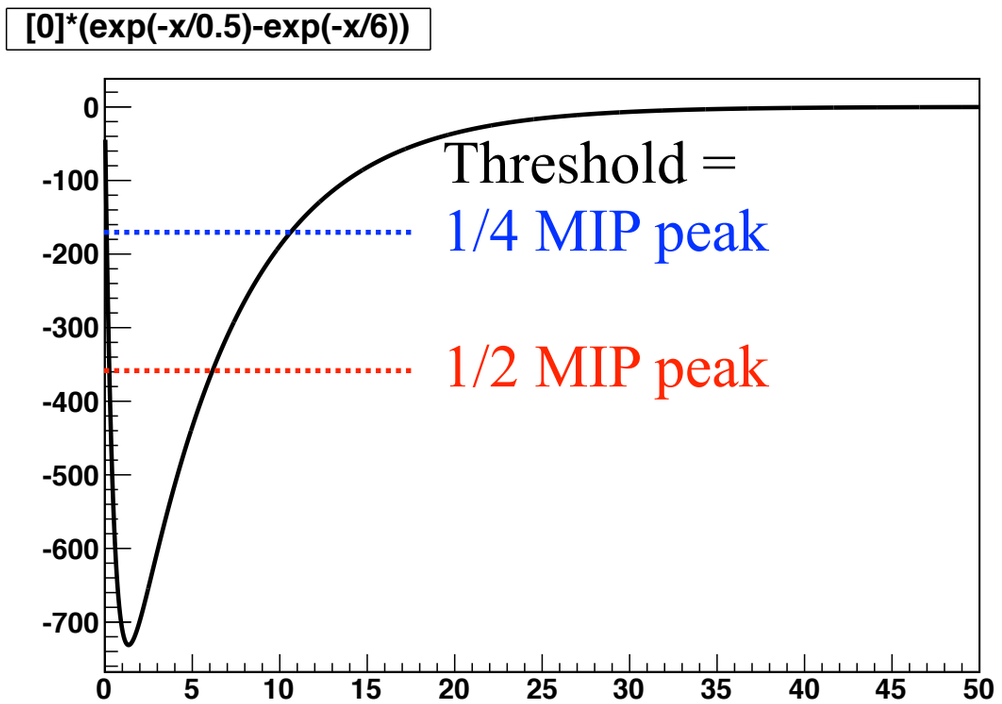
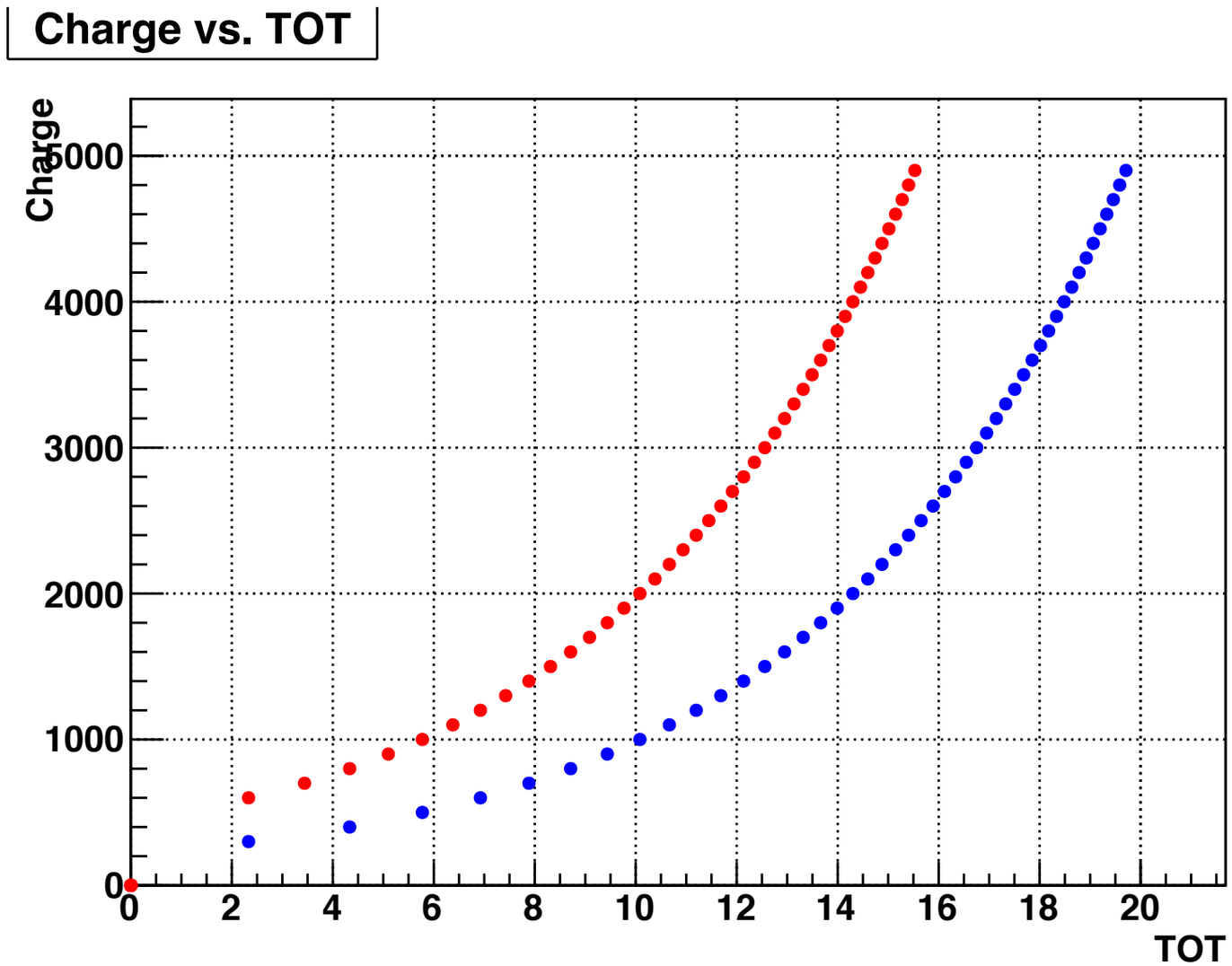


図 5.3: クラスターの ξ 方向の長さ分布

1個しかならない時も結構有る。。。

Ideal case for TOT

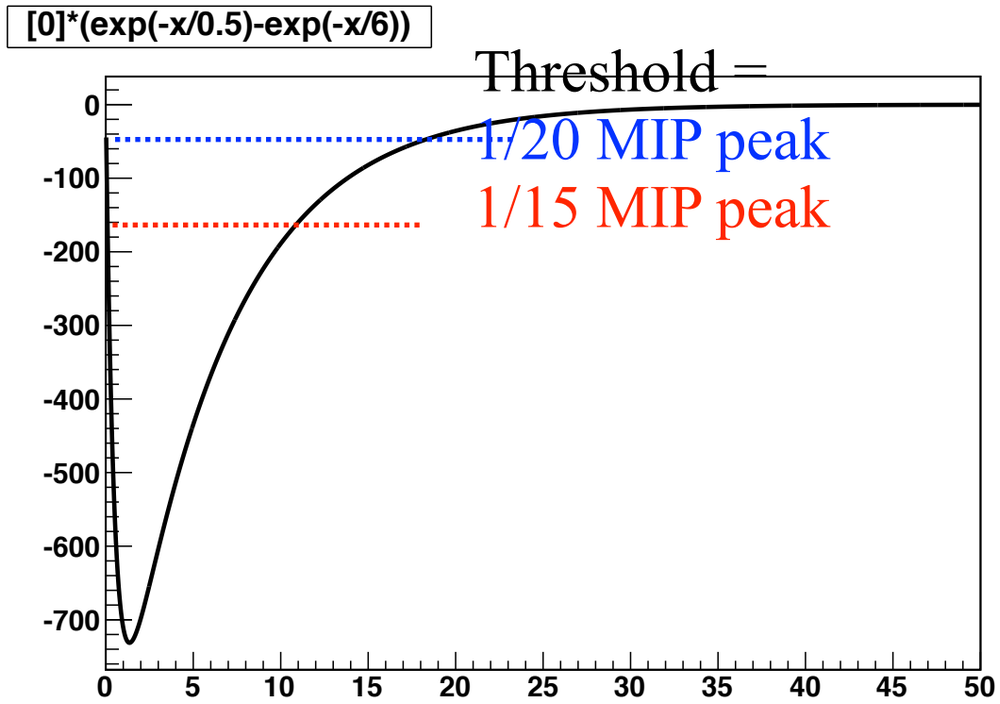


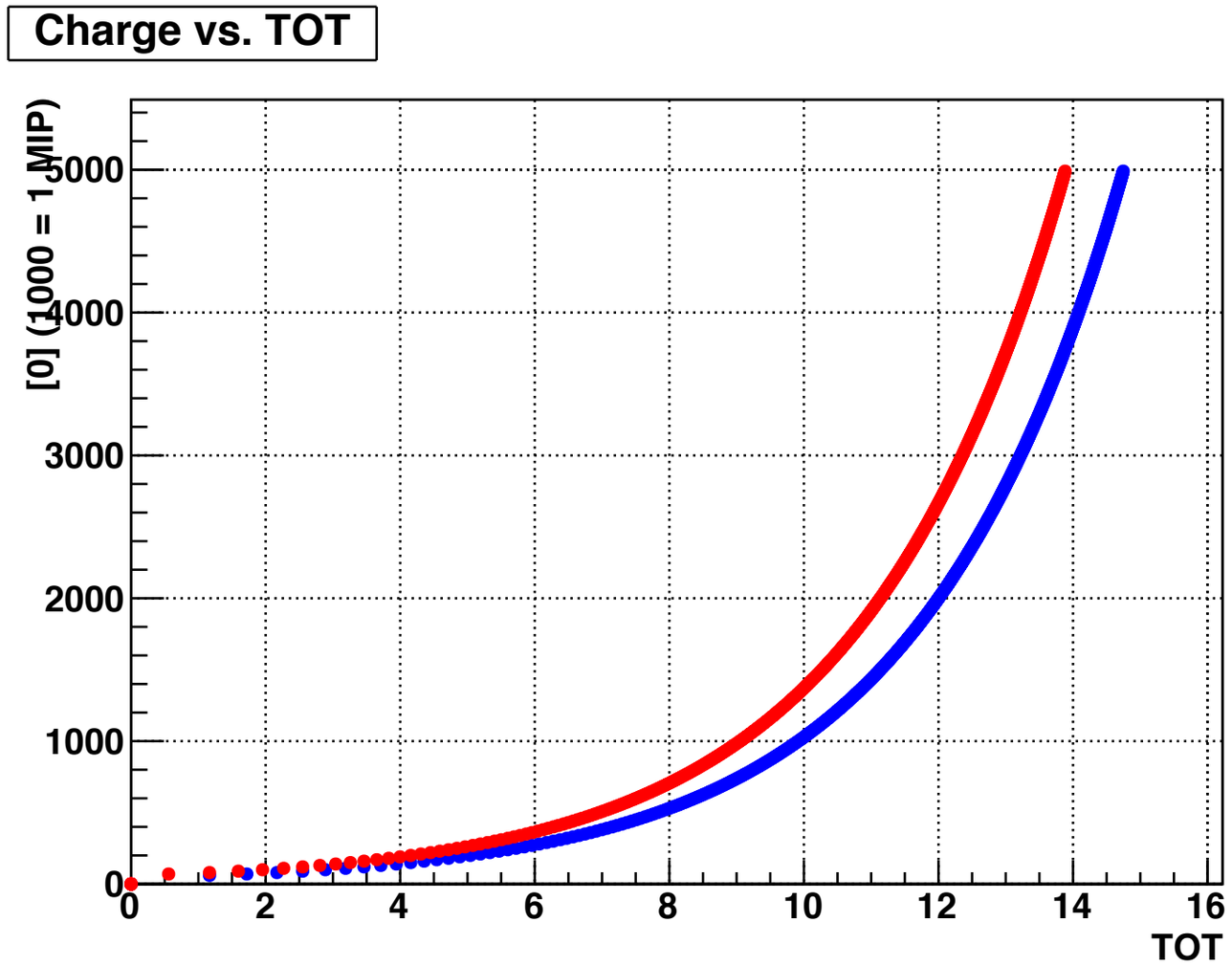


- 低いエネルギー側でnon-linearity
- 低いエネルギーをカバーする為にはThreshold低めが必要
- エネルギー情報は必要なので普通のADCの方が良い

低いエネルギー側で分解能が良い

低いエネルギーを見る為に低いthreshgold



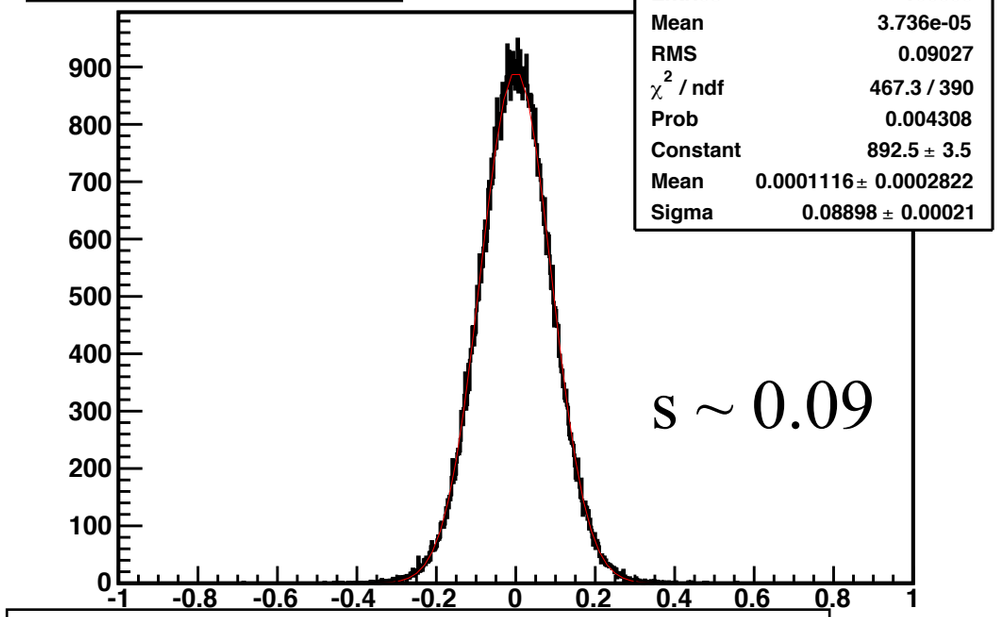


- 1/20 MIPをpol7 fitして関数化して、位置分解能に対する影響を見る。
- 横軸は4 bits（=16）に収まる様に調整

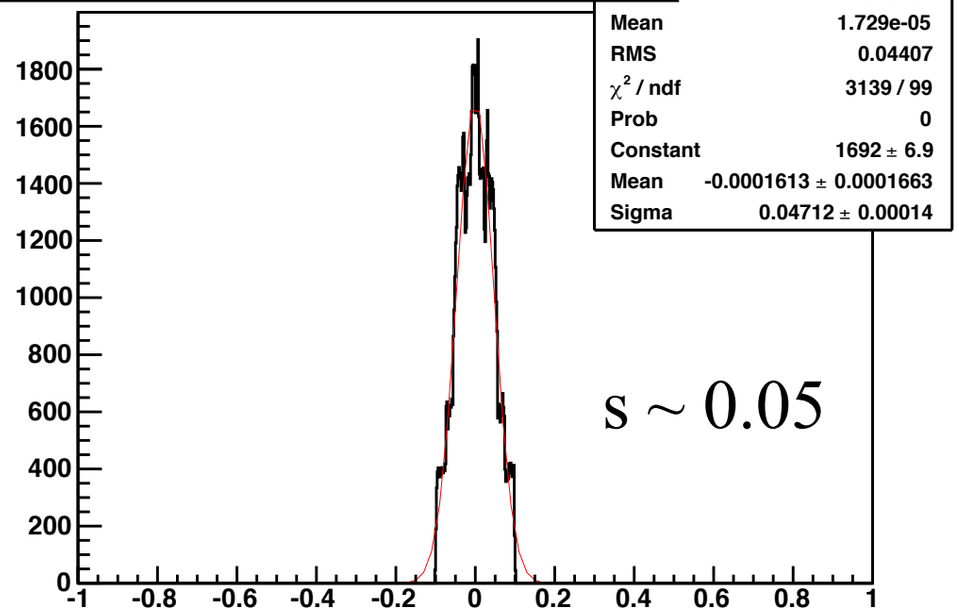
ADCのbit conversionの代わりに1/20 thre.のTOT conversionを入れてみた。

(pos. w/o noise) - (pos. w/ noise and/or bit conversion)

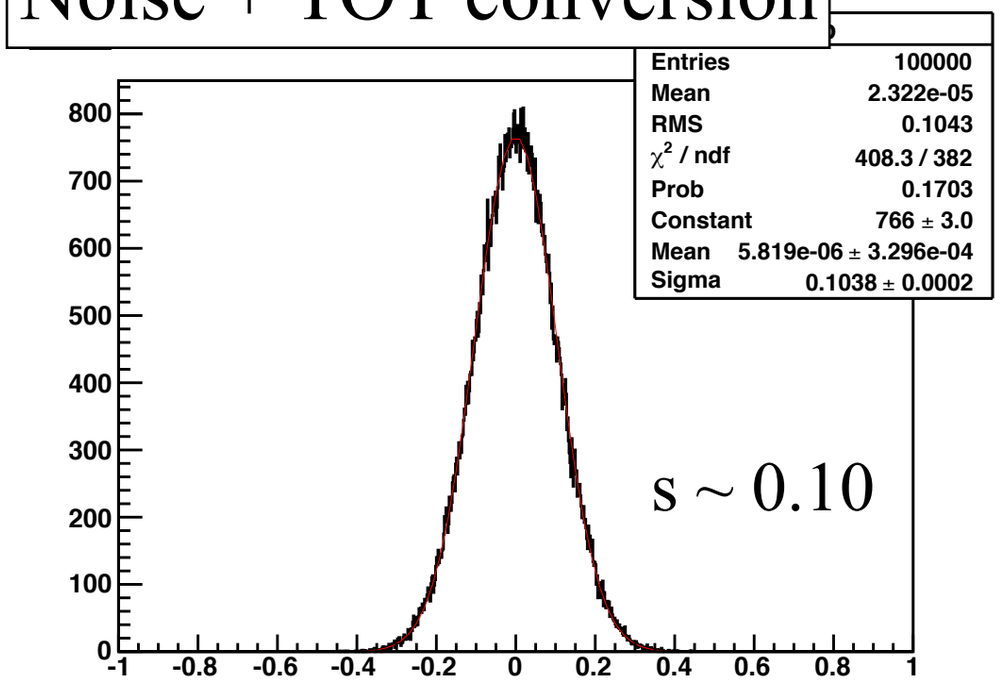
Noise only

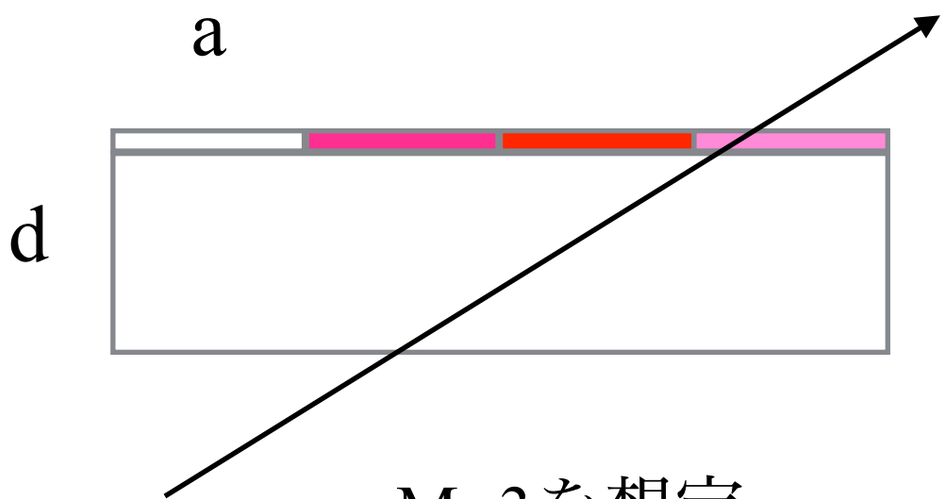


TOT conversion only



Noise + TOT conversion

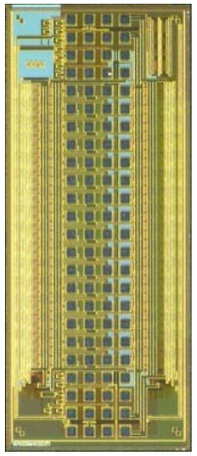


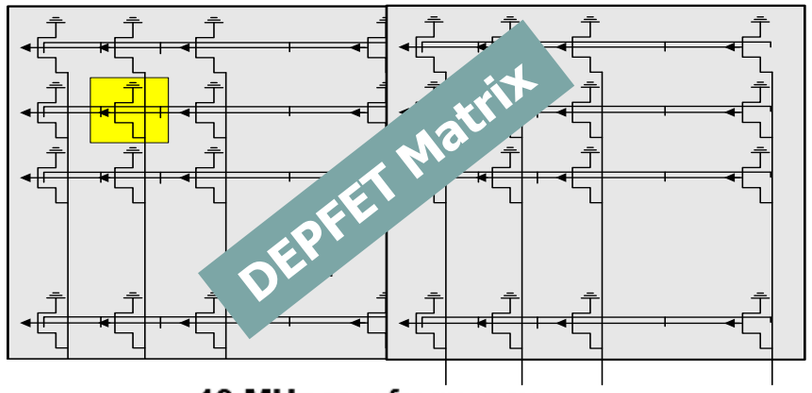


M=3を想定

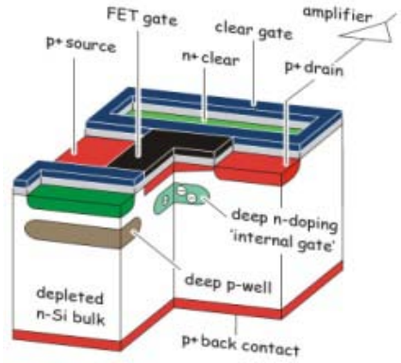
DEPFET and auxiliary ASICs

Switcher:
180nm HVCMOS AMS
Size 3.6 × 1.5 mm²
Gate and Clear signal
Fast HV up to 20V

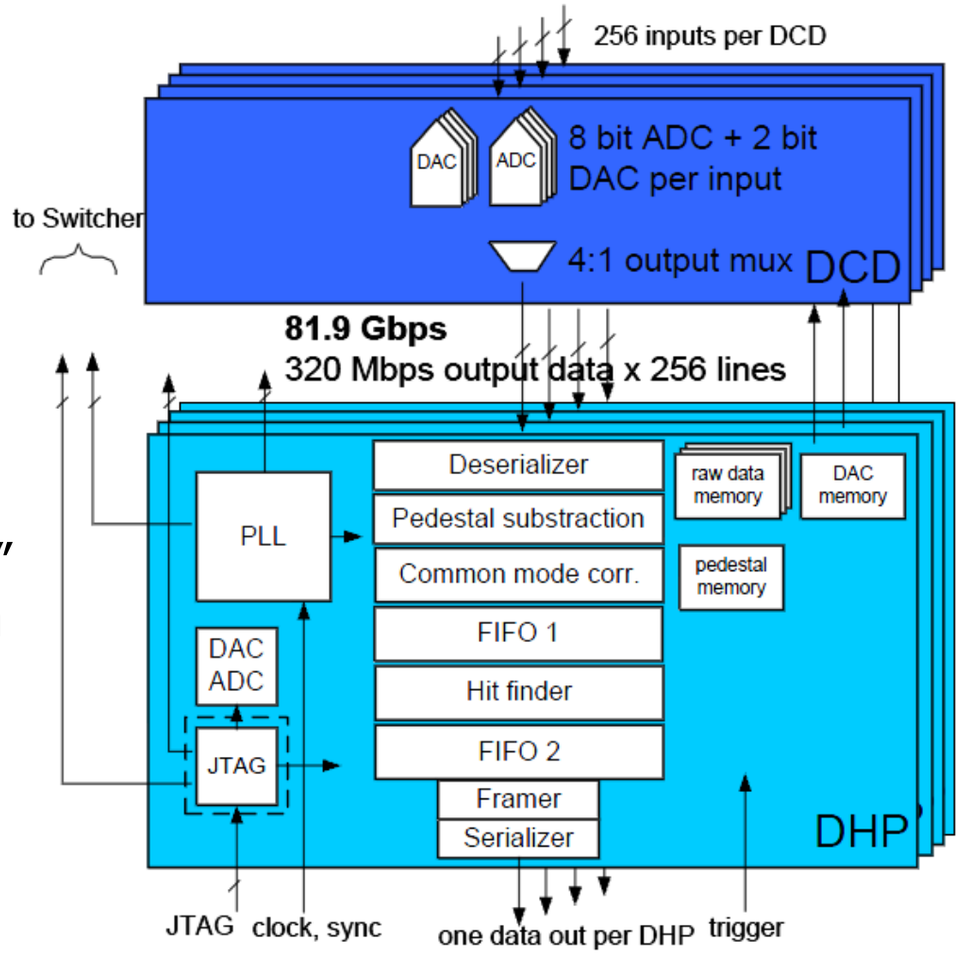




10 MHz row frequency
100 ns ADC conversion time



DCD:
"Drain Current Digitizer"
UMC 180nm
f/e and ADC



DHP:
"Data Handling Processor"
IBM 90nm → TSMC 65nm
Digital control chip

Power dissipation
DEPFETs ~ 1 W
Switcher ~ 1 W
DCD/DHP ~ 8 W on each ladder end

→ 160 W on each side of the detector
→ 40 W in sensitive volume

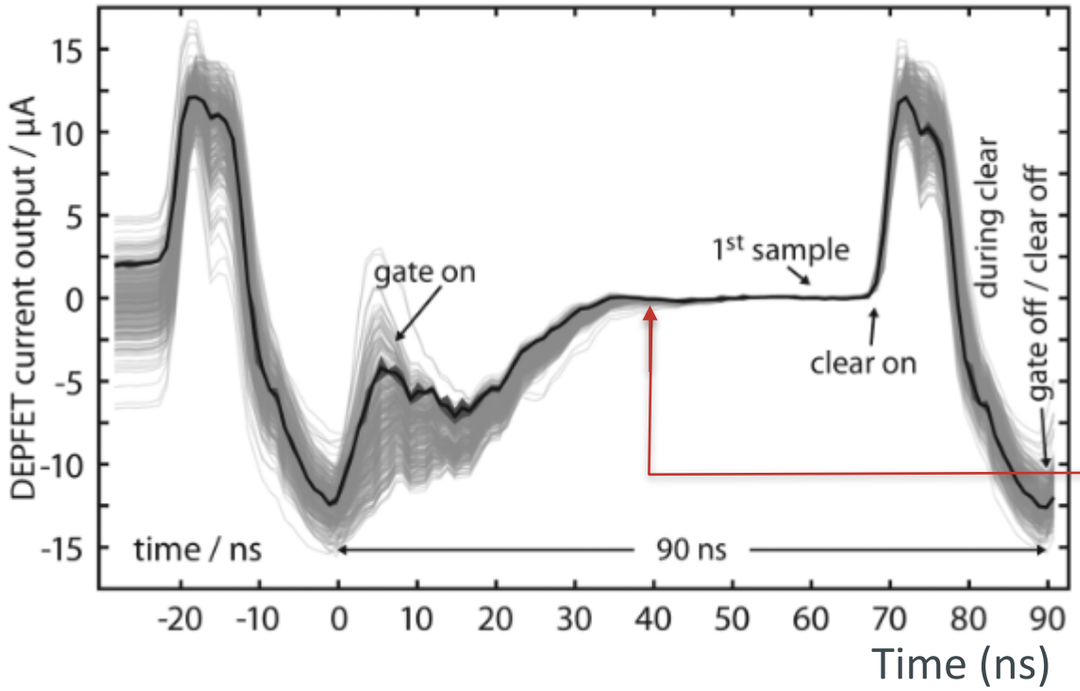
- CO_2 cooling at end flange
- gentle gas flow in sensitive region

→ see Arantza's talk in R&D7, Thursday morning

DEPFET

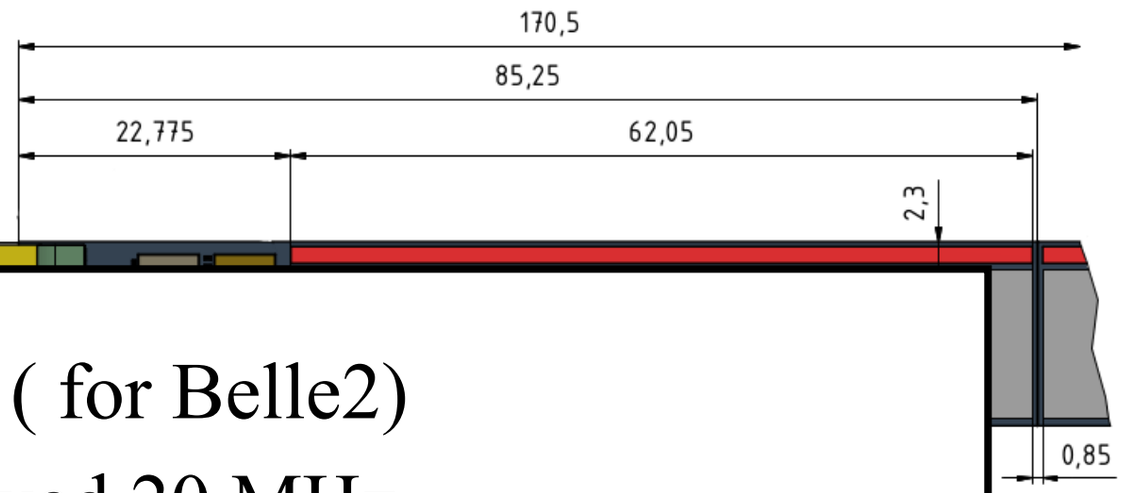
Slide from "A DEPFET vertex detector for a future linear e+e- collider" on https://indico.mpp.mpg.de/conferenceOtherViews.py?confId=2809&view=standard

Readout speed



Read-out speed: current state-of-the-art allows for a row rate of 1/100 ns.
Room for improvement.

start to clear immediately drain current is stable
reduce the time of read-out 30 ns



VXD0 –
read-o

Pixel si

Cent
1 <|z
|z| > 2 cm → 25 x 100 µm2

- Row rate achieved 10 MHz (for Belle2)
  - For ILC, it will be improved 20 MHz.
  - By design, it can be achieved to be 40 MHz.

Frame time: *40 µs (20 µs)*