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CMOS pixel sensors for vertex detector of CEPC

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On behalf of the CEPC CMOS pixel project group

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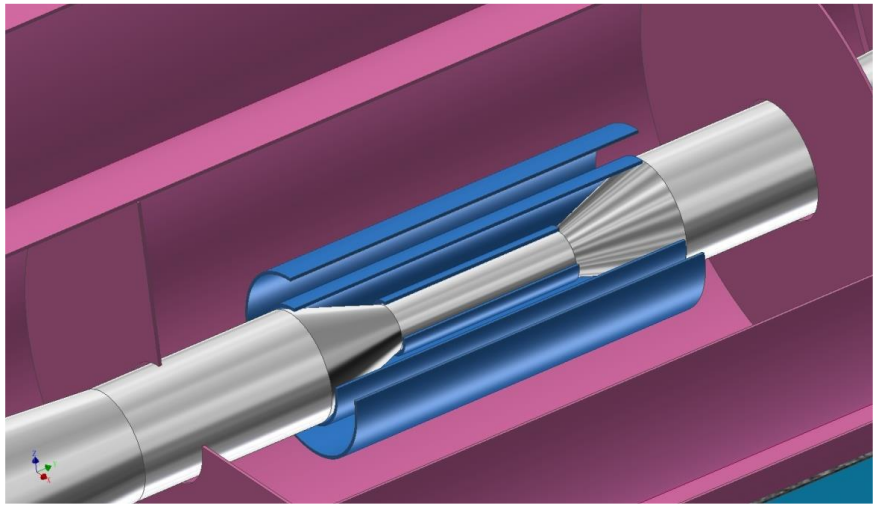
Outline

- Introduction on CEPC vertex detector
- Charge collection simulation
- Prototype design
- Summary and outlook

CEPC vertex detector concept

Baseline design for the pre-CDR: ILD-like but different forward region design

- 3 layers of double-sided pixels
- σ_{SP} = 2.8 μm, inner most layer
- readout time < 20 μs



CEPC VXD Geometry

	R (mm)	|z| (mm)	$\|\cos\theta\|$	σ_{SP} (μm)	Readout time (μs)
Layer 1	16	62.5	0.97	2.8	20
Layer 2	18	62.5	0.96	2.8	20
Layer 3	37	125.0	0.96	4	20
Layer 4	39	125.0	0.95	4	20
Layer 5	58	125.0	0.91	4	20
Layer 6	60	125.0	0.90	4	20

CEPC vertex detector requirements

- **Excellent impact parameter resolution required for the identification of heavy quarks and τ-leptons (essential for CEPC physics)**

$$\sigma_{r\emptyset} = 5 \oplus \frac{10}{(p \cdot sin^{3/2}\theta)}\ \mu m$$

- **Stringent requirements on the vertex detector:**
  - Spatial resolution near the interaction point $\sigma_{sp} \leq 3$ μm → high granularity (small pixel size)
  - Material budget ≤ 0.15% X_0/layer → monolithic pixel sensors

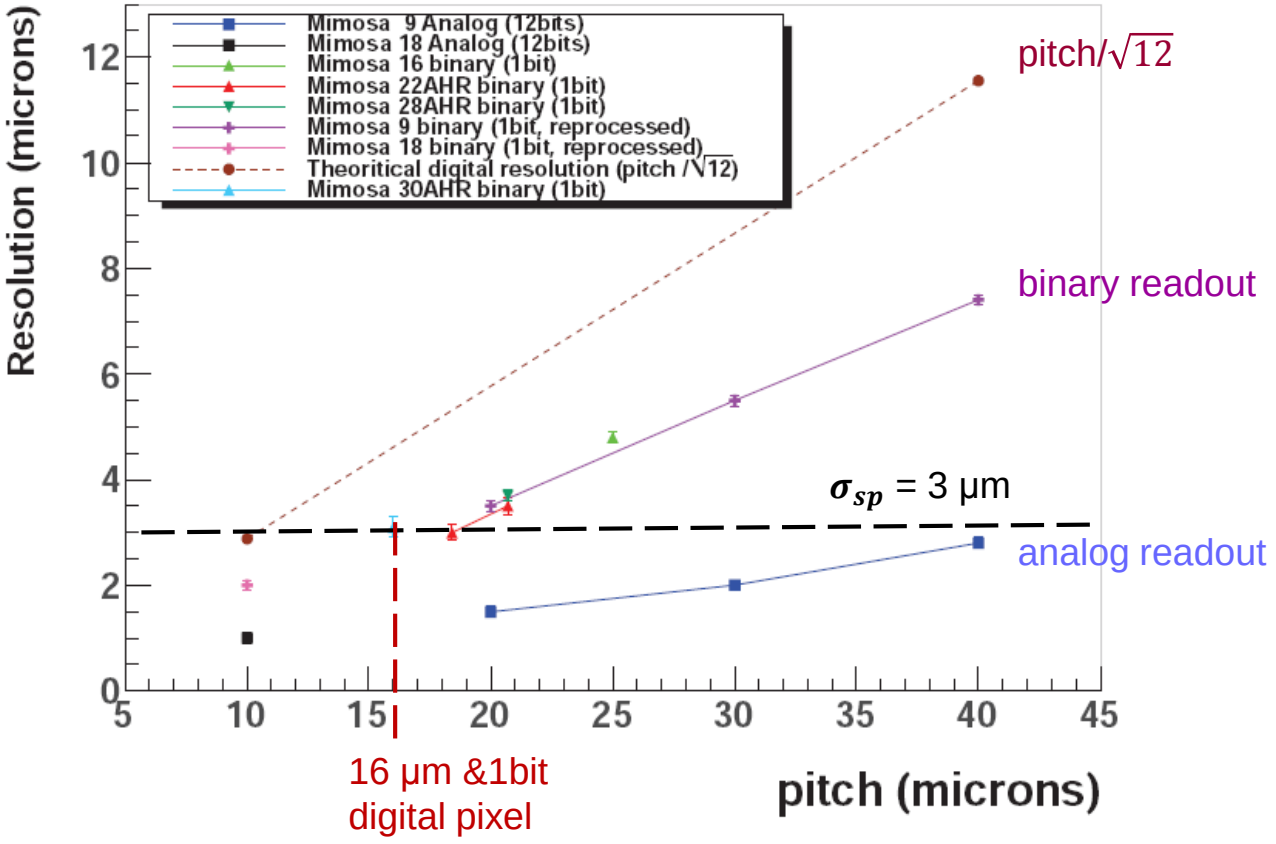
    (sensor + embedded electronics, thinned down to e.g. 50 μm) + air cooling (power dissipation ≤ 50 mW/cm^2)
  - Low detector occupancy below 1% → fast readout (~ 20 μs) + high granularity
  - Radiation tolerance (pre.): Total Ionizing dose ~1 MRad/yr

    Non-ionization energy loss ~10^{12} n_{eq}/cm^2/yr

Unprecedented challenges in CEPC vertex (1)

Single point resolution σ_{sp} ≤ 3 μm ➔ pixel size ?

spatial resolution vs. pixel pitch

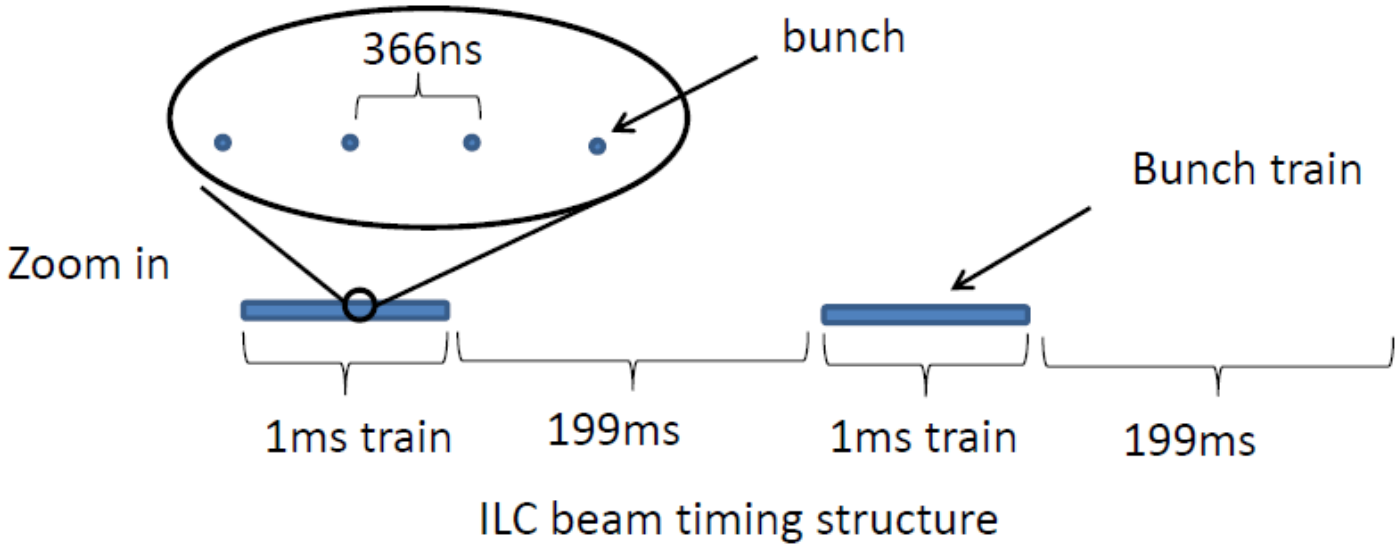


Y. Voutsinsa, et al., Vertex Detectors 2012

Unprecedented challenges in CEPC vertex (2)

Low power consumption

- **Power pulsing will NOT work at the CEPC**
  - Instantaneous power ~600 W @ ILC
  - Average power ~20 W @ ILC by applying power cycling



- **The maximum heat load of 150 W imposed by air cooling**

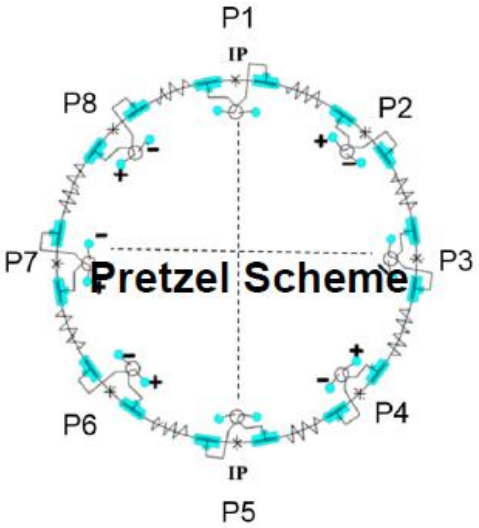
➔ **CEPC has to cut down the power by a factor of 4**

Ref.: Y. Lu, CEPC-SppC study group meeting, 2016 April

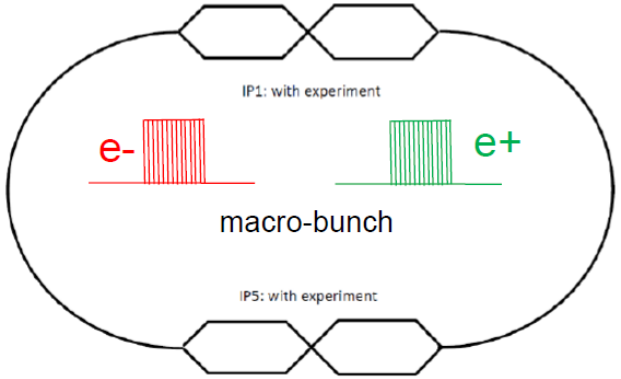
Unprecedented challenges in CEPC vertex (3)

Fast readout speed

- **Readout intervals of ~ 1 μs will be required if the Local Double-ring Scheme is used to increase the hit density**
  - **One magnitude lower than the-state-of-art design**
  - Background estimates are still in early stage



- baseline design in pre-CDR
- colliding every 3.6 μs, continuously



- to reduce beam and AC power
- to increase the flexibility and luminosity
- 196 ns bunch spacing
- Duty cycle: 9.4 μs/181 μs

Ref.: Y. Lu, CEPC-SppC study group meeting, 2016 April

Technology options

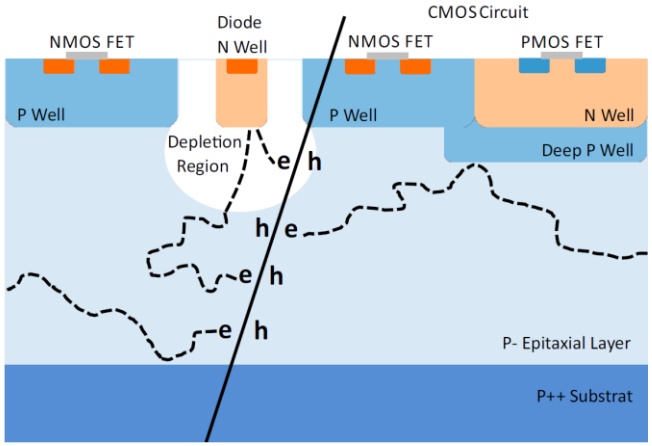
Many technologies from ILC/CLIC could be options.

But, unlike the ILD/CLIC, power pulsing will NOT work at the CEPC

- **CMOS pixel sensors (CPS)**
  - relatively mature technology
  - < 50 mW/cm^2 expected
  - capable of readout time ~4 μs/frame
- **SOI sensor**
  - Fully depleted HR substrate, potential of 15 μm pixel size design
  - Full CMOS circuits
- **DEPFET**
  - Possible application for the inner most vertex layer
  - Small material budget, low power consumption in sensitive area
- **Others: 3D-integration**

This talk will concentrate on CMOS pixel sensors

CMOS Pixel Sensor



- **Integrated sensor and readout electronics on the same silicon bulk with "standard" CMOS process → low material budget, low power consumption, low cost …**
- **Ultimate (Mimosa 28) installed for STAR PXL, technology for ALICE ITS Upgrade**

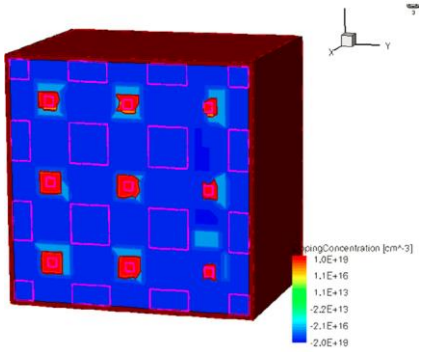
- **Selected TowerJazz 0.18 μm CIS technology for CEPC R&D, featuring:**
  - Quadruple well process: deep PWELL shields NWELL of PMOS transistors, allowing for full CMOS circuitry within active area
  - Feature size of 0.18 μm and 6 metal layers: good for high-density and low power
  - Thick (18-40 μm) and high resistivity (≥1 kΩ•cm) epitaxial layer: larger depletion
  - Thin gate oxide (< 4 nm): robust to total ionizing dose

Charge collection simulation

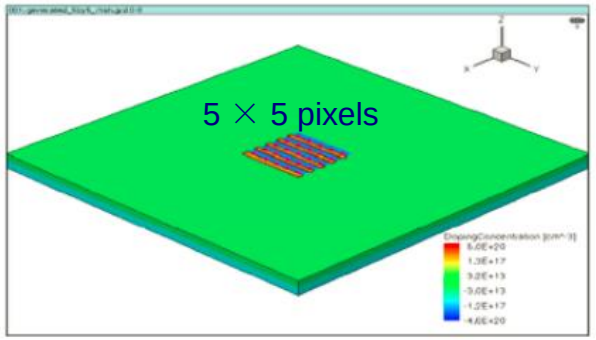
Y. ZHANG, M. FU, H.ZHU

- **Motivation:**
  - Guide the diode geometry optimization and study radiation damage with different types of epitaxial layer
- **Simulated structure**
  - Building the 3-D device structure with Sentaurus-TACD tool
  - Setting boundary: extending the auxiliary silicon surrounding the device volume to hundreds of micro-meters, which approximates the real device condition, replacing:
    - **Reflective boundary condition (default) → overestimated signals.**
    - Introducing four **SiO_2 belts surrounding the detector** volume and **artificially high recombination velocity** at the interface → **unreliable result**.

Simulated structure using SiO_2 belts



Simulated structure in this work

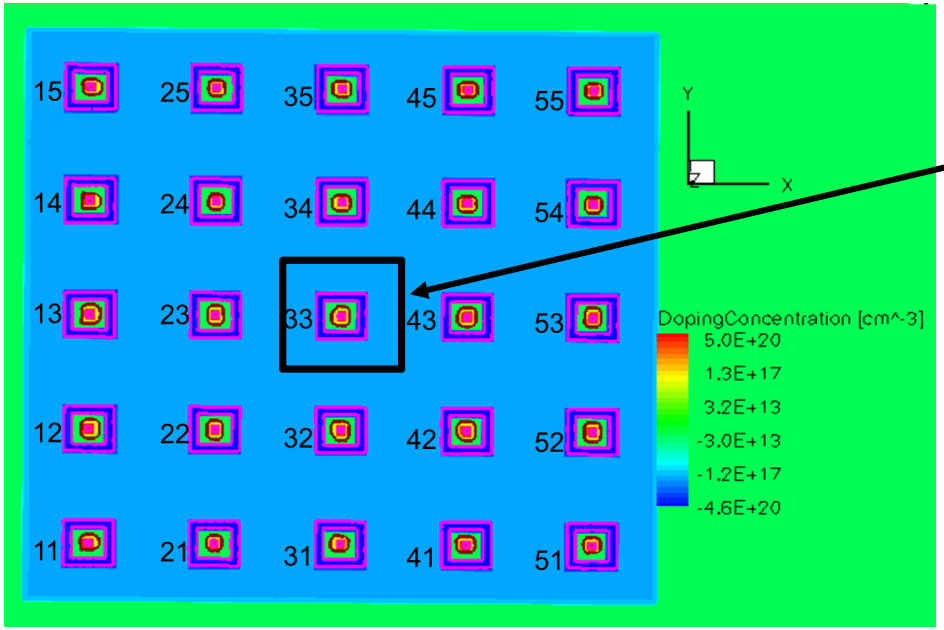


Charge collection simulation

Y. ZHANG, M. FU, H.ZHU

- **Simulation with different parameters**
  - Hit position
  - Diode geometry
  - Thickness and resistivity of the epitaxial layer
  - Radiation damage

Top-view of the simulated 5 × 5 cluster



Shooting MIP particle vertically at the central pixel and calculate the collected charge in neighboring pixels

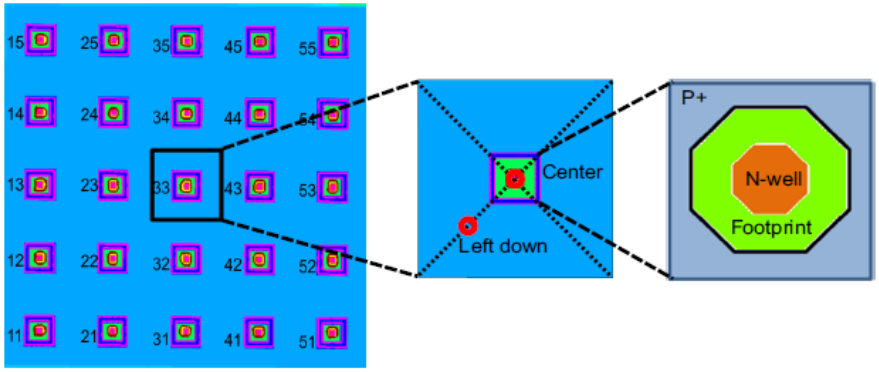
pixel size: 16 μm ×16 μm

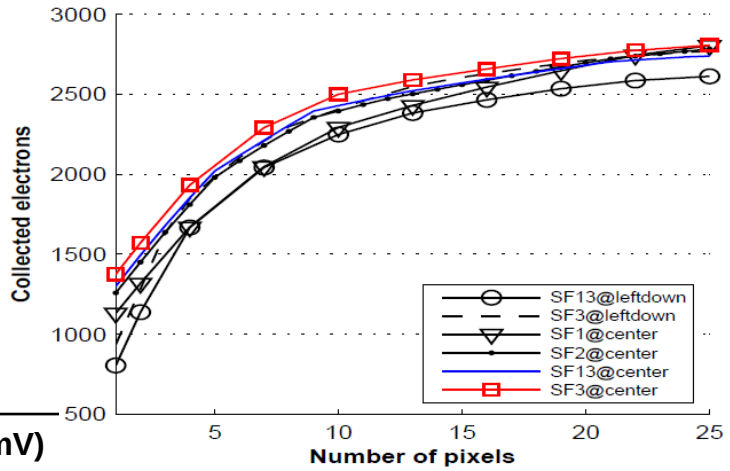
Charge collection vs. diode geometry

Y. ZHANG, M. FU, H.ZHU

- **sensing diode area**
  - should be small for the sake of low C, low noise, high gain

    because $V_{sig} = Q_{coll}/C$; $N \propto C$
  - BUT not too small to preserve charge collection efficiency (important against NI irradiation)
  - spacing (free of p- and n-wells) between the diode n-well and the surrounding p-well affects CCE





Structure	N-well (μm²)	Footprint (μm²)	C_{in} (fF)	Q/C_{seed} (mV)
SF1	3	20	4.5	40
SF2	4	20	5.1	39
SF3	8	20	6.8	32

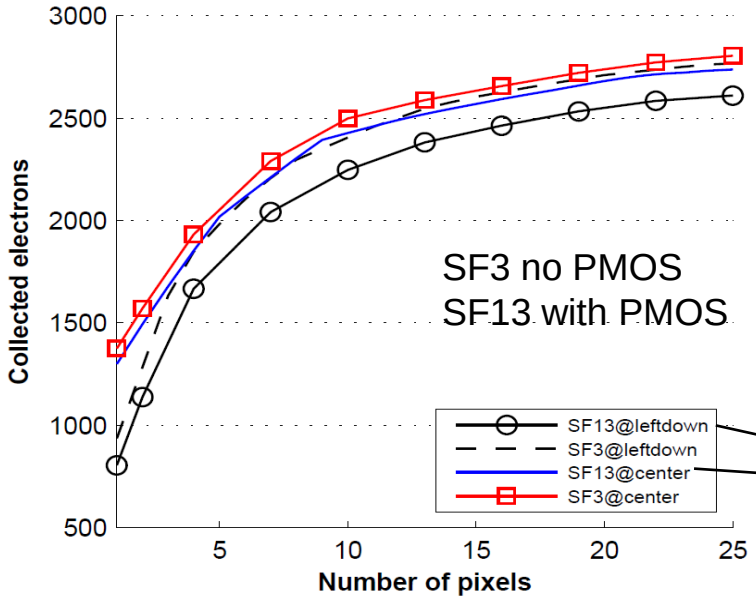
The collected charge of seed pixel increase with N-well area, but Q/C decrease

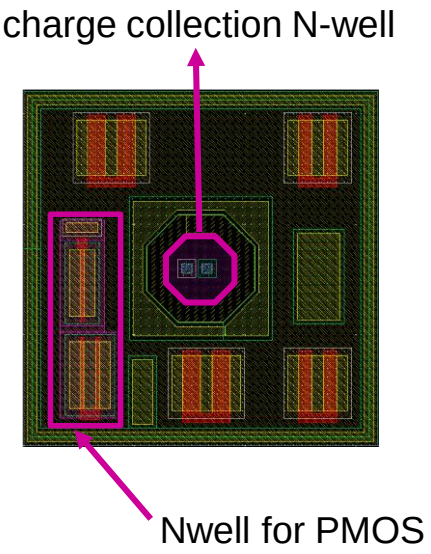
Charge collection with competitive N-well

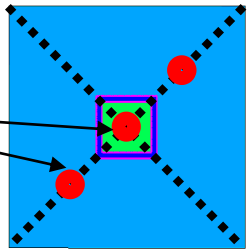
Y. ZHANG, M. FU, H.ZHU

- **PMOS within the pixel introduces a competitive N-well to the charge collection N-well; using the deep P-well is expected to shield the competition**

Sector	Diode area	Footprint area	Structure
SFB3	8 μm²	20 μm²	2T_nmos
SFB13	8 μm²	20 μm²	2T_pmos







hit position on the central pixel

With the shielding of deep P-well, the competition of PMOS on charge collection is almost negligible ➔ allow full CMOS within the pixel

Charge collection with different epitaxial layers

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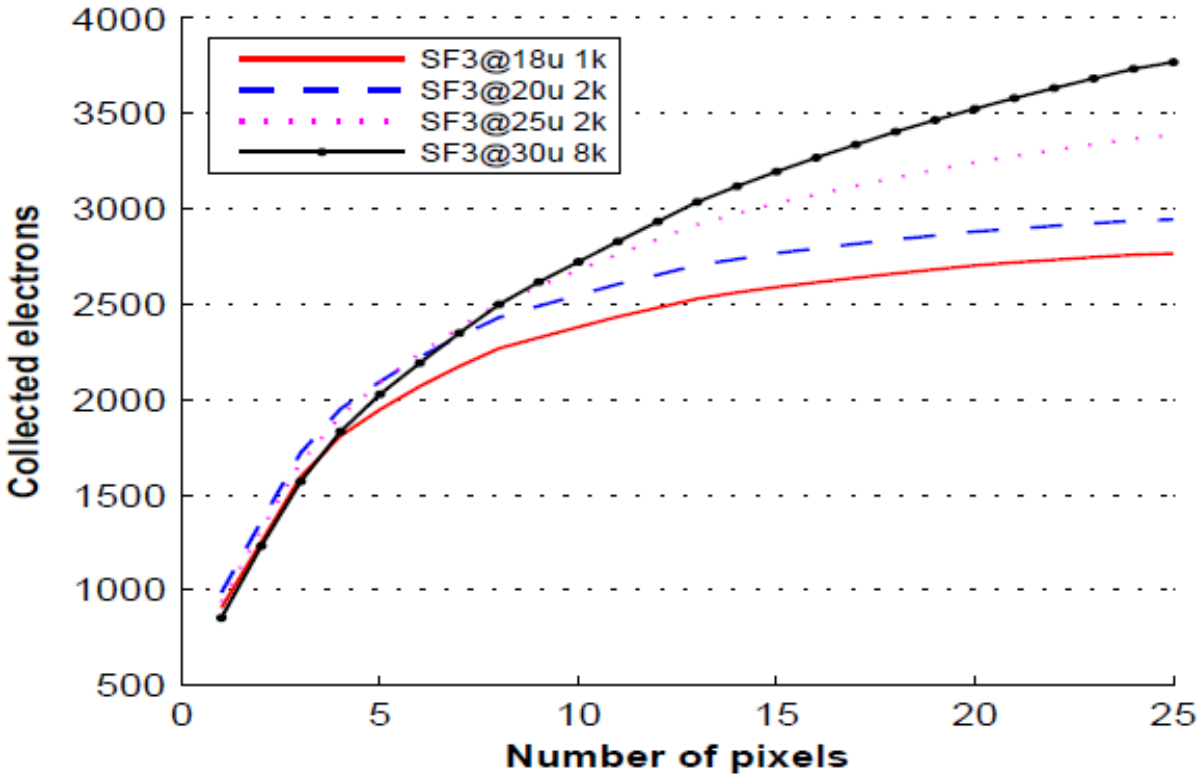
- **Pixel cluster with four different epitaxial layers**
  - With the same pixel structure (SFB3)



Total charge increases with the thickness and resistivity of the epi-layer, so the charge sharing → figure out an optimal configuration

Charge collection with non-ionizing damage

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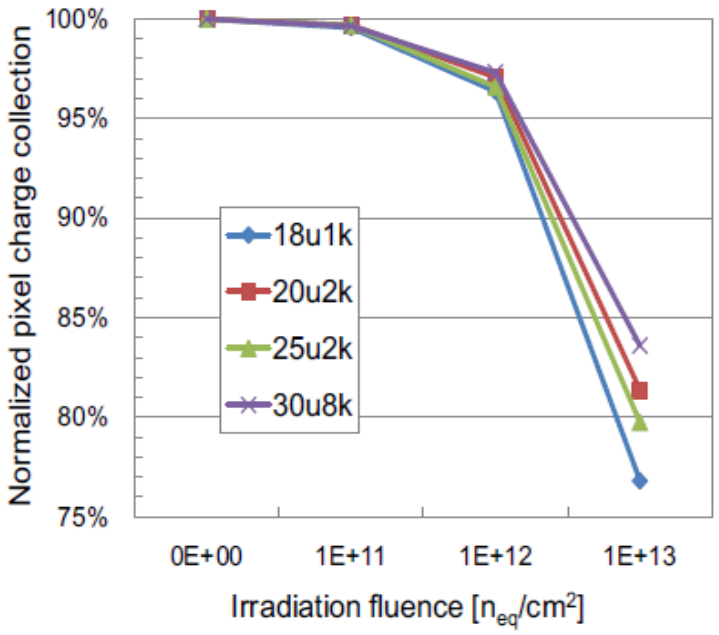
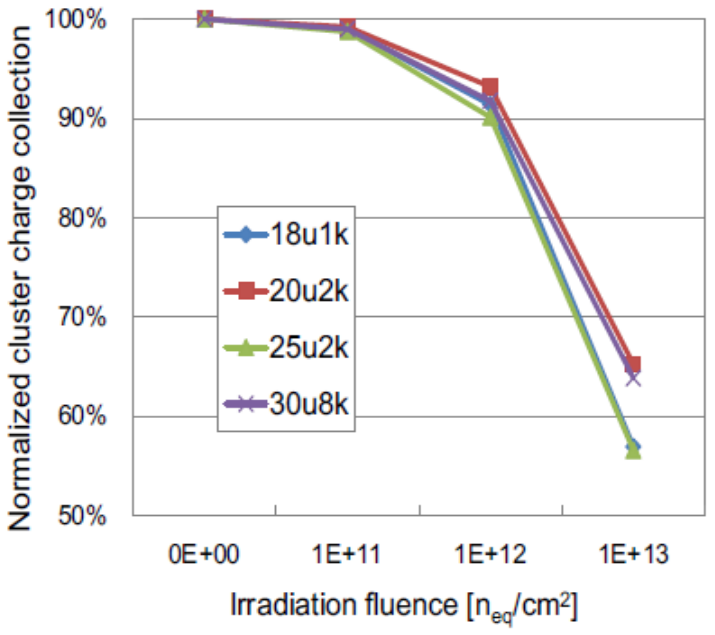
- **Charge collection efficiency decreased with radiation fluence**

Seed pixel



5 × 5 cluster



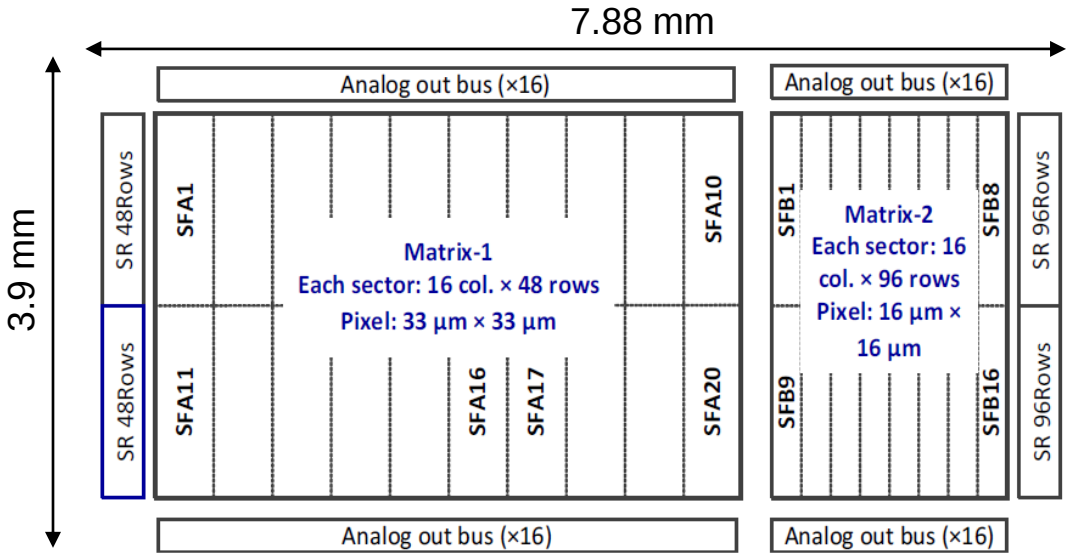
- **Charge collection remain ~ 80% and ~60% for seed and total pixels at CEPC annual fluence**
- Seed pixel: **higher resistivity → better radiation**
- Pixel cluster:
  - **25 μm thick epi-layer worse than 20 μm (same resistivity)→ charge sharing and radiation-caused-traps in a thicker epi-layer may degrade the performance**
  - **30 μm 8 kΩ similar to 20 μm 2 kΩ → advantage of high resistivity can be partly neutralized by thicker epi-layer**

First prototype design

- **Goal：sensing diode optimization and in-pixel pre-amplifier study**

  ➔ improves SNR ➔ enhances detection efficiency

- **Chip floor plan**
  - Contains two matrices, Matrix-1 with 33 × 33 μm^2 pixels (except SFA20), Matrix-2 with 16×16 μm^2 pixels. Each matrix includes 16 SF (source follower) blocks for sensor optimization
  - Matrix-1 includes 3 blocks with in-pixel pre-amplifier
  - SFA20 in Matrix-1 contains pixel with AC-coupled pixels

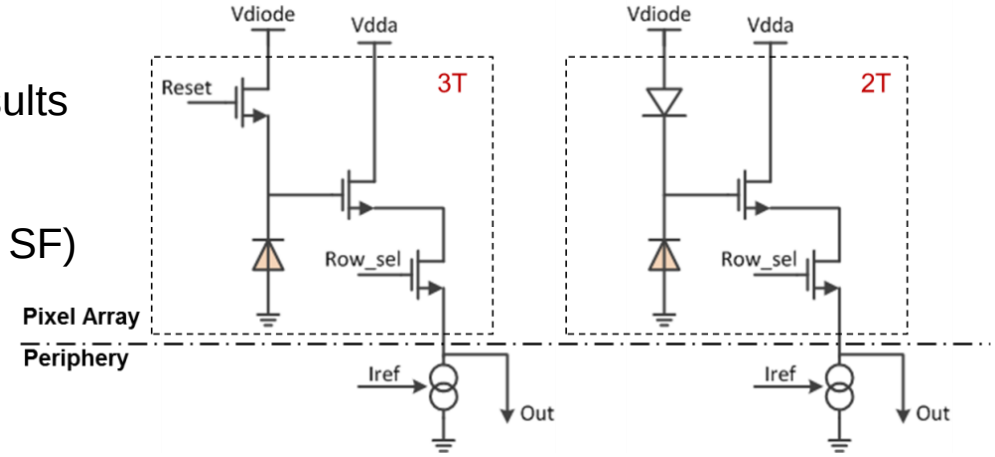


- First submission in TowerJazz 0.18 μm CIS process
- Two types of wafer:
  - 18 μm HRES epi wafer
  - 700Ω Czochralski wafer

First prototype design —— pixel structures

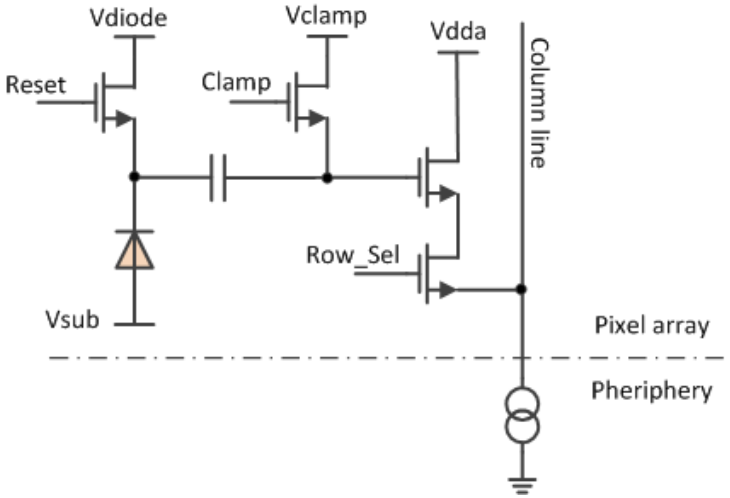
Y. ZHANG, Y. ZHOU

- **DC-coupled SF pixels: 2T/3T structure**
  - different diode geometries
  - ➔ to verify the TCAD simulation results
  - two biasing modes (2T/3T)
  - two transistor types (nmos/pmos SF)



- **AC-coupled pixel**
  - sensing node AC-coupled with circuit
  - diode bias voltage could be higher than power supply, i.e. up to 10 V
  - ➔ **larger depletion region & lower Cd**
  - ➔ **higher SNR**

AC-coupled structure



First prototype design —— pixel structures

Y. ZHANG

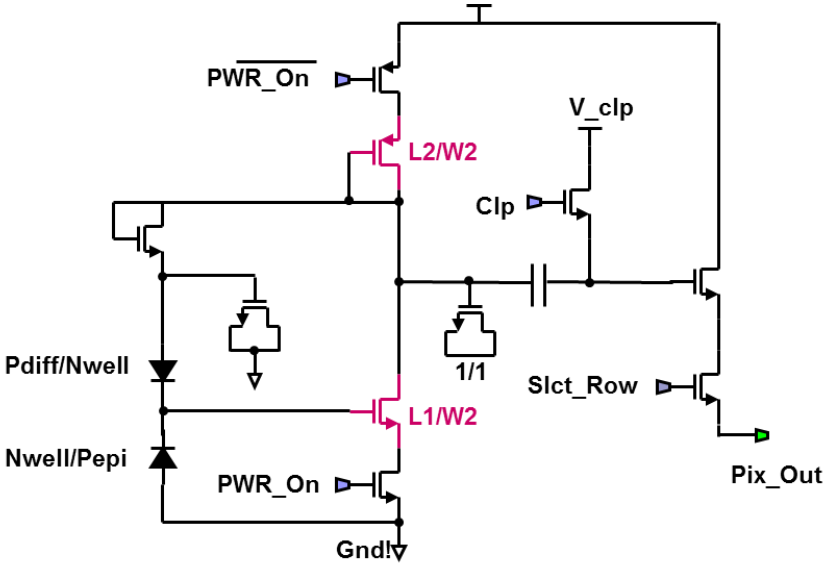
- **In-pixel pre-amplifier**
  - Common source amplifier with AC feedback, CDS in pixel
  - Only active when the row is selected to be read → power saving
  - Using a twin-well process only NMOS can be used, **while both types of transistors are used in our prototype**

Trade-off between :

✓ *Noise (TN, 1/f, RTS)*

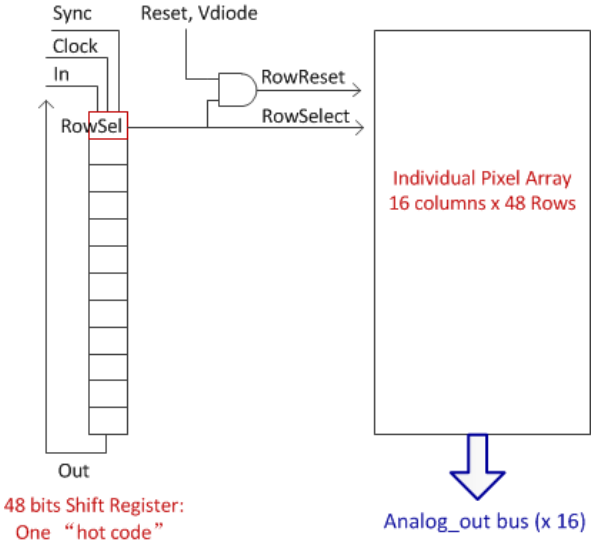
✓ *PSRR*

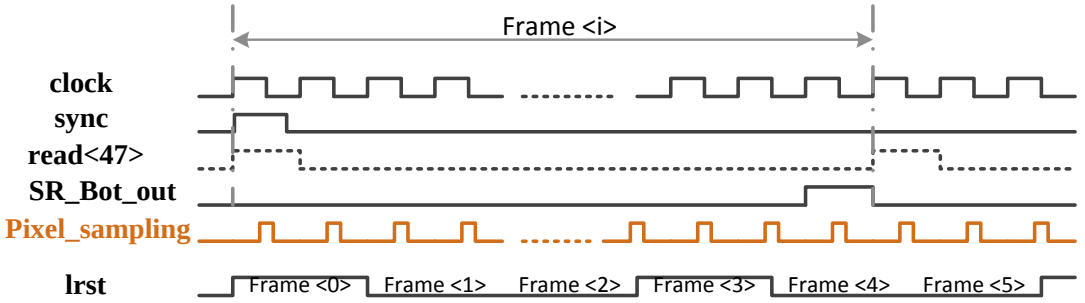
✓ *Diode Bias Voltage*



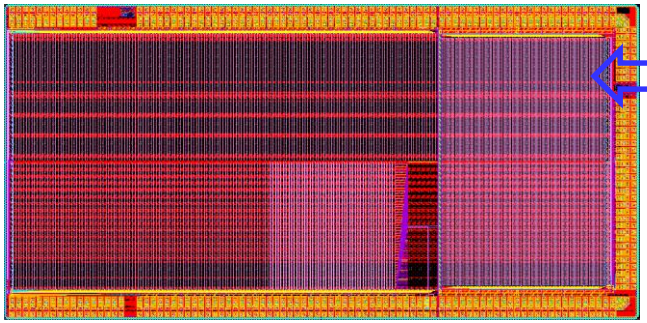
First prototype design —— readout

- **Pixel array steering：**
  - selecting one row, 16 columns read out in parallel
  - each row needs one clock cycle，readout time of a frame is 24 μs @ 2MHz



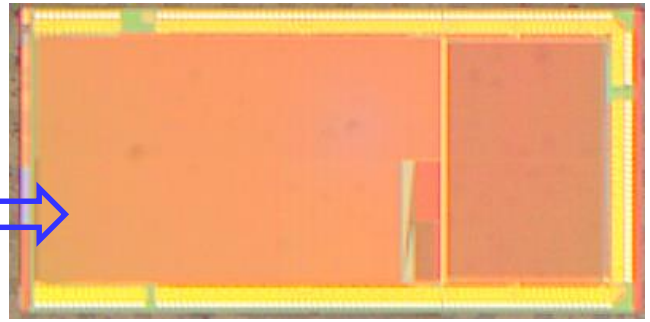


chip test in preparation



chip layout

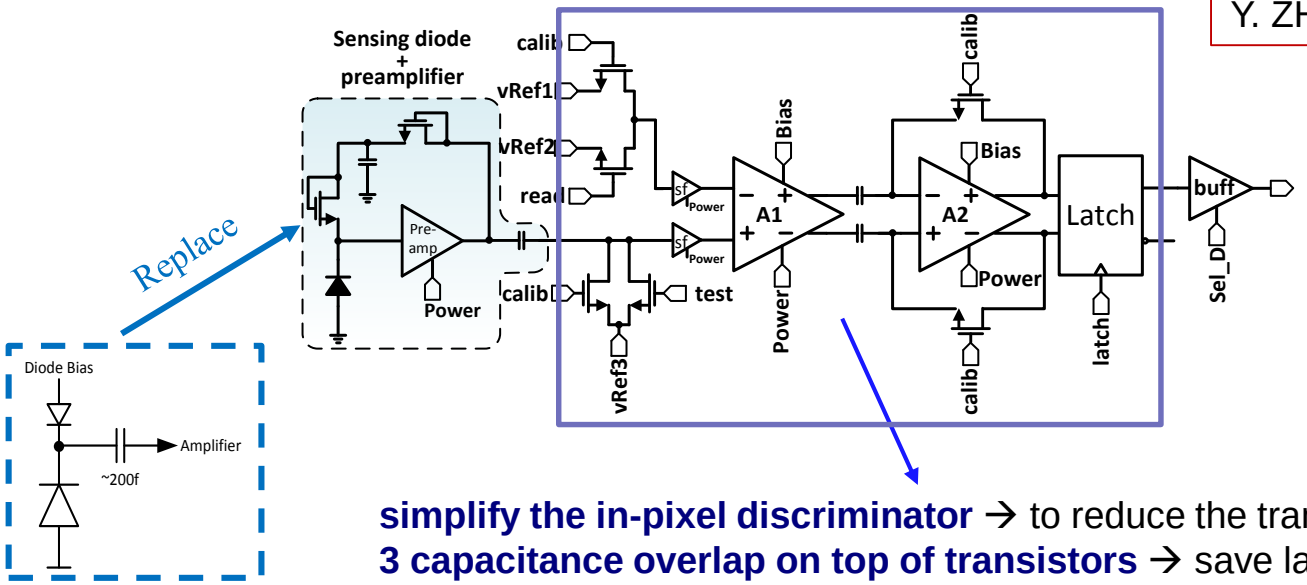
Chip photo



Next prototype design

- **Goal：small digital pixel design and characterization**
  - Signal digitized in pixel ➔ reduce power consumption
  - Minimize pixel size in the current process (0.18 μm), i.e. ~20 μm pitch
- **A preliminary proposal for the pixel design**
  - Based on the ASTRAL pixel configuration
  - Keep in-pixel discrimination & rolling shutter readout mode, depleting the sensor, simplify the in-pixel circuitry design to shrink the pixel size

Y. ZHOU, Y. LU, C. HU



simplify the in-pixel discriminator → to reduce the transistor num.
3 capacitance overlap on top of transistors → save layout space

Summary and outlook

- **To address the challenges from the CEPC vertex detector, R&D of the CMOS pixel sensors is proceeding**

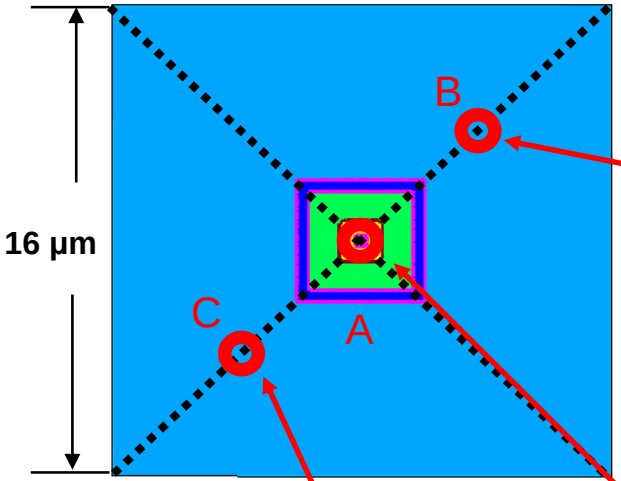
- **Performed preliminary TCAD simulation to understand the impacts on charge collection, including:**
  - collection diode geometry
  - epitaxial layer
  - non-ionizing radiation damage

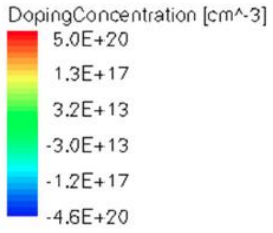
- **First prototype designed and fabricated in the TowerJazz 0.18 μm CIS technology**
  - Sensor characterization expected this year and TCAD simulation results to be verified with measurement
- **Second submission expected this November, targeting on the design of small size digital pixels**

Thanks for your attention !

Charge collection vs. hit position

- **The symmetrical pixel model makes the charge collection distribution symmetrical**
  - Two different hit positions selected in the following simulations (A, C)





integrating current