July 15, 2016@IHEP

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Discussion Items

Technology

- Is present SOI Pixel process good enough?
  Radiation Hardness, Circuit Density, Leakage Current, Design Rule,,,
- Is frequency of MPW run adequate?
- Do you need 3D integration to fulfill your requirements?
  Attach anther digital chip of fine process, CdTe, Ge, …
- Do we need faster readout board?
  SEABAS3?

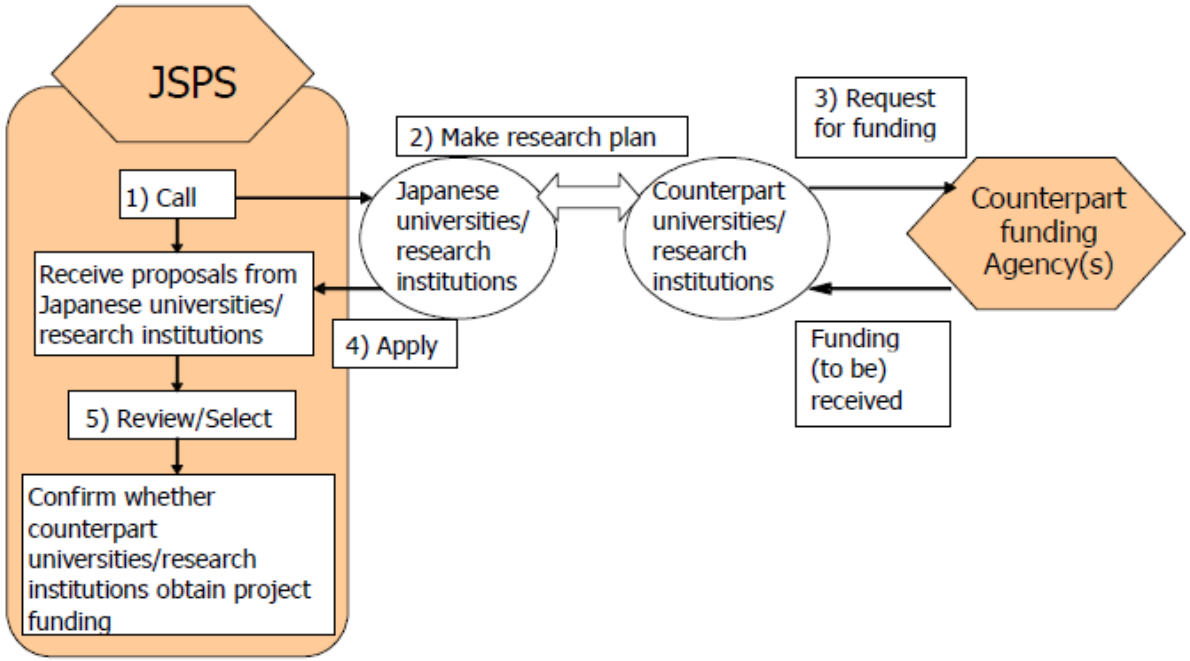
Collaboration

- Budget
  How to get R&D/Project money?
- People
  How to recruit people? What kind of person do we need?
  Exchange Researchers?
- Collaboration Item
  How to share Design, Evaluation of chip, Radiation Test,
  Beam Test, Back side process, SPICE model, Library,,,,
- Meeting
  How often do we need meeting?
  Regular Video meeting, Workshop, Short term stay,,,

An Example of Collaboration Budget

JSPS Core-to-Core Program: Advanced Research Networks

* Object: Create world-class research hubs in research fields considered to be cutting-edge. Fostering the next generations of trailblazing young researchers
* Eligible Countries: At least two or more countries that have diplomatic relations with Japan.
* Japanese Funding: \18M Yen(1M RMB)/year
* Application Deadline: 6th Oct. 2016
* Period: 3~5 year



2nd International Workshop on SOI Pixel Detector (SOIPIX2017)