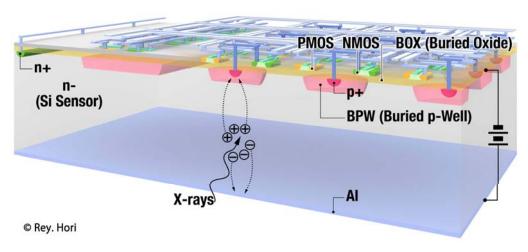
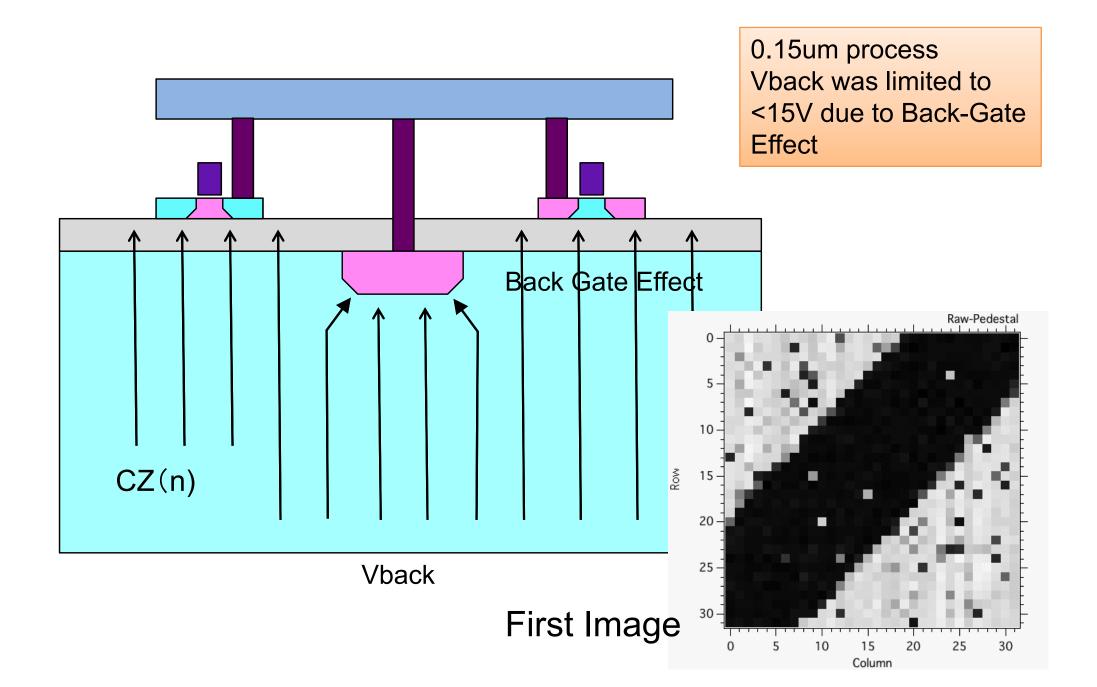


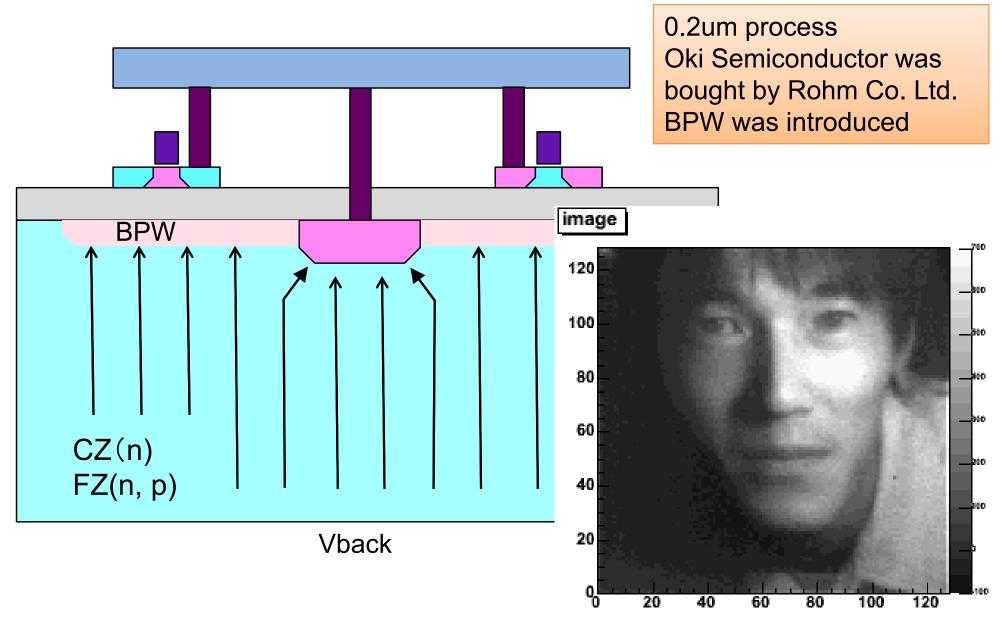
外形

- I. Short History of SOIPIX
- II. Introduction of SOI Pixel Process
- III. Recent Progress
- IV. Detector Developments
- V. Summary



2006

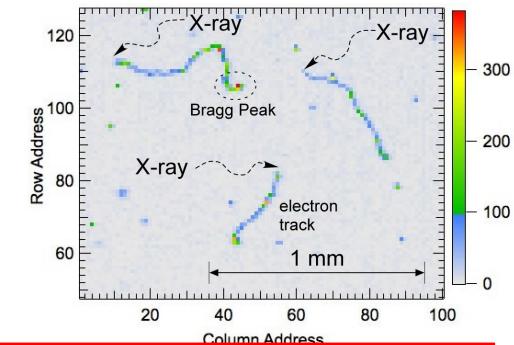


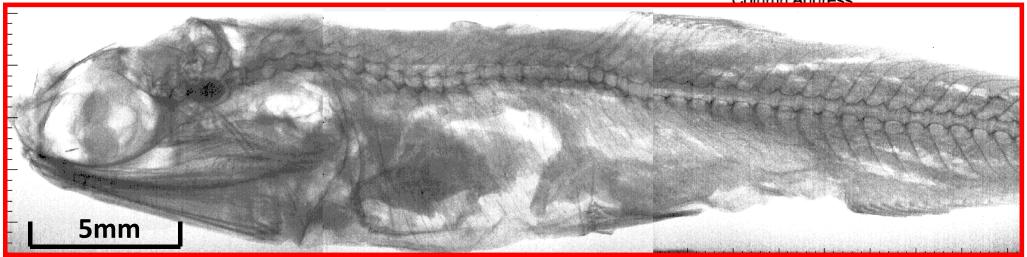


History of SOIPIX

2010~11

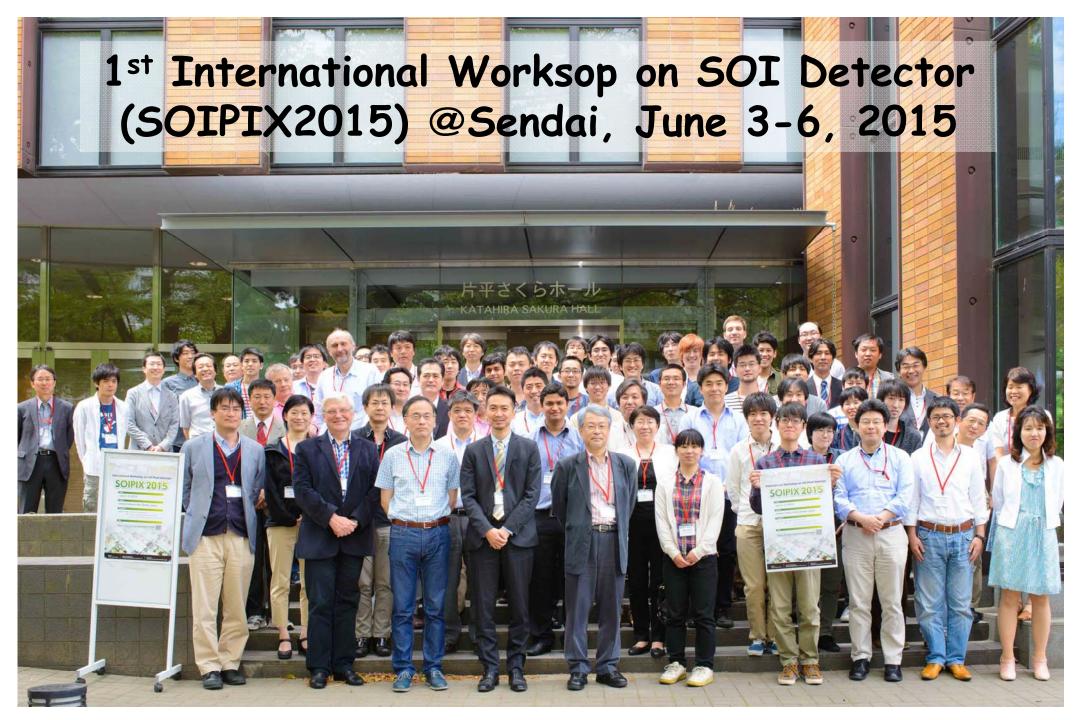
SOI Pixel (INTPIX4)
Pixel Size: 17 um x 17 um
No. of Pixel: 512 x 832 (= 425,984)
Chip Size: 10.3 mm x 15.5 mm
Vsensor=200V, 250us Int. x 500
X-ray Tube: Mo, 20kV, 5mA



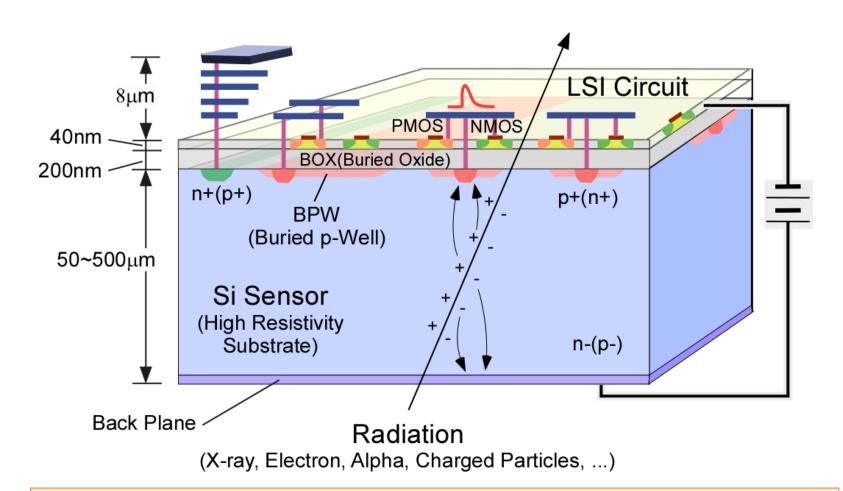


X-ray Image of a small dried sardine taken by a INTPIX4 sensor (3 images are combined).





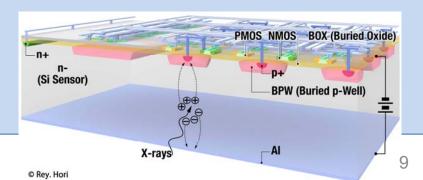
II. Silicon-On-Insulator Pixel Detector (SOIPIX)



Monolithic Detector having fine resolution of silicon process and high functionality of CMOS LSI by using a SOI Pixel Technology.

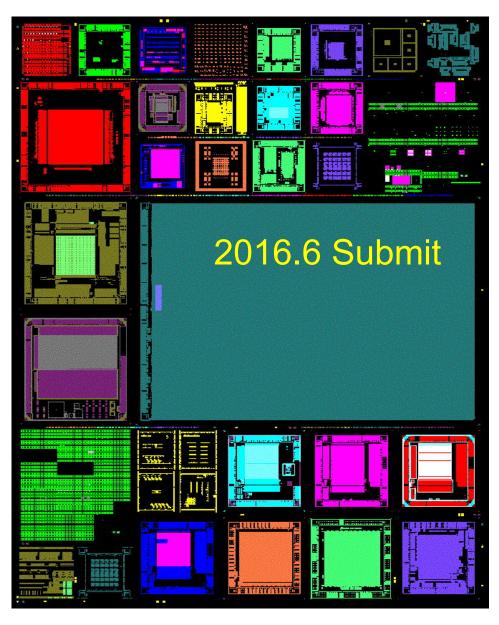
Features of SOI Pixel Detector

- Monolithic device. No mechanical bonding.
- Fabricated with semiconductor process only, so high reliability and low cost are expected.
- High Resistivity fully depleted thick sensing region with Low sense node capacitance.
- On Pixel processing with CMOS transistors.
- 100% Fill-Factor with Back Illumination.
- No Latch up and Low single event cross section.
- Can be operated in wide temperature (1K-570K) range.
- Based on Industry Standard Technology.



Multi-Project Wafer (MPW) run.



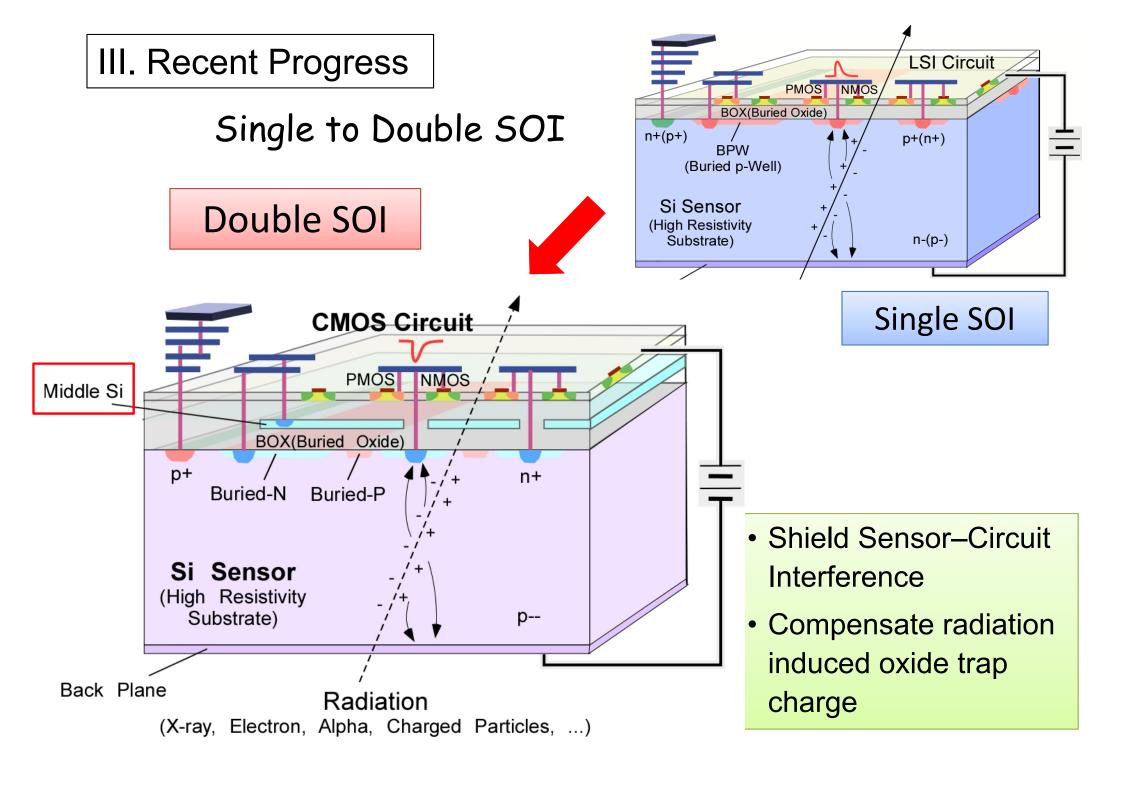


30 design

Lapis (*) Semiconductor 0.2 µm FD-SOI Pixel Process

Process	0.2μm Low-Leakage Fully-Depleted SOI CMOS 1 Poly, 5 Metal layers. MIM Capacitor (1.5 fF/um²), DMOS Core (I/O) Voltage = 1.8 (3.3) V
SOI wafer	Diameter: 200 mm ϕ , 720 μ m thick Top Si : Cz, ~18 Ω -cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz (n) ~700 Ω -cm, FZ(n) ~7k Ω -cm, FZ(p) ~25 k Ω -cm etc.
Backside process	Mechanical Grind, Chemical Etching, Back side Implant, Laser Annealing and Al plating

^(*) Former OKI Semiconductor Co. Ltd.

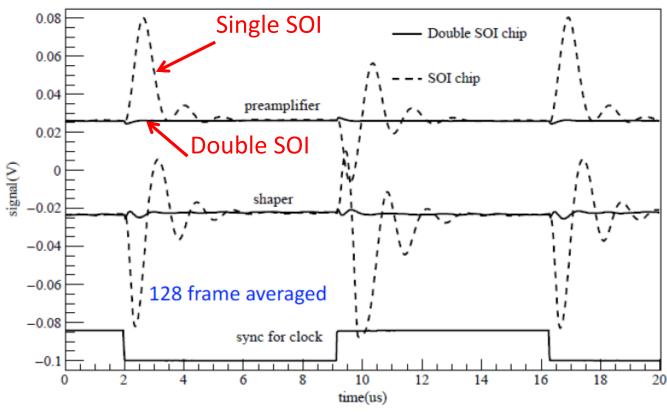


Cross section of the Double SOI Pixel Middle Si Middle Si Metal 1 Contact Transistor Sensor Contact x9.0k TE 12/10/16 3.00µm

- Crosstalk from counter, pixel(0,63)
 - 5mV @ shaper output for DSOI (74 e⁻ referred to input charge), neg
 when superimposed with noise (ENC ~ 113e⁻)
 - 95mV for normal SOI (note the gain of shaper reduced)
 - Compelling proof of shielding effectiveness

By using Double SOI wafer, Coupling between Circuit and Sensor is reduced to 1/20.

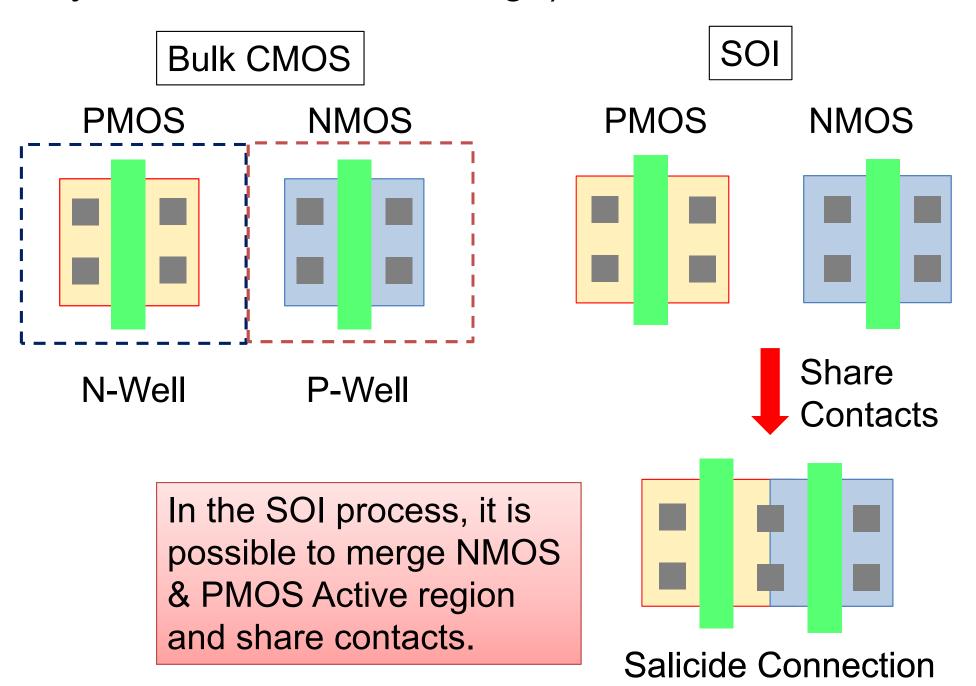
(Lu Yunpeng @SOIPIX2015)



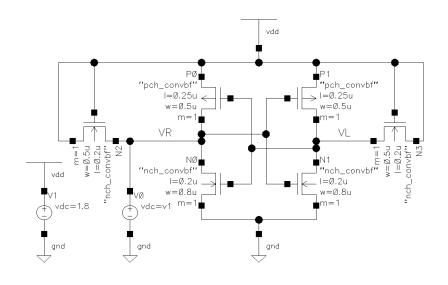
	Double-SOI	Normal SOI
Preamp output(peak to peak)	3.7mV	60mV
Shaper output(peak to peak)	5mV	100mV

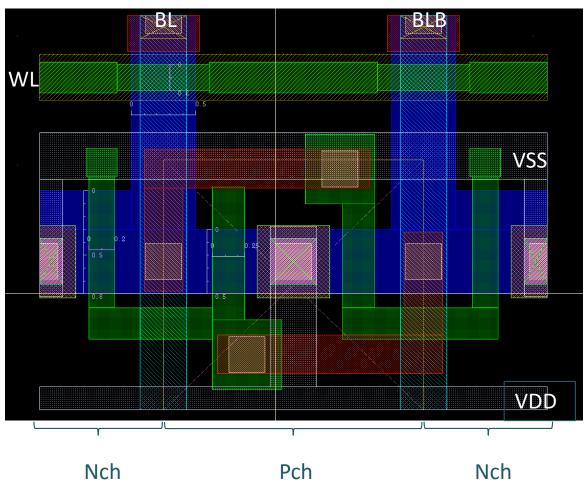
SOIPIX2015, June 2-6, 2015, Sendai

Layout Shrink (Active Merge)



Single Port SRAM Bit Cell

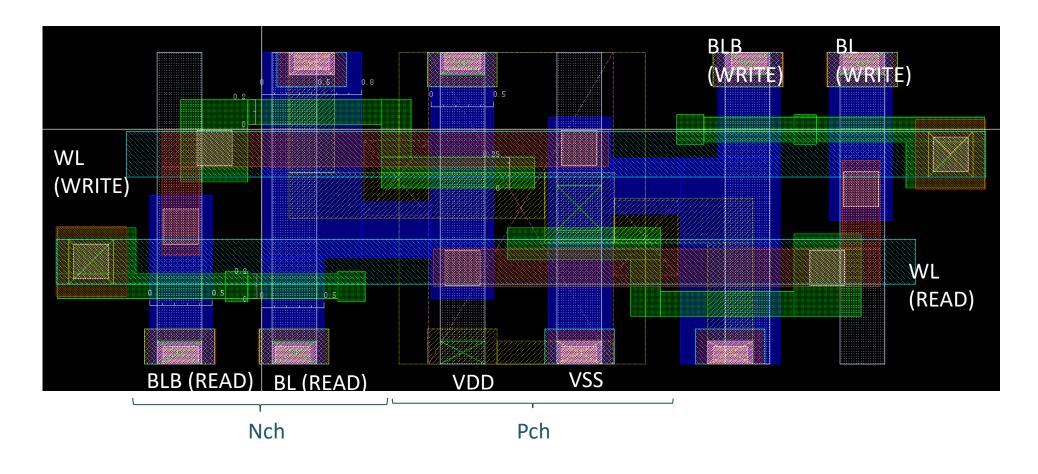




Cell Size : $3.94\mu m\ X\ 3.06\mu m = 12.06\mu m^2$

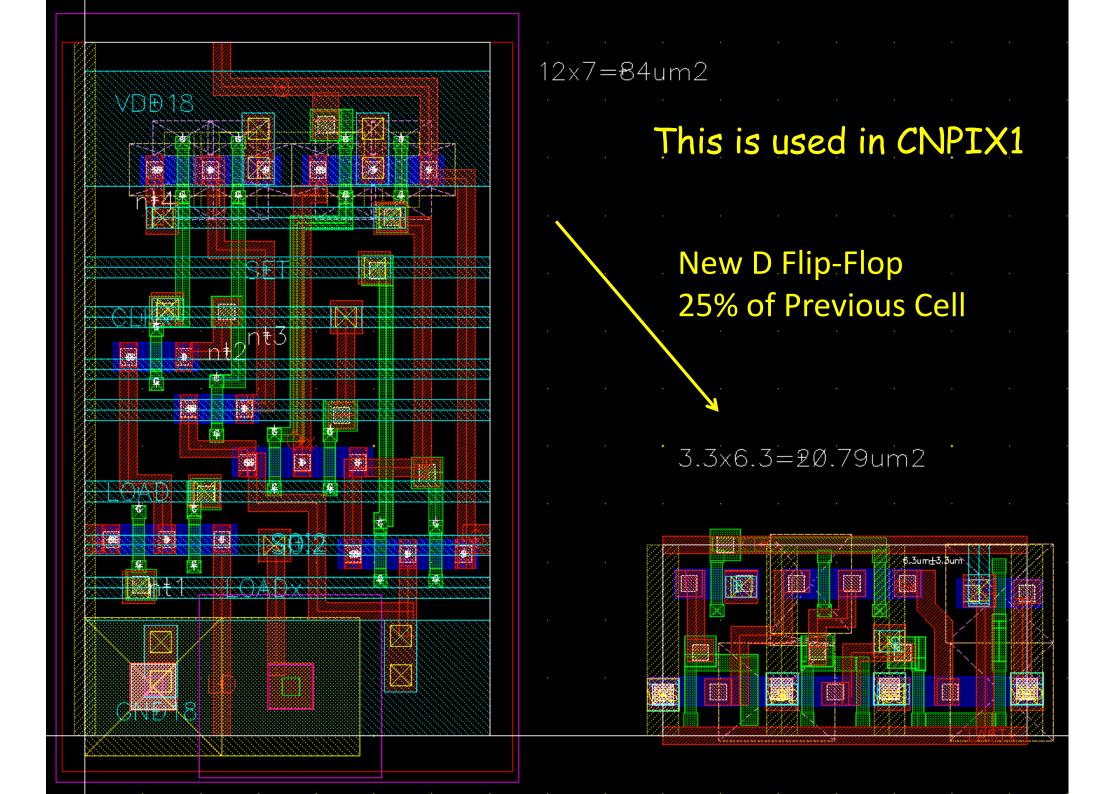
(designed by I. Kurachi)

Dual Port SRAM Bit Cell



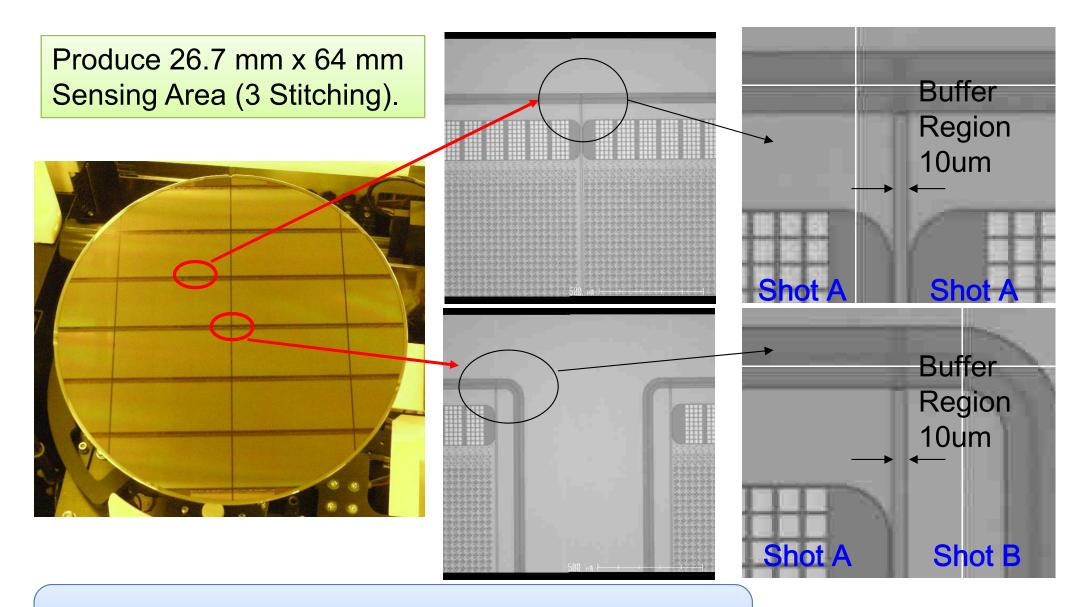
Cell Size : $6.90 \mu m \ X \ 2.50 \mu m = 17.25 \mu m^2$

(designed by I. Kurachi)



Stitching Exposure for Large Sensor

SOPHIAS by RIKEN

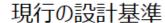


- Width of the Buffer Region can be less than 10um.
- Accuracy of Overwrap is better than 0.025um.

設計基準改良案(マスクイメージ)

New Stitching Rule



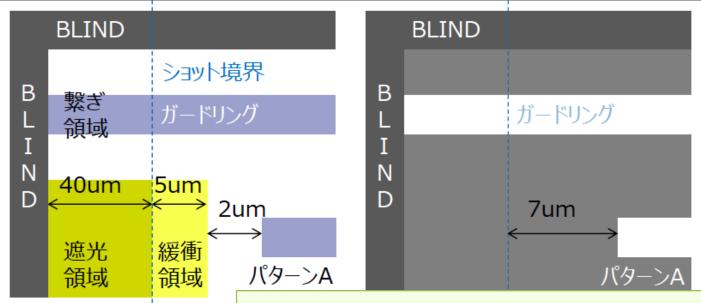




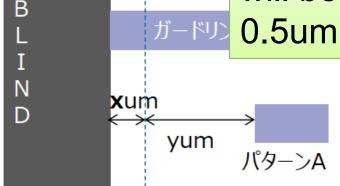
改良版設計基準案

x:0.3um (ARの合わせずれが ショット境界を超えない)

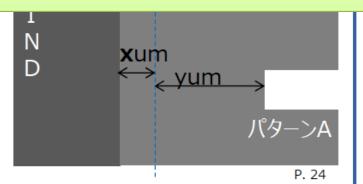
y: 0.5um (Scanner) 3.0um (Wide)



Minimum Distance between Stitching edge to Transistor will be reduced from 7um to 0.5um



BLIND



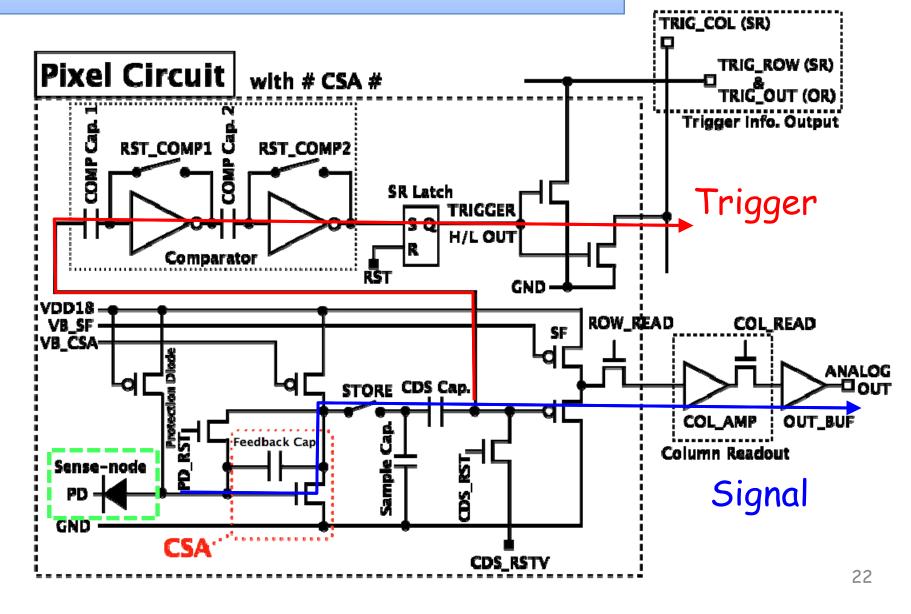
© 2016 LAPIS Semiconductor Miyagi Co., Ltd.

IV. Detector Developments

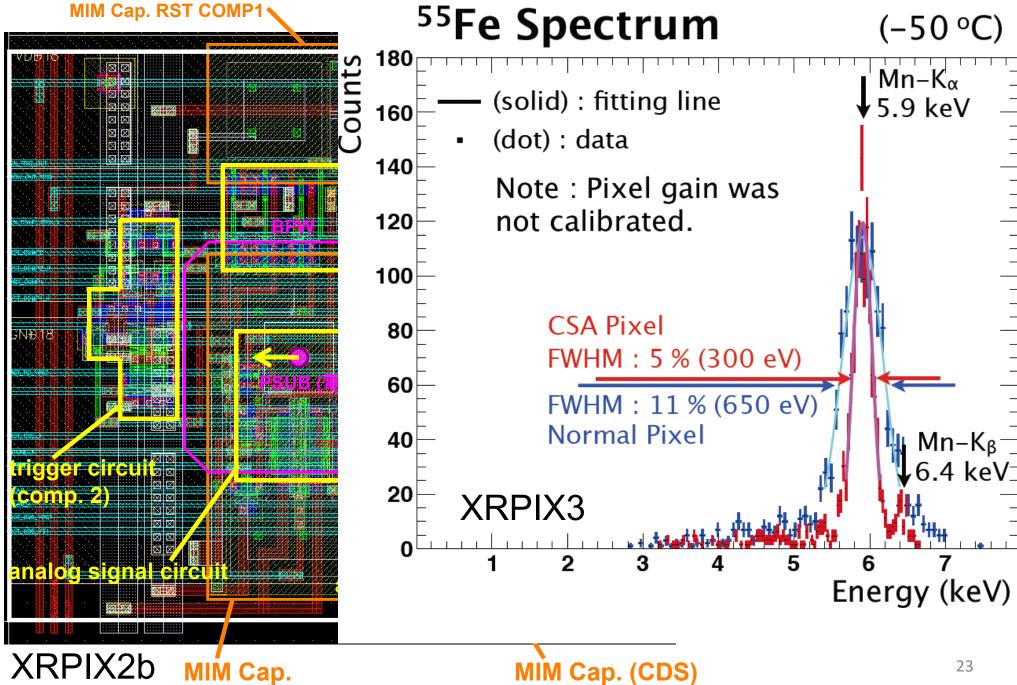
- Integration Type Pixel (INTPIX)
 - → Nishimura's Talk
- Counting-type pixel (CNPIX)
 - → Yunpeng, Arai's Talk
- Vertex Detector for Charged Particles (SOFIST)
 - → Ono, Yamada's Talk
- X-ray Detector for Astrophysics (XRPIX)
- XFEL detector(SOPHIAS)
 - (→ Hashimoto's Talk)

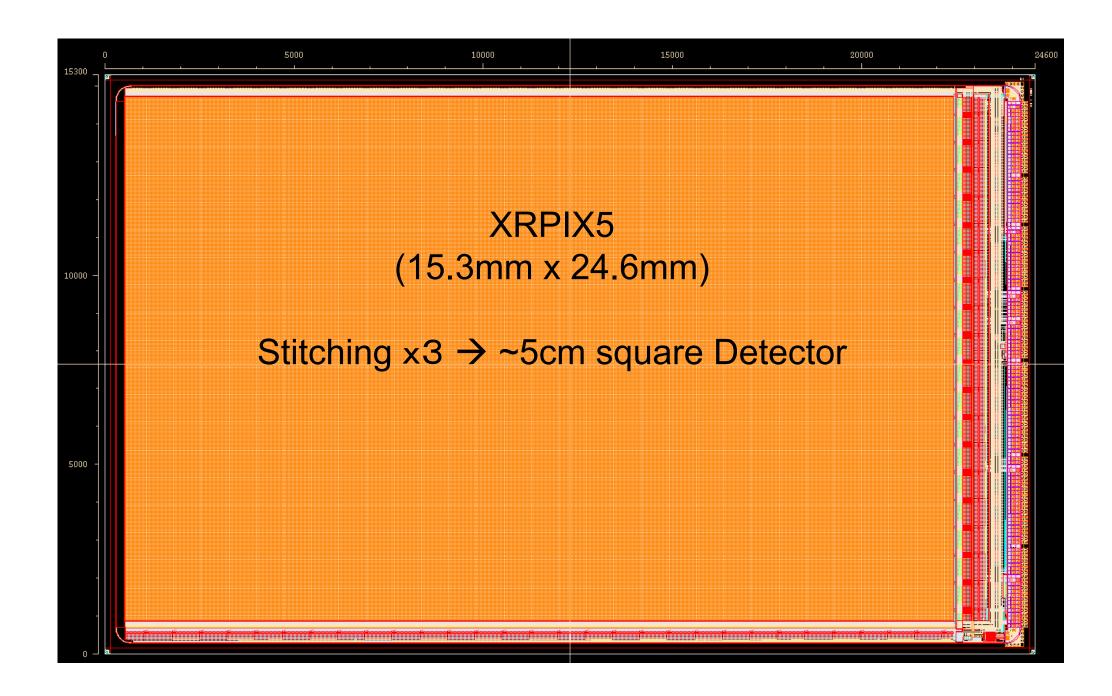
XRPIX (SOI Pixel sensor for X-ray Astronomy)

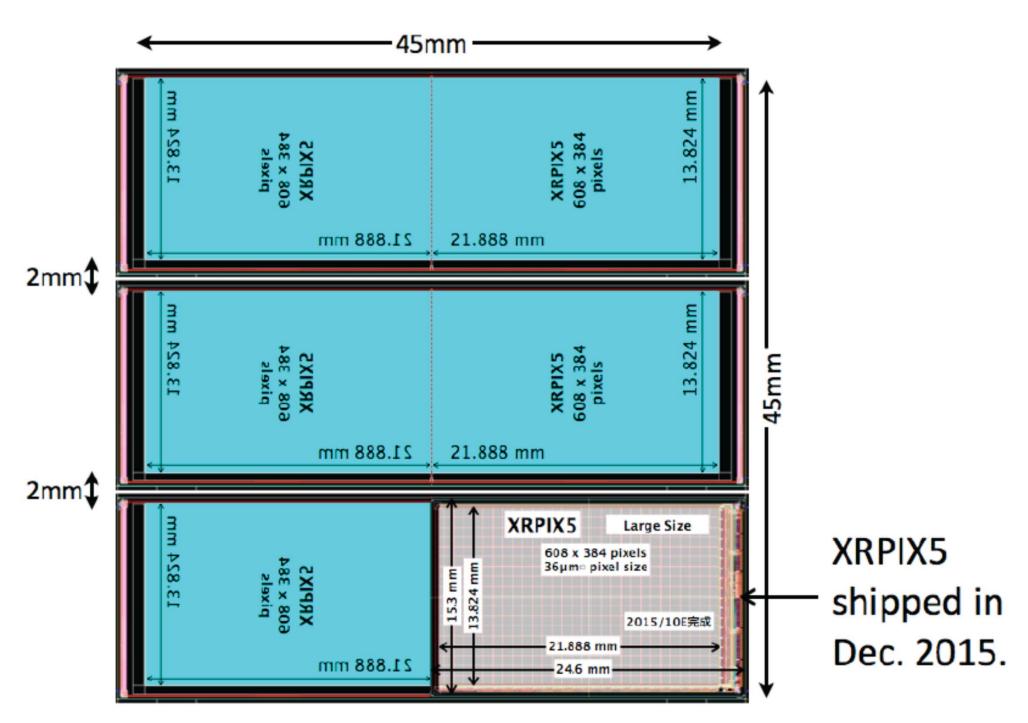
- Generate Trigger signal when a hit is occurred.
- Then X- and Y- addresses of the hit are sent out.



Pixel Layout







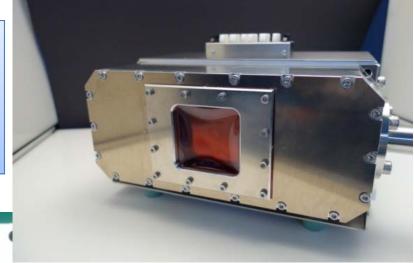
SOI Photon-Imaging Array Sensor (SOPHIAS) for X-ray Free Electron Laser (XFEL) SACLA

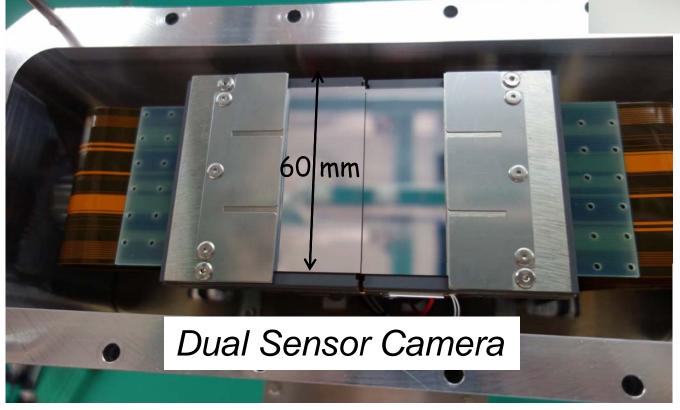




Utilization of SOPHIAS has been started for various experiments in SACLA@RIKEN.

- Dynamics of Atomic Structure
- Direct Observation of Chemical Reactions
- etc.



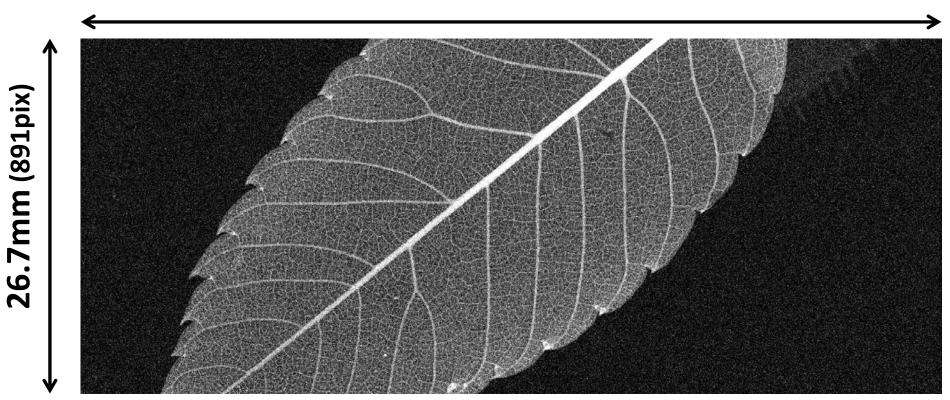


Easy

Beautiful

Pix size: 30um × 30um

High gain Image! 64.8mm (2160 pix)



22kV 200uA Target Cu Kα 8keV 1000 shot averaged

1.9M pixels !!

0.5 photon/pix/shot

摘要

- Technology of SOI Pixel become mature, and a few detectors are already used in real experiments.
- Furthermore, many development plans are on going.
- Layout size of pixel can be shrunken by using NMOS/PMOS active merge technique.
- Dead area of Stitching can be reduced in new rule.
- Radiation hardness is improved with double SOI and high dope LDD (→ Kurachi's Talk)
- However, we are still lack of manpower (design, evaluation, camera system etc.), so strengthen the China-Japan collaboration is very important.