Radiation hardness improvement of FD-SOI MOSFETs for X-ray detector application

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Introduction

FD-SOI is suitable structure for monolithic charged particle image sensor.
However, radiation tolerance of FD-SOI MOSFET is generally lower than that of bulk-CMOS in total ionizing dose effect (TID).

How low? Any improvement ?

0.2 μm FD-SOI X-ray Sensor Process is based on FD-SOI process for ultralow power operation not for radiation hardness.

We have chance to find some room to improve radiation tolerance by analyzing mechanisms of radiation damage of FD-SOI MOSFET in detail.

Target radiation tolerance: >1 MGy

LHC pixel : ~ 500 kGy, 10^{15}neq/cm^2@ATLAS (*x*10 for HL-LHC)
Belle-II : ~ 10 kGy/y, 2x10^{12}neq/cm^2 /y
ILC (e.g., ILD @ *r*=15 mm) : ~ 1 kGy/y, ~10^{11}neq/cm^2 /y
X-ray imaging: : kGy/y ～MGy/y

Experimental Procedure

Lapis Semi. 0.2 μm FD-SOI X-ray Sensor Process

Nch LDD Condition

ULP-LDD : X1

RH-LDD : X2.5

Pch LDD Condition

ULP-LDD : X1

RH-LDD : X6

X-ray irradiation

Molybdenum Target with acceleration voltage of 40 kV

0.5 mm Aluminum filter to suppress X-ray below 10KeV

Dose rate : 0.018 or 3 Gy(Si)/s

All terminals of MOSFETs are grounded during irradiation

In detail, refer to T. Kudo et al., IEEE Trans. Nucl. Sci. 61 (3), pp. 1444-1450, 2014.

MOSFET

RADTEG

BF W=10 μm L=0.2/0.3/0.5/1.0/10 μm core Normal Vt （I-V）

BT W=5 μm L=0.2/1.0 μm core Normal Vt (Charge Pumping)

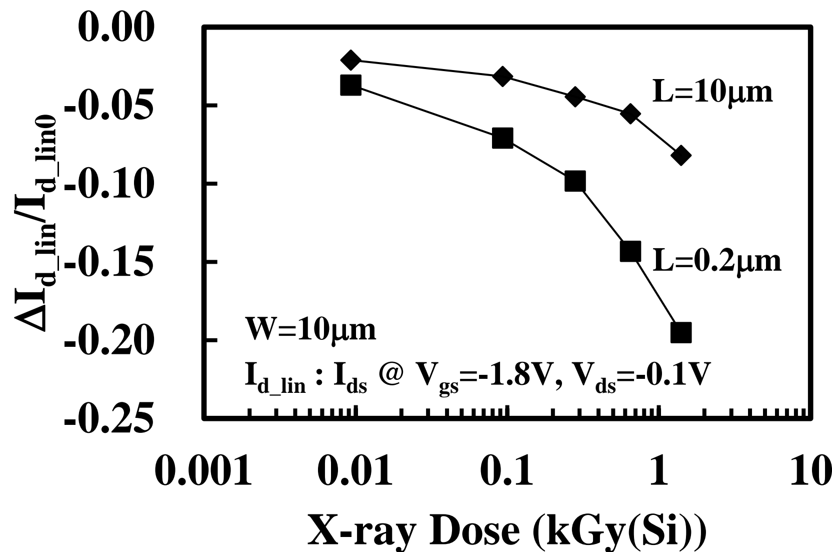
I_{ds_lin} : Vds=0.1V, Vgs=1.8V, Ids_sat : Vds=1.8V, Vgs=1.8V

V_{to} : extrapolated from Id-Vg @ Vds=0.1V around gm_max points

Charge Pumping : f=1MHz, tr=tf=1nS, duty 50%, delta Vg=1.5V, $N_{it}=I_{cp}/qSf$

PMOS Drain Current Degradation due to RIGLEM

- Linear drain current degradation of shorter gate length MOSFET is faster than that of longer gate length MOSFET.
- Drain current degradation is mainly caused by Radiation Induced Gate LEngth Modulation (RIGLEM) not Vt shift nor mobility reduction.



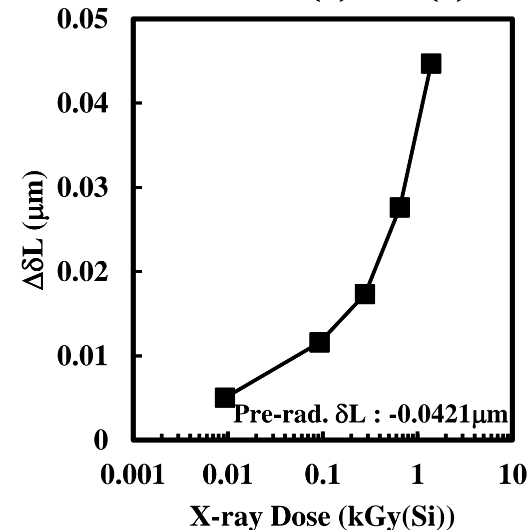
Dose Rate : 0.018 Gy(Si)/s

Terada's method

$$R_m = \rho_{ch}\frac{L_{eff}}{W_{eff}} + (R_s + R_d)$$

$$L_{eff} = L + \delta L$$

$$\Delta\delta L = \delta L(x) - \delta L(0)$$

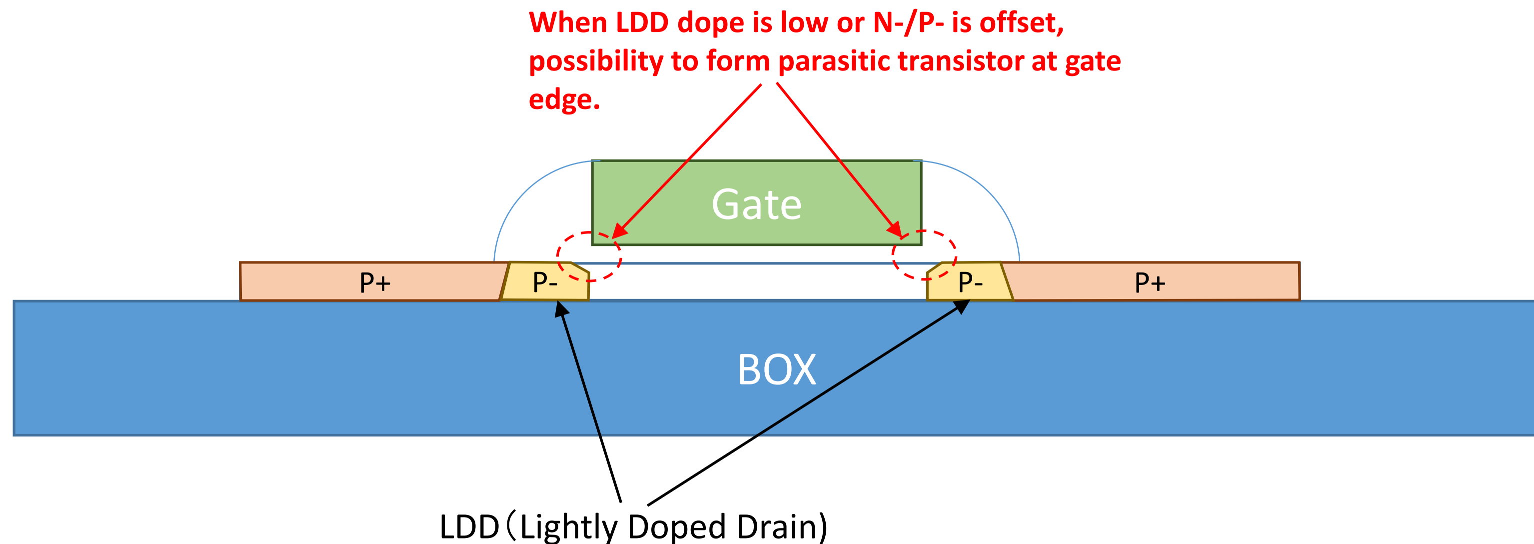


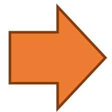
In detail, please refer to

I. Kurachi et al., "Analysis of Effective Gate Length Modulation by X-Ray Irradiation for Fully Depleted SOI p-MOSFETs," IEEE Trans. Electron Devices, Vol. 62, No. 8, pp. 2371-2376, 2015.

Possible Cause of RIGLEM

- Drain current degradation due to RIGLEM has gate length dependence. Thus, the cause must be located at gate edges.
- SOI MOSFET is designed for ultralow power operation. To reduce off-leakage by GIDL, the LDD dope is low. LDD may be slightly offset from gate.
- Formation of parasitic transistors at gate edges and positive charge generation in sidewall spacer are the most possible causes!!

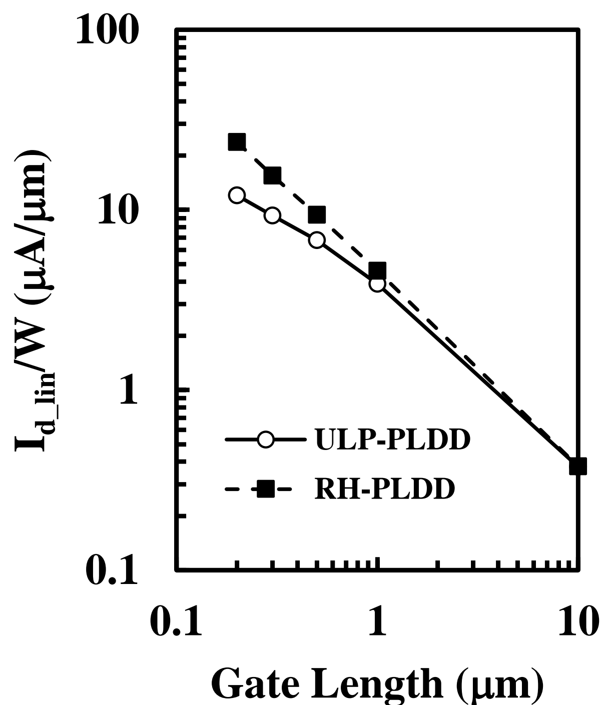


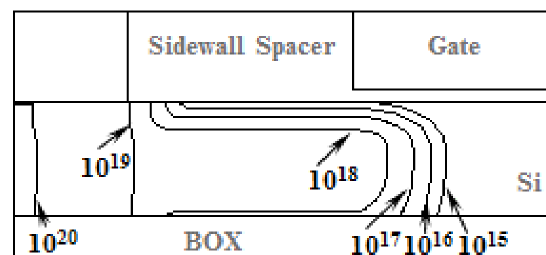


If so, higher LDD dose must be a solution to eliminate RIGLEM.

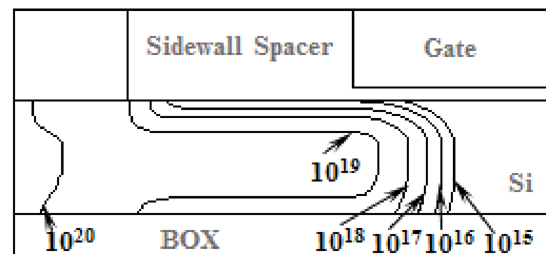
Elimination of Gate Offset by Higher LDD Dose (Pch)

- High dose LDD : RH-LDD is 6 time high dose of ULP-LDD
- Improvement of linearity between gate length and drain current by RH-LDD is confirmed.
- Higher boron concentration underneath gate for RH-LDD is also confirmed using TCAD.
- “offset” structure can be eliminated by using RH-LDD.





(a) ULP-PLDD



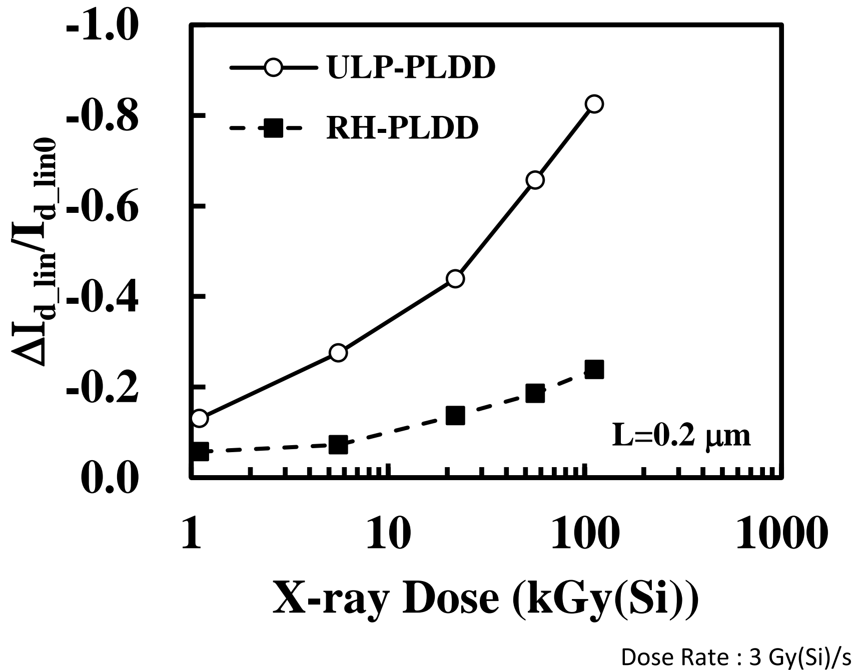
(b) RH-PLDD

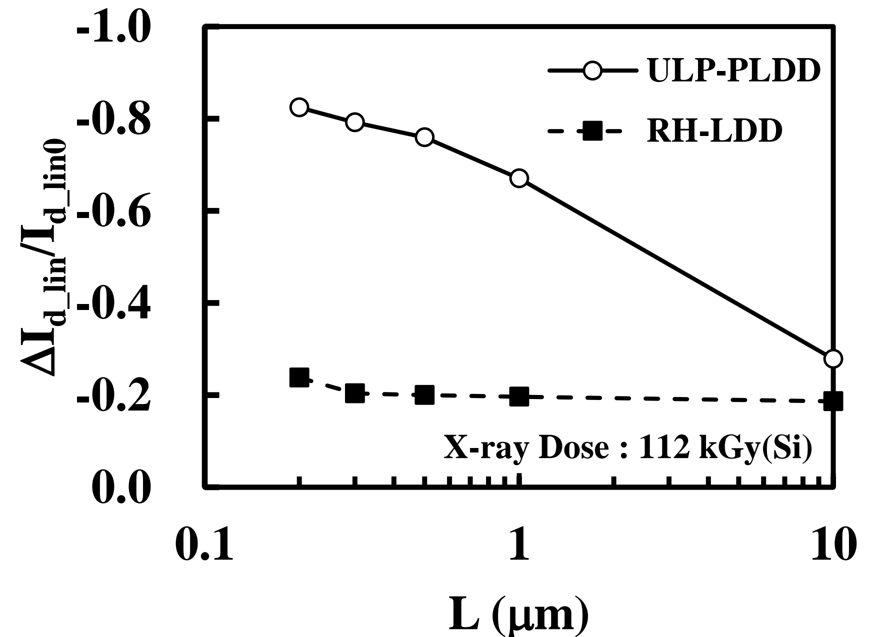
Boron concentration distribution

I. Kurachi et al., “Tradeoff Between Low-Power Operation and Radiation Hardness of Fully Depleted SOI pMOSFET by Changing LDD Conditions,” IEEE Trans. Electron Devices, Vol. 63, No. 6, pp. 2293-2298, 2016.

Radiation Tolerance Improvement by RH-LDD

- Drain current degradation improvement : 80 to 20% after 112kGy irradiation by ULP-LDD to RH-LDD.
- Almost no gate length dependence of drain current degradation when RH-LDD is used.
- Radiation hardness improvement by RH-LDD is confirmed.
- Radiation degradation is mainly caused by Vt shift of parasitic MOSFET at gate edges due to generated positive charge in sidewall spacer.



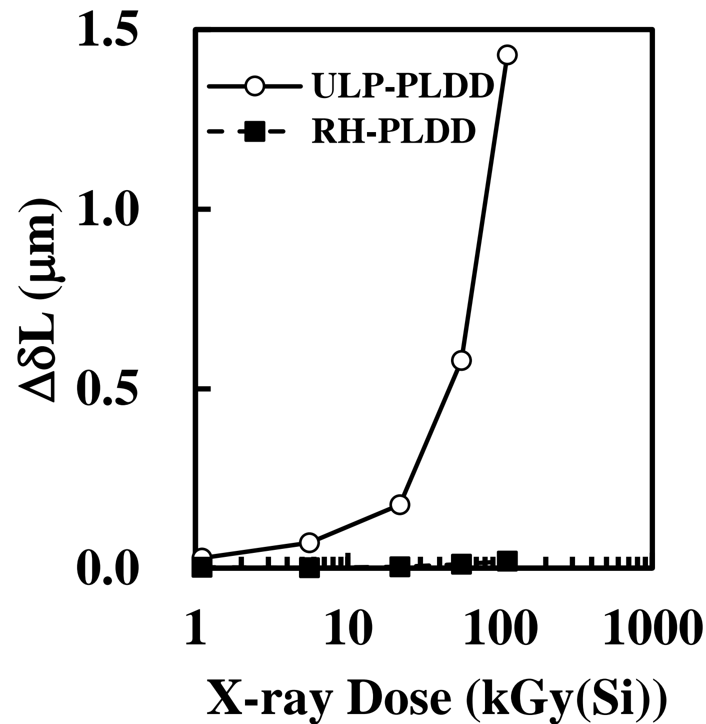


Dose Rate : 3 Gy(Si)/s

I. Kurachi et al., "Tradeoff Between Low-Power Operation and Radiation Hardness of Fully Depleted SOI pMOSFET by Changing LDD Conditions," IEEE Trans. Electron Devices, Vol. 63, No. 6, pp. 2293-2298, 2016.

Improvement for Gate Length Modulation

- For RH-LDD, no or less gate length modulation is observed.
- High LDD dose improves offset gate structure and eliminates RIGLEM. Consequently, improve radiation hardness and reduce gate length dependence of drain current degradation.



Dose Rate : 3 Gy(Si)/s

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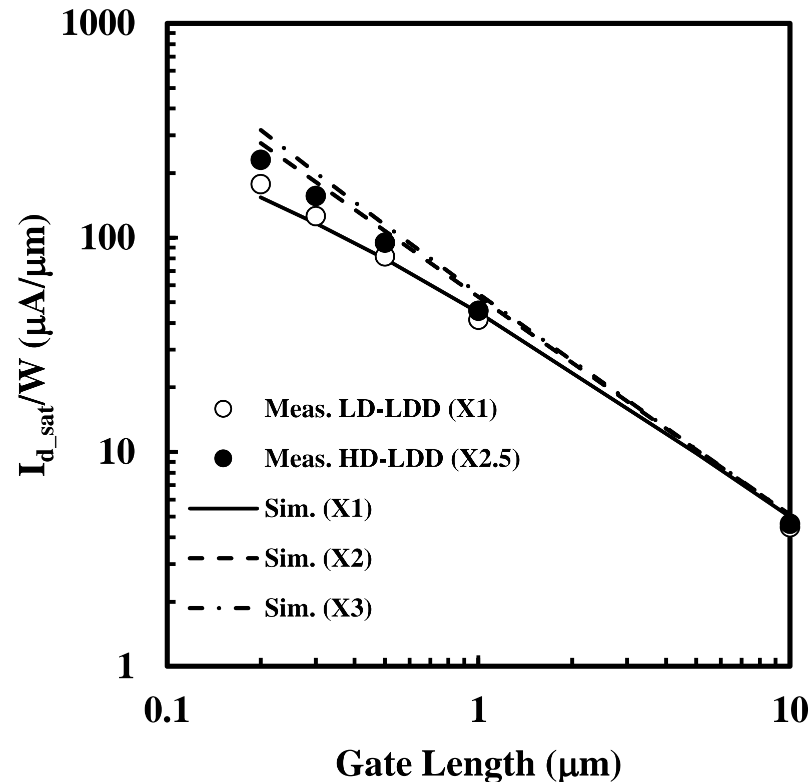
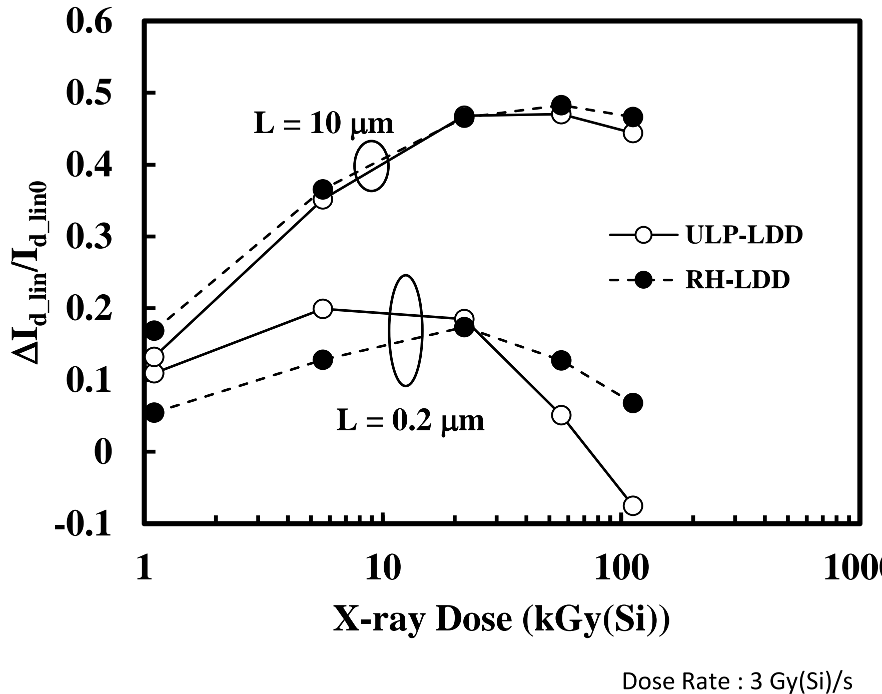
Elimination of Gate Offset by Higher LDD Dose (Nch)

- High dose LDD : RH-LDD is 2.5 time high dose of ULP-LDD
- Improvement of linearity between gate length and drain current by RH-LDD is confirmed.
- X2 LDD dose is enough to eliminate gate offset from TCAD results.
- "offset" structure can be eliminated by using RH-LDD.

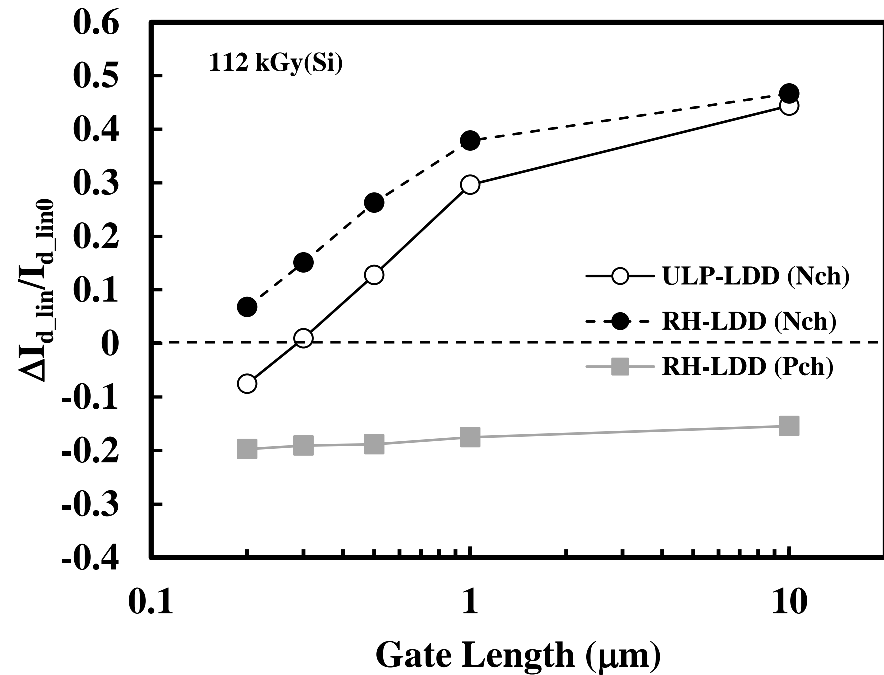


NMOS Radiation Tolerance Improvement by RH-LDD

- In L=10 μm case, no difference between ULP-LDD and RH-LDD.
- In L=0.2 μm case, drain current degradation rate is slightly improved by RH-LDD.
- Gate length dependence of drain current degradation is also slightly improved by RH-LDD.
- Why NMOS case is so different from PMOS case??????

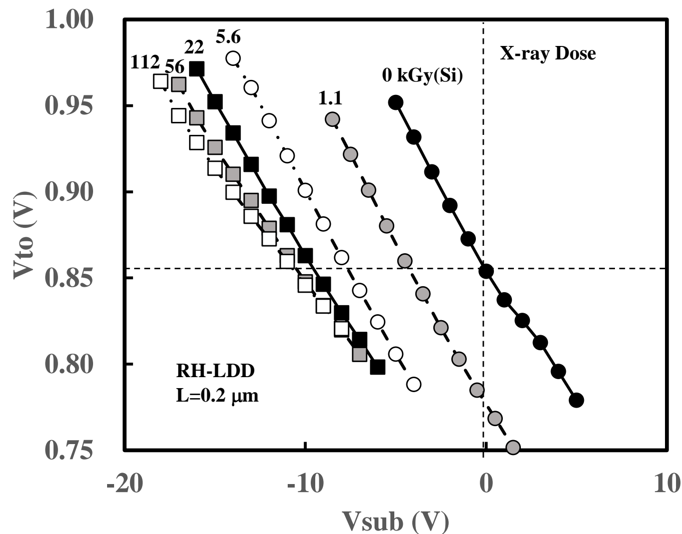


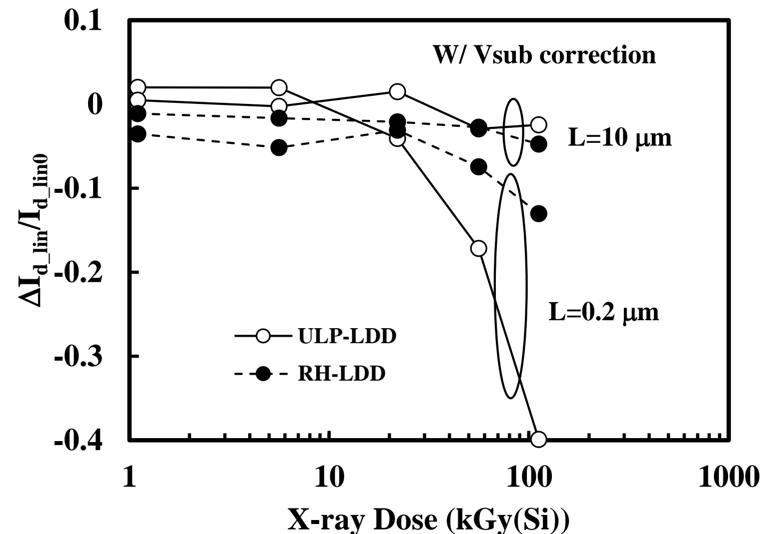
Dose Rate : 3 Gy(Si)/s



Compensation by Substrate Bias

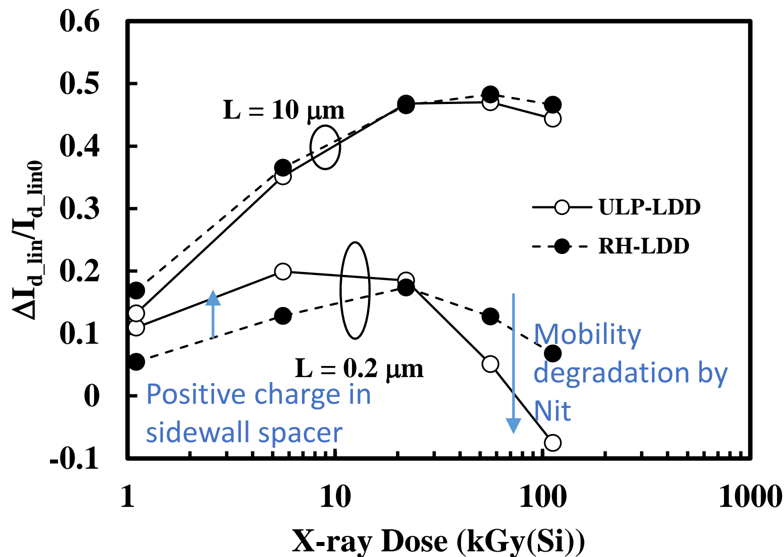
- Substrate bias (Vsub) which aligns Vto to fresh one can be found from Vsub-Vto relation.
- With compensation by correct Vsub, almost no drain current degradation in L=10 μm case. This means major cause of drain current change of L=10 μm is generated positive charge in BOX.
- In case of L=0.2 μm, still 15% degradation with Vsub correction even if RH-LDD is used.





Dose Rate : 3 Gy(Si)/s

NMOS Drain Current Degradation Mechanism



L=10 μm

Drain current change is mainly caused by **generated positive charge in BOX** because the change can be suppress by applying Vsub.

L=0.2 μm

Assuming

- ULP-LDD : gate offset structure,
- RH-LDD : no gate offset structure

Up to 20 kGy

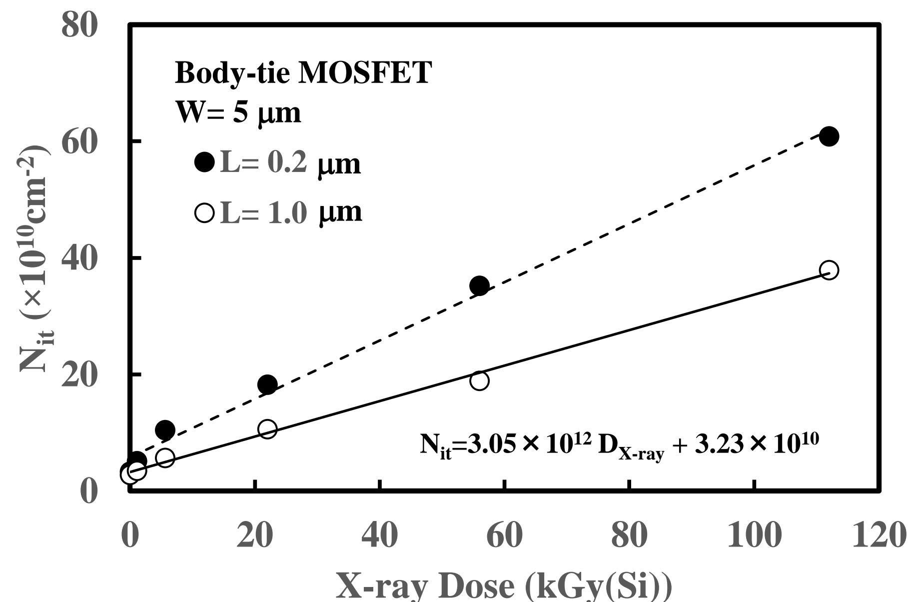
- ULP-LDD : due to **generated positive charge in BOX and Sidewall Spacer**.
- RH-LDD : due to **generated positive charge in BOX**.

More than 20 kGy

- Drain current reduction means **mobility reduction** by generated interface states.
- There is gate length dependence of drain current reduction rate. Generated interface states at **gate edges** are suspected to be **higher** than those at **center of gate**.

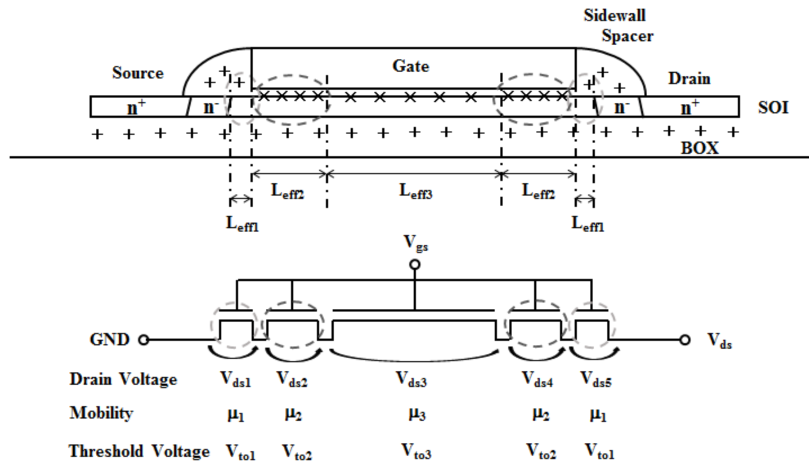
Evidence of Higher Interface State Region at Gate Edge

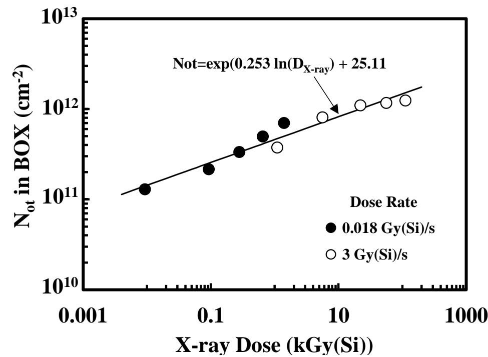
- When there are higher interface state regions at gate edge by X-ray irradiation, generated interface states must be higher for shorter gate length MOSFETs.
- Even though initial Nit is the almost same, generated interface states of L=0.2 μm are almost twice of L=1.0 μm.
- It is confirmed that there are higher interface state regions at gate edge.

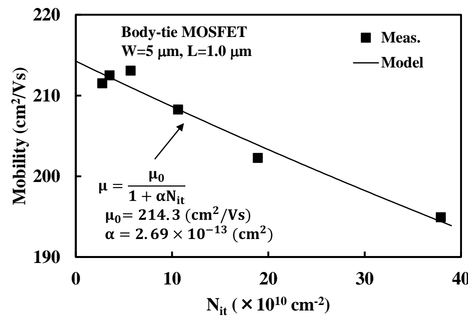


Dose Rate : 3 Gy(Si)/s

NMOS REGLEM Degradation Model







$$I_{ds} = \frac{W_{eff}}{L_{eff1}}\mu_1 C_{ox}(V_{gs} - V_{to1})V_{ds1}$$

$$I_{ds} = \frac{W_{eff}}{L_{eff2}}\mu_2 C_{ox}(V_{gs} - V_{ds1} - V_{to2})V_{ds2}$$

$$I_{ds} = \frac{W_{eff}}{L_{eff3}}\mu_3 C_{ox}(V_{gs} - V_{ds1} - V_{ds2} - V_{to3})V_{ds3}$$

$$I_{ds} = \frac{W_{eff}}{L_{eff2}}\mu_2 C_{ox}(V_{gs} - V_{ds1} - V_{ds2} - V_{ds3} - V_{to2})V_{ds4}$$

$$I_{ds} = \frac{W_{eff}}{L_{eff1}}\mu_1 C_{ox}(V_{gs} - V_{ds1} - V_{ds2} - V_{ds3} - V_{ds4} - V_{to1})V_{ds5}$$

$$V_{ds} = V_{ds1} + V_{ds2} + V_{ds3} + V_{ds4} + V_{ds5} \quad (1)$$

Assuming $\mu_1 = \mu_3$ and $V_{to2} = V_{to3}$, $\Delta\delta L = L_{eff}(x) - L_{eff}(0)$ becomes

$$\Delta\delta L = -2L_{eff1}\Delta V_{to1} + 2\frac{\mu_3 - \mu_2}{\mu_2}L_{eff2}$$

$$\Delta V_{to1} = \frac{qT_{ox_sw}N_{ot_sw}}{\varepsilon}$$

$$\mu = \frac{\mu_0}{1 + \alpha N_{it}}$$

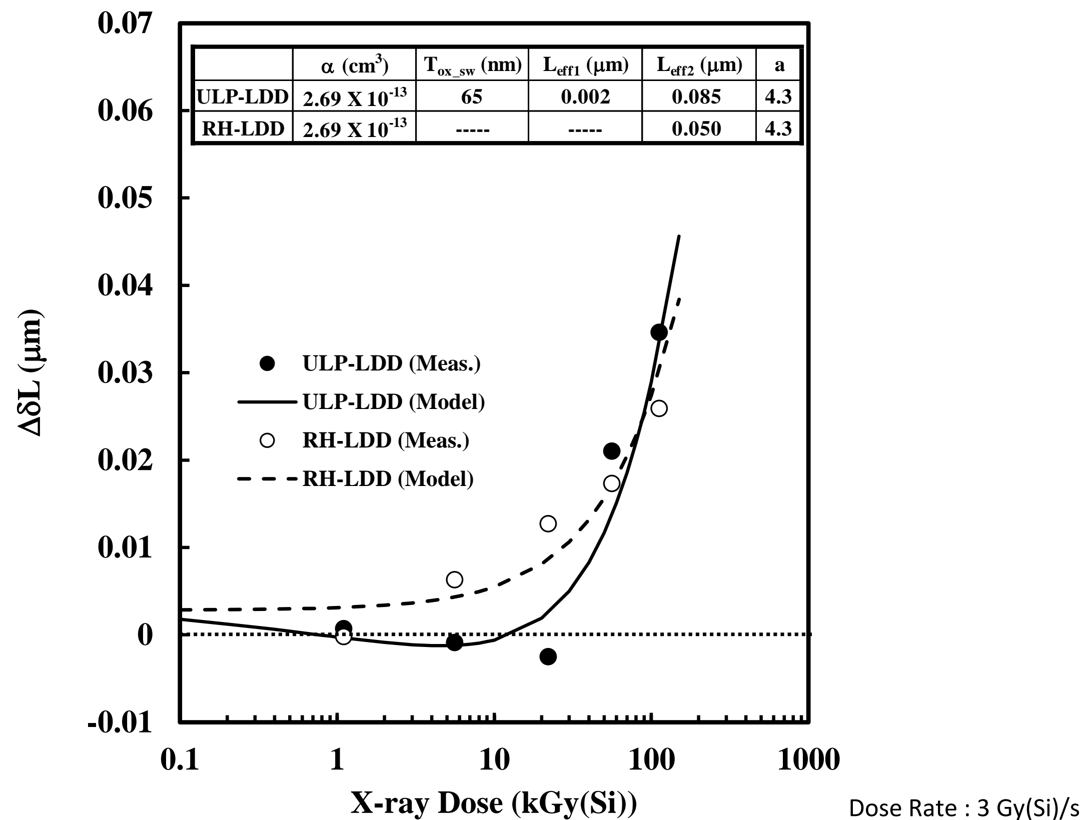
$$\frac{\mu_3 - \mu_2}{\mu_2} = \frac{\alpha(N_{it2} - N_{it3})}{1 + \alpha N_{it3}} = \frac{\alpha(a-1)N_{it3}}{1 + \alpha N_{it3}}$$

$$N_{it2} = aN_{it3}$$

If ΔδL is minimized, dependence of drain current degradation on gate length can be improved and major cause of drain current change must be due to generated positive charge in BOX.

Comparison between Measured and Calculated ΔδL

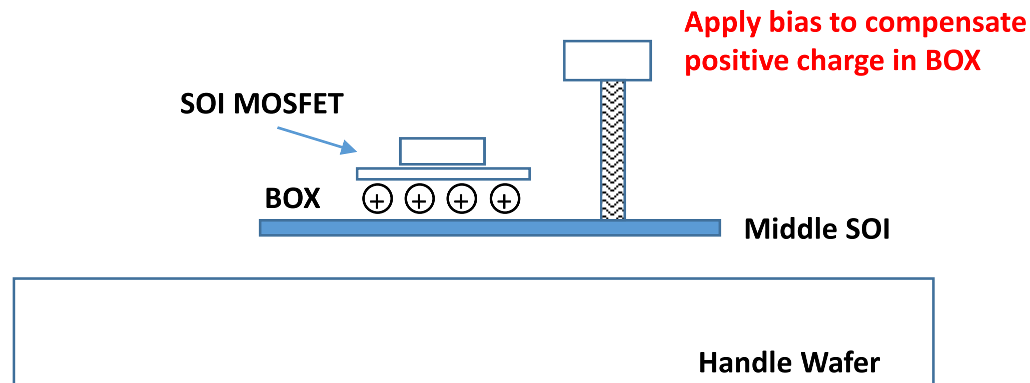
- Fitting curves based on model can be obtained for both ULP-LDD and RH-LDD which indicates accuracy of model.
- Interface state generation at gate edge is one of major factors for radiation damages in NMOS. It is suggested that suppression of interface state generation such as F dope or NO annealing is key improvements for NMOS radiation hardness.



	α (cm^3)	T_{ox_sw} (nm)	L_{eff1} (μm)	L_{eff2} (μm)	a
ULP-LDD	2.69 X 10^{-13}	65	0.002	0.085	4.3
RH-LDD	2.69 X 10^{-13}	-----	-----	0.050	4.3

Further Improvement of Radiation Hardness

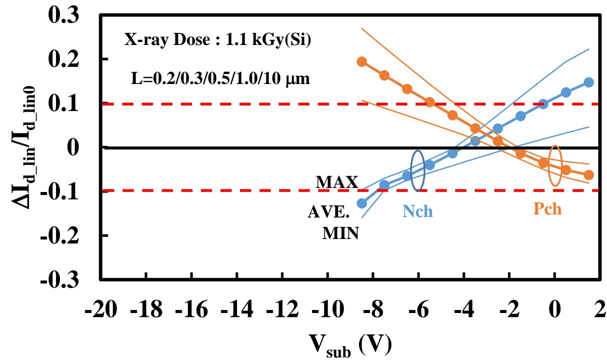
- When gate length dependence of drain current change is eliminated or reduced, major cause of change is generated positive charge in BOX for SOI-NOSFET.
- Fortunately, we have back bias layer (middle SOI) in double SOI structure. We can apply compensation back bias (Vsub) to reduce effect of positive charge in BOX.



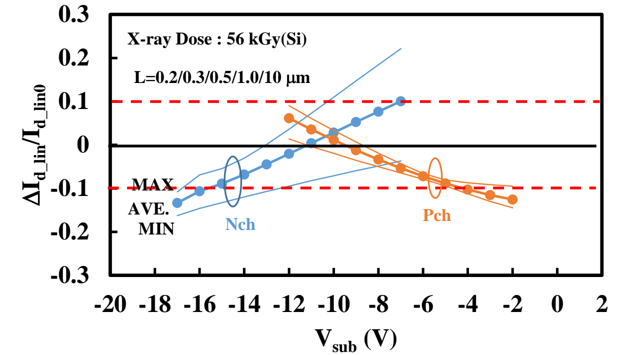
Can we have accepted bias (Vsub) to reduce drain current change for both NMOS and PMOS, or for wide range of gate length?

Drain Current Change on Vsub

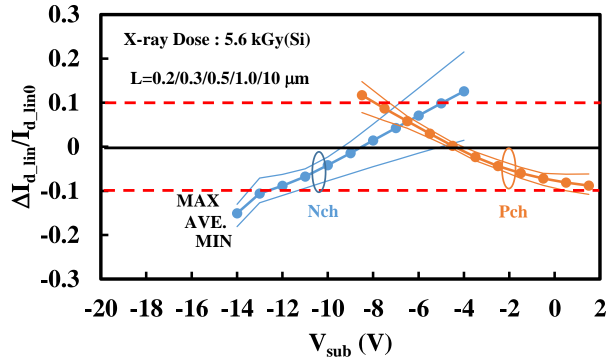
1.1 kGy(Si)



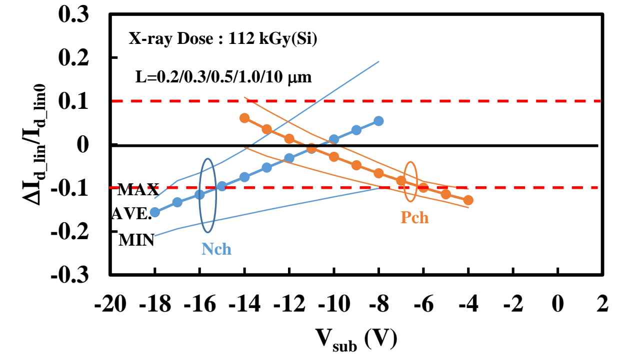
56 kGy(Si)



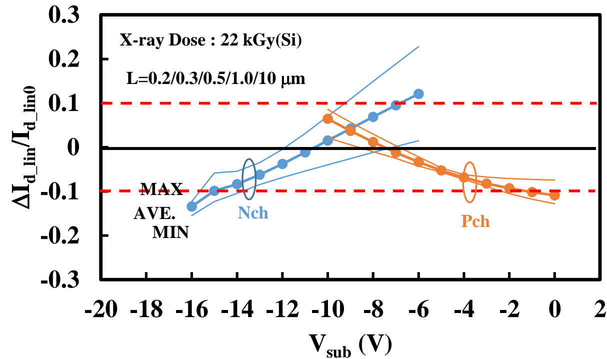
5.6 kGy(Si)



112 kGy(Si)



22 kGy(Si)

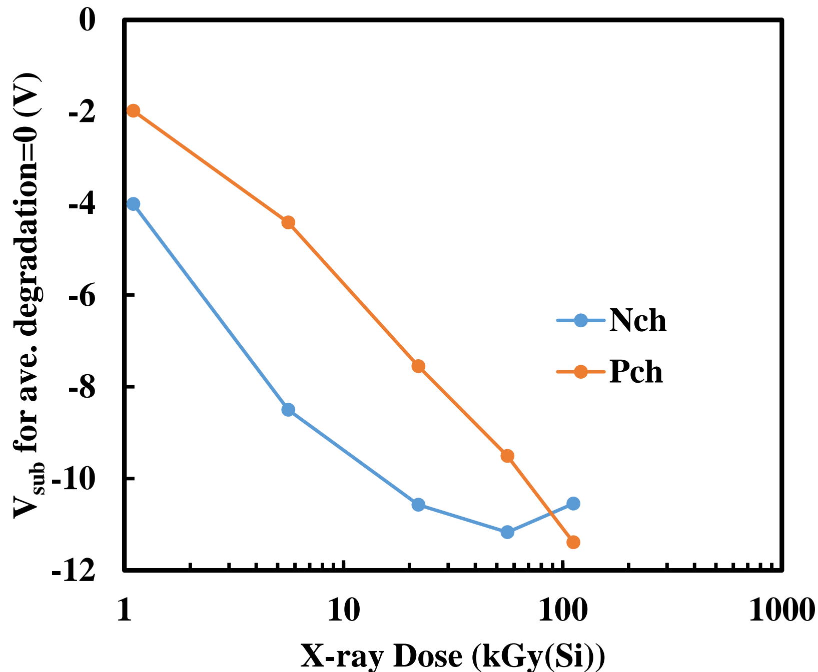


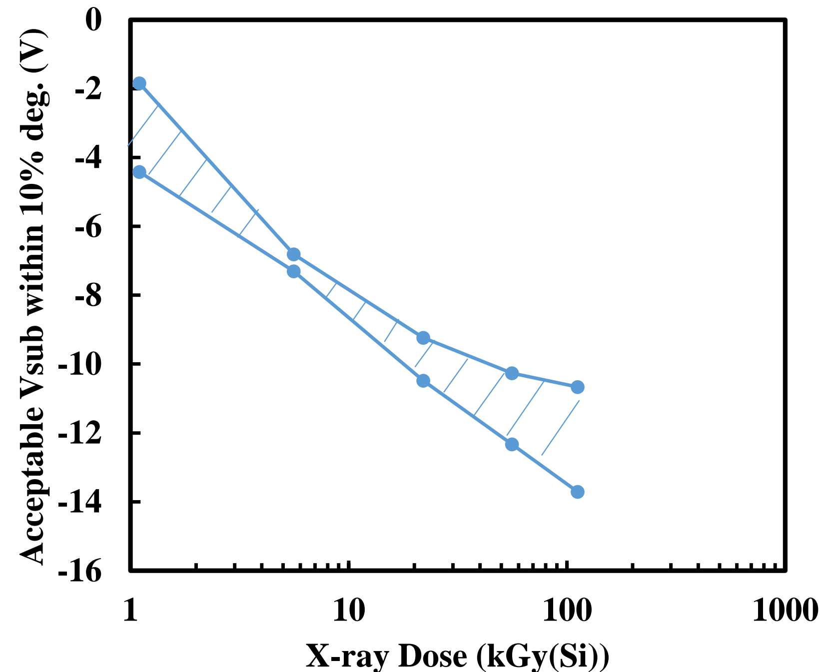
NLDD:RH-LDD
PLDD:RH-LDD

Dose Rate : 3 Gy(Si)/s

Drain Current Change Compensation by Applying Vsub

- Required Vsub to recover drain currents are different between NMOS and PMOS.
- Even though, Vsub to make drain current change within 10% for NMOS and PMOS with L=0.2-10 mm up to 100 kGy exists.
- Compensation of BOX charge by applying Vsub may be the best way to improve radiation hardness to MGy range even for FD-SOI MOSFET.





Dose Rate : 3 Gy(Si)/s

Summary

1. Current LDD structure (ULP-LDD) is weak in radiation tolerance because of RIGLEM.

2. Higher dose LDD structure (RH-LDD) improves radiation hardness.
   PMOS : Improve 80% to 20% degradation after 100 kGy(Si) irradiation
   NMOS : Slightly improve for shorter gate length MOSFETs

3. Major degradation mechanism by X-ray radiation except for generated positive charge in BOX is interface state generation at gate edge. Therefore, improvement by changing LDD concentration is not so obvious.

4. Generated positive charge in BOX can be compensated by applying substrate bias.

5. Substrate bias which can be suppress the drain current change within 10% for NMOS and PMOS, and L=0.2 to 10 μm, up to 100 kGy(Si) irradiation is confirmed to exist.

6. Further radiation hardness improvement must be done by automatic substrate bias control to compensate BOX charge.