Design of First China-Japan Counting Pixel (CNPIX1)

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http://rd.kek.jp/project/soi/

概论

- Shield effect of middle Si (SOI2) layer in the Double SOI wafer is confirmed. Then it become possible to include complex digital circuit in a pixel.
- We, IHEP and KEK member, started to develop advanced counting-type X-ray pixel detector based on previous CPIXTEG3B and CPIXPTEG1 chips.
- To reduce charge sharing effect, Hexagonal shape pixel is adopted, and new charge compare circuit is developed.

Collaborator

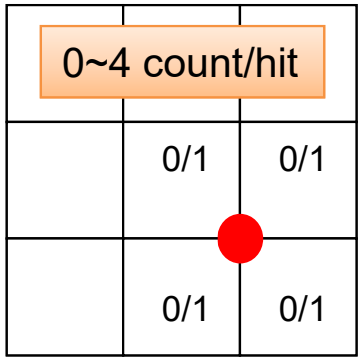
IHEP China: Yinpeng Lu, Yang Zhou

KEK Japan: Yasuo Arai, Ryo Hashimoto, Ryutaro Nishimura

Square vs. Hexagonal

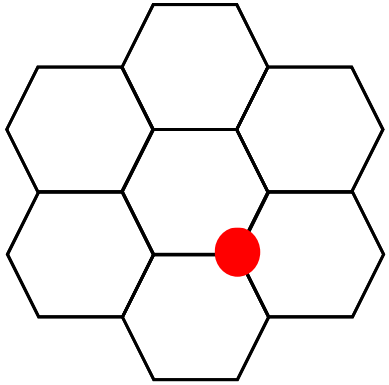
In small size counting-type pixel,
Charge Sharing becomes severe issue.

Square Pixel



worst(E_{photon})=4•Vth

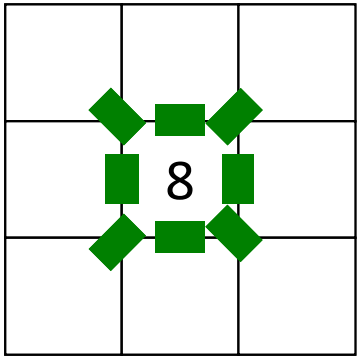
Hexagonal Pixel



worst(E_{photon})=3•Vth

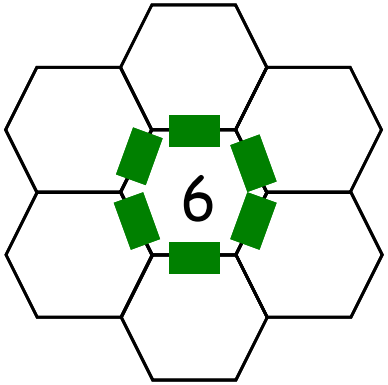
Hexagonal pixel can detect 3•Vth energy photon even in the case of charge share in 3 pixel.
While in square pixel, this will be 4•Vth.

Square Pixel



Vth = 1/4 E_{photon}

Hexagonal Pixel

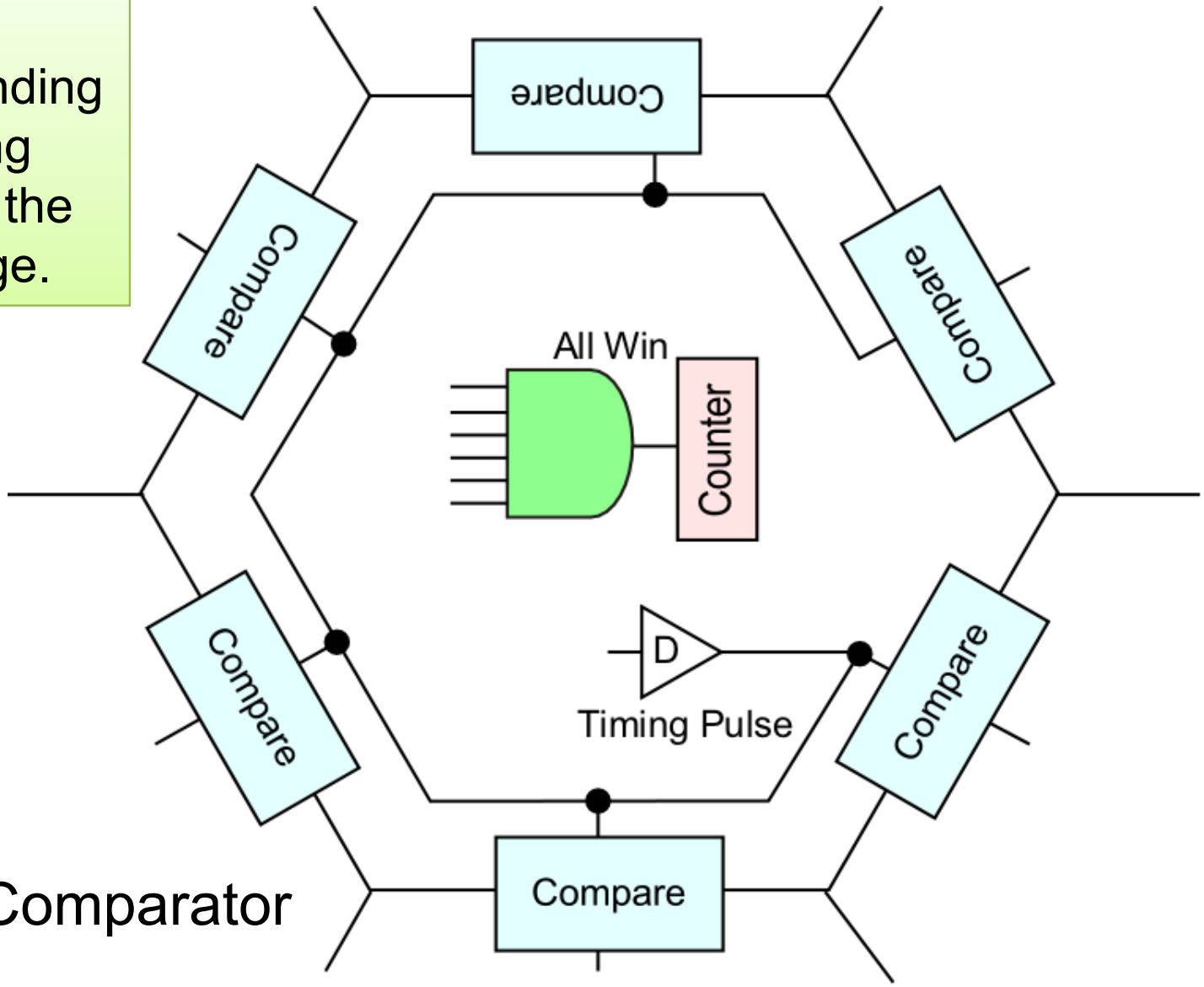


Vth = 1/3 E_{photon}

No. of comparing circuit is 6 in Hexagonal pixel, while in square pixel, there needs 8 circuit.

Charge Sharing Handling Circuit

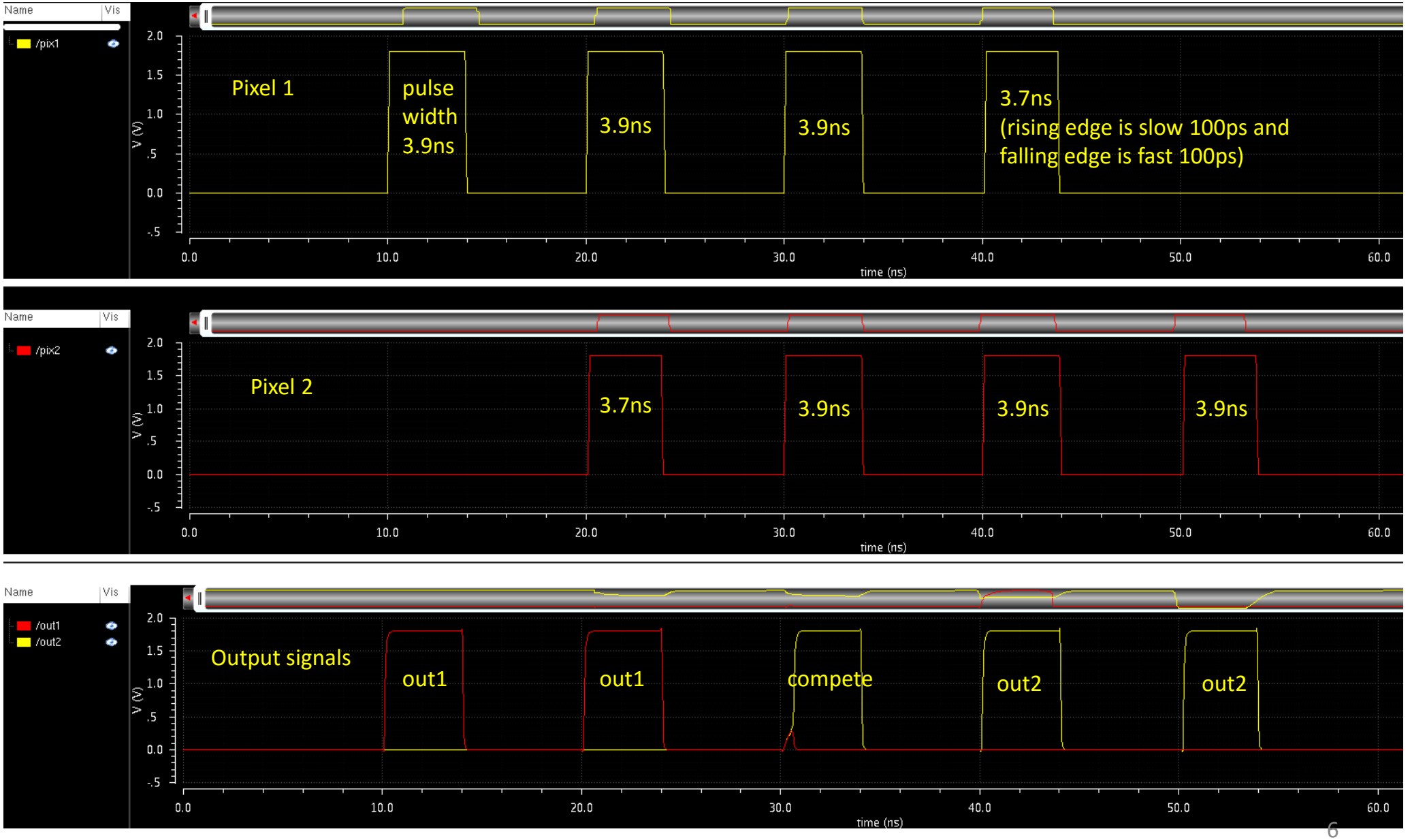
Compare Charge Amplitude with surrounding 6 pixels by using Timing Pulse, and Count only the pixel with largest charge.



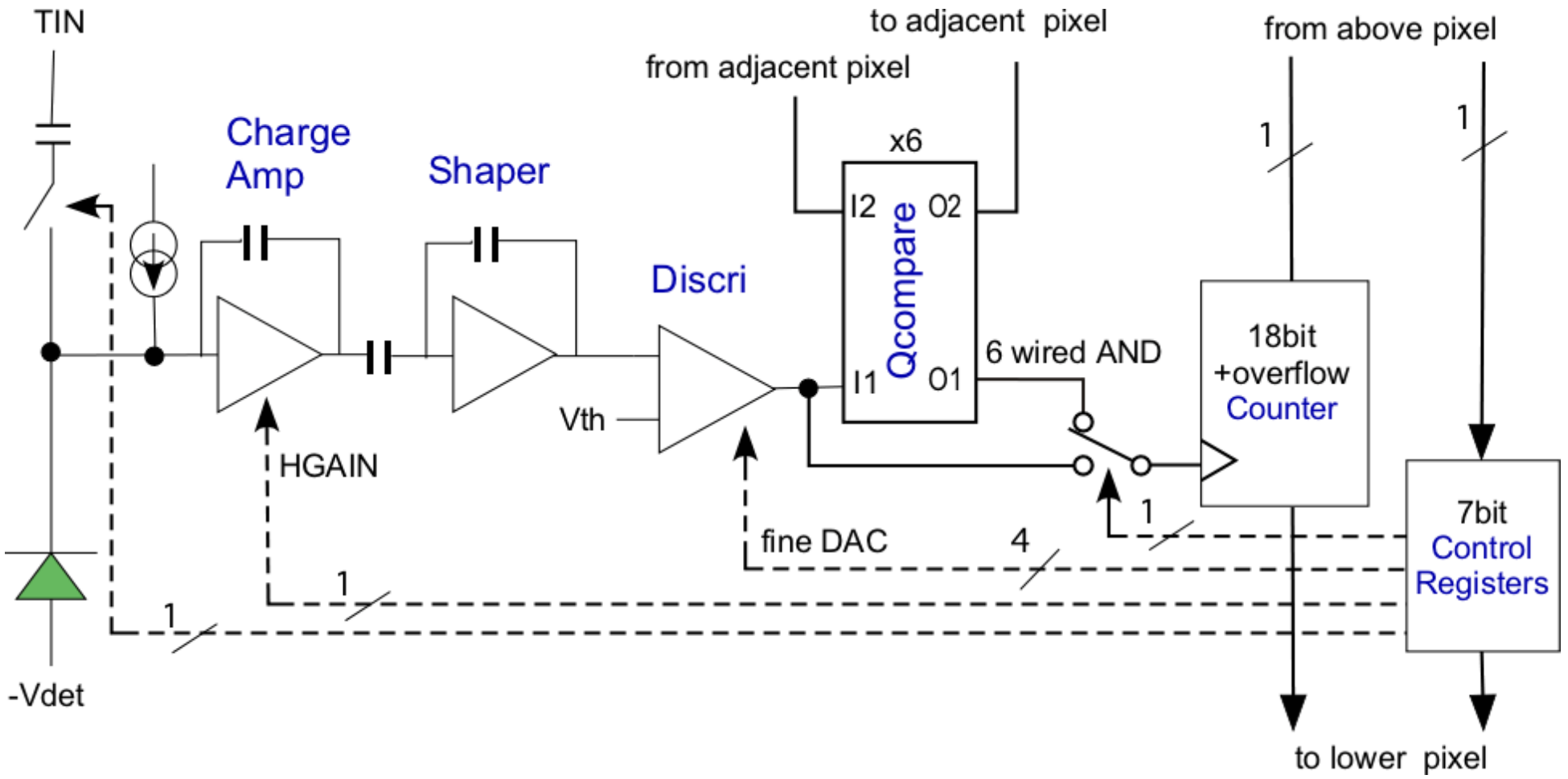
Timing + Phase Comparator

Assuming output signal from a discriminator, which receive larger signal than adjacent cell, has faster rising edge and longer pulse width, the Compare circuit can select right counter clock.

Simulation results



Block Diagram of a Pixel

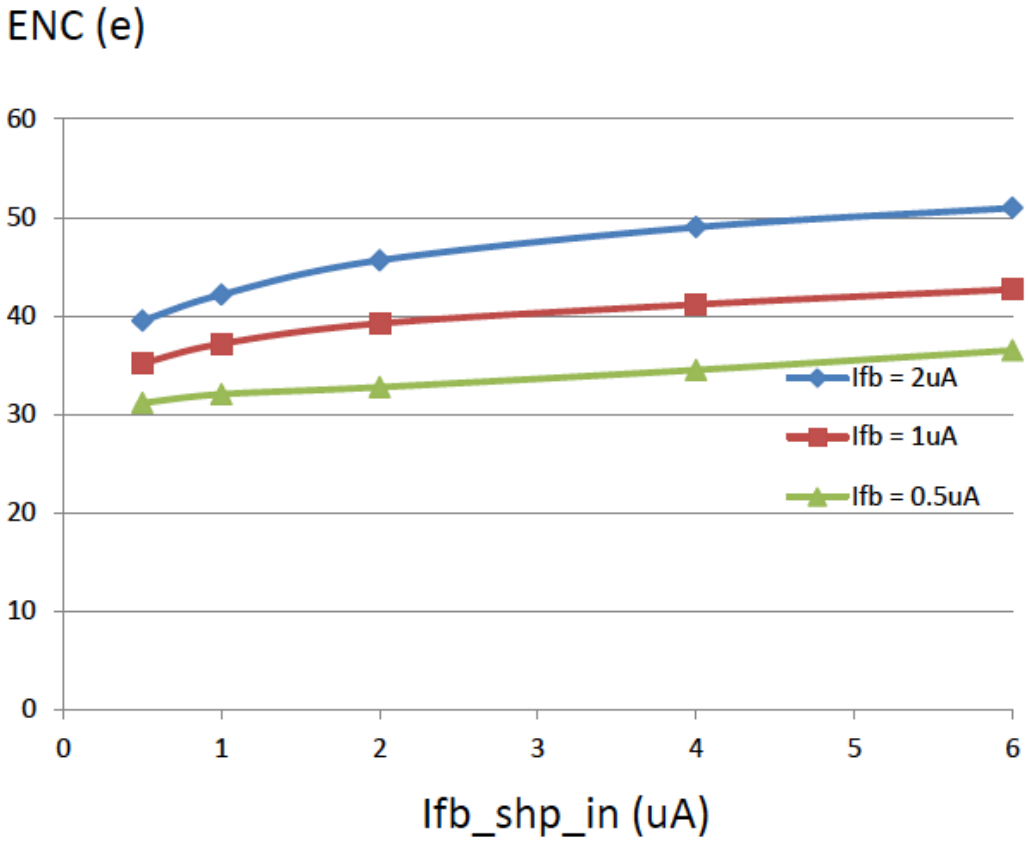


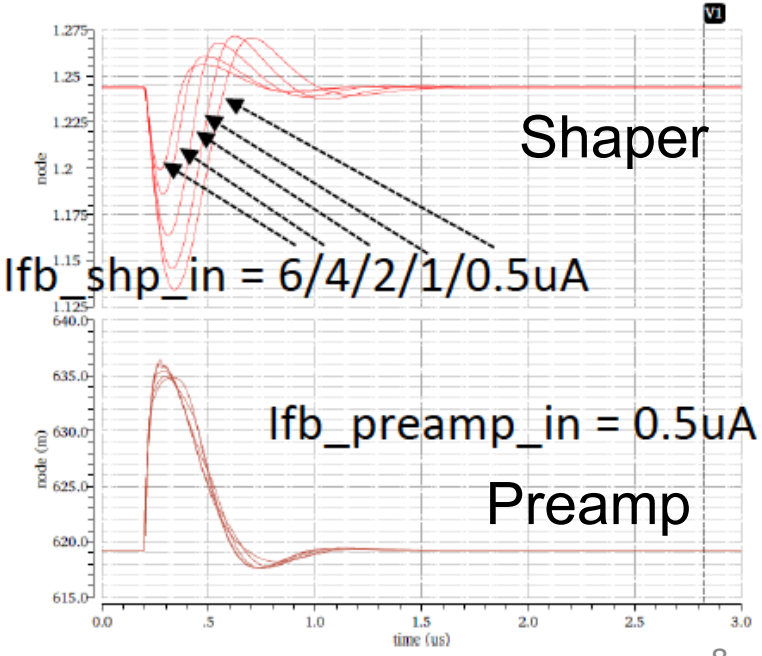
PREAMP_12_B and SHP_12_B design (HGAIN)

- Optimum results @ Ifb_preamp_in = 0.5uA, Ifb_shp_in = 0.5uA
  - Maximum amplitude 109.6mV
  - Minimum ENC = 31.2e

Conditions

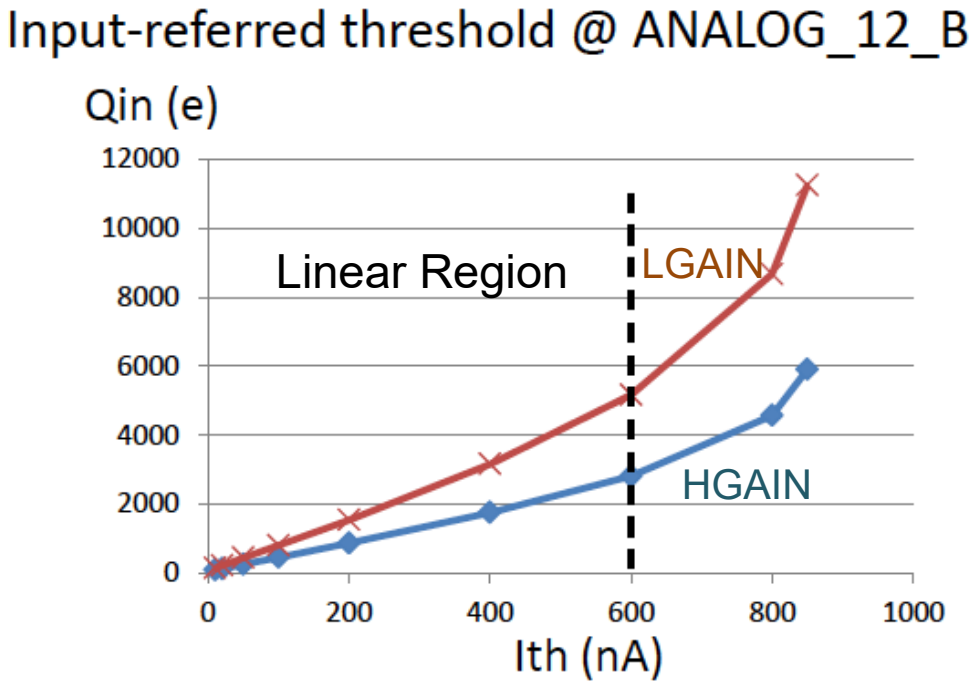
- I_{leak} = 20pA
- C_d = 50fF
- Q_{sig} = **400e**
- C_{f_preamp} = 0fF + 1fF (LPE)
- C_{f_shp} = 4fF (DMOS) + 1fF (LPE)
- Ith = 100nA

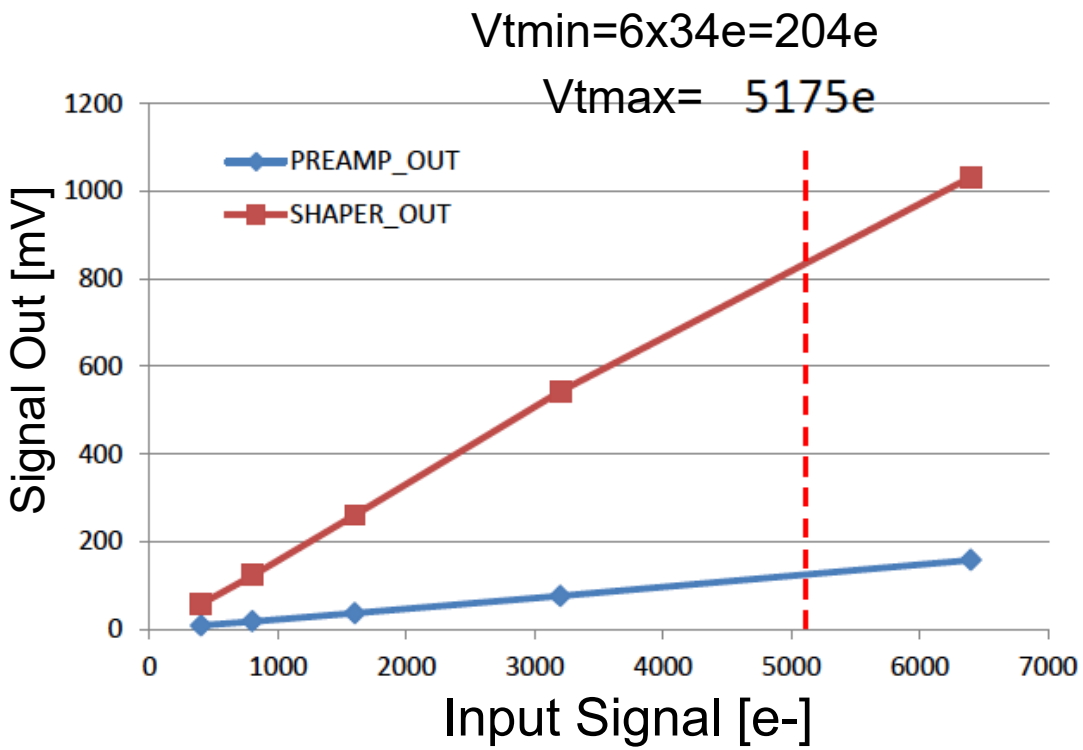


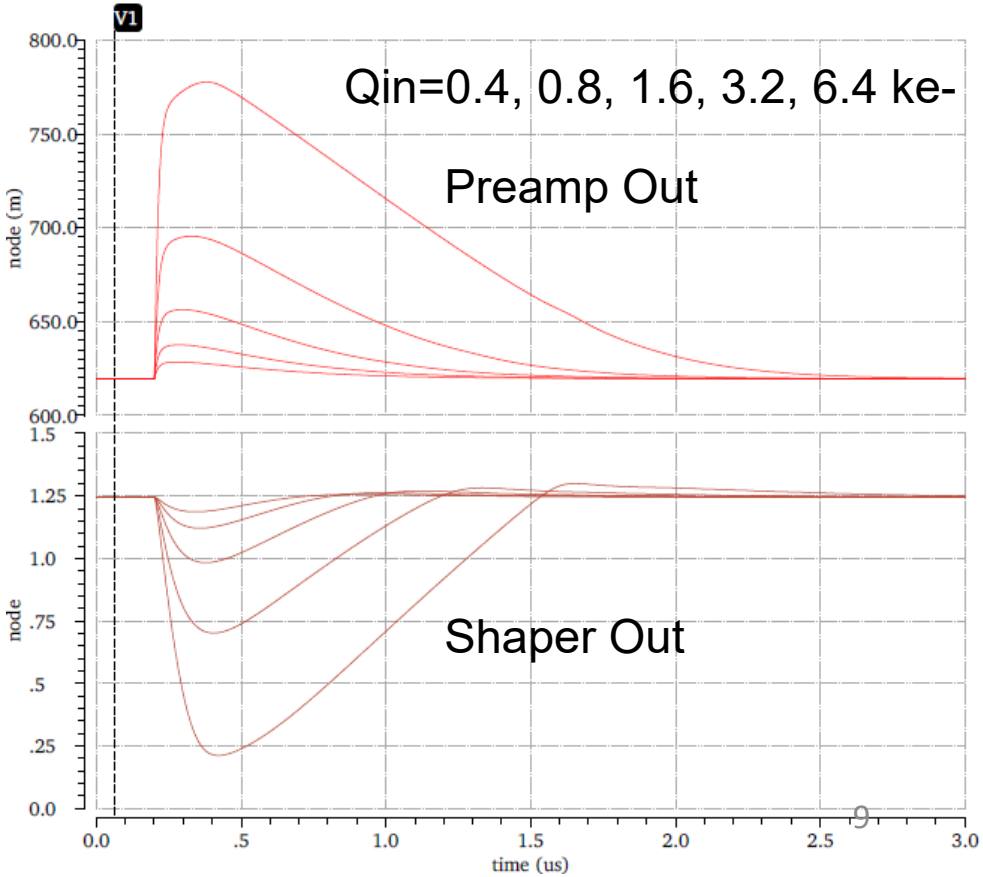


LGAIN mode Simulation

Preamp Out: 24 uV/e
Shaper Out : 173 uV/e



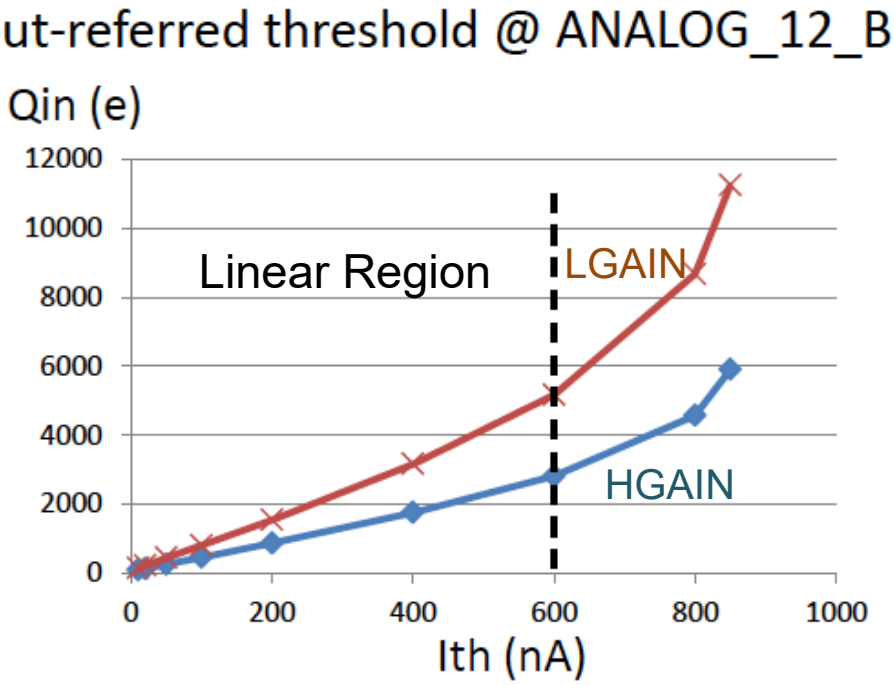


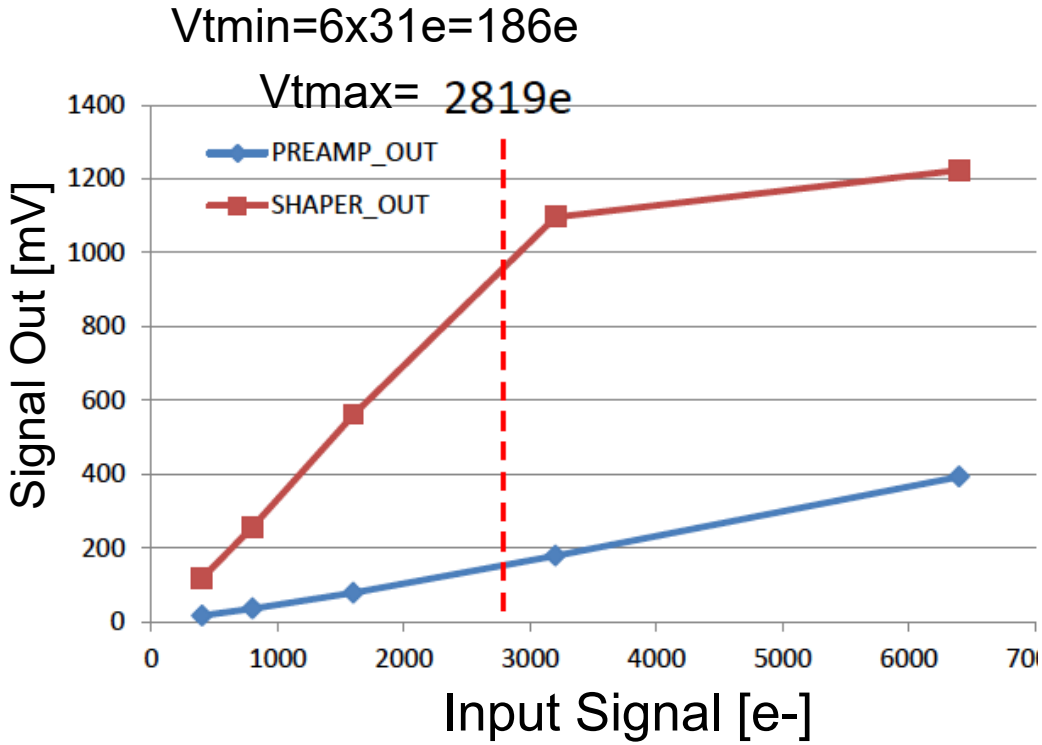


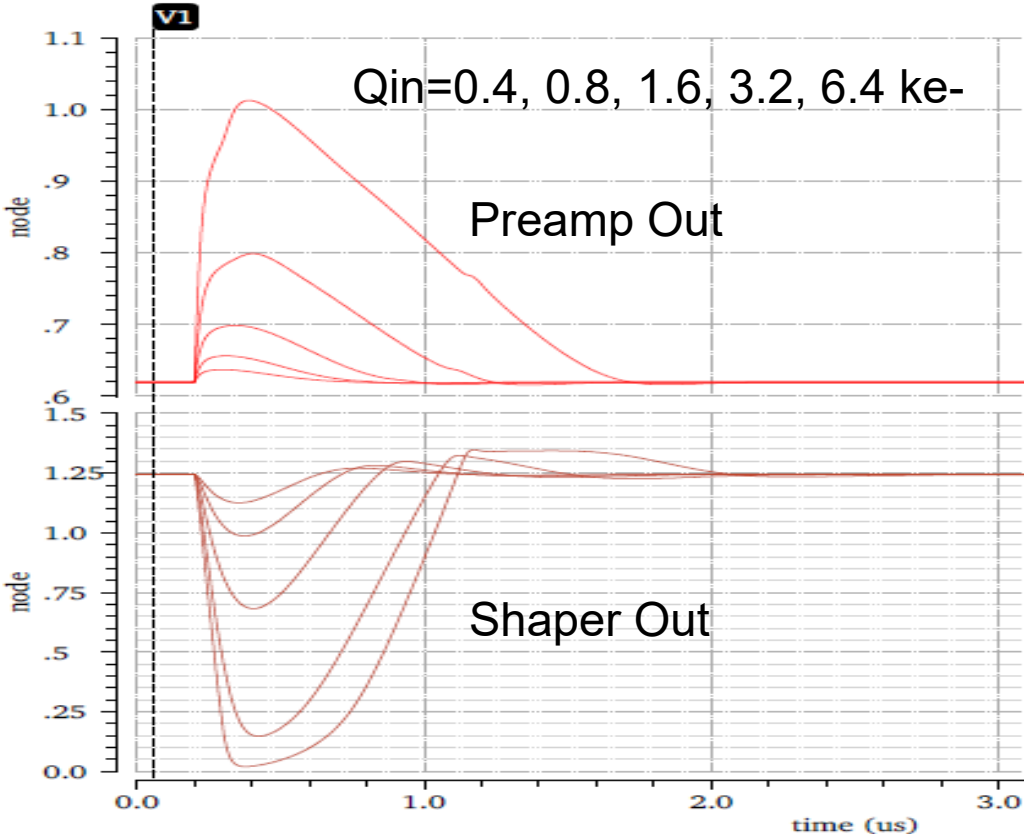
(by Yunpeng Lu)

HGAIN mode Simulation

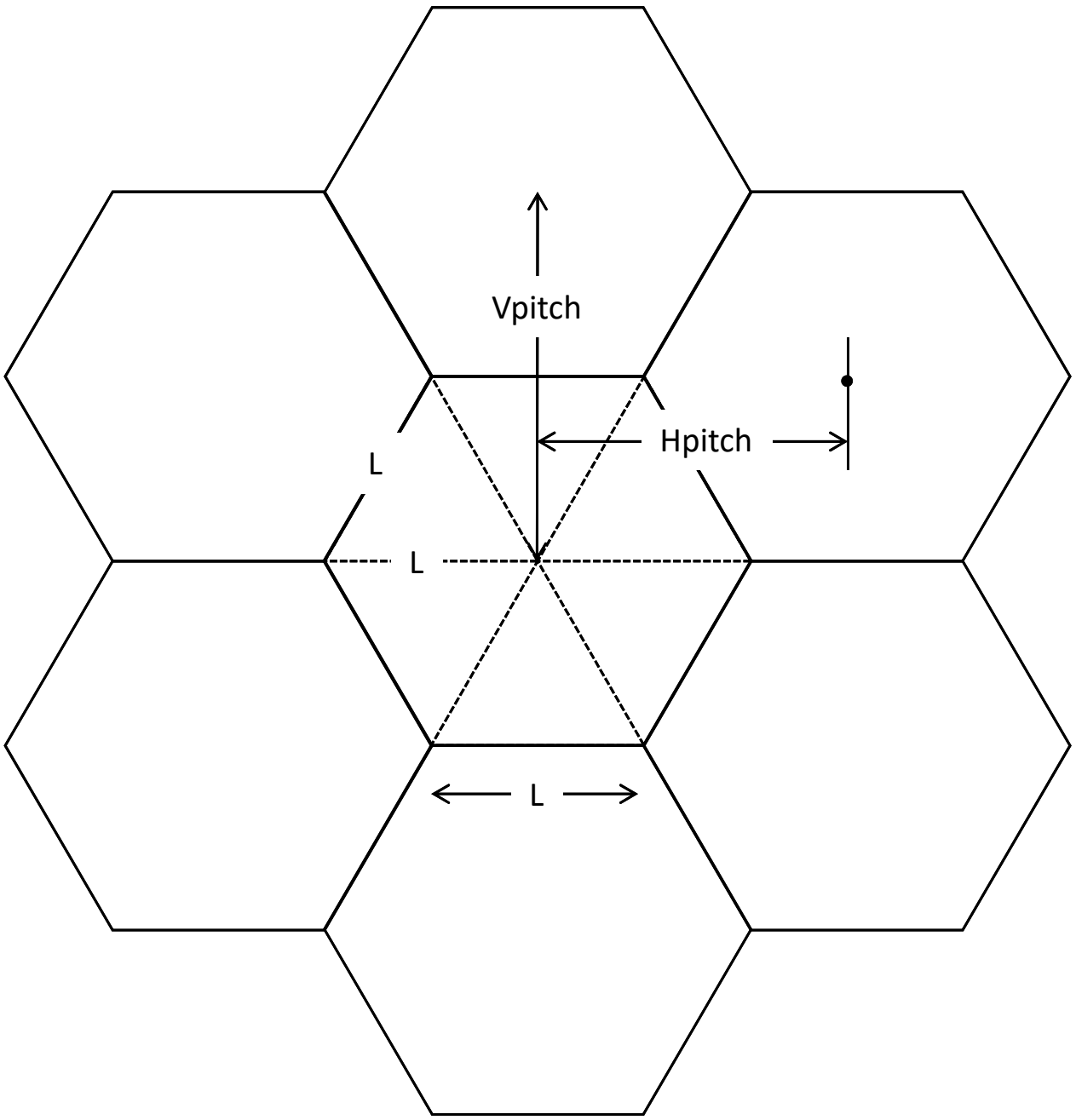
Preamp Out: 51 uV/e
Shaper Out : 369 uV/e







(by Yunpeng Lu)



$$Vpitch = \sqrt{3} \cdot L$$

$$Hpitch = 1.5 \cdot L$$

$$PixArea = \frac{3\sqrt{3}}{2} L^2 = 2.598 \cdot L^2$$

Taking L = 30 um

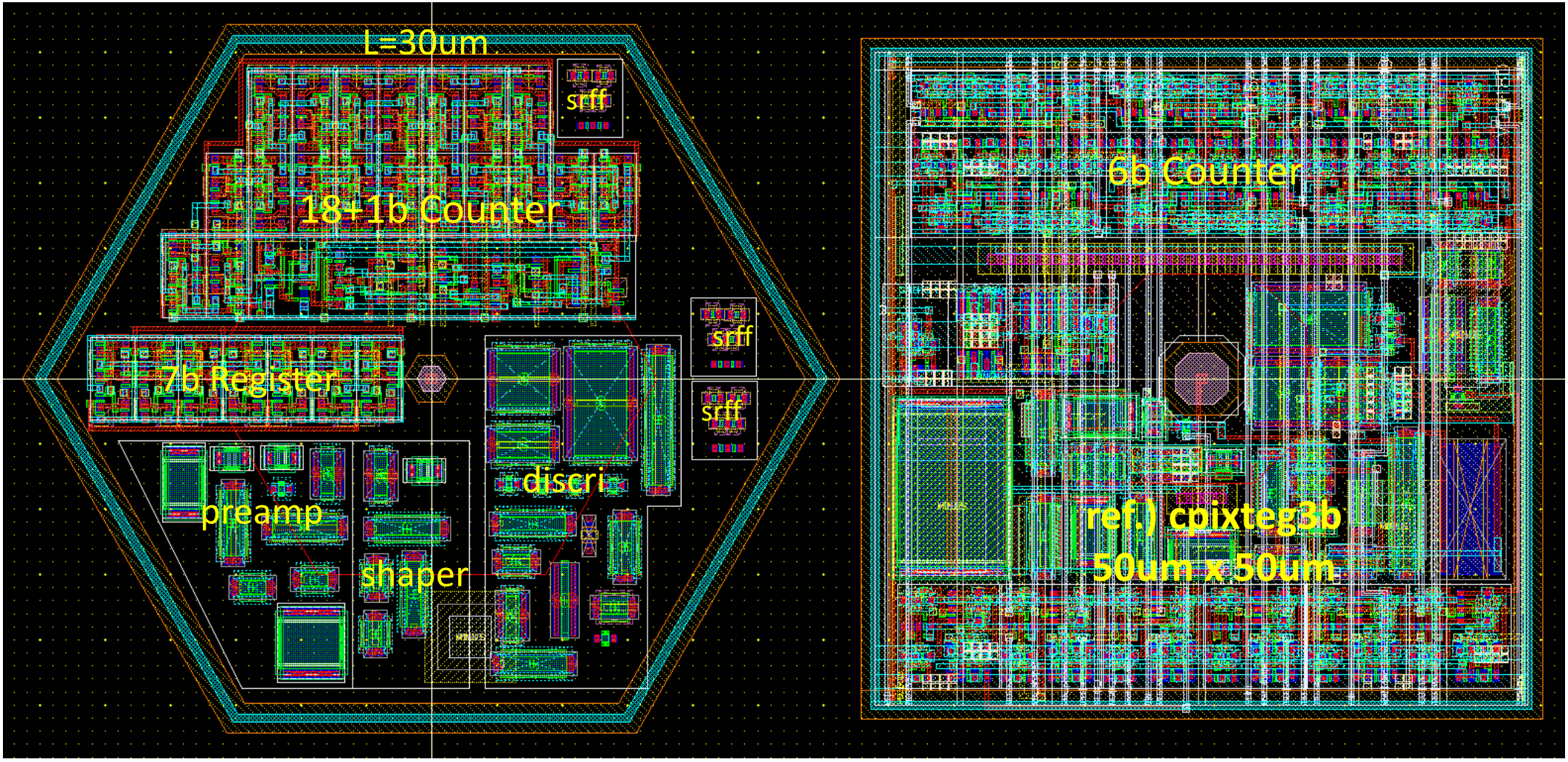
Vpitch ≅ 52 um

Hpitch = 45 um

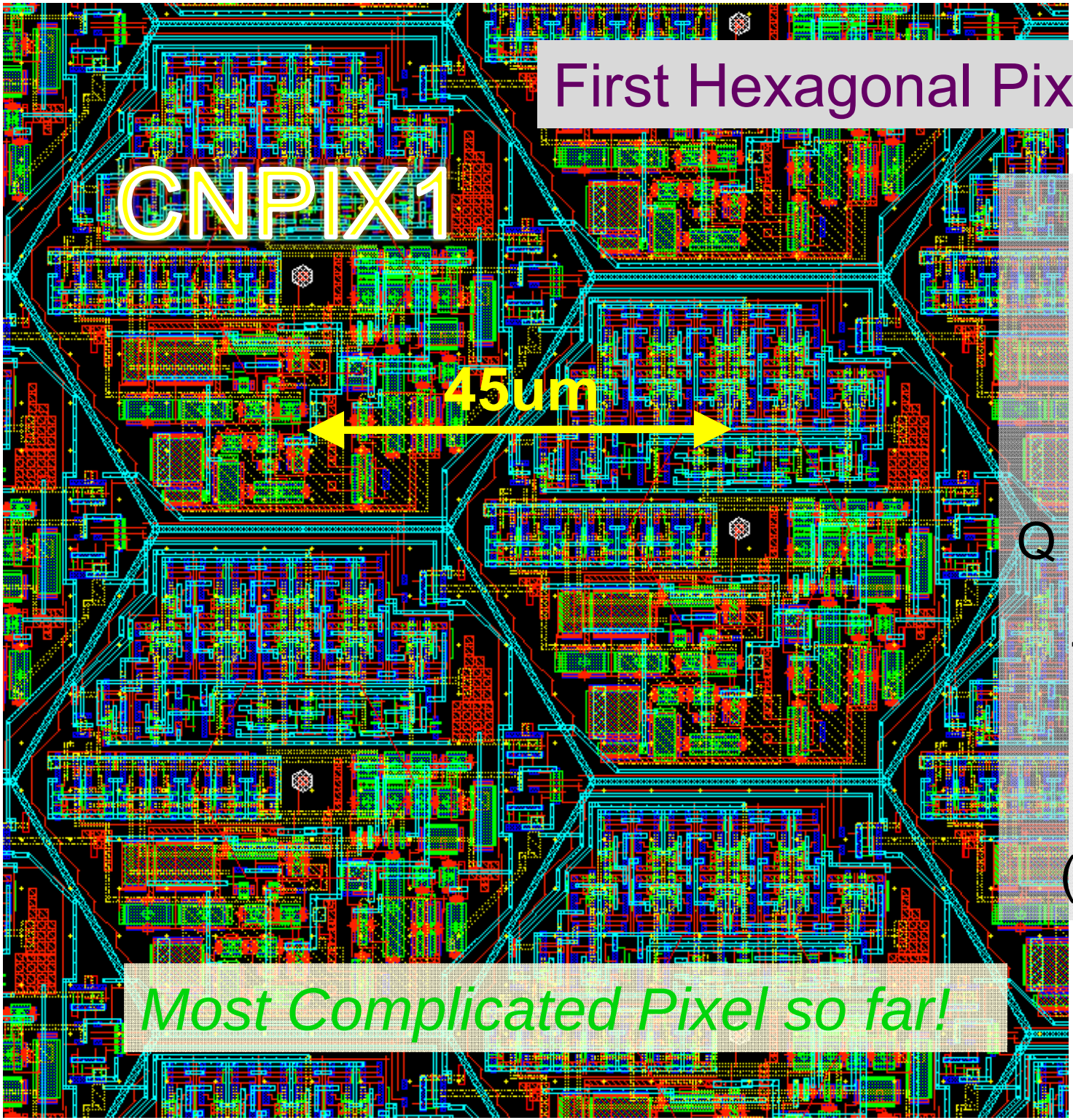
PixArea = 2338.2 um²

cf) 50x50um²=2500um²

Layout Plan


L=30um
srff
18+1b Counter
6b Counter
srff
7b Register
srff
discri
preamp
shaper
ref.) cpixteg3b
50um x 50um

First Hexagonal Pixel in SOIPIX



Charge Amp
+
Shaper
+
Discriminator
+
Q Share Handling
+
19bit Counter
+
7bit register

(in 2,340 um^2)

Most Complicated Pixel so far!

Comparison of Counting-type Pixel

	Pilatus3	Eiger	Medipix2	Medipix3RX	Timepix3	CNPIX1
pixel size	172um x 172um	75um x 75um	55um x 55um	55um x 55um	55um x 55um ($3025um^2$)	**45um x 52um ($2340um^2$)**
No. of pixels	487 x 195 (94,965)	256 x 256 (65,536)	256 x 256 (65,536)	256 x 256 (65,536)	256 x 256 (65,536)	**328 x 256 (83,968)**
counter depth	20bits	12bits	13bits	12bits x 2 or 24bits x1	14bits(ToA) + 10bits(ToT)	**18+1 bits**
No. of threshold	1	1	2	1 or 2	1	**1**
Care for Charge Share	No	No	No	Yes	No	**Yes**
Process	CMOS 0.25um	CMOS 0.25um	CMOS 0.25um	CMOS 0.13um	CMOS 0.13um	**SOI 0.2um**
Lowest Eth (noise)	2.7 keV	2.7 keV		(72 e-)		**1.5 keV (<40e-)**
Counting rate	10 MHz	~1 MHz		Unkown		**>1MHz**
Pixel Shape	Square	Square	Square	Square	Square	**Hexagonal**

Vertical Read Layout

Merit

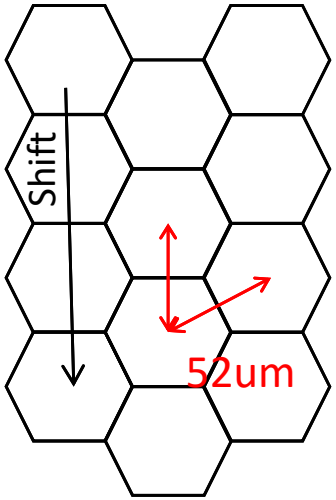
•Better for multiple sensor layout.

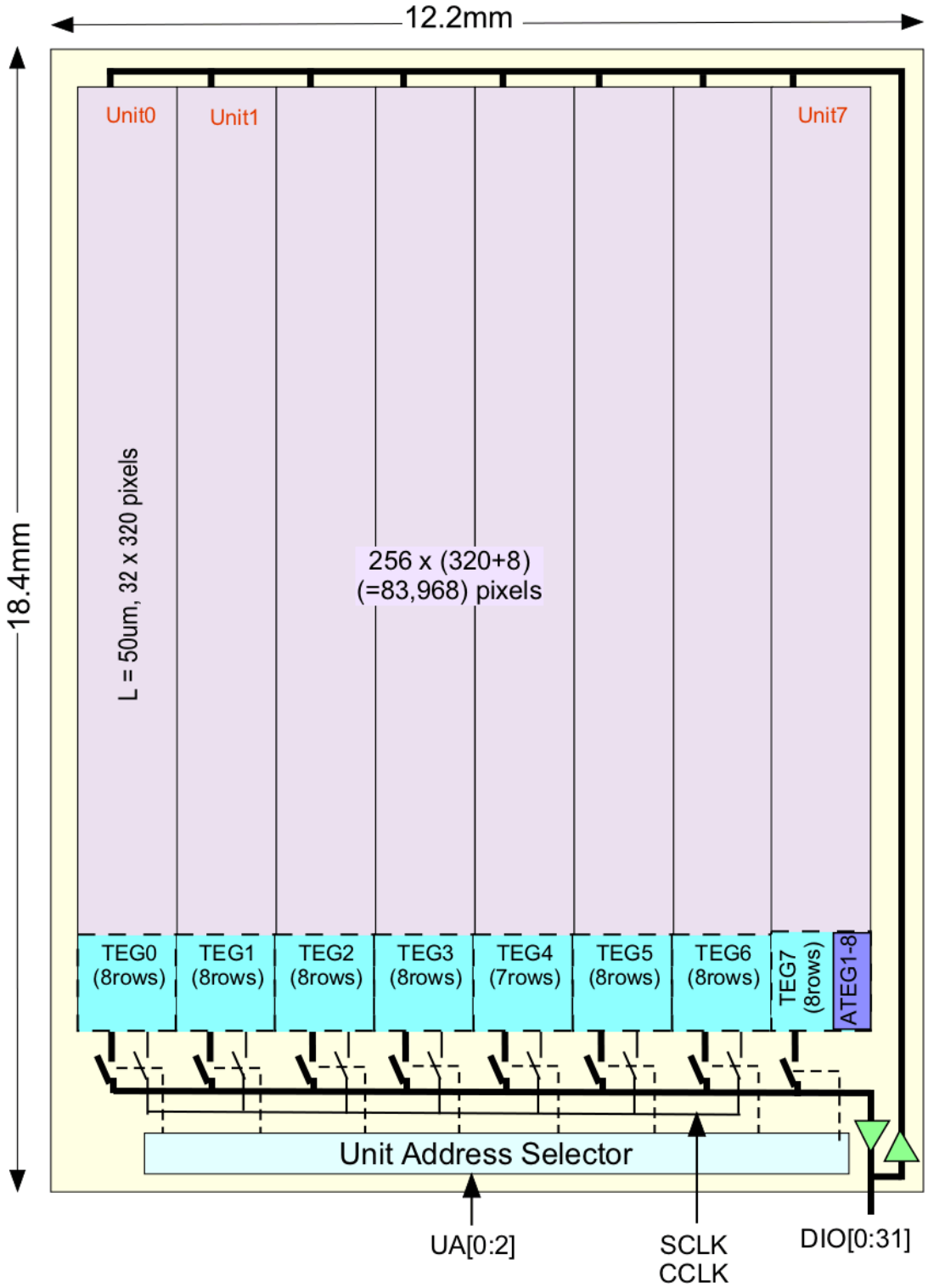
•No. of Unit become small.

Demerit

•It takes longer time to read out a column data.

•Voltage drop along a column becomes large.

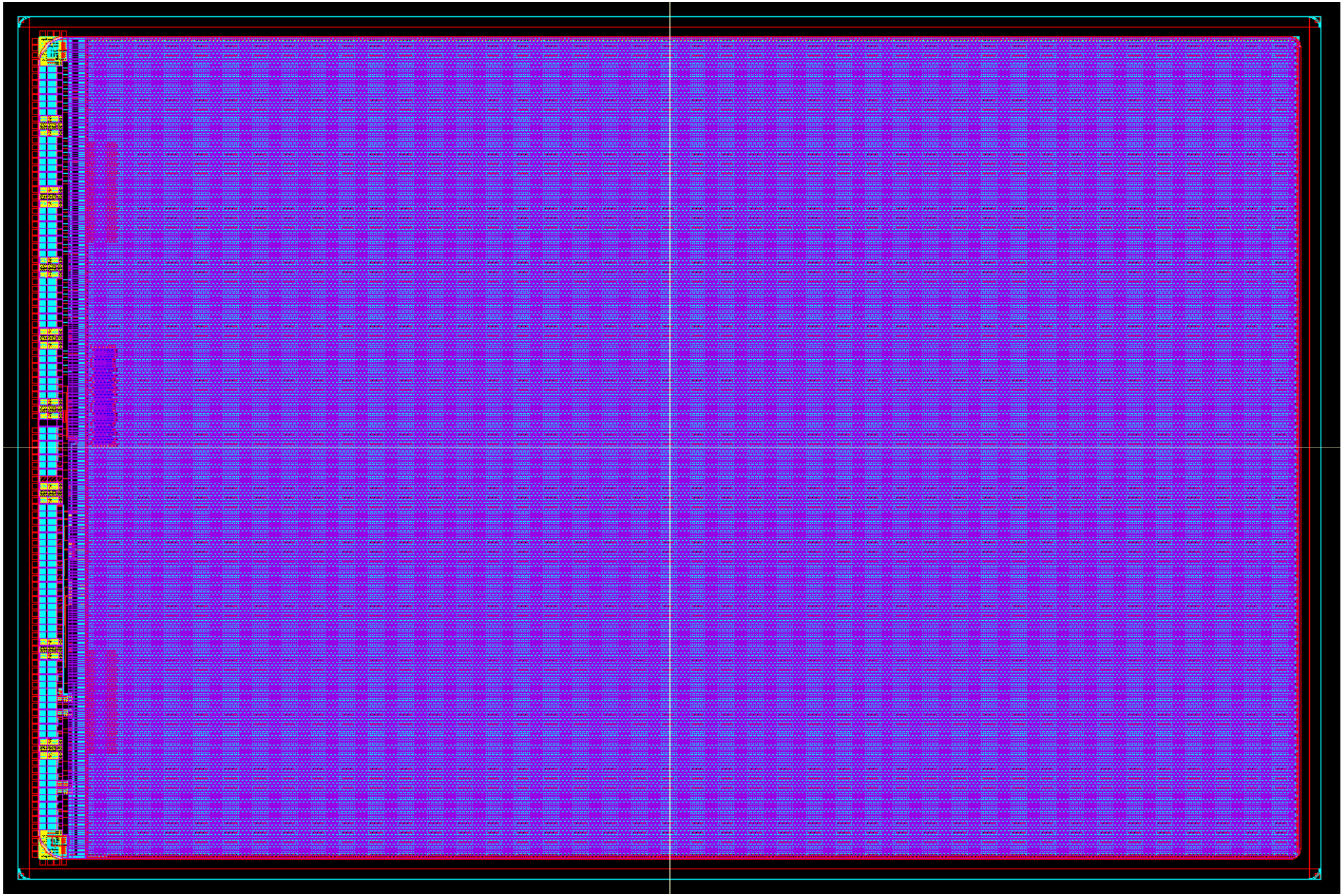




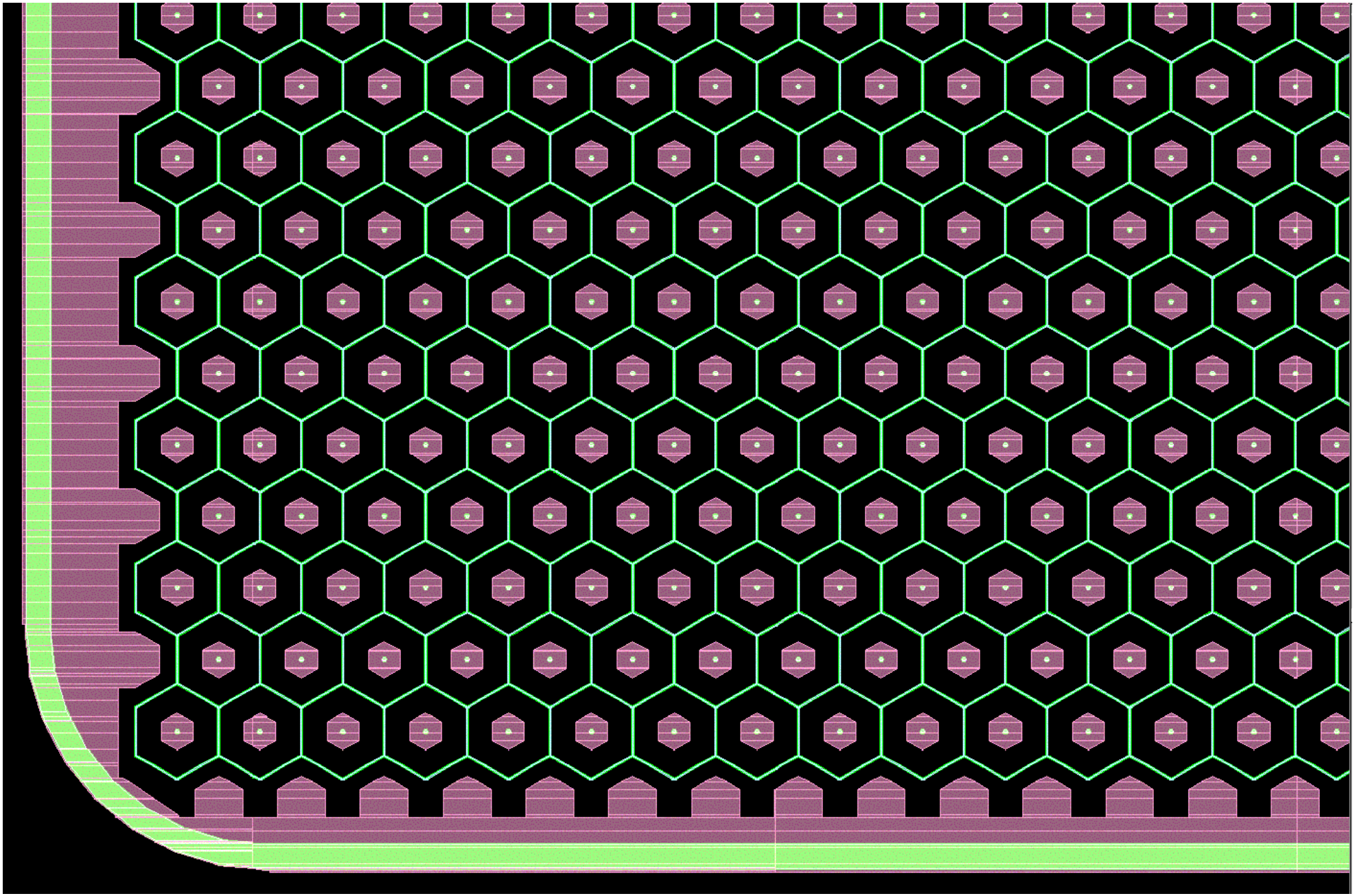
Block Diagram of CNPIX1 Chip

2016.6.6 Y.Arai

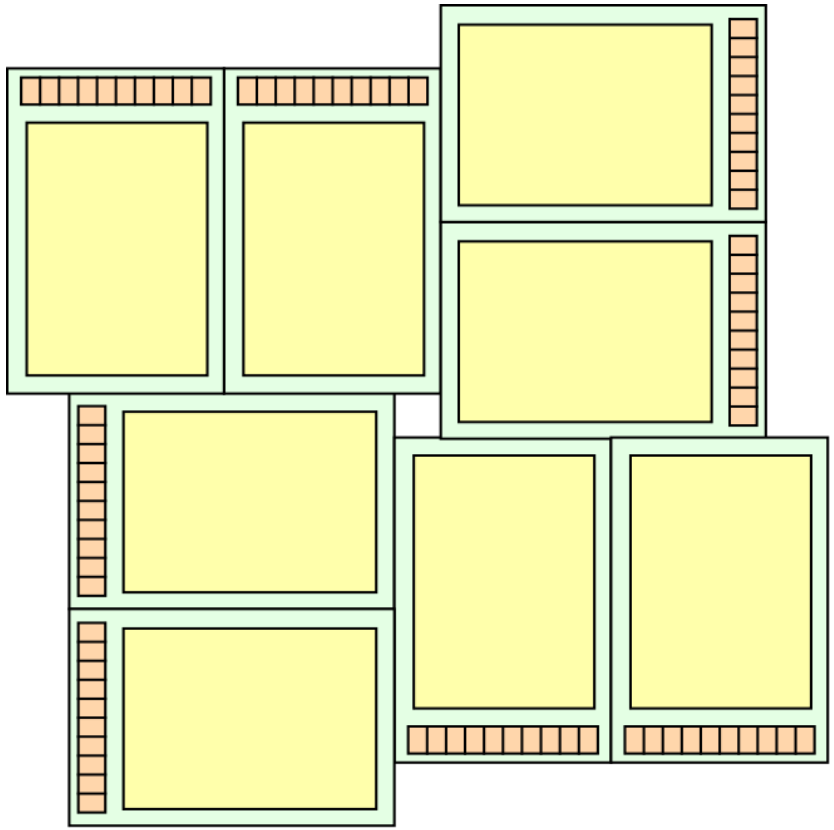
CNPIX1 (Whole Chip)

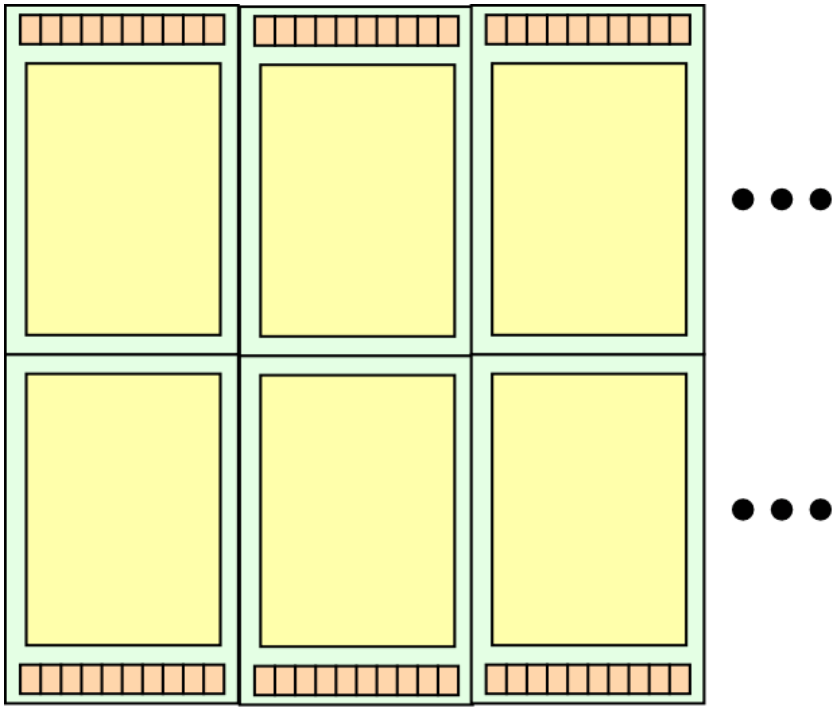


CNPIX1 (Corner)



Examples of Multiple Sensor Layout

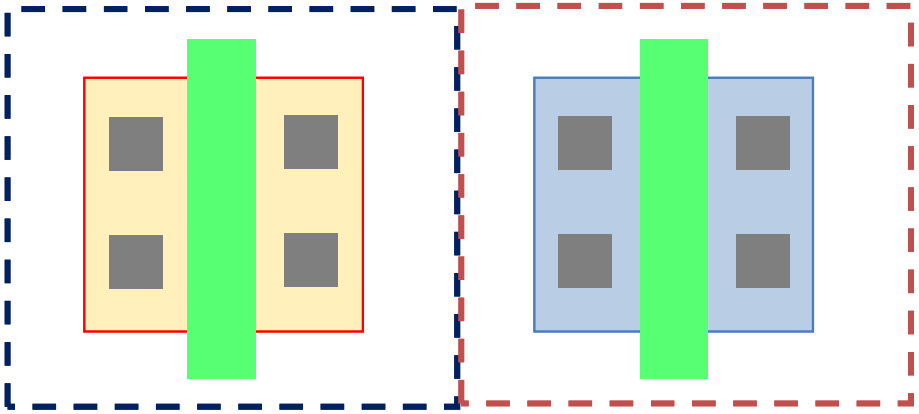




Layout Shrink（Active Merge)

Bulk CMOS

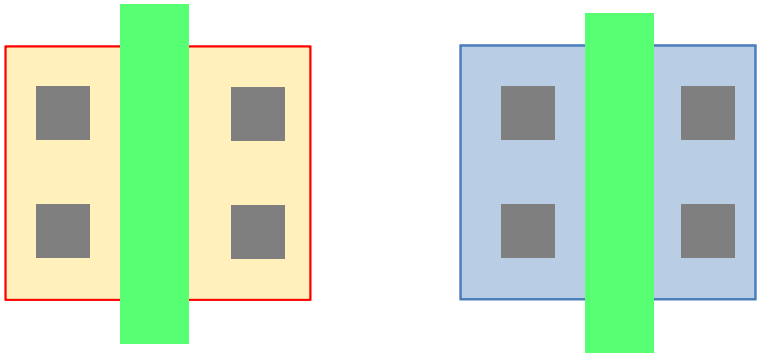
PMOS NMOS



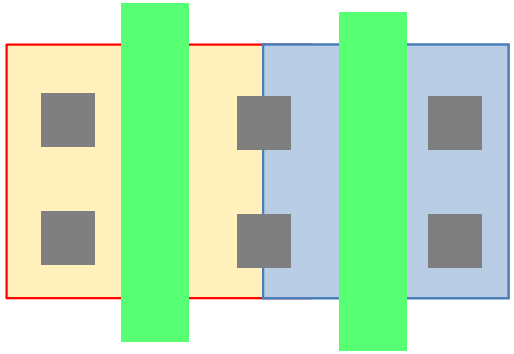
N-Well P-Well

SOI

PMOS NMOS



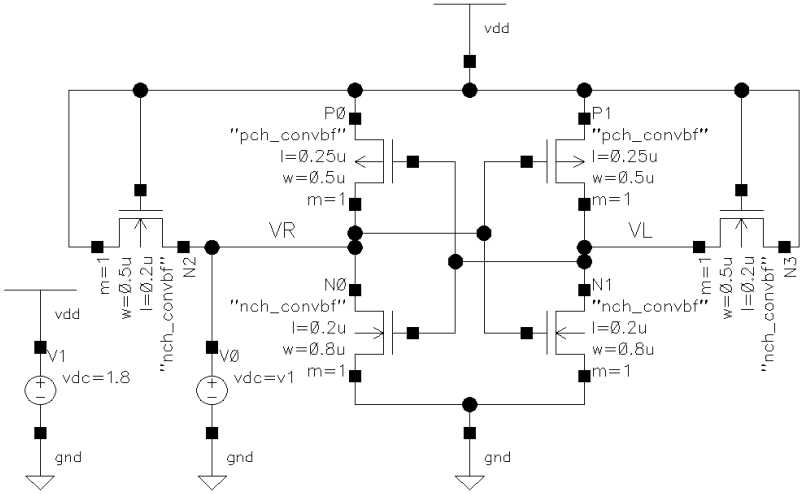
Share Contacts

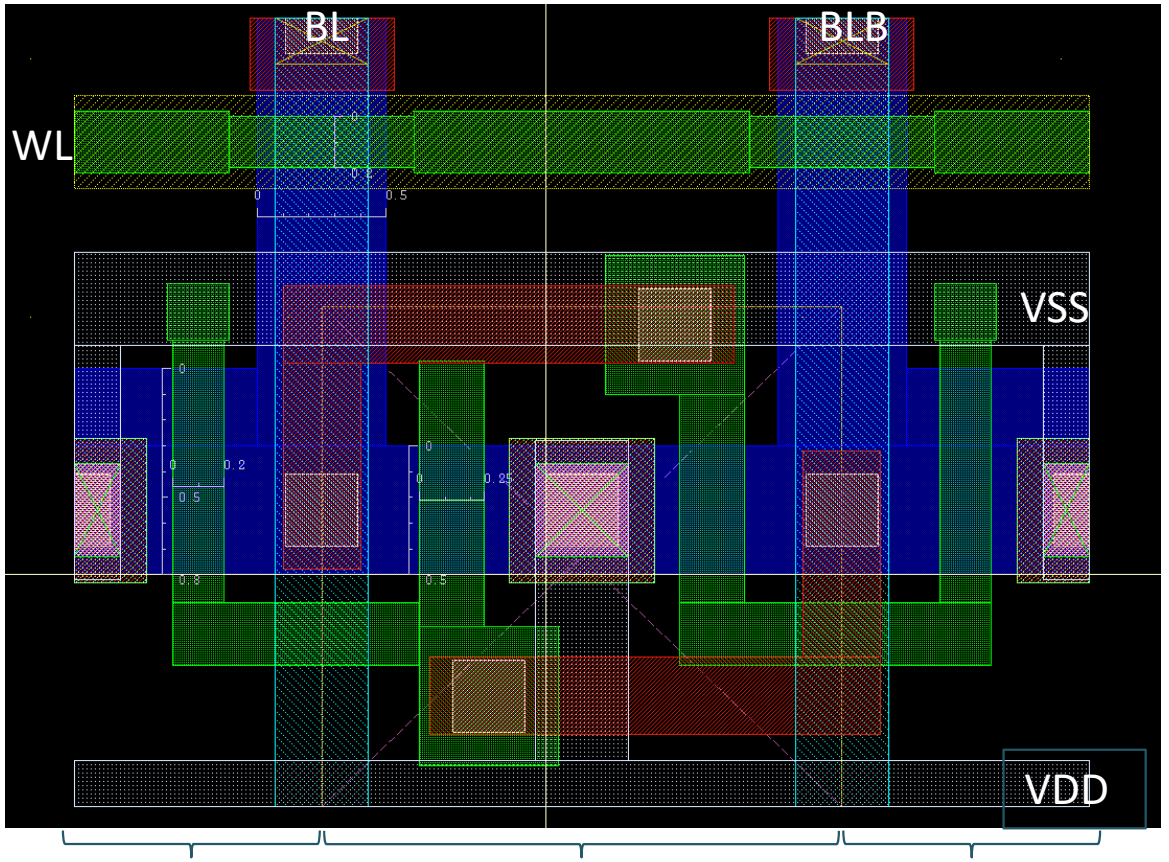


Salicide Connection

In the SOI process, it is possible to merge NMOS & PMOS Active region and share contacts.

Single Port SRAM Bit Cell

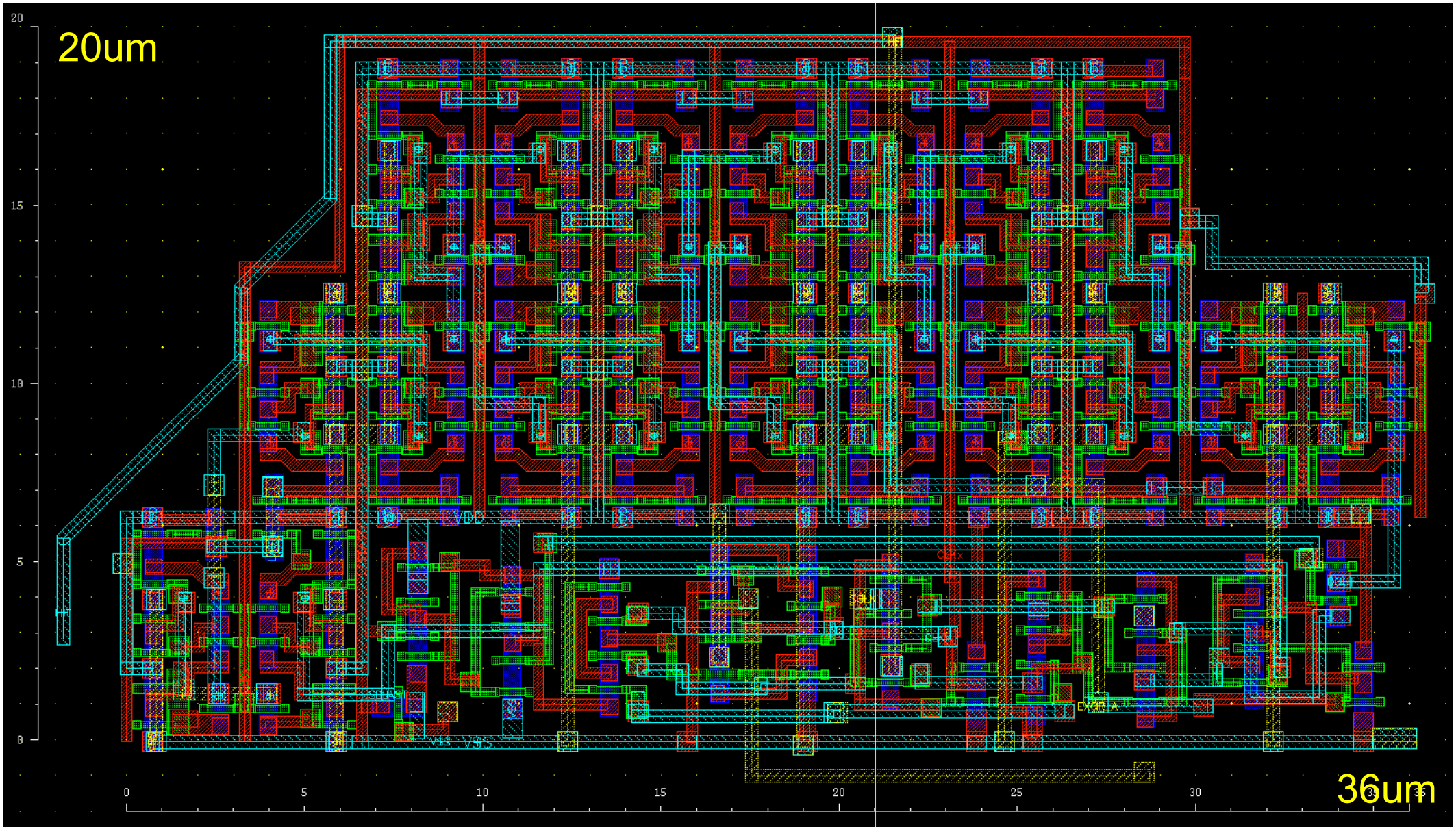


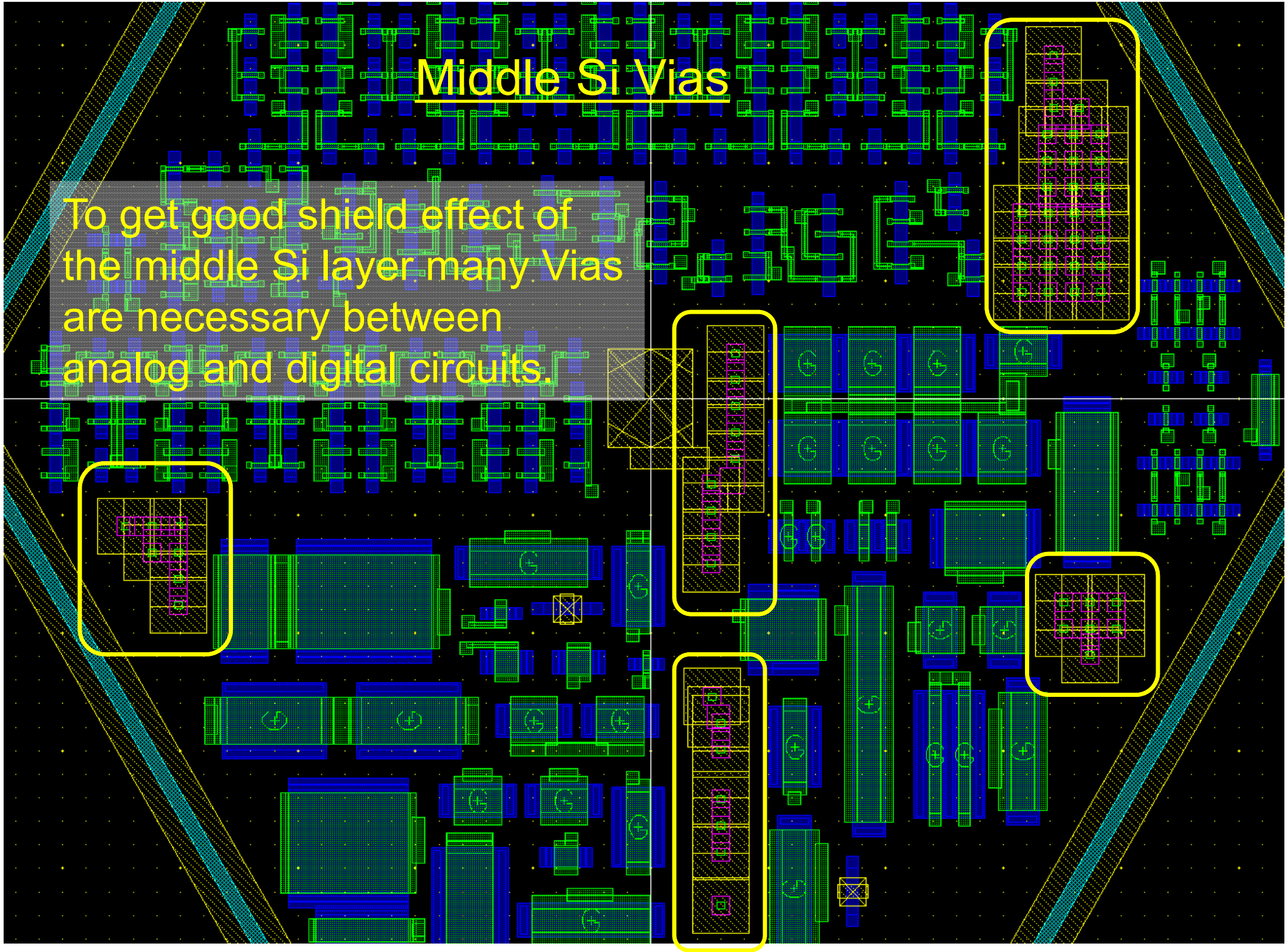


(designed by I. Kurachi)

Cell Size : 3.94μm X 3.06μm = 12.06μm²

18bit Counter + Overflow bit with Serial I/O



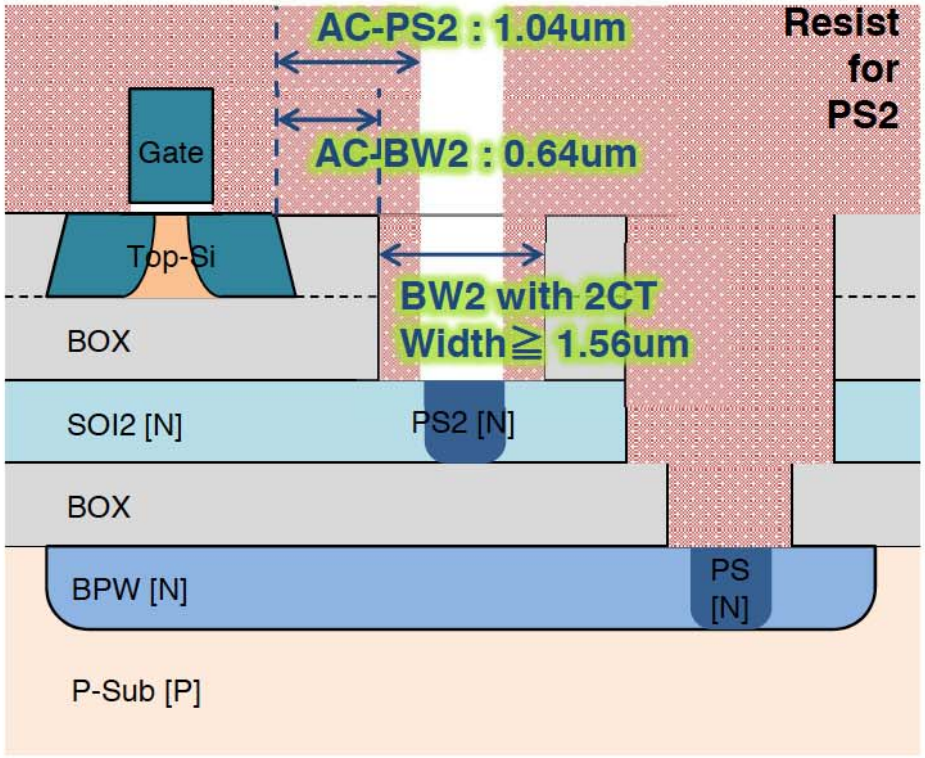

Middle Si Vias
To get good shield effect of the middle Si layer many Vias are necessary between analog and digital circuits.

PS2基準縮小

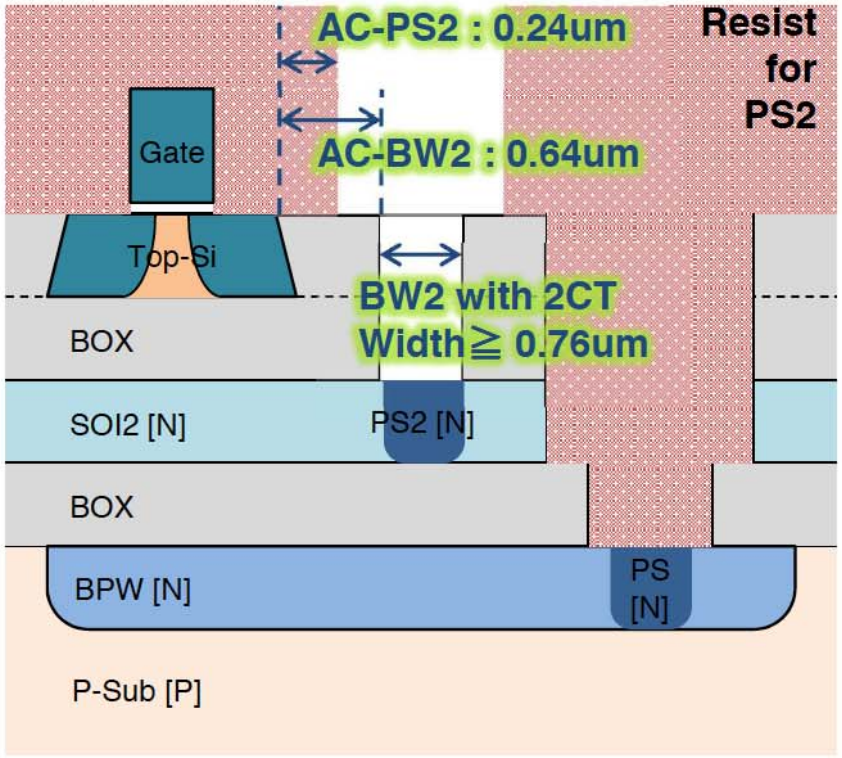
From Next MPW run, design rule for the middle Si Via will be shrunken from 1.56um to 0.76um.

現行ではPS2の外側にBW2を発生させているが、内側にBW2を発生させることで、
BW2最小幅が 1.4 ⇒ 0.6um に、2CT有の場合は 1.56 ⇒ 0.76um に縮小。
（但し、AC-BW2距離は変わらない）
PS2はBW2でエッチングされた領域にセルフアラインで注入される。

a) 現行の断面図@PS2ホトリソ



b) 提案の断面図@PS2ホトリソ



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摘要

- We, IHEP and KEK team, designed new counting-type X-ray pixel detector.
- The pixel size of our 0.2um SOI process is smaller than that of 0.13um CMOS process by using NMOS/PMOS active merge technique.

  Size of counting-type pixel is smallest in the world !

- To relax charge sharing effect, we adopted hexagonal shape pixel, and to solve charge sharing issue, new compare circuit is designed.
- Further shrink or better performance may be possible by introducing smaller SOI2 VIA rule.