

Silicon Hit Position Studies

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Silicon Tracker Study Meeting, July 28, 2016

Outline of presentation:

- Introduction.
- Silicon Hit position in CEPC V1
- Resolutions in full silicon option CEPCSI V4
- To-do list

Introduction

- Latest instructions can be found at http://cepc.ihep.ac.cn/cepc/cepc_twiki/index.php/Pure_Silicon

Motivation

There are two design options for ILC detectors, ILD and SID, with very different design approaches. But the overall detector performance at the end is quite similar. In the preCDR initial study, the ILD detector has been adopted as the starting point for the CEPC detector design. In this study, we will start with the basic design of ILD silicon detectors (VXD, STT, FTD) and replacing TPC with additional silicon layers as an alternative all-silicon tracker option for CEPC as CEPC-SID. We have implemented it in full simulation and have made reconstruction working.

The initial performance is encouraging, see the slides. (<http://indico.ihep.ac.cn/event/6218/contribution/1/material/slides/0.pdf>)

Instructions for Mokka Simulation

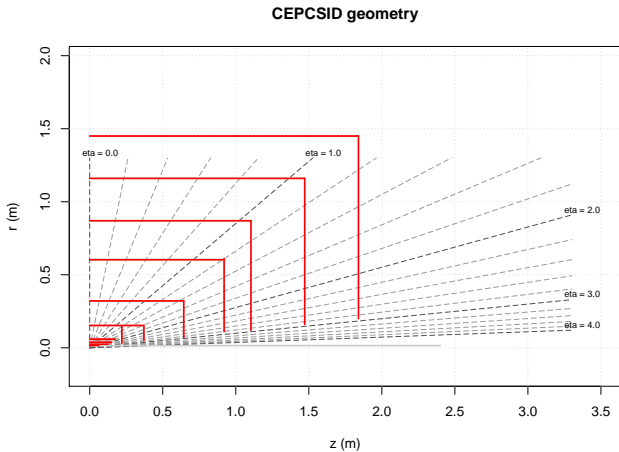
1. copy `/workfs/bes/fucd/Mokka/mokka-08-03/env.sh`
2. copy `/workfs/bes/fucd/Mokka/mokka-08-03/test/cepc_new4_macro`
3. copy `/afs/ihep.ac.cn/users/y/yaowm/Mycepc/cepsi/event_macro`
4. copy `/afs/ihep.ac.cn/users/y/yaowm/Mycepc/cepsi/job_cepsi.sh`
5. source `env.sh`
6. source `job_cepsi.sh`
7. Simulated single muon sample can be found at `/besfs/groups/higgs/users/yaowm/cepsi_new4.slicio`

Instructions for Marlin Reconstruction

1. copy `GearOutput.xml` from simulation area above
2. copy `/afs/ihep.ac.cn/users/y/yaowm/Mycepc/test/MarlinReco/reco_cepsi_new4X_example.xml`
3. copy `/afs/ihep.ac.cn/users/y/yaowm/Mycepc/test/MarlinReco/job.sh`
4. source `job.sh`
5. Reconstructed single muon sample can be found at `/besfs/groups/higgs/users/yaowm/cepsiRec_new4.slicio`

Silicon tracker concept

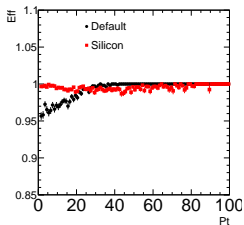
- CEPC full silicon option



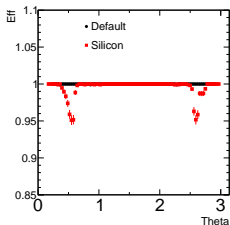
(b) CEPCSID

Tracking Efficiencies

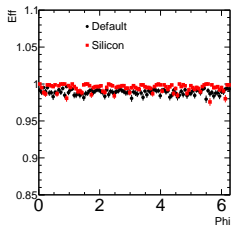
- Requiring $P_T > 1.0$ GeV and $2.96 < \theta < 0.18$.
- Tracking efficiency is slight lower in barrel and endcap overlap region.



(a) pt



(b) theta

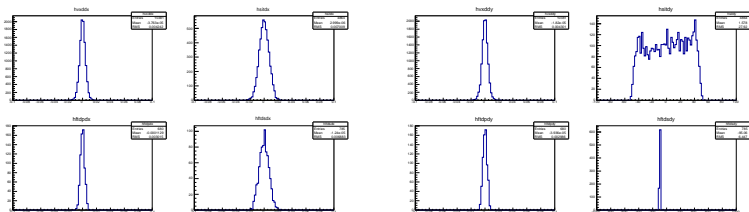


(c) phi

Figure: Efficiencies vs pt, theta and phi

Silicon Hit Resolution in CEPCV1

- Check hit resolution in each detector (VXD, SID, FTDPixel, FTDSrip)



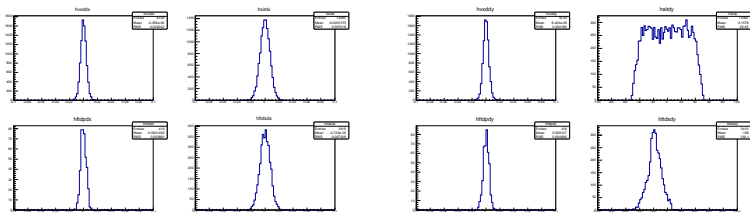
(a) dU

(b) dV

Figure: Resolutions in dU and dV, FTD strip seems offset by 10 cm in dV.

Silicon Hit Resolution in CEPCSI4

- Check hit resolution in each detector (VXD, SID, FTDPixel, FTDSrip)



(a) dU

(b) dV

Figure: Resolutions in dU and dV, the FTD strip seems offset 10 cm in dV

To-do List

- There seems an offset of 10 cm for FTD strip position in dV, which needs to fix.
- The offset seems caused failing in track fitting.
- Few more questions:
 - To check if the feature presents in ILD simulation.
 - Are we simulating the hits at detector level including digitalization and clustering ?
 - Are the hits merged when they are overlap ?
 - Is there way to implement the misalignment in simulation ?
 - ...