The CMS ECAL Upgrade
for Precision Crystal Calorimetry at the HL-LHC

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for the CMS Collaboration

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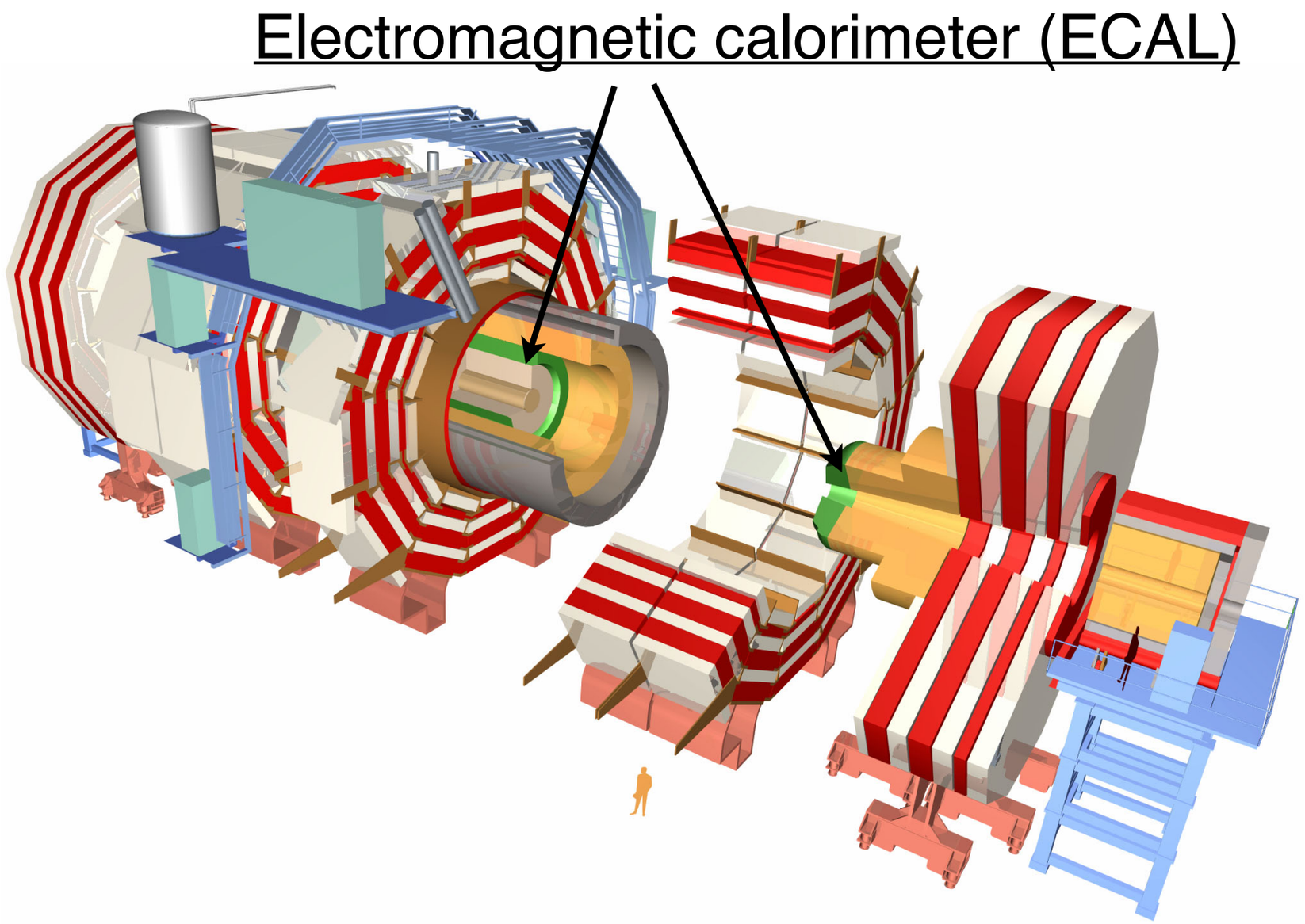
1. Current Detector

The ECAL in CMS
Elements of the ECAL
Physics Output Involving ECAL

The CMS Detector and the ECAL

CMS:

Length: 21.5m
Diameter: 15m
Weight: 14kT
Magnetic field: 3.8T



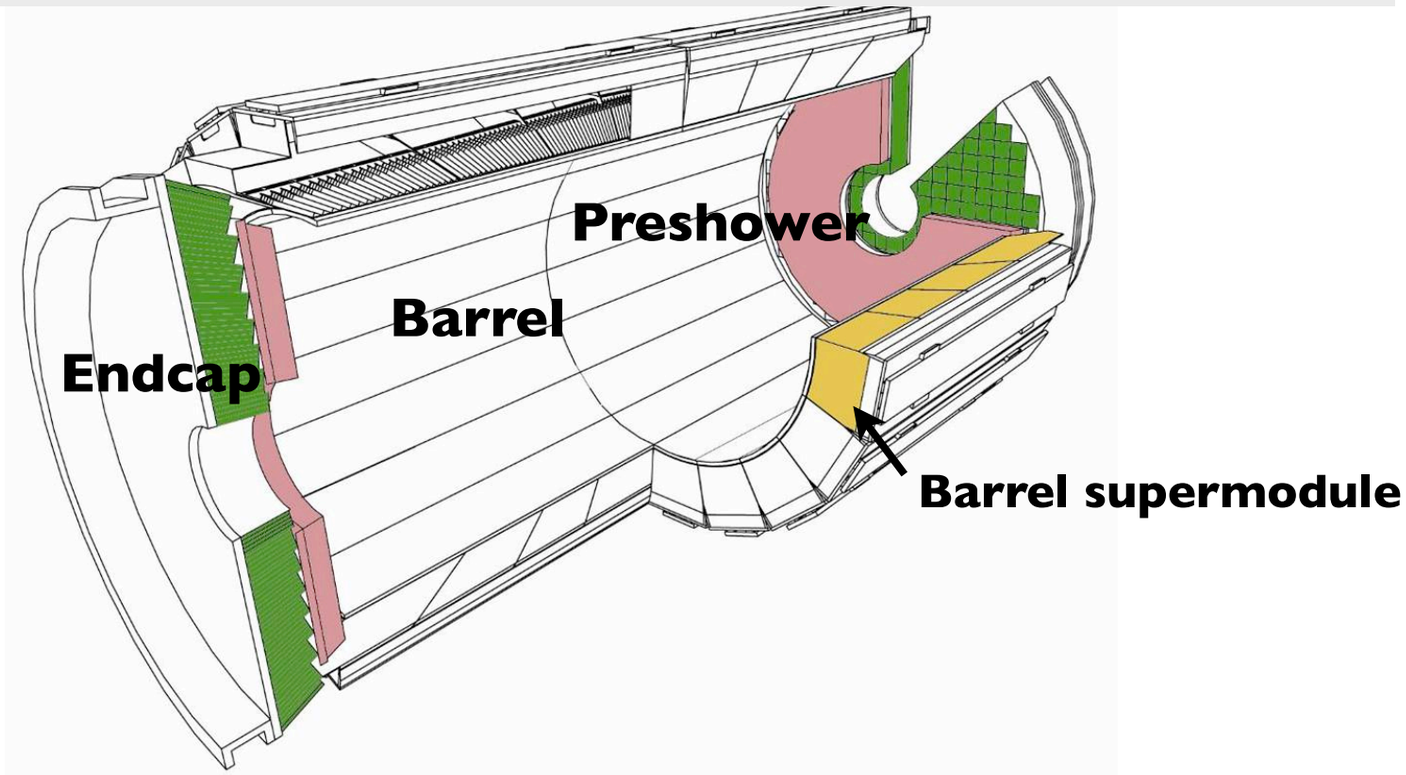
ECAL: the main component of CMS to **detect and precisely measure** the energies of **electrons and photons**.

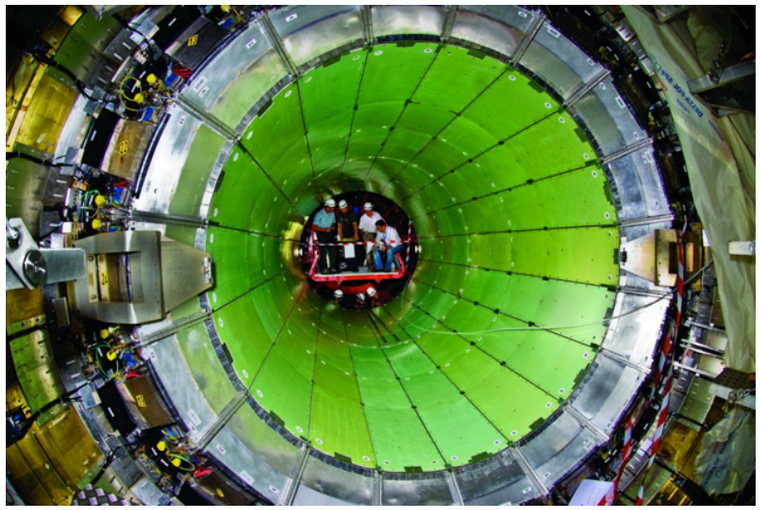
Goal: **excellent diphoton mass resolution** (~1%), needed for H→γγ observation

The CMS Electromagnetic Calorimeter

Crystal Barrel & Endcaps ($PbWO_4$) + Lead/Si Preshower

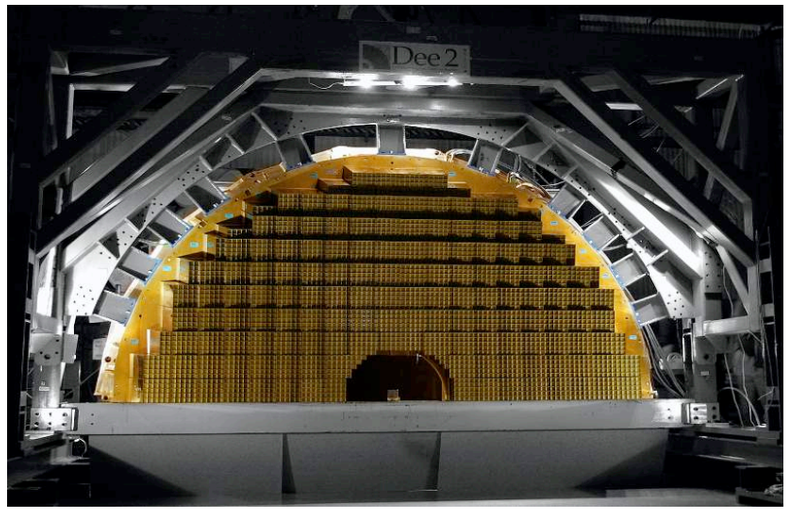
Two crystal producers:
BTCP (Russia)
SIC (China)





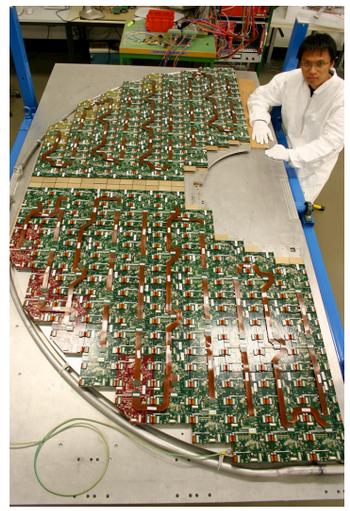
Barrel (EB)

36 supermodules (1700 crystals)
Total of 61200 $PbWO_4$ crystals
Avalanche PhotoDiode readout
coverage: $|\eta|<1.48$



Endcap (EE)

4 half-disk Dees (3662 xtals)
Total of 14648 $PbWO_4$ crystals
Vacuum PhotoTriode readout
coverage: $1.48<|\eta|<3.0$

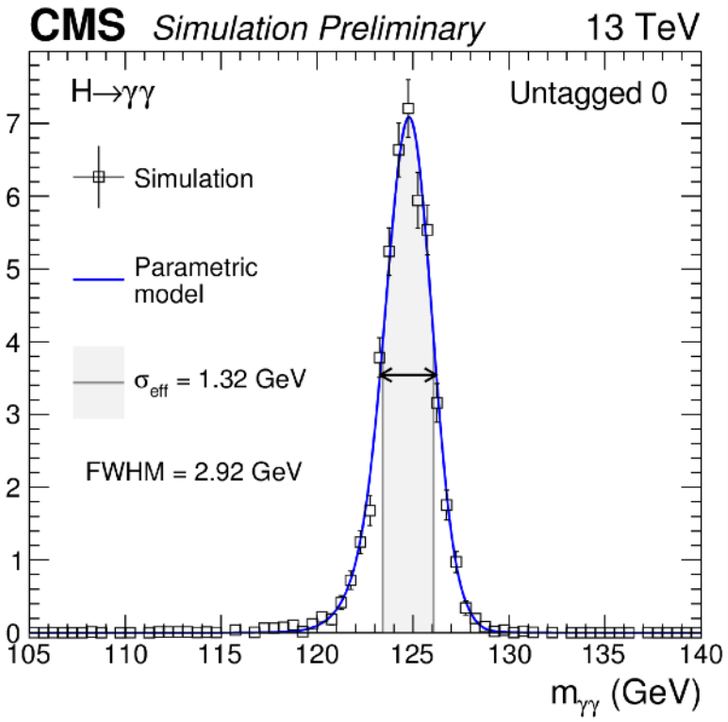


Preshower (ES)

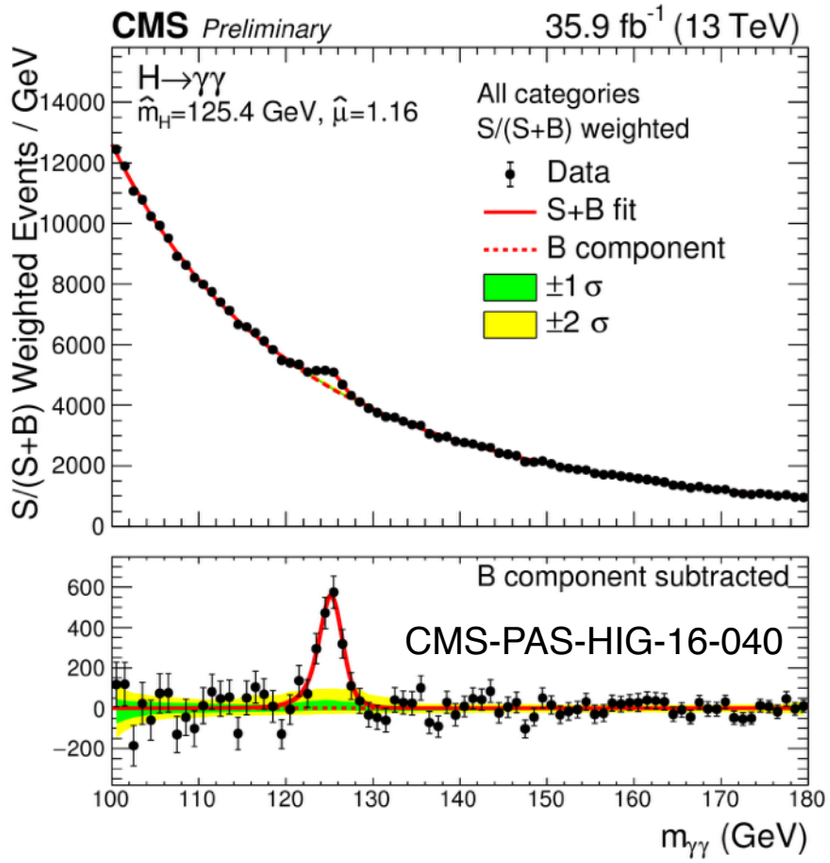
Two Lead/Si planes
137216 Si strips ($1.8 \times 61 mm^2$)
coverage: $1.65<|\eta|<2.6$

Physics output

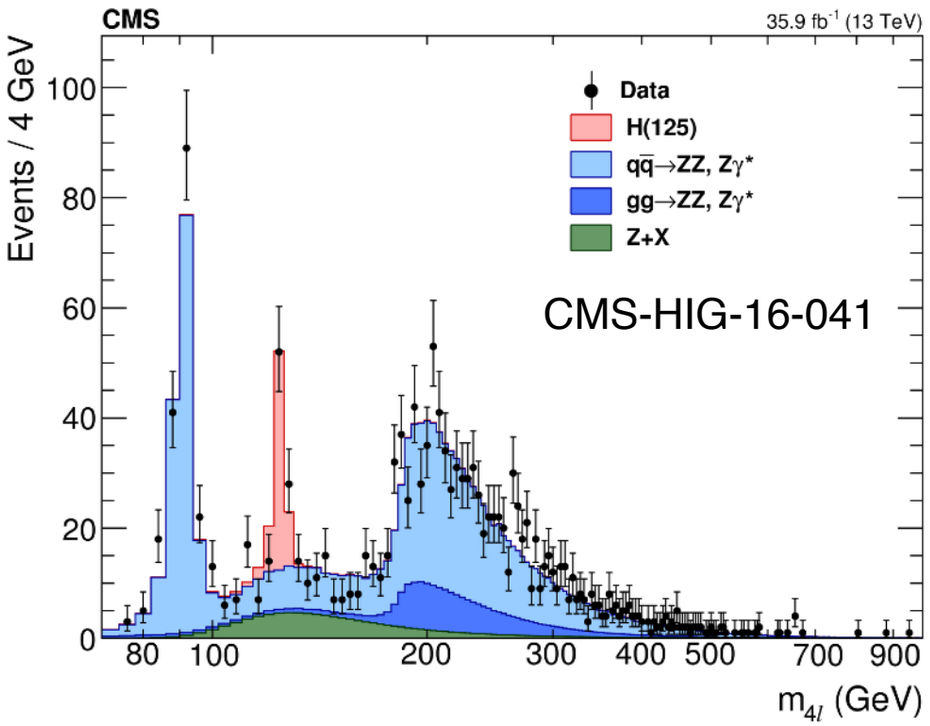
H→γγ



Mass resolution in best category ~1%



H→ZZ→4l



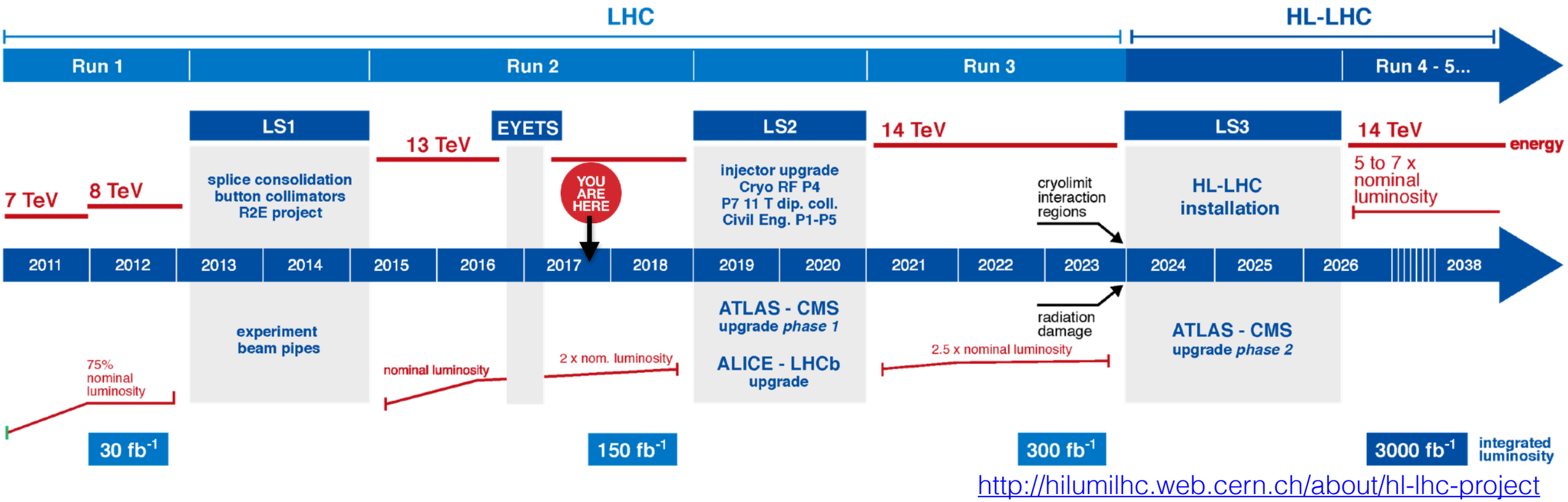
The **excellent resolution and electron/photon ID** of the CMS ECAL was crucial in the discovery and subsequent characterisation of the **125 GeV Higgs Boson**

The **continued excellent performance** of ECAL in the **entire pseudorapidity range** is a key component of many **searches for new Physics**

2. The High Luminosity LHC upgrade (HL-LHC)

The HL-LHC Programme
ECAL Longevity
Detector Requirements for HL-LHC
The ECAL Barrel Upgrade Scope

HL-LHC upgrade plan



http://hilumilhc.web.cern.ch/about/hl-lhc-project

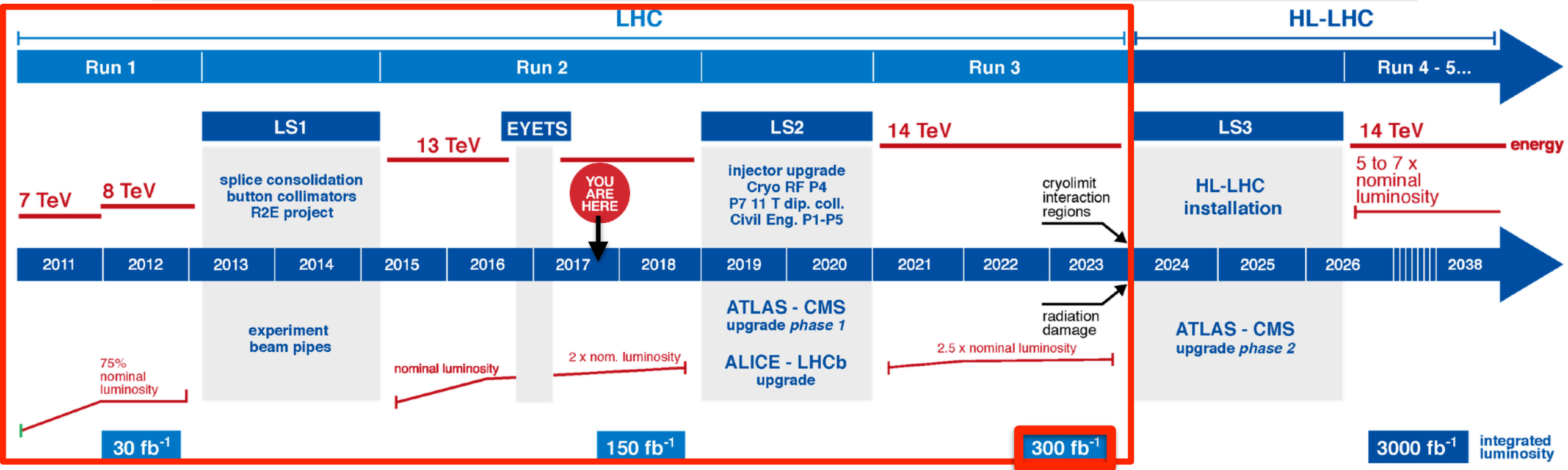
HL-LHC: accelerator upgrade in LS3 to provide **x10 larger dataset** for physics
focus on new physics searches, Higgs coupling and precision SM measurements

Large increases in peak lumi, integrated dose relative to LHC:

	Inst. lumi ($cm^{-2}s^{-1}$)	peak pileup	integ. lumi (fb^{-1}/yr)
today (2017)	1.7×10^{34}	50	40-50
HL-LHC (baseline)	5×10^{34}	140	250
HL-LHC (stretch goal)	7.5×10^{34}	200	320

R. Tomas presentation at Chamonix 2017

HL-LHC upgrade plan



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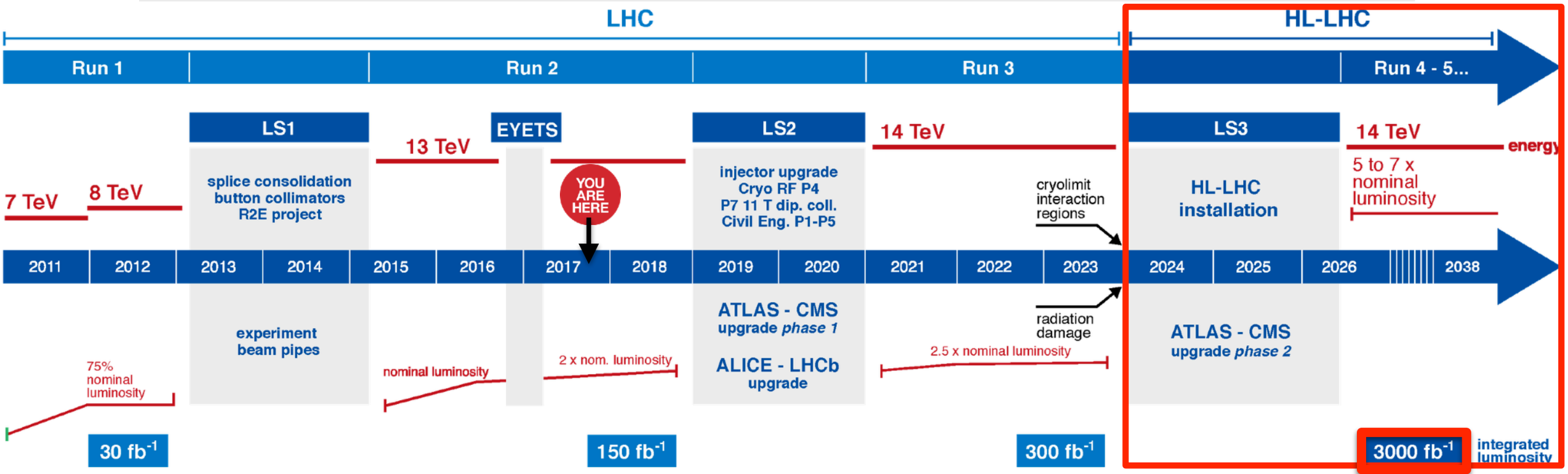

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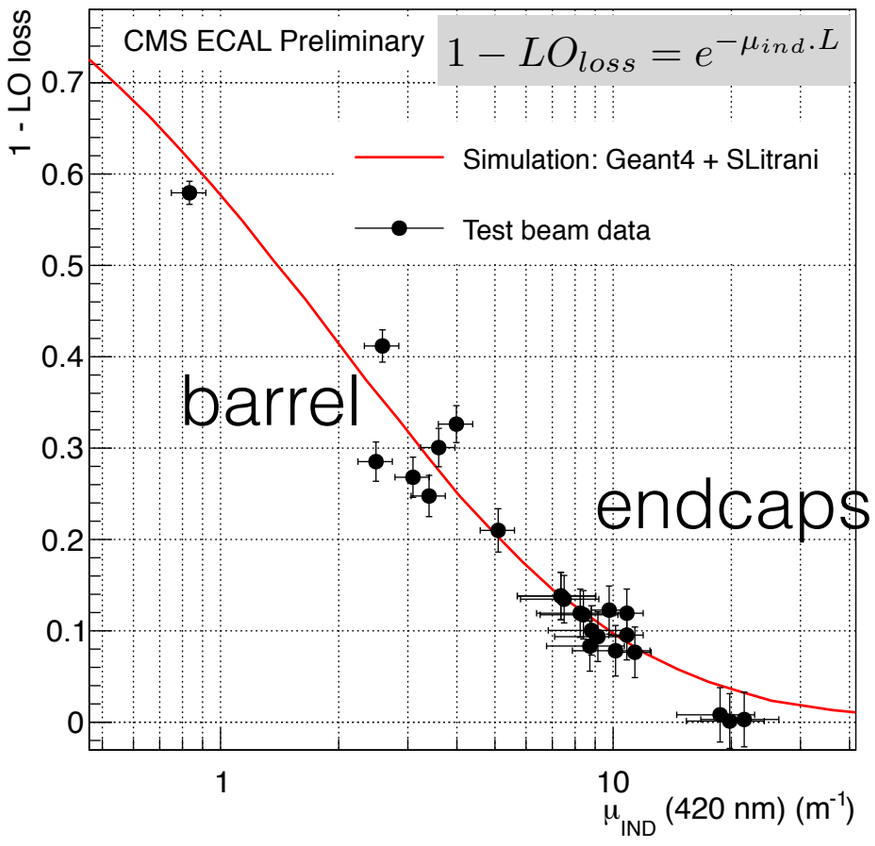
R. Tomas presentation at Chamonix 2017

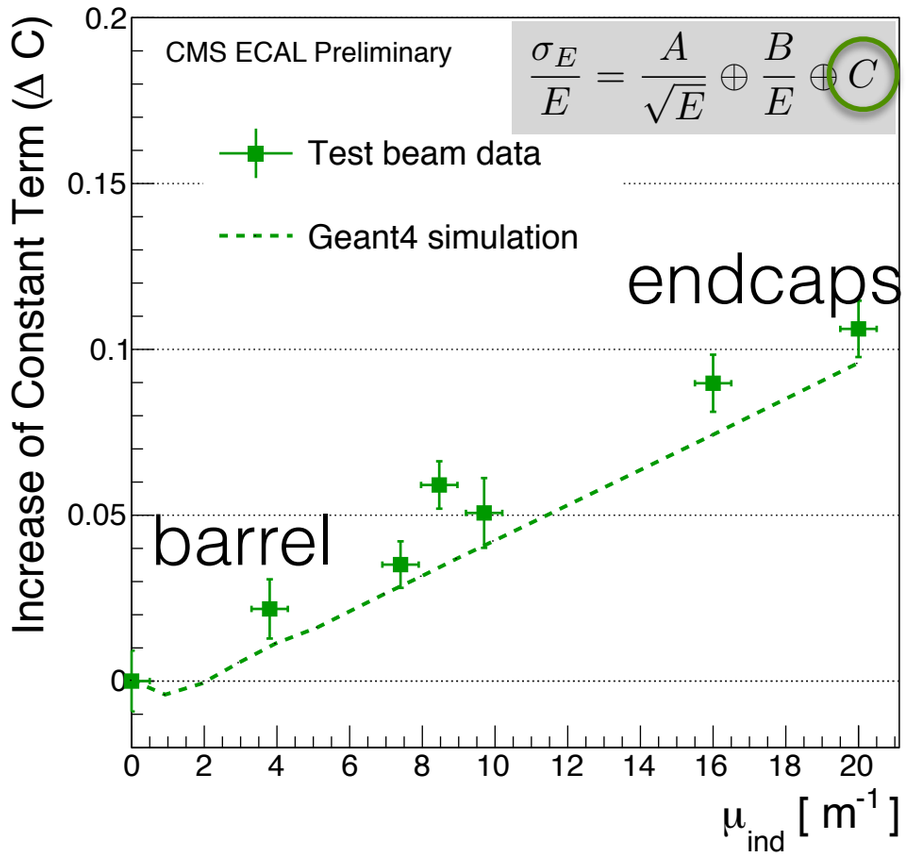
ECAL lead tungstate crystal performance

Main effect at HL-LHC due to hadron irradiation

Loss of light output



Degradation of energy resolution



Barrel crystals will perform well during HL-LHC:

will retain ~50% of light after 3000fb^{-1}

small degradation of energy resolution

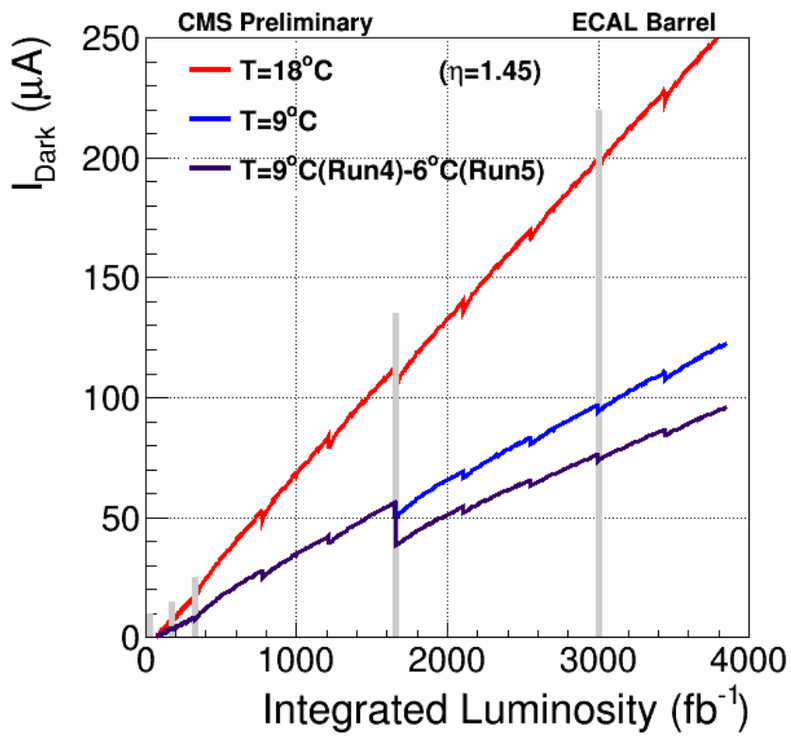
Endcaps will suffer large light output losses

will be replaced by High granularity calorimeter for HL-LHC

(see Luca Mastrolorenzo talk)

ECAL APD performance

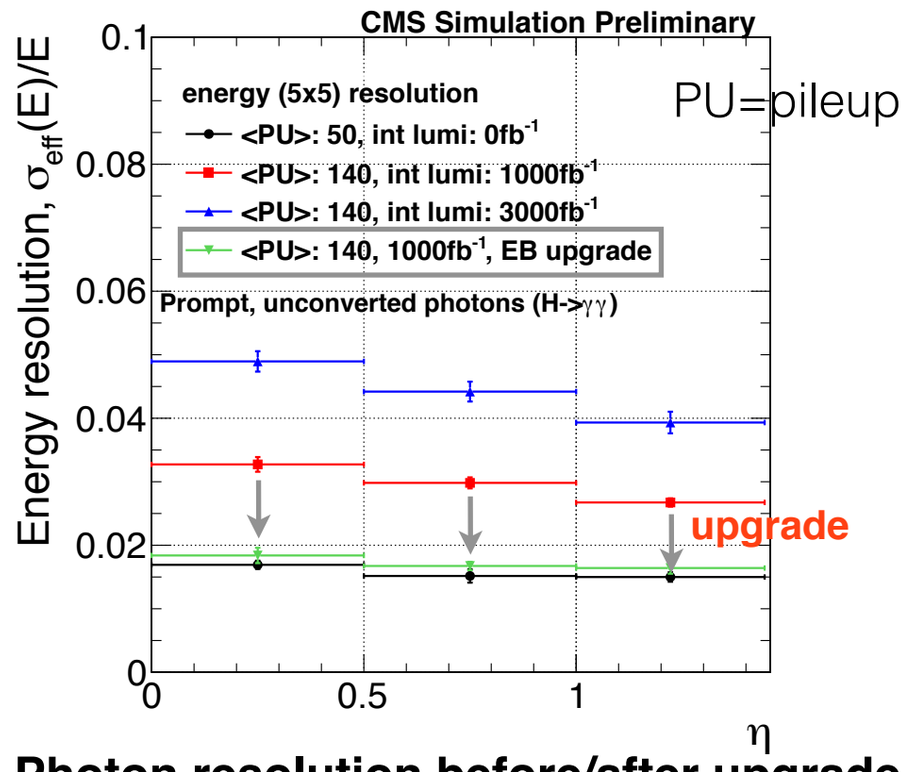
- **APDs will continue to operate well during HL-LHC**
  - but will experience **larger leakage currents** due to LHC irradiation
  - increase in **noise (x10) would dominate resolution** for HL-LHC luminosities



- **Mitigation strategy:**
  - **Cool supermodules** from 18° to 9°C
  - Implement **shorter pulse shaping** in a new front-end pre-amplifier
  - Explore possibility of **running even colder** after LS4

These upgrades are necessary to maintain good electron/photon resolution during HL-LHC running

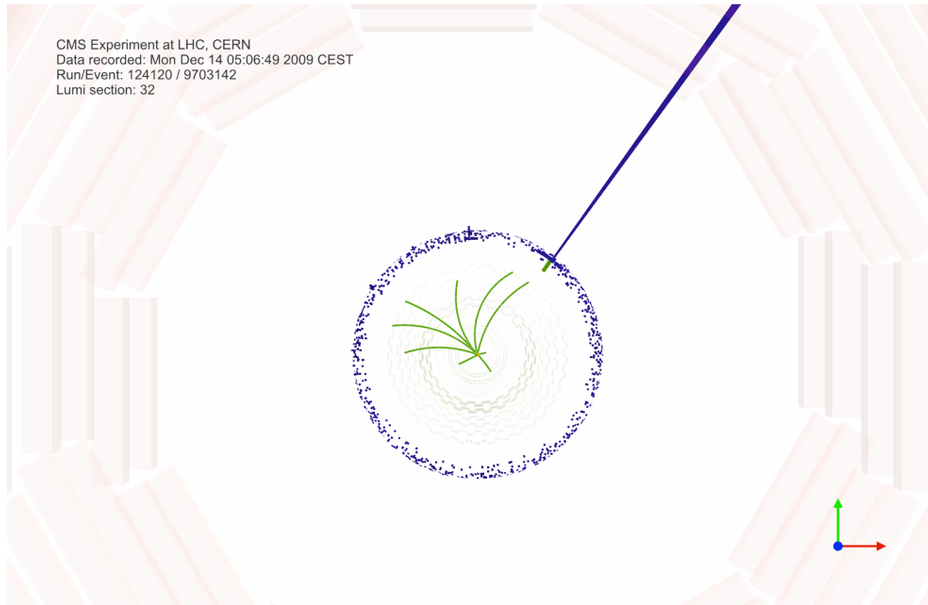
Predicted APD dark current in HL-LHC



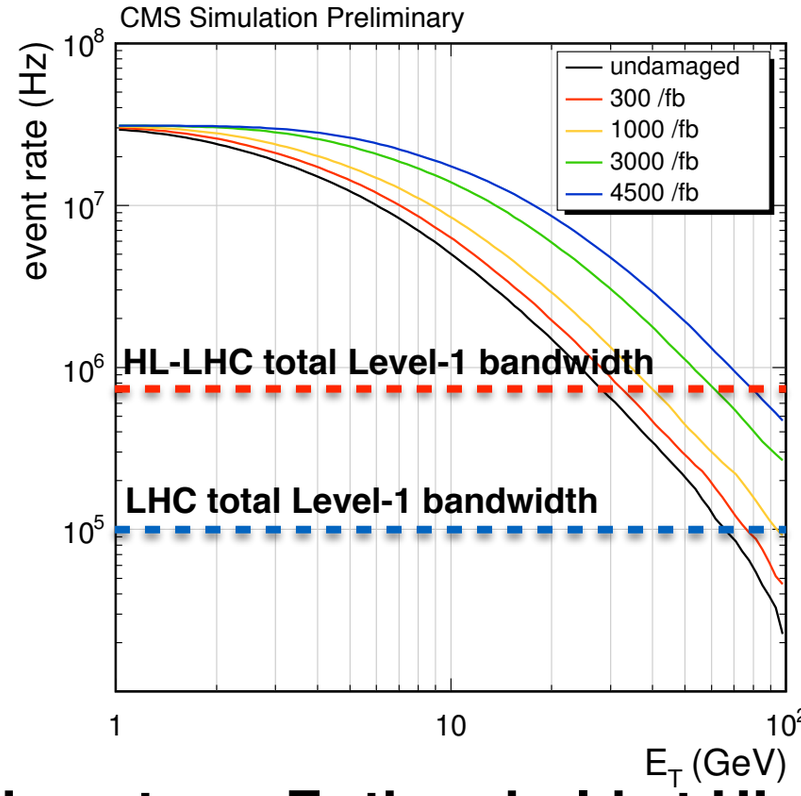
Photon resolution before/after upgrade, from CMS Technical Proposal

ECAL triggering

- **Improved Level-1 trigger capabilities needed at HL-LHC**
  - larger trigger **rates** and trigger **latencies mandatory** to exploit larger luminosity and implement Level-1 track-trigger
  - **requires replacement of ECAL front-end and off-detector electronics**
- **Improved rejection of ECAL APD anomalous signals required**
  - "**spike**": large isolated signal due to hadron interactions within APD volume
  - will **dominate** L1 trigger rate at HL-LHC if unsuppressed
  - **improved spike rejection needed in re-designed on-detector electronics**



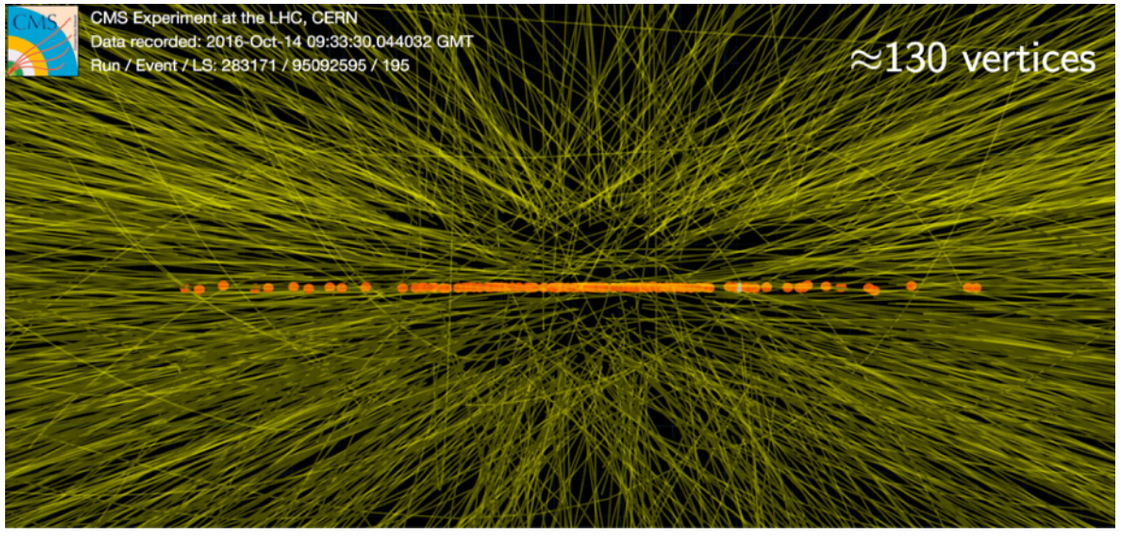
APD spike in CMS



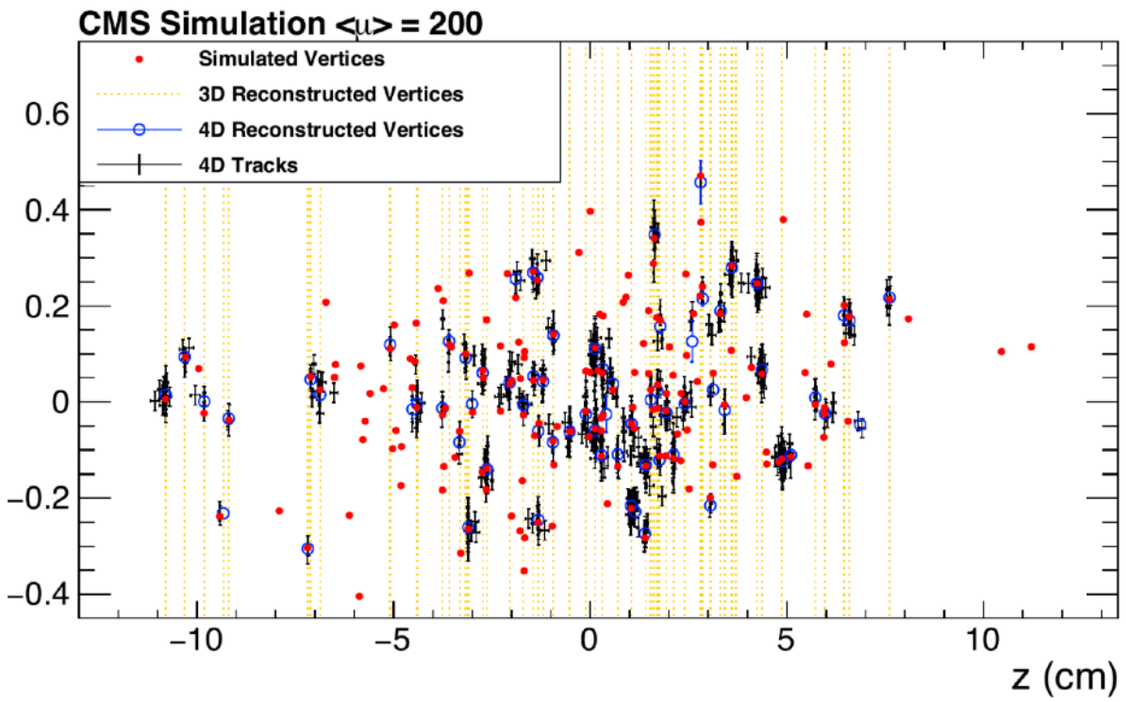
Spike rate vs E_T threshold at HL-LHC

Pileup and precise timing

- **Maintaining reconstruction performance at high pileup is a challenge**
  - reduced primary vertex efficiency from H→γγ decays affects sensitivity for pileup=200
- **Improved vertex localisation possible with precise (~30ps) timing capability**
  - both in the calorimeters (ECAL and HGCAL) and for charged particles (MIPs)
  - **precise timing capability needs to be considered in ECAL upgrade electronics design**
  - **See Paolo Meridiani talk for further details**



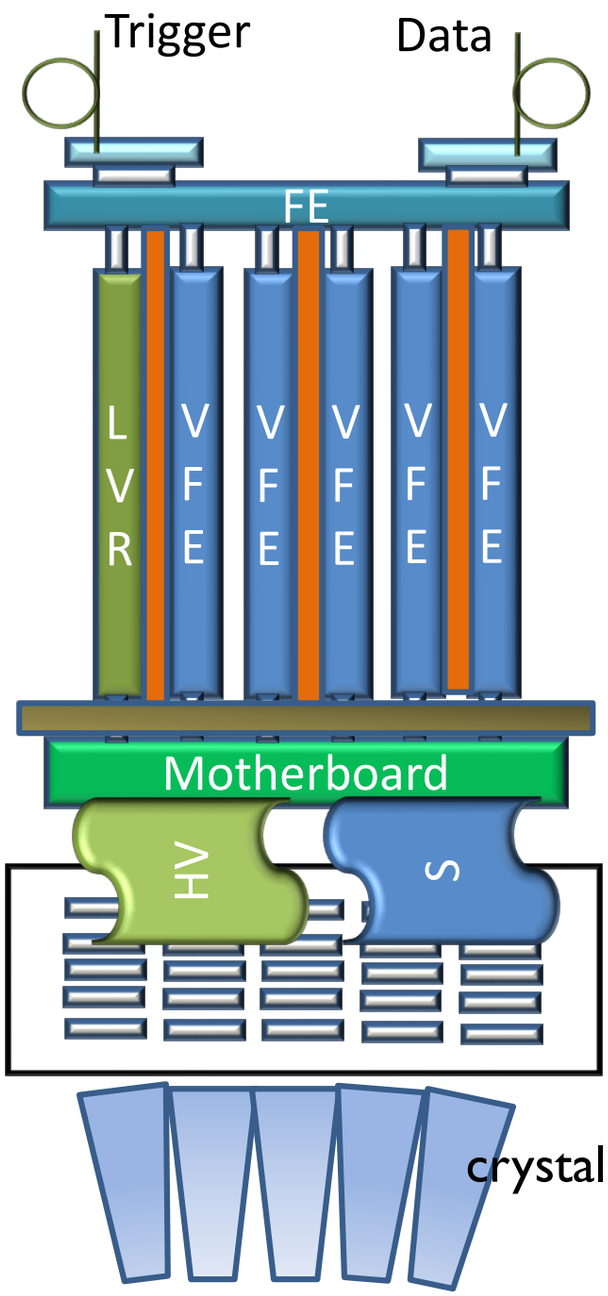
CMS event with 130 reconstructed vertices



Distribution of vertices in space and time for a simulated event with pileup=200

ECAL Barrel upgrade scope

- **<u>Refurbish Barrel Supermodules during Long Shutdown 3 (2024-6)</u>**
  - **Replace Front-End (FE) and Very-Front-End (VFE) readout**
    - to cope with challenging HL-LHC conditions (noise, pileup, APD spikes).
    - Explore possibility of precise (~30ps) timing measurements for high energy photons.
  - **Run colder** to mitigate increase in radiation induced APD dark current
  - **New off-detector (OD) readout** to cope with higher output bandwidth from FE
  - **<u>Crystals + APDs will be retained</u>**
- **<u>The upgrade is needed to retain the excellent ECAL performance in Phase II</u>**



ECAL barrel "trigger tower" (25 crystals)

3. ECAL barrel upgrade R&D status

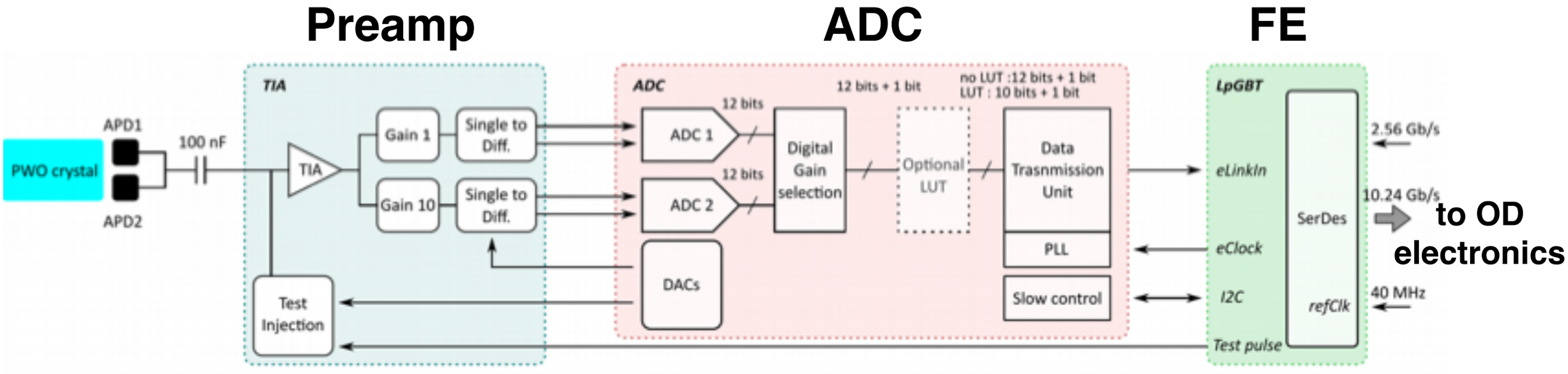
Architecture of the On-Detector Upgrade
Test results from Prototype Devices
ECAL Trigger Upgrade
Supermodule Refurbishment and Cooling

Recent design choices

- **We have made the architecture choices for the ECAL upgrade on-detector electronics**
  - **chose Trans Impedance Amplifier (TIA) architecture**
    - **this design meets the physics requirements of HL-LHC**
  - **focus on fast timing, consistent with CMS goals for HL-LHC**
    - **30 ps resolution @ ~30 GeV achieved in test beams**
    - **requires 160 MHz sampling ADC**
  - **Analogue to Digital Converter (ADC) design clarified**
    - **using commercial ADC core + data compression**
  - **Front End card design**
    - **transfer crystal data off-detector using high-speed optical links**
      - **using CERN GBT/VL+ chipsets**

Decisions documented in Barrel Calorimeter Technical Design Report

EB Phase II architecture

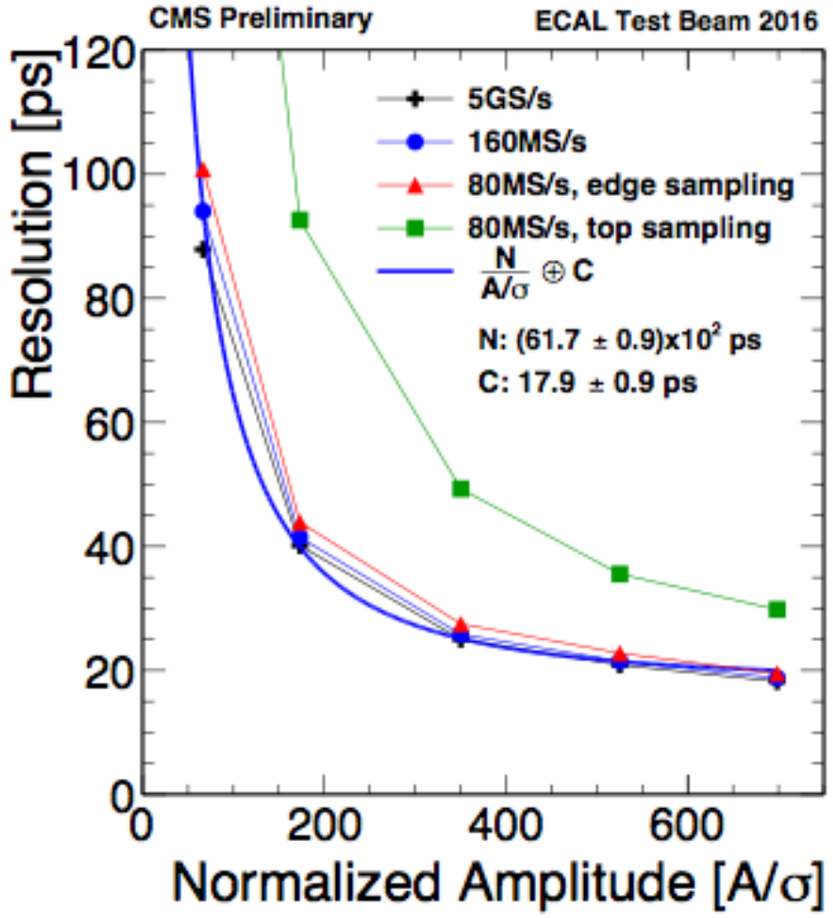


- **<u>TIA preamp:</u>**
  - Two gain ranges (G1,G10). 2 TeV dynamic range with 50 MeV LSB
- **<u>ADC</u>**
  - 12 bit, 160 MHz sampling, dual channel with gain selection logic
  - Data Transmission Unit (DTU) implements data compression before FE
- **<u>FE</u>**
  - lpGBT (4x10.24 Gb/s data links, 1x2.56 Gb/s control link)
  - eLink serial interface to ADC, clock and i2C interface
- **<u>Low voltage regulator (LVR):</u>**
  - needed voltages (1.2, 2.5V) supplied by point-of-load FEAST DC/DC converters

Preamp ASIC R&D progress

Timing resolution of discrete component TIA

in H4 test beam



30 ps resolution achieved

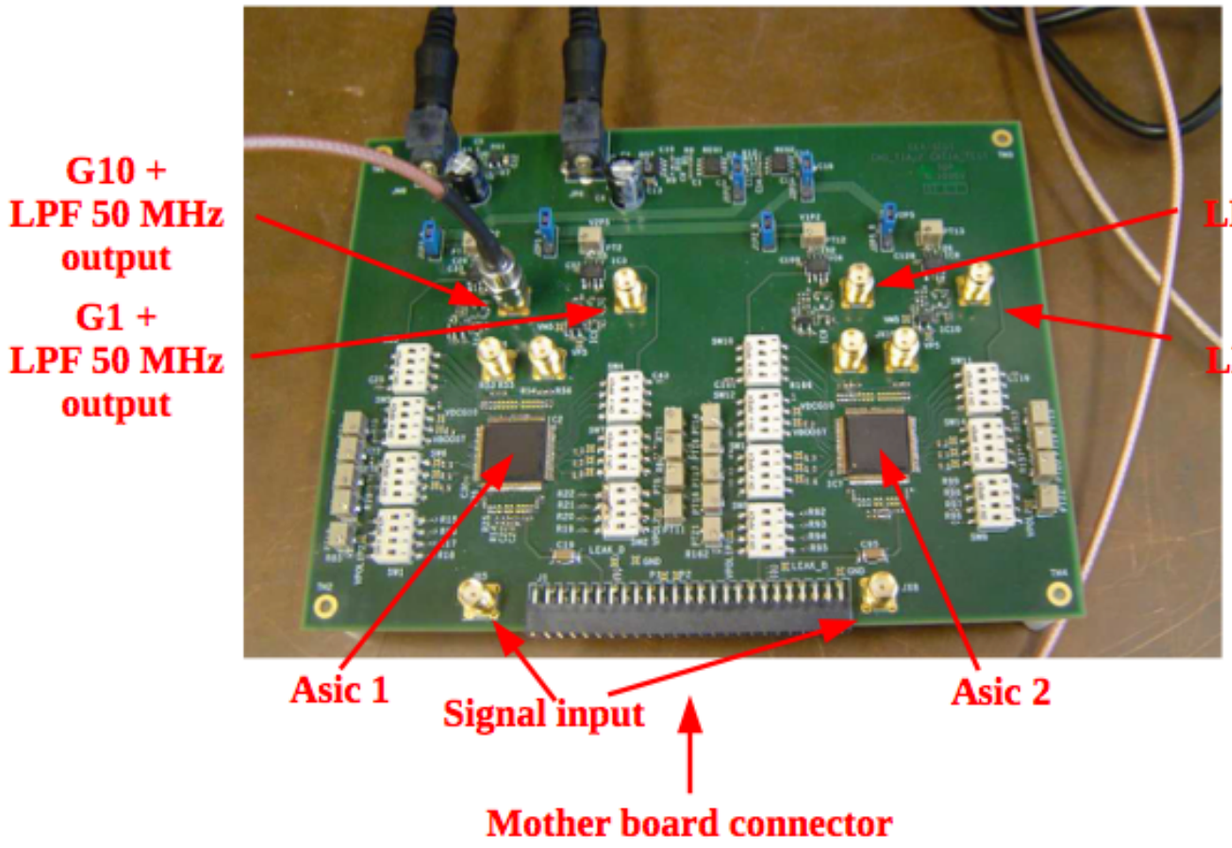
Needs 160 MHz sampling

30 ps resolution reached at:

25 GeV (HL-LHC start)

60 GeV (HL-LHC end)

First bench tests of TIA ASIC: CATIA (CAlorimeter TIA)



Silicon received from TSMC, packaged and tested in the lab

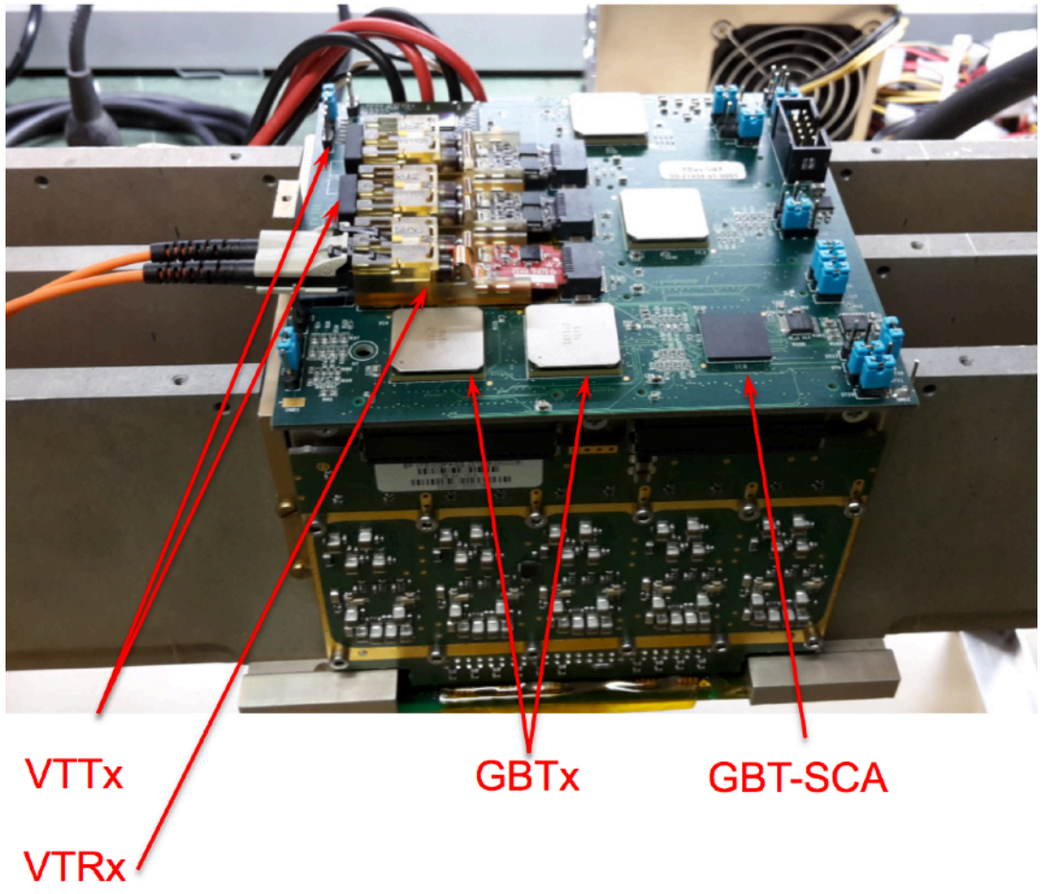
very promising noise performance

will go to test beam later this year

Front End card design

- **“streaming” FE**
  - **all crystal data transferred from VFE to off-detector electronics.**
  - **Trigger primitive formation in off-detector FPGA. No latency buffer/pipeline.**
- **Data rates:**
  - **~30 GB/s per 25 channels (with data compression)**
  - **fits in four 10 Gb/s lpGBT links**
- **FE demonstrator with GBT chipset being tested**
  - **with legacy VFE, using Phase I trigger board for DAQ**

FE demonstrator



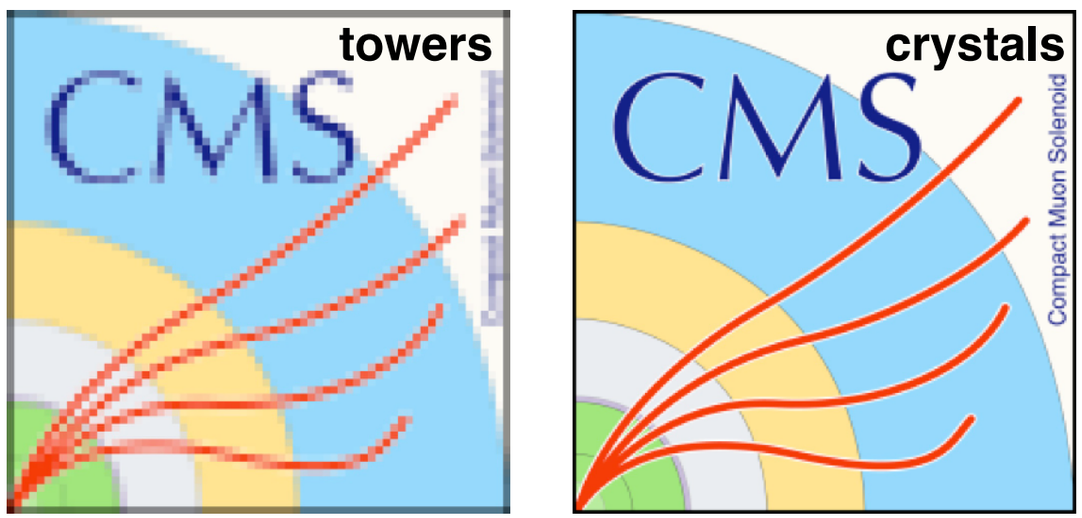
will be exercised in test beams with prototype upgrade VFE

GBT: GigaBit Transceiver
http://cds.cern.ch/record/1235836

ECAL trigger upgrade

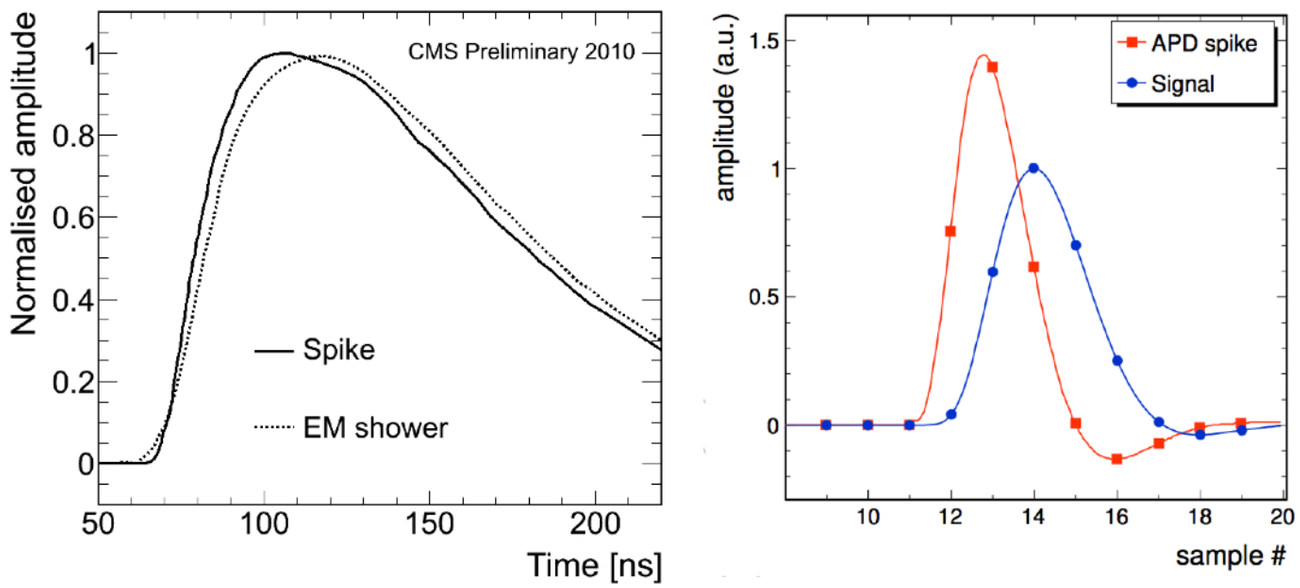
- **<u>ECAL upgrade will replace on-detector and off-detector electronics</u>**
- **<u>This will provide improved information to the Level-1 trigger</u>**
  - **Full ECAL granularity** available to L1 trigger (**improved by factor of 25)**
    - **Advanced clustering algorithms possible** in new off-detector electronics
      - with matching to Level-1 tracks— <u>implement particle flow algorithms at L1</u>
  - **Much improved rejection of spikes** in the EB photodetectors
    - due to new on-detector electronics with shorter pulse shaping

<u>Current</u> **<u>Upgrade</u>**



25x better trigger granularity

<u>Current</u> **<u>Upgrade</u>**

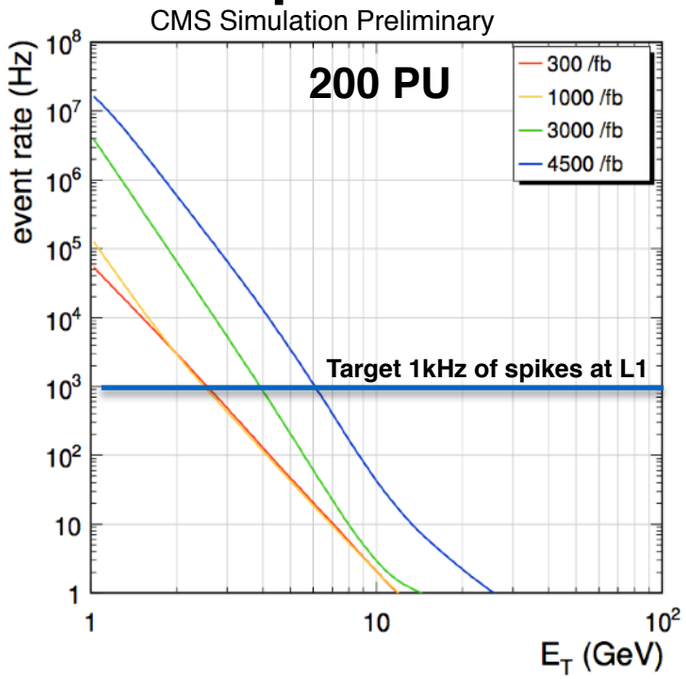


Much better "spike" rejection

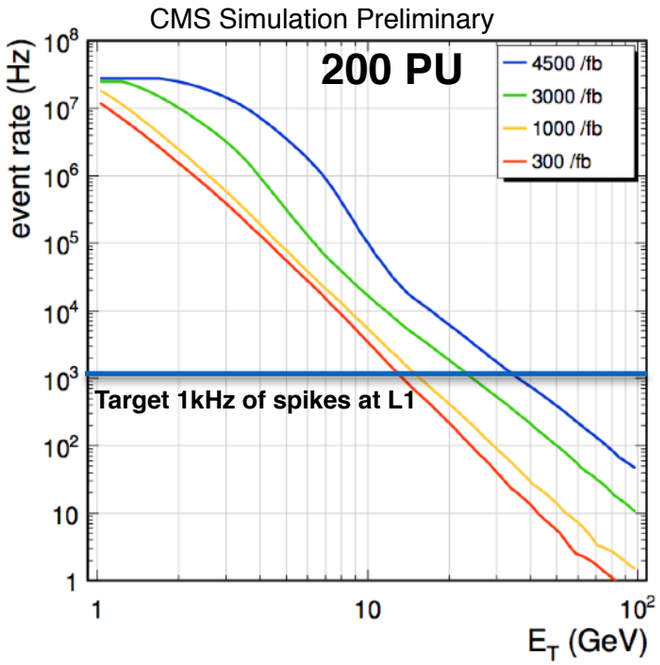
APD spike rejection at HL-LHC

- **<u>Studying performance of two new spike killing algorithms</u>**
  - **pulse shape** discriminant based on different signal shapes
  - **event topology** discriminant based on different spike/EM shower shapes
  - <u>both can be implemented in off-detector readout</u>

Pulse shape discriminant



Event topology discriminant

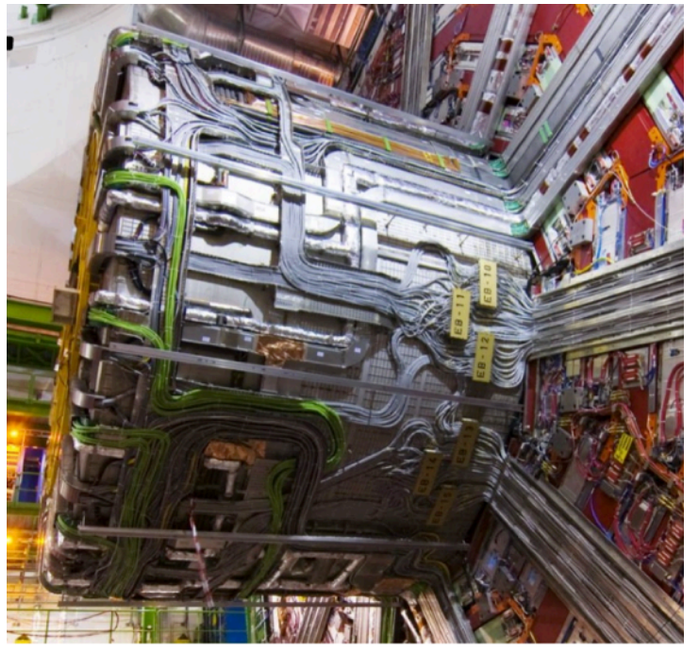


Rate of spikes triggering Level-1 vs E_T for two Phase II spike killing algorithms

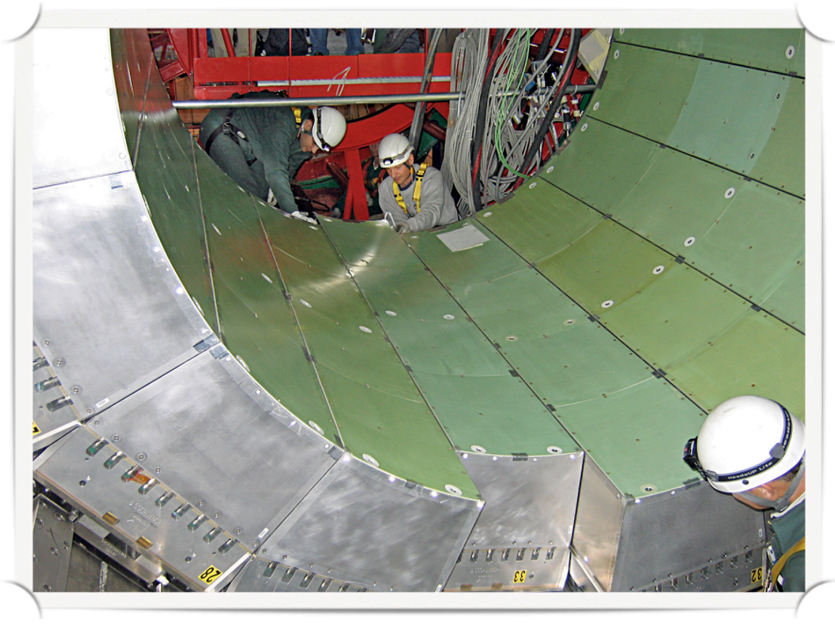
- **<u>Pulse shape discriminant performs well at all HL-LHC luminosities:</u>**
  - **<1kHz of residual spikes** triggering Level-1 for signals with E_T>5 GeV
  - Event topology more sensitive to noise and PU, but can be used as a backup

Detector cooling, refurbishment

- **<u>All supermodule services to be replaced during LS3</u>**
  - **Low/High voltage, cooling pipes, readout fibres**
  - **Improved insulation of water cooling pipes + new cooling system (chilled water)**
    - **to operate at 9°C instead of current 18°C**
- **<u>Supermodules to be removed/ refurbished/reinstalled during LS3</u>**
  - **using specially prepared rework area at point 5 surface building**



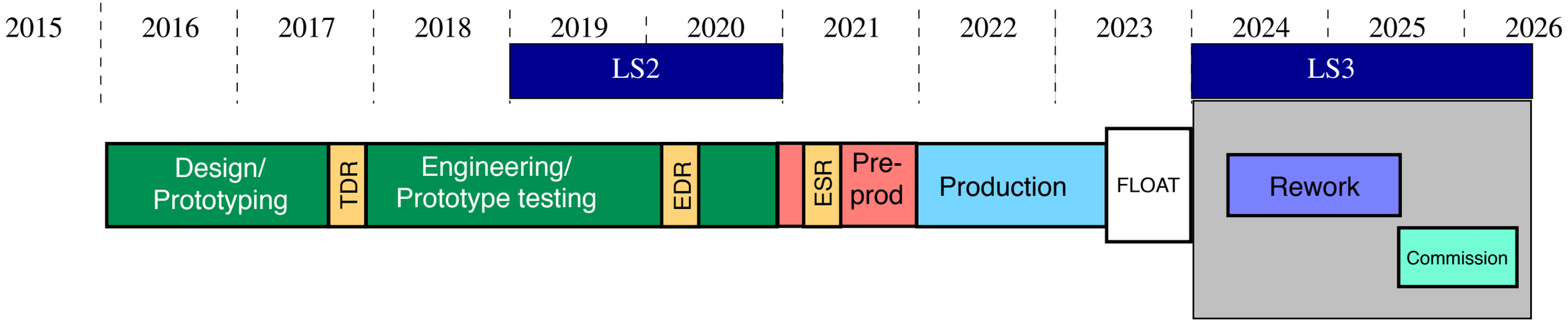
current supermodule services



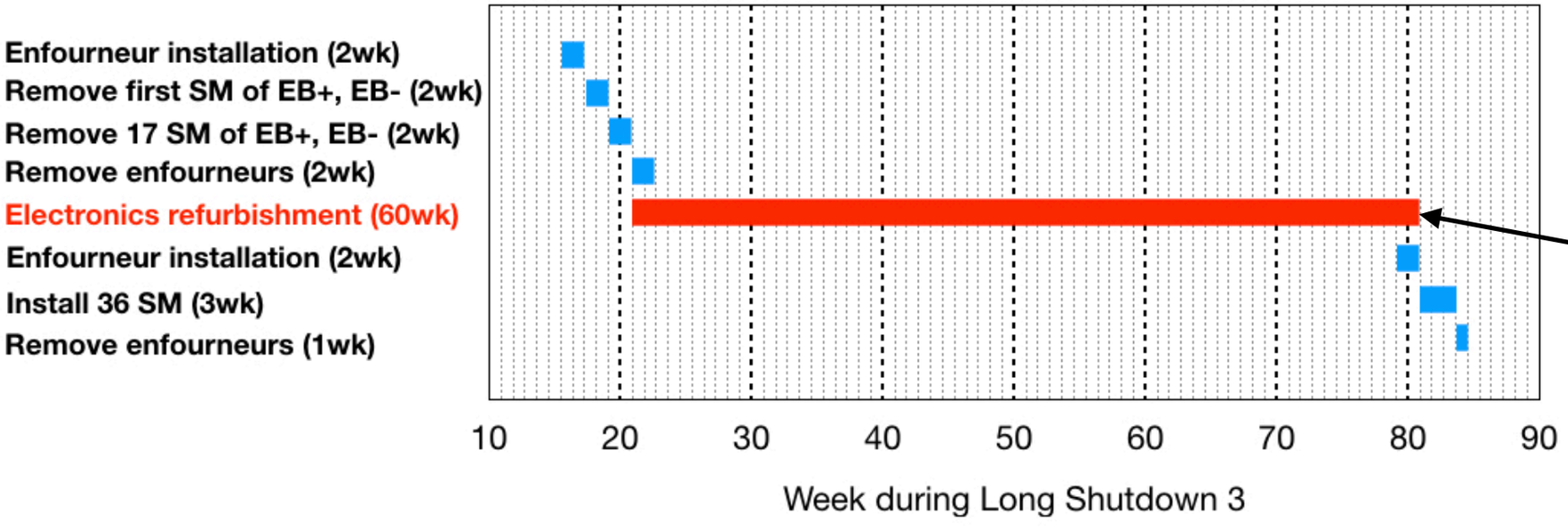
supermodule insertion

Schedule and planning

Overall schedule



Supermodule refurbishment in LS3



TDR submitted to LHCC this month

Summary

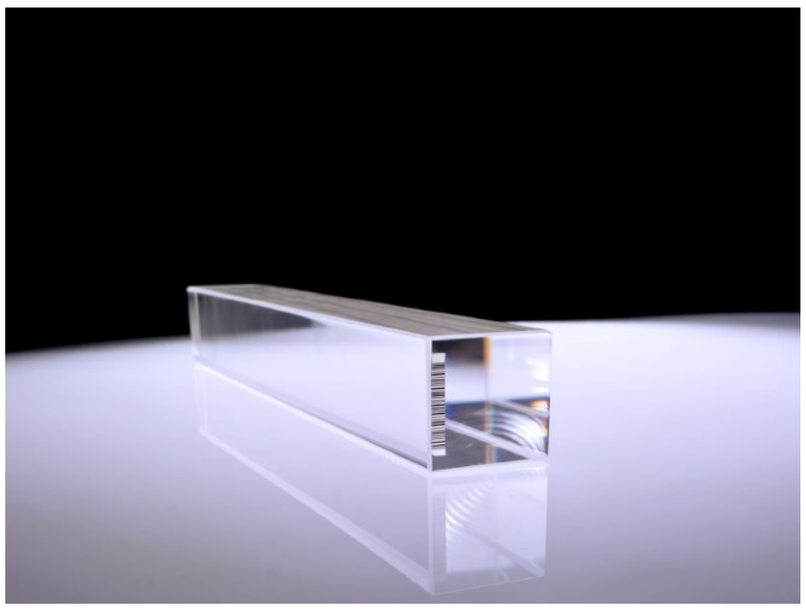
- **ECAL barrel upgrade planned during Long Shutdown 3**
  - **Involves extraction and refurbishment of 36 barrel supermodules**
  - **Replacement Front-End readout being designed**
    - **to be compatible with increased CMS Phase II trigger requirements and more challenging HL-LHC conditions**
    - Targeting **precise timing measurements** (**~30 ps**) for high energy photons and electrons.
      - **Prototype front-end architecture under test at CERN SPS (H4 test beam)**
        - very promising timing performance achieved
    - **Run colder** (to mitigate increases in radiation induced APD dark current)
    - **New off-detector readout** to cope with higher output bandwidth from front-end and provide **more flexible and powerful data processing** for trigger/readout
- **Basic architecture defined, and documented in TDR**
  - **now moving to design and test of prototype chips and readout boards**
- **With these upgrades we will provide a detector that retains excellent photon/electron performance, and meets the challenges of HL-LHC**

Science & Technology Facilities Council

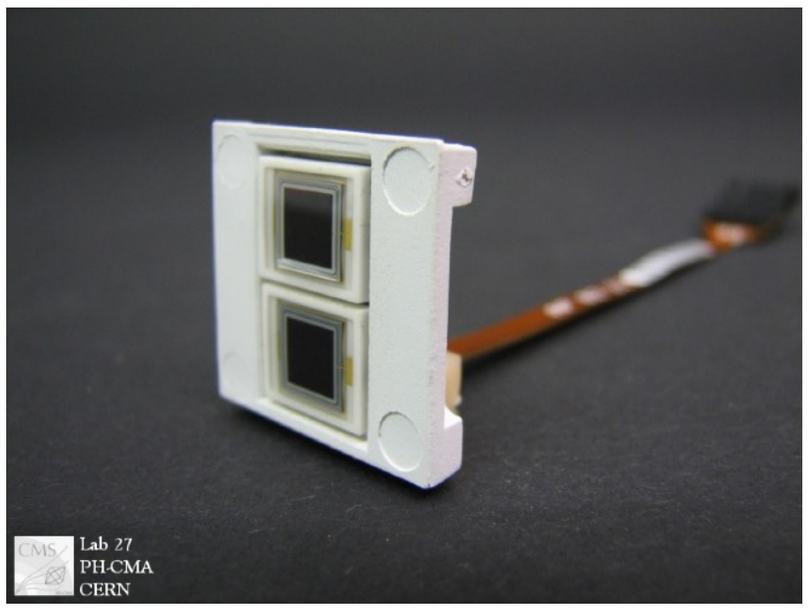
Backup slides

CMS ECAL

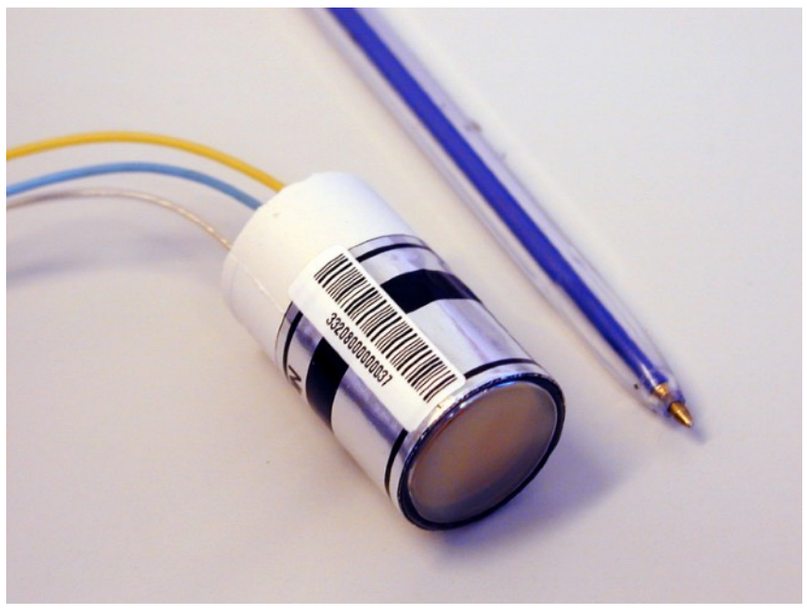
- **The CMS ECAL was designed with challenging goals:**
  - **Extreme energy resolution** in the harsh LHC radiation environment
    - **achieve 1% mass resolution** for low-mass Higgs in the γγ decay channel
  - **Hermetic and compact detector** with coverage up to |η| = 3.0
- **Solutions were obtained through intense R&D campaigns**
  - Lead tungstate (**$PbWO_4$**) **crystal calorimeter**
    - compact, fast, radiation tolerant
    - Radiation and B-field tolerant **APD and VPT photodetectors**
    - Fast and radiation hard **on-detector readout and trigger primitive generation**



Lead Tungstate ($PbWO_4$) crystal



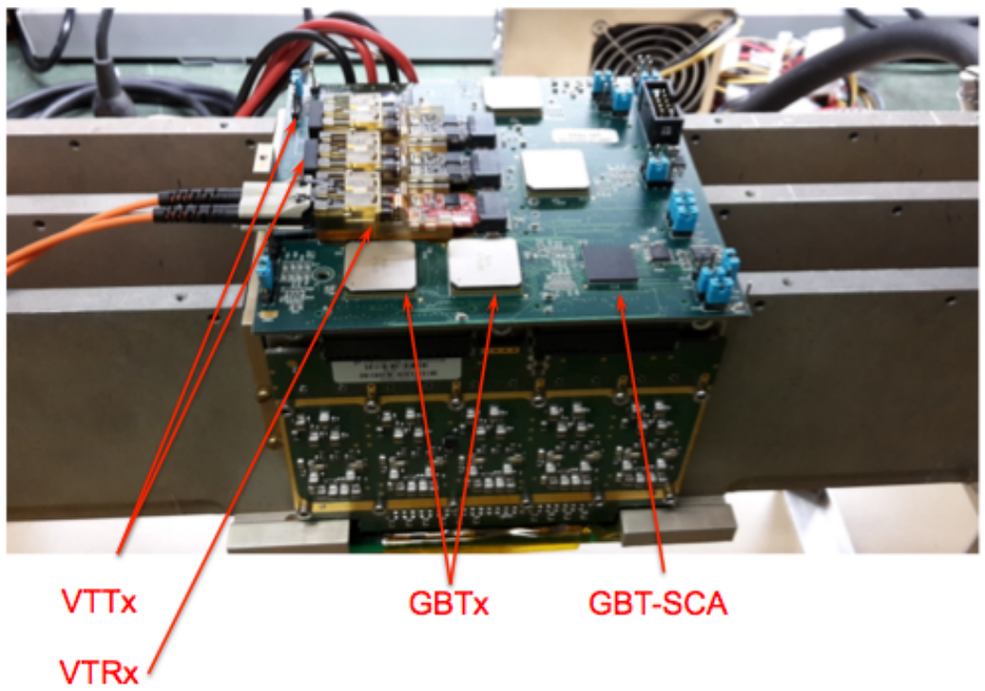
Avalanche PhotoDiode (APD)



Vacuum PhotoTriode (VPT)

Current CMS R&D on EB upgrade

- **<u>Current focus: define specifications for upgraded EB on-detector and off-detector electronics</u>**
  - Hardware specifications documented in EB Technical Design Report (Q3 2017)
- **<u>Trigger primitive algorithm and firmware development</u>**
  - **Perform initial studies of trigger primitive algorithms** using simulated data with full ECAL spatial resolution.
    - **Document For EB TDR and Level-1 Trigger Interim Document (Q3 2017)**
  - **Perform algorithm and firmware tests** using “demonstrator” front-end readout (bench tests and test beam studies) planned for late-2017 onwards



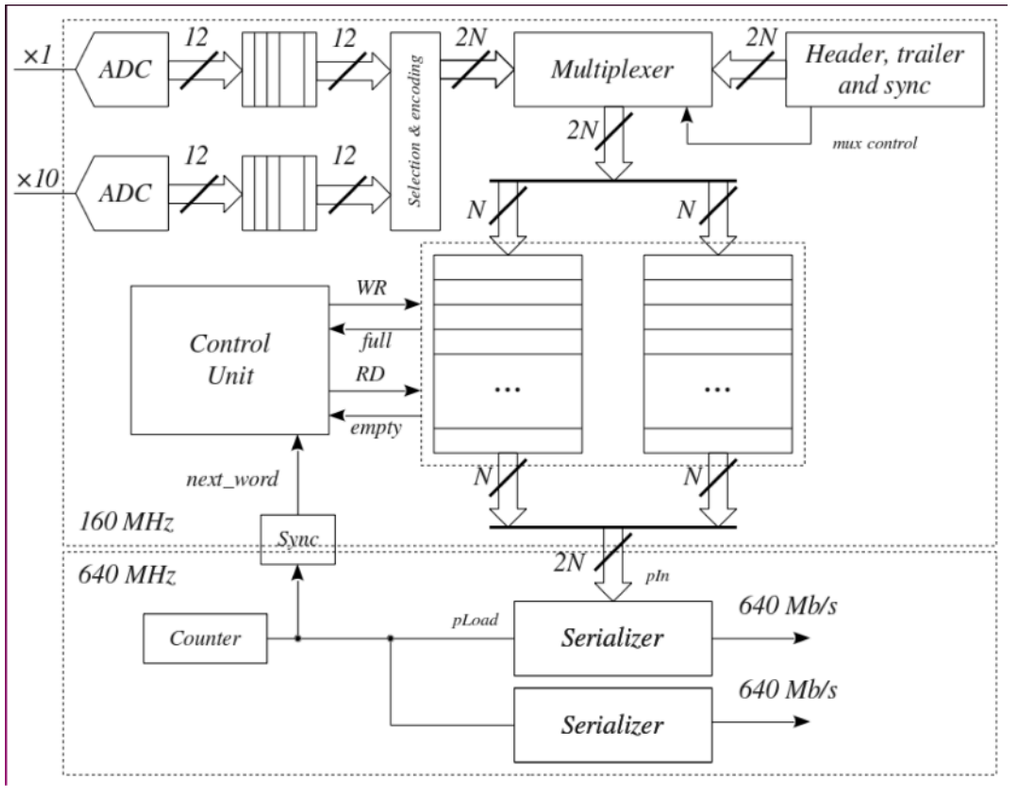
<u>Demonstrator system for EB Phase II on-detector electronics</u>

“Streaming” front-end readout board, using CERN GBT/Versatile link chipsets
Interface to demonstrator off-detector board (from CMS Phase I calorimeter trigger) to develop algorithms/firmware and test performance

ADC design

- **Propose to adapt commercially available ADC core,** with custom-designed **data transmission unit (DTU)**
  - **ADC core identified:**
    - **core specs:** 160 MHz, 65nm TSMC CMOS, radiation tolerant (to ~10 Mrad)
    - **MPW submission with first version of DTU block early next year.**

DTU schematic



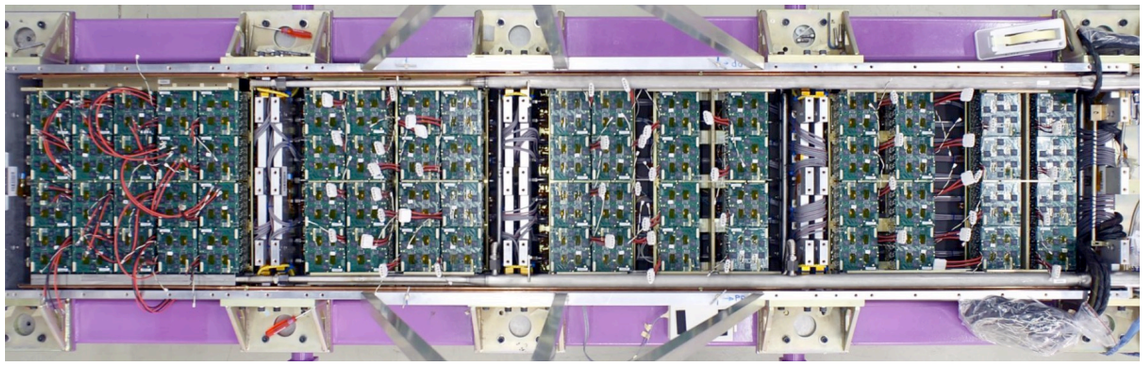
- **DTU output data format** uses either **6 bits** for "low resolution" data or full **12 bit resolution for "signal" data**
- **reduces data volume**
  - **number of readout fibres** required per 25 crystals reduced **from 7 to 4**

Elements of the ECAL Barrel

36 Supermodules

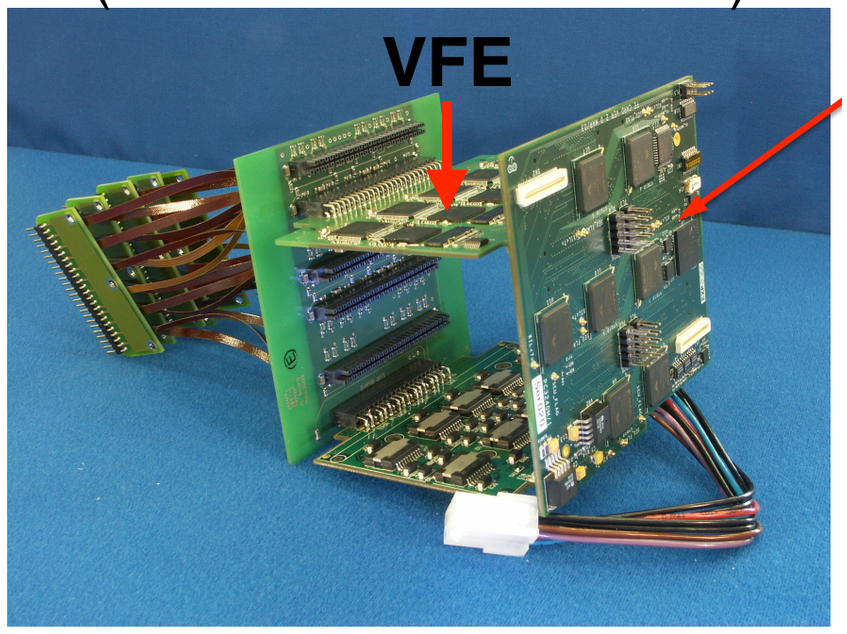
61200 Lead Tungstate crystals
61200 APD pairs

Supermodule in the process of electronics installation



2448 Trigger towers

(readout of 5x5 channels)

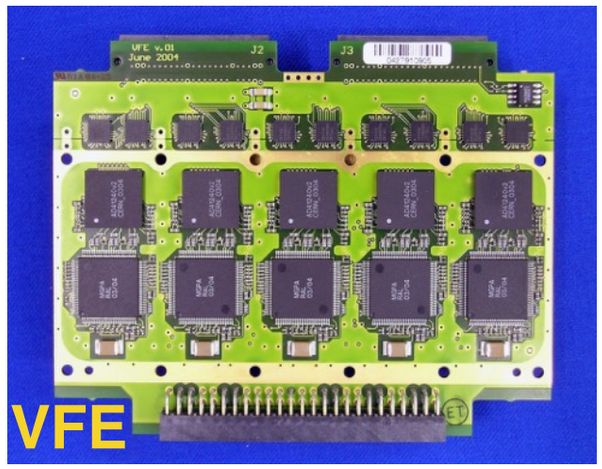


12240 Very Front End cards

pulse amplification, shaping, digitization

2448 Front End cards

data pipeline and transmission, TP formation, clock/control



Architecture and TP definition

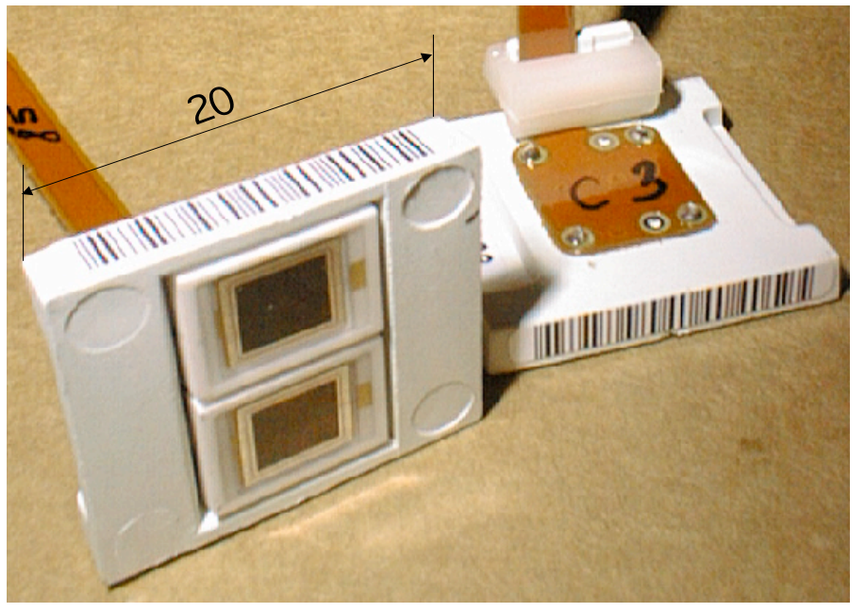
- **Back-end board combines trigger primitive, DAQ and clock/control functions**
  - 108 ATCA boards for whole EB, each with two Ultrascale B2104 XCKU115
- **Two possibilities for trigger primitive definition being studied**
  - **Single crystal TPs:**
    - transmit energy + timing + spike ID bit of **all EB crystals (16 bits, 61200 crystals)**
      - **output data size: 39 Tb/s** assuming no zero suppression
  - **Cluster of crystal TPs:**
    - transmit energy of **"basic" cluster (e.g. 3x5 crystals)** + timing + spike ID bit + eta/phi location + number of crystals **(40 bits, ~1000 clusters)**
      - **output data size: 1600 Gb/s** assuming no cluster threshold
      - transmit **"unclustered" energy in 5x5 blocks** for PU estimation, L1 energy sums: **(additional 1566 Gb/s bandwidth)**

ECAL Phase II Upgrade scope

Background slide

- **<u>Extraction and refurbishment of 36 EB Supermodules during LS3</u>**
  - **Replace Front-End readout**
    - **to be compatible with increased CMS Phase II trigger requirements**
    - to cope with **more challenging HL-LHC conditions** (noise, pileup, anomalous APD signals).
    - Explore possibility of **precise timing measurements** (**~30 ps**) for high energy photons.
      - <u>precise timing capabilities now a core component of CMS Phase II upgrade</u>
  - **Run colder** (to mitigate increase in radiation induced APD dark current)
  - **New off-detector readout** to cope with higher output bandwidth from front-end
    - will stream all data off detector with faster sampling (160 MHz)
      - **higher sampling rate needed for precise timing capabilities**
  - **Prototype front-end architecture under test at CERN SPS (H4 test beam)**
    - very promising timing performance achieved

ECAL photodetectors



Hamamatsu S1848 APDs

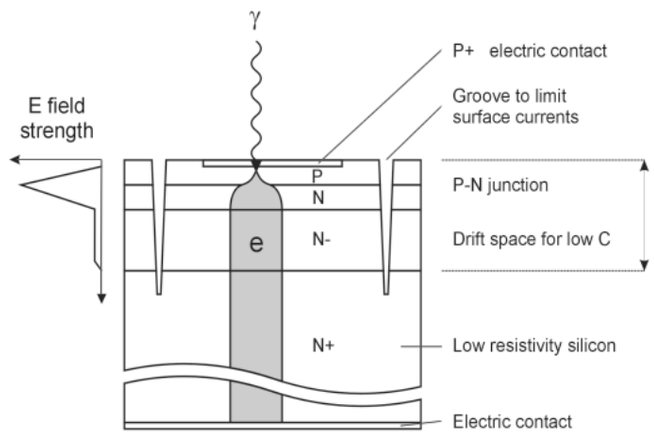
Barrel: Avalanche PhotoDiodes (APD)

two 5x5mm^2 sensors
glued to back of $PbWO_4$ xtal

high QE: ~75%

operate at gain 50
operating voltage 340-440 V

Temperature sensitivity
-2.4%/°C



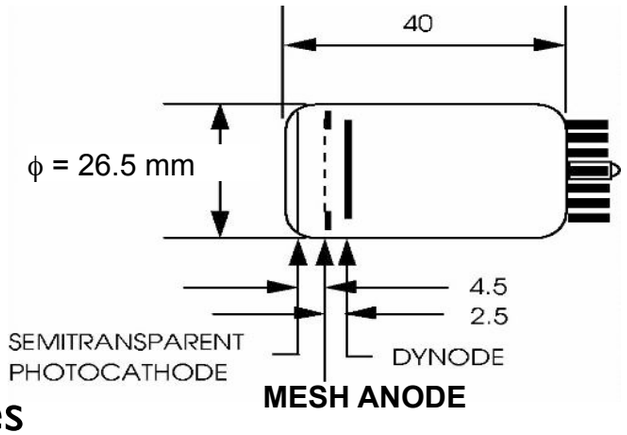
NRIE (St Petersburg) PMT188 VPT

Endcaps: Vacuum PhotoTriodes (VPT)

280mm^2 sensor area
glued to back of $PbWO_4$ xtal

QE: ~20% (420nm)

operate at gains 8-10 (4T)
anode/dynode voltage 800/600 V

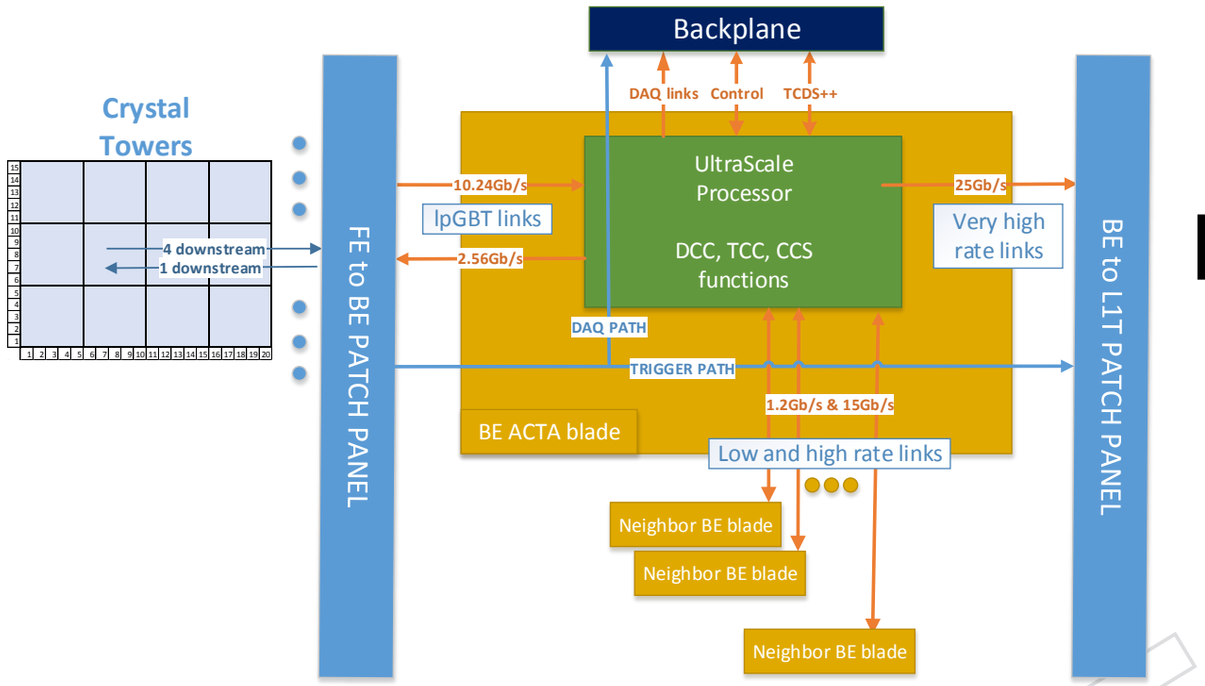


More radiation tolerant than Si diodes
UV glass window

~4.5 photoelectrons/MeV @18°C in both APDs and VPTs

Back-end architecture

Background slide



each FPGA serves 12 ECAL towers (5x5 crystals)

corresponds to a 20x15 crystal area

Figure 3.28: General overview of the FE-BE-L1 chain

15 links/FPGA to L1 (16 Gb/s)

for single crystal TP option

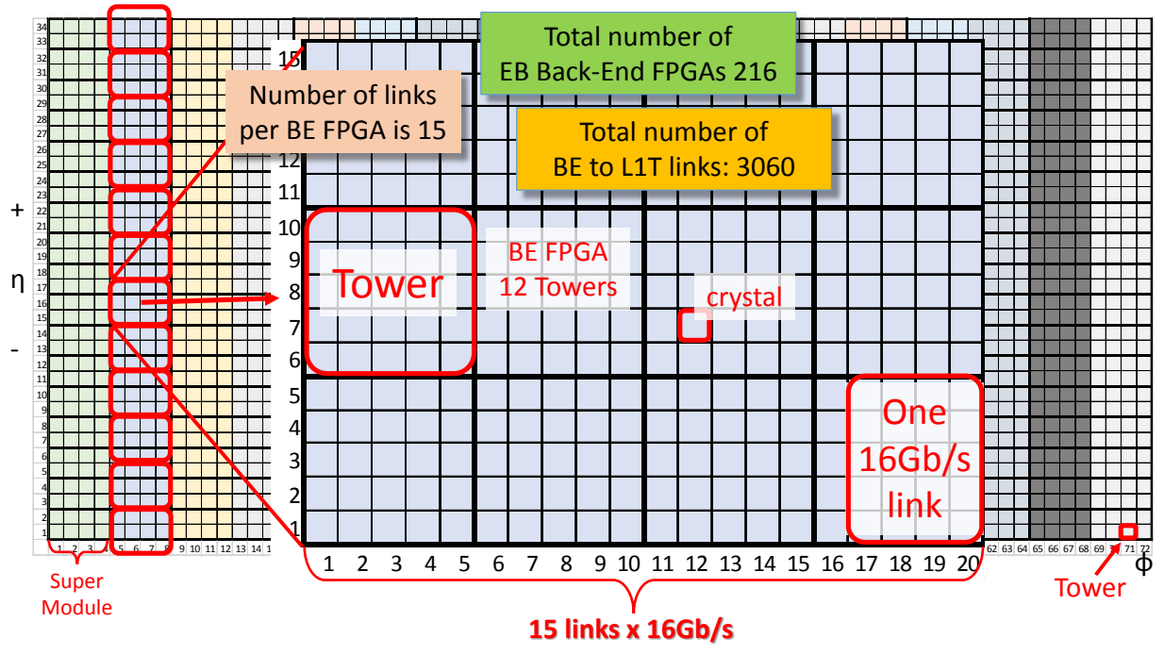


Figure 3.30: BE to L1 interface