Readout electronics for the TPC detector in the MPD/NICA project

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Abstract. The article is aimed at describing the development status, design features and advanced version of the TPC data readout system.

The TPC is placed in the middle of the Multi-Purpose Detector and provides tracking and identification of charged particles in the pseudorapidity range $|\eta| < 1.2$.

Tracks in the TPC are registered by 24 readout chambers that are placed at both end-caps of the sensitive volume. The readout system of each chamber consists of the front-end cards (FECs, 62 per chamber) and a readout control unit (RCU). FECs collect signals directly from the chamber pads, amplify them, digitize, process and transfer it to the RCU.

The design concept and improvement have been motivated by NICA project requirements for a trigger rate up to 7 kHz with mean tracks multiplicity of 300 tracks (maximum multiplicity – up to 1000 tracks) and by the requirement of TPC end-caps transparency about X/Xo=(15÷20)%.

Keywords: Time projection Chambers (TPC), Front-end electronics for detector readout.

1 Introduction

The new research complex NICA aimed to study hot and dense baryonic matter is under active realization in JINR (Dubna) [1]. It will operate with heavy ion collisions (up to Au) at centre-of-mass energies 11 GeV per nucleon. The MPD detector will operate at one of two interaction points of the collider [2].

The Time Projection Chamber (TPC) is the main tracker of MPD. It has been designed for tracking and identification of charged particles [3].

2 Design requirements and concept

The TPC detector produces most complex events among other MPD subdetectors. The NICA collider will provide the trigger rate up to 7 kHz with mean multiplicity of 300 tracks and maximum multiplicity – up to 1000 tracks per event. The data readout system is to receive the data from all 95232 detector pads and then transmit them to the MPD DAQ.

The TPC data is zero dominated. For this reason zero suppression modes should be implemented in the TPC Front-End Electronics (FEE). The mean data stream from the TPC detector is expected to be at the value 7 GByte per second (with zero suppression).

Another significant requirement for the data readout system is end-caps transparency requirement. TPC electronics will be located at the end-caps of the TPC barrel and it will shadow other MPD subdetectors. For this reason the FEE size should be as small as possible, and it should dissipate as small power as possible to simplify the cooling system.

The TPC's data acquisition system consists of 24 identical parts. Each part serves to one readout chamber and electronics of each chamber is an independent system. There are two main blocks in the data readout system. They are FECs and RCUs. The whole data readout system contains 95 232 registration channels, 1488 64-channels FECs and 24 RCUs.

At that moment we are considering two versions of the TPC FEE. First one is based on the PASA and ALTRO chip set [4]. These two ASICs were designed for the ALICE TPC. They are also suit well for our design and allow us to reach all requirements except end-caps transparency requirement. This system has already been designed and its functionality is enough for the startup period of operation. The second version of the TPC FEE is based on the new ASIC SAMPA [5]. The SAMPA chip has few advantages to PASA and ALTRO chip set, namely double input signal polarity, switchable preamplifier gain, and picking time, continuous readout mode. The FEE design that is based on the SAMPA chip is under realization now.

Block diagram of the readout system for one chamber is shown in Fig. 1.

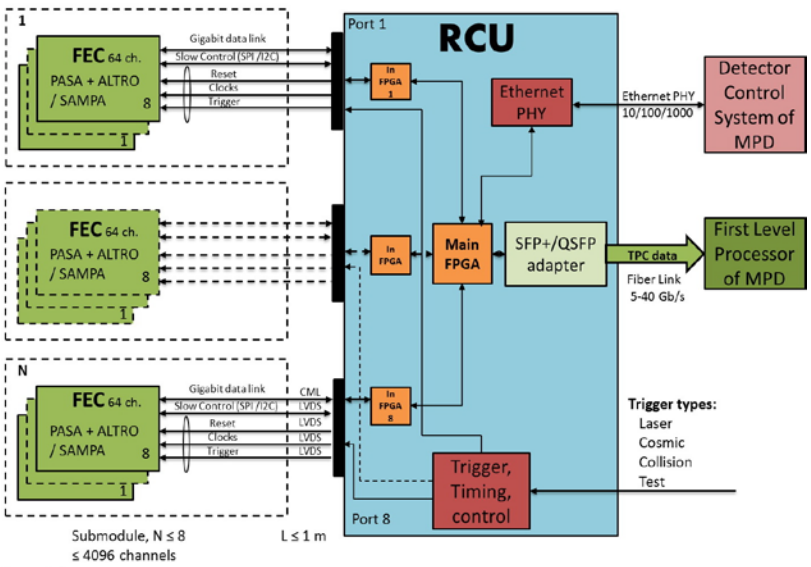

Fig. 1. Block diagram of one chamber readout system.

3 PASA and ALTRO chip set based design

The FEC64S is advanced version of the prototype card FEC64 [3, 6]. The card is based on the 4 PASA and 4 ALTRO chips which produce 64 independent registration channels in total. View of the FEC64S is shown in Figure 2 and main parameters are summarized in Table 1.

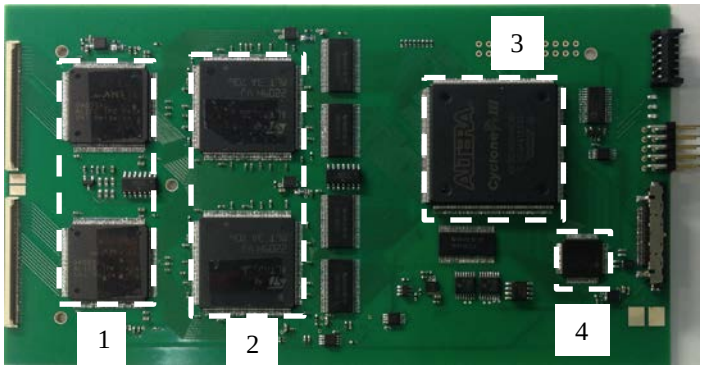

Fig. 2. Top view of the FEC64S. 1) PASA chips – low noise amplification of the signal; 2)ALTRO chips – digitization and signal processing; 3) ALTERA FPGA; 4) Serializer/Deserializer chip.

Table 1. FEC64S main parameters.

Parameter	Value
Signal to noise ratio at MIP	30 : 1
ENC at detector capacitance 10-20 pF, electrons	< 1000
Shaping time, ns	180-190
Shaped signal tail cancellation after 1 μs	< 1%
ADC resolution, bits	10
Sampling rate, MHz	10
Buffering, events	4 – 8
Effective serial interface speed, Gbps	1.6 – 2.5
Power consumption, mW per channel	< 100

PASA chip receives analogue signals through short kapton cable directly from detector pads. It amplifies detector signals with conversion gain 12 mV/fC over the range of input charge up to 150fC. Each of the 64 PASAs channels has a single-ended input and a differential output which are directly connected to the ALTRO chip inputs.

The incoming analog data stream is digitized, processed, formatted by ALTRO's embedded digital signal processor, and outputted as an array of 40-bit words. The most significant factor affecting upon the output data volume is zero suppression function of the signal-processor. It allows providing the necessary throughput of the data acquisition system.

Another essential part of the card is ALTERA FPGA. Its main function is multiplexing of the parallel ALTRO words from all 64 independent channels to one stream. The Serializer/Deserializer chip TLK2711 was chosen as a readout interface. It provides bidirectional access to the ALTRO and FPGA at speed up to 2.5 Gbps. The FPGA implements the connection function of 40-bits ALTRO bus with 16-bits parallel input of Ser/Des chip and vice-versa.

The multiplexing of data in the card is carried out in 4 steps. The 16 ALTRO channels are multiplexed in the chip. Then parallel outputs of the two chips are multiplexed into one bus and organize two groups from two ALTROs each. Power regulator of the PASAs and ALTROs chips also are combined into two groups that allows to disable the half of the card if some problems occur. Parallel outputs of two groups are combined into one that is directly connected to the FPGA.

The FPGA slices 40-bits ALTRO words into 10-bits words, codes them with Hamming code, and at the end feed forms 16-bits words to the parallel input of the Ser/Des chip. The Ser/Des chip is implemented the last step of multiplexing in the FEC64S. Outgoing data are transmitted to the RCU as a serial stream with data rate from 1.6 to 2.5 Gbps.

The FEC64S can operate in two acquisition modes: the Individual Readout Mode (IRM), and the Automatic Scan Mode (ASM). In IRM the RCU should send Channel Readout command (CHRDO) independently to all of 64 channels on the card. This acquisition mode does not allow achieving the fastest data readout speed from all FECs, which are connected to the RCU.

After activating ASM the FPGA takes some functions of the RCU. The ASM algorithm was implemented at the FPGAs state machine. ASM cycle starts after receiving level 2 trigger (LVL2) that confirms validation of data in the ALTROs multi-event buffers memory. After receiving LVL2 state machine starts to read Address and Event Length registers (ADEVL) of all ALTROs channels that contain information about available data in the buffers. The contents of that registers are stored in the dedicated FIFO buffer in the FPGA. When all ADEVL registers information is received state machine starts to send command only to those channels which contains information. The flowgraph of the ASM is shown in Fig. 3.

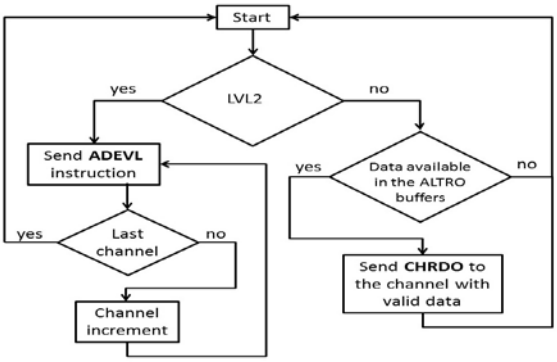

Fig. 3. Flowgraph of the ASM.

Information copying about the data volume of the last received event in the ALTRO channels into the FPGA FIFO memory is the main idea of ASM. Being a master for the ALTRO as well as the RCU, ASM state machine transfers data from the ALTROs multi-event buffer memory into the controller.

The ASM significantly accelerates the data readout process. In this mode all FECs operate simultaneously. The RCU needs only to receive data.

RCU is a significant unit of the data readout system. Its main function is control and data collection from 62 FECs. The whole data acquisition system will be equipped with 24 RCUs each one for a single readout chamber. Every RCUs are based on the 8 input FPGAs and one main FPGA. Input FPGA is connected to the 8 FECs through high-speed transceivers. The multiplexing of the data in RCU is implemented in two steps. The input FPGA multiplexes data from 8 FECs. The main FPGA multiplexes data from 8 input FPGAs. After multiplexing the data are transmitted to the first level processor system through optical link.

Other key functions of the RCU are monitoring of the FECs conditions and fan-out of synchronization pulses. The RCU is equipped with independent Ethernet line to the slow control system.

4 SAMPA based design issues

The SAMPA chip has been under development during last few years for ALICE TPC and MCH upgrade at CERN. It has 32 channels and is composed of an analog front-end part, an ADC, a digital processor and serial links. The SAMPA chip is more integrated then PASA and ALTRO chip set. Its square is only 225 mm^2 per 32 channels while squares of PASA and ALTRO are 484 mm^2 and 708 mm^2 respectively per 16 channels. Estimates show that the size of the FEC PCB can be reduced by a factor of 3. The amount of background substance will be proportionally reduced in front of corresponding parts of the CPC Tracker, the Straw EC Tracker and the Time of Flight system that located next to the TPC end-caps. Besides in this case the FEC planes can be oriented parallel to the TPC end-caps plane that is the essential factor affecting to the quality of the tracks reconstruction in the MPD.

Another significant advantage of the SAMPA chip is its possibility operating with multi-wire proportional chambers as well as with GEM chambers that is necessary for a future TPC upgrade.

A few pilot chips were tested and the results of measurements show us the feasibility of SAMPA-based FEC for the TPC MPD/NICA. The idea of using the SAMPA chip in the FECs by modification of the designed one seems very productive.

5 Conclusion

The FEE system based on PASA and ALTRO chip set was designed. The present system provides opportunities for read out of physics events at the trigger rate up to 7 kHz which meets the NICA project requirements for startup period of operation.

The usage of the SAMPA chip for the TPC readout system will satisfy all requirements. In addition such a system gives an opportunity for future TPC upgrade. The SAMPA based FEE is under designing.

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References

1. V.Kekelidze et al., Status of the NICA project at JINR. // EPJ Web of Conference 95, 01014 (2015).
2. K.Abraamyan et al., The MPD detector at the NICA heavy-ion collider at JINR, Nucl. Instrum. Meth. A 628 (2011) 99; MPD collaboration, The Multipurpose Detector (MPD), Conceptual Design Report, JINR, Dubna, Russia (2010).
3. Aver'yanov et al., Time-Projection Chamber of the MPD Detector at NICA Collider Complex. // Yadernaya fizika i inzhiniring. 2013. V. 4. № 9.P. 867 [in Russian]; Averyanov et al., Time-Projection Chamber for the MPD NICA project. // J. Instrum. 2014. V. 9. P. C09036; A.V.Averyanov et al., Readout System of the TPC/MPD NICA Project. // Yadernaya fizika i inzhiniring. 2014. V 5. № 11 – 12. P. 916 [in Russian]; A.V.Averyanov et al., Readout System of TPC/MPD NICA Project. // Physics of Atomic Nuclei, 2015, Vol. 78, No. 13, pp. 1556–1562.
4. ALICE TPC Electronics. Charge Sensitive Shaping Amplifier (PASA). Technical Specifications, CERN, 2003; ALICE TPC Readout Chip. User Manual. CERN, June 2002, Draft 0.2. ALTRO chip web page, http://ep-ed-alice-tpc.web.cern.ch/ep-ed-alice-tpc.
5. S.H.I.Barboza et al. SAMPA Chip: a New ASIC for the ALICE TPC and MCH Upgrades. // J. Instrum. 2016. V. 11. C02088; J.Adolfsson et al., SAMPA Chip: the New 32 Channels ASIC for the ALICE TPC and MCH Upgrades. // J. Instrum.2017 V. 12. C04008.
6. Bazhazhin A. et al., Front End Electronics for TPC MPD/NICA. // Proc. "XXIII International Symposium on Nuclear Electronics & Computing". 2011. Varna. JINR.E 10.№ 11. P.133; Averyanov A. et al, R&D readout electronics of the TPC MPD/NICA // Proc. "XXIV International Symposium on Nuclear Electronics & Computing". 2013. Varna. JINR. E 10, 11 – 2013-136. P. 265.