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An front-end ASIC for APD array detector in high time resolution x-ray experiments

The silicon avalanche-photodiodes (APD) detector has been already used in time-resolved experiments with pulsed synchrotron X-rays, such as Nuclear Resonance Scattering (NRS) experiments and Laser Pump / X-ray Probe experiments, since more than two decades. However, the traditional time-resolved APD detectors only have a single APD sensor and adopt a commercial circuit or discrete element circuit to readout the weak signal outputted by the APD sensor. In order to acquire a larger reception solid angle, higher count rate and higher integration density, it is necessary to develop an APD array detector for X-ray time-resolved experiments. This paper presents a prototype ASIC chip for the APD array detector. The prototype chip includes five channels: four complete channels and one test channel with an analog output. Each complete channel consists of a preamplifier, a voltage discriminator and an open-drain output driver. The readout noise and the power consumption are reduced by using the flipped voltage follower (FVF) as the input stage of the preamplifier. An AC coupling circuit is also employed in the preamplifier to decrease the DC offset of the preamplifier. The discriminator is based on a cascade of four low-gain and high bandwidth differential amplifiers with a hysteresis function. To match the LVDS output levels, the open-drain differential circuit is adopted as the output driver which can configure the output level by programming external resistors. The prototype chip is designed and fabricated in a 0.13 μm CMOS technology with a chip size of 1.3 mm × 1.9 mm. Electrical characterizations of the circuit demonstrate a very good intrinsic time resolution (rms) on the output pulse leading edge, with the test result better than 30 ps for high input signal charges (> 75 fC) and better than 100 ps for low input signal charges (30 fC −75 fC), while keeping a low power consumption of 5 mW per complete channel.

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