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CMS
Compact Muon Solenoid

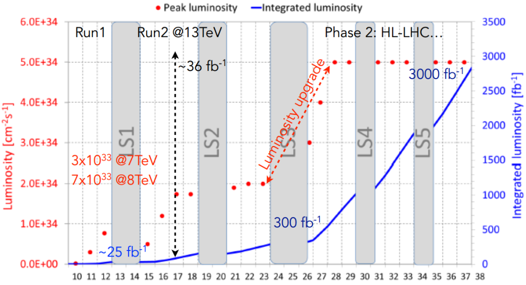
TIPP - 22-26 May 2017, Beijing

Construction and first beam-tests of silicon-tungsten prototype modules for the CMS High Granularity Calorimeter for HL-LHC

Francesco Romeo

On behalf of the CMS collaboration

Motivation for the High Granularity Calorimeter (HGCal) in HL-LHC



In the High-Lumi (HL) LHC era, we need to maintain:

- smoothly running detector
- high quality object reconstruction/identification

Extreme conditions in endcap region

- High radiation (up to $10^{16} n/cm^2$ at $\eta \sim 3$)
- High pileup (140-200)

Use silicon-based HGCal detector

- Radiation tolerant
- High granularity and fast timing

For more motivations, please refer to talk by Florian Michael Pitters

HGCal overview

Key Parameters:

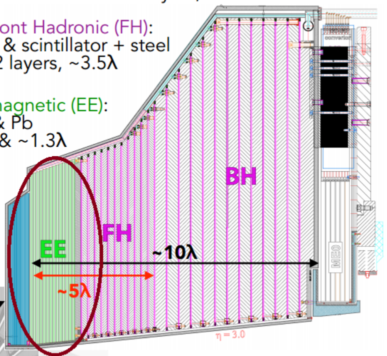
- HGCal covers $1.5 < \eta < 3.0$
- Full system mantained at -30 $^{\circ}C$
- $\sim$ 600 m^2 of silicon sensors
- 6 M channels, 0.5 or 1 cm^2 cell size
- $\sim$ 22000 modules
- Power at end of HL-LHC:
  $\sim$ 60 kW per endcap

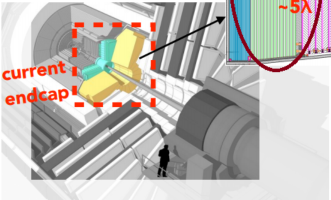
Backing Hadronic (BH):
Si & scintillator + steel
12 layers, ~5λ

Front Hadronic (FH):
Si & scintillator + steel
12 layers, ~3.5λ

Endcap Electromagnetic (EE):
Si + Cu & CuW & Pb
28 layers, 25 X0 & ~1.3λ

Discuss results for beam-tests on EE-like setup





More on HGCal in the talk by Florian Michael Pitters

2016 beam-tests at FNAL and CERN

Primary goals:

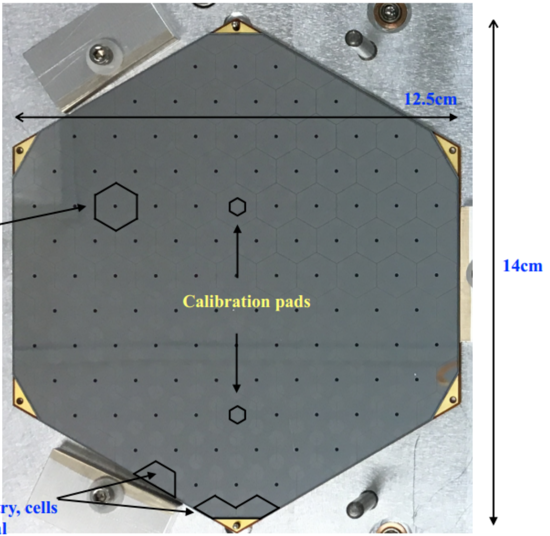
- Proof of concept of the baseline HGCal design
  with a closely spaced stack-up of modules
- Validation of the overall design concept of a hexagonal silicon sensor
  mounted on a baseplate with a PCB with holes for the wire-bonding

Performance of silicon-tungsten prototype modules:

- Studies:
  - Pedestal and noise
  - Single particle calibration
- Measurements:
  - Longitudinal and transverse shower shapes
  - Energy, position, time resolution
- Compare results with simulation

Hexagonal Si-Sensor (128 channels)

"p on n" with 200 μm active thickness, made from 6" wafer, cell size 1.1 cm^2



shows one of the hexagonal cell on the wafer

Due to the hexagonal geometry, cells around the edges need special attention

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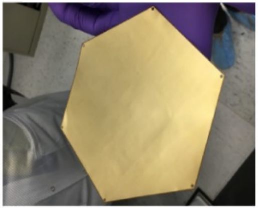
Module assembly

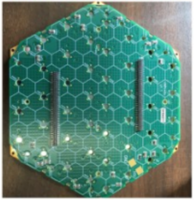
Glued stack of **baseplate**, **kapton**, sensor and 2 **PCBs**

Golden plated Kapton

. Connection to the backplane of the silicon sensor for bias voltage

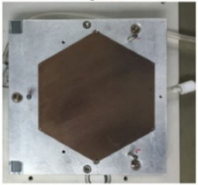


1st PCB wire-bonded to sensor

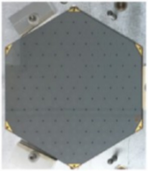


CuW baseplate

. Mechanical rigidity
. Coefficient thermal expansion close to that of silicon
. Part of calorimeter absorber

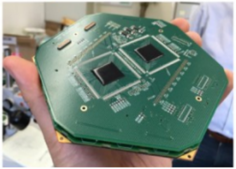


Silicon sensor



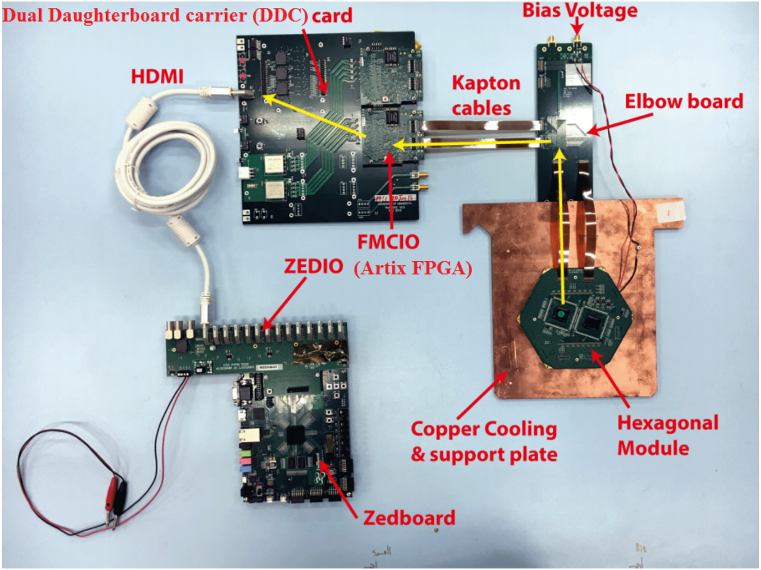
Full module

. Double PCB layer readout
. 2 'Skiroc2' ASIC, 64 ch each (originally developed for CALICE)



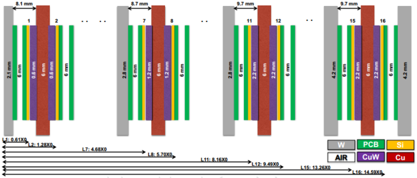
Data Acquisition System

Use commercial components mounted on custom PCBs



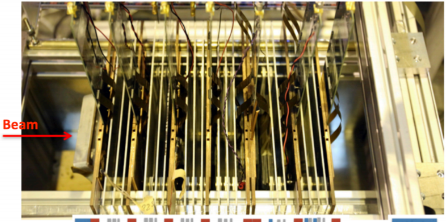
Data taking setup & conditions

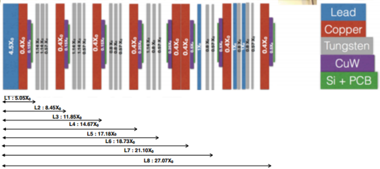
FNAL



- 16 modules, 15 X_0
- e beam (4-32) GeV
- p beam 120 GeV

CERN

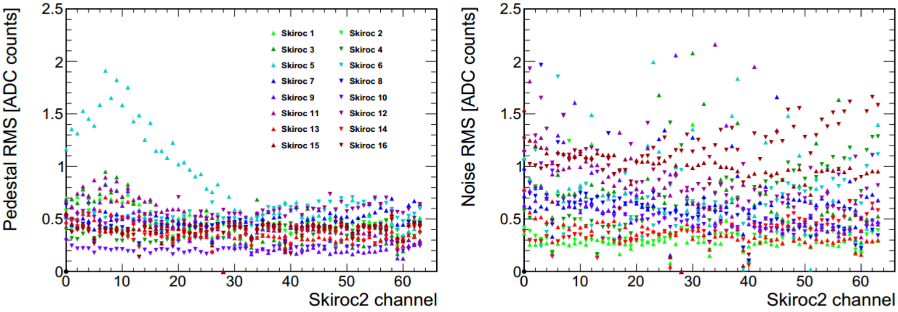




- 8 modules, 5-27 (6-15) X_0
- e beam (20-250) GeV
- π(μ from π) beam 125 (120) GeV

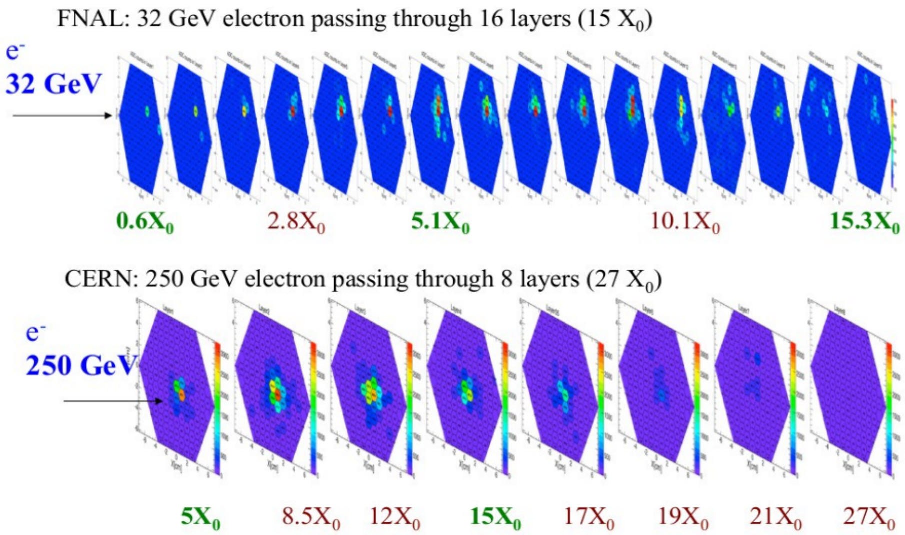
Pedestal and noise stability

From CERN test with 8 layers (16 Skiroc2 ASICs)



Pedestal and noise stable within 2 ADC count (1 ADC $\approx 1/17$ MIP)

Electron beams: event display



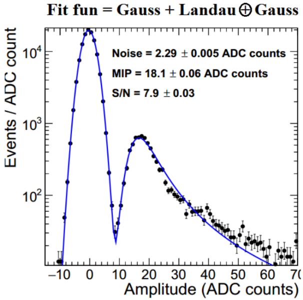
MIP calibration

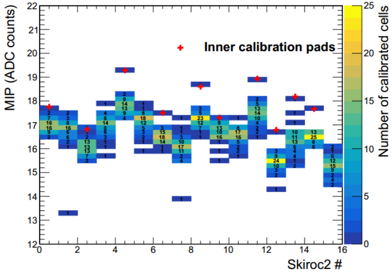
FNAL: *p* beam 120 GeV

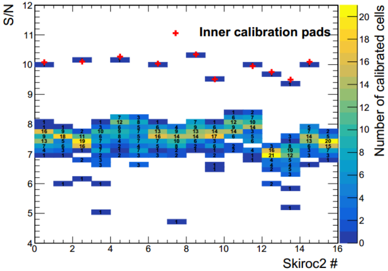
CERN: π(μ from π) beam 125 (120) GeV

Calibrate only central cells of sensor within trigger area

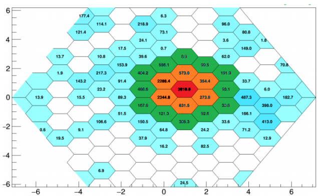
Variations due to the electronic and cell size

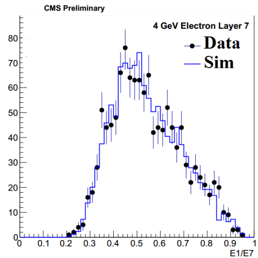


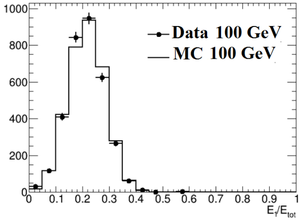


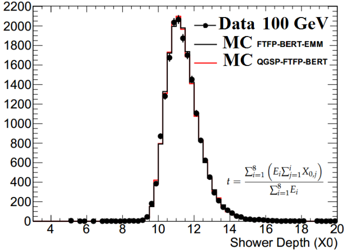


Transverse and longitudinal shower shapes





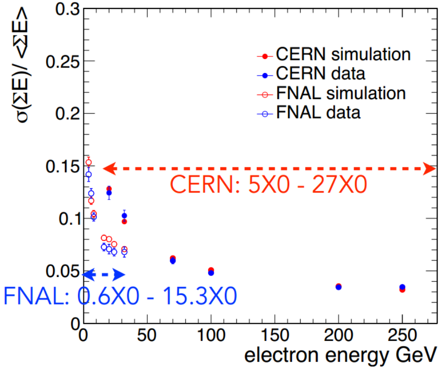




Excellent agreement between measurements and simulation

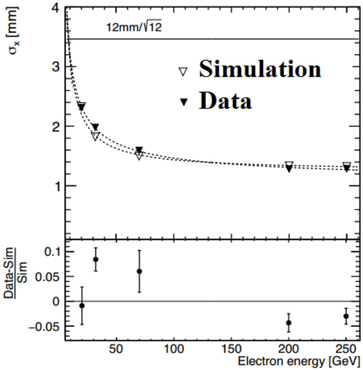
→ one of the main goals achieved

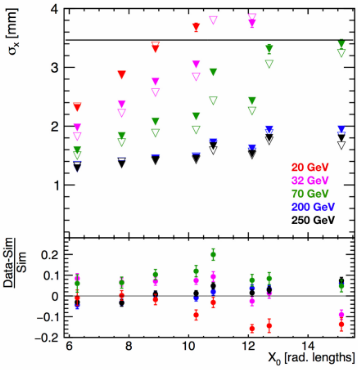
Energy resolution



- Energy measured in the silicon layers plus sampling factors for the absorbers
- Wide range of energies covered
- FNAL, CERN trends VS energy reflect different sampling regimes
- Limited longitudinal samplings limit the achievable electron energy resolution
- Good agreement between data and simulation

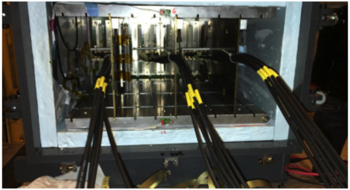
Position resolution

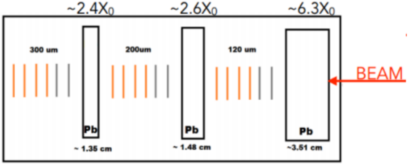


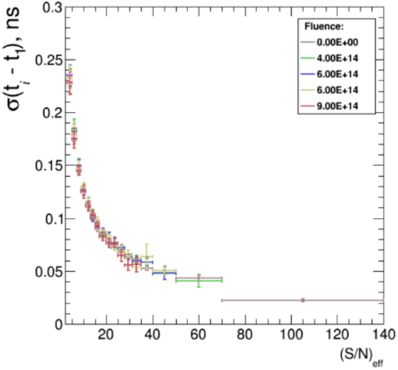


- Measure the difference between a track extrapolated from two wire chambers (upstream of first HGCal module) and the shower position (logarithmic weight E_{19} cell)
- Precision of a few mm can be achieved
  It increases with energy and decreases with depth in calorimeter
- Good agreement with simulation

Time resolution







. Use p-type and n-type 5x5 mm^2 diodes

. Non-Irradiated and Irradiated

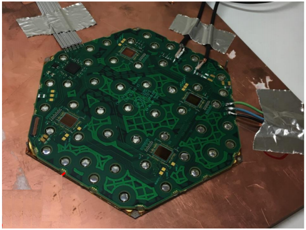
. Use 1 Non-Irradiated and 1 Irradiated diodes (in turn) as references for time resolution measurement

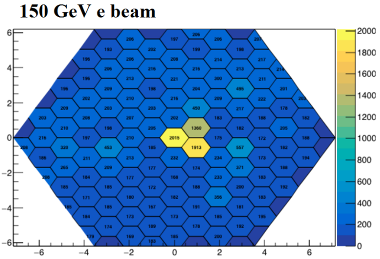
- Can achieve 20ps timing resolution for reasonably-large signals
- No degradation in performance with radiation

HGCal beam test in 2017 (Goal 1)

- Updated front-end chip, 'Skiroc2-CMS', featuring HGCal ASIC:
  - 25 ns peaking time ($\sim$ 200 ns in SKIROC2)
  - Time Over Threshold (ToT) for large signals
  - Time of Arrival information ($\sim$ 50 ps timing) to explore timing performance
- Single layer PCB to achieve the desired compactness

For more details, see talk by Johan Borg

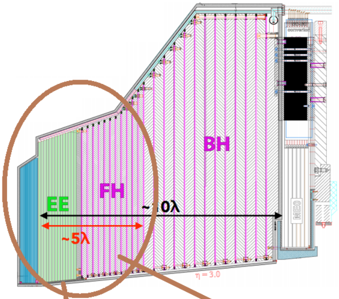


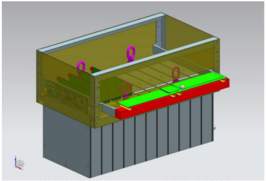


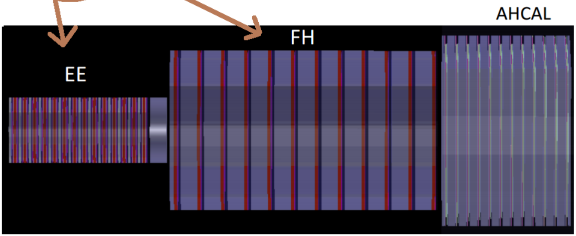
New DAQ required
First beam-test on a single module successfully completed in May

HGCal beam test in 2017 (Goal 2)

Aim to test full EE+FH+BH - like setup







Summary

- HGCal is the CMS decision for replacing its current endcap in HL-Lumi era:
  • Good energy resolution for electromagnetic and hadronic particles in an extremely high-radiation environment
  • High granularity and fast timing to deal with high pileup

- Proof of concept through construction and first beam-tests of silicon-tungsten prototype modules

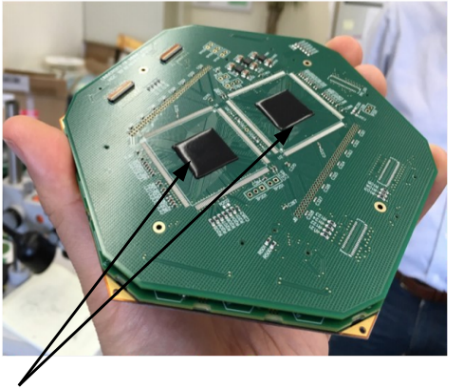
- Measured resolution for:
  • Energy: below $\sim$7%, for e energy $>$ 50 GeV
  • Position: below $\sim$ 2mm, for e energy $>$ 50 GeV
  • Time: $\sim$ 20 ps

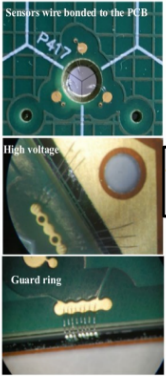
- Basic validation of the simulation

- In 2017 campaign, we aim to study full system performance (EE+FH+BH)

Fullly assembled module

- Chosen for flexiblity so that the top board can be changed with a different readout chip design.
- Not the final design as the overall thickness is much larger than what is foreseen in the final design.

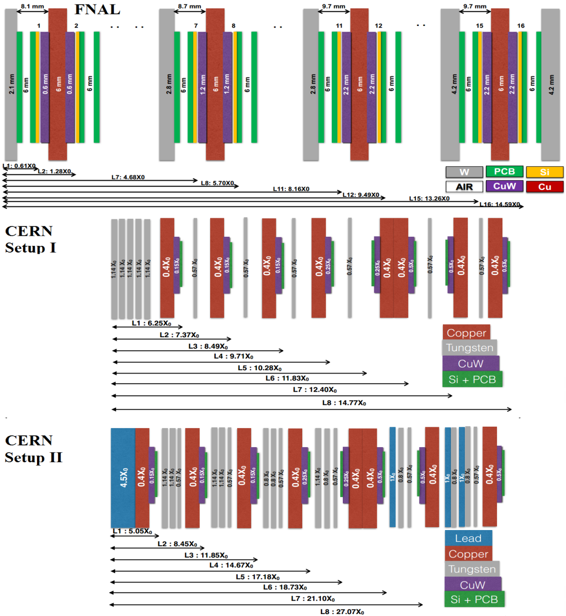




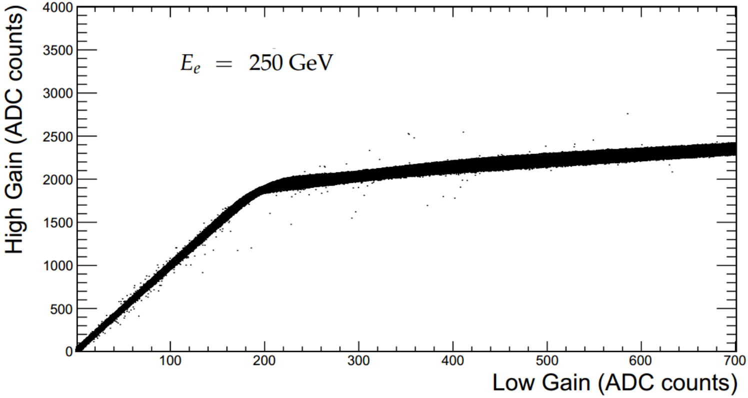
~ 700 wire bonds per module.

- SKIROC 2 ASIC(64 channels per chip, 2 chips per module) developed by OMEGA group designed for the ILC. Not the final front-end chip for HGCAL.

Data taking setup



High gain - Low gain correlation



- High gain saturation around [1800;200] ADC in [HG;LG] plane
- HG/LG ratio ~ 10

Exciting year ahead. Opportunities to join the effort.