Electronics, trigger and data acquisition systems for the INO ICAL experiment

Satyanarayana Bheesette

For and on behalf of the INO/ICAL Electronics team

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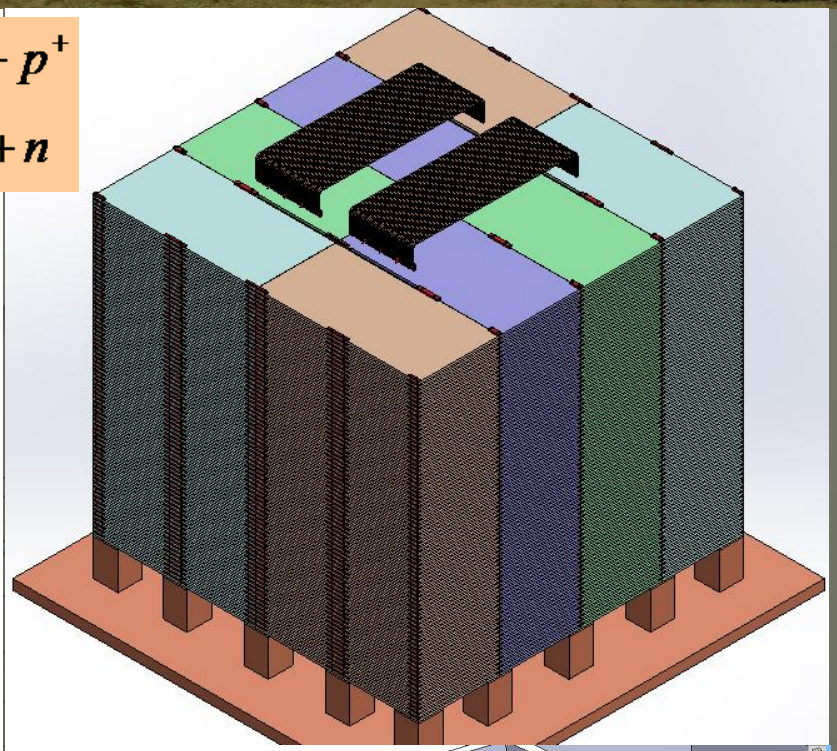
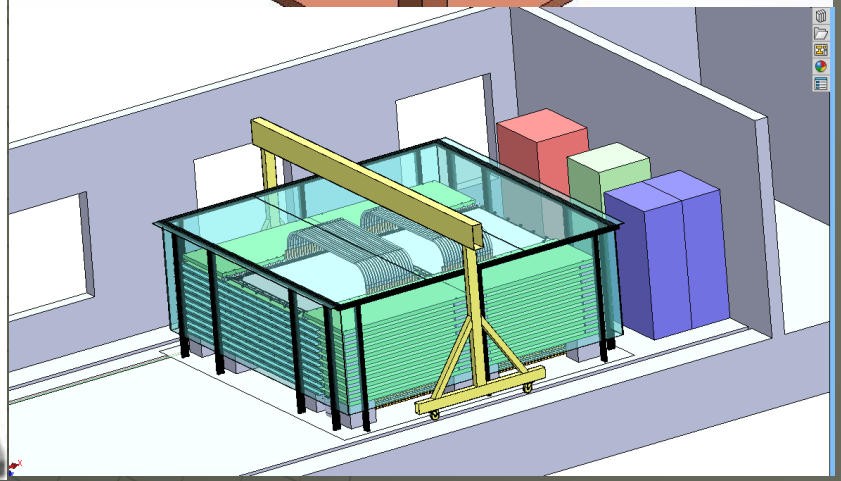
ICAL, e-ICAL and m-ICAL

$$\nu_\mu + n \rightarrow \mu^- + p^+$$

$$\bar{\nu}_\mu + p \rightarrow \mu^+ + n$$



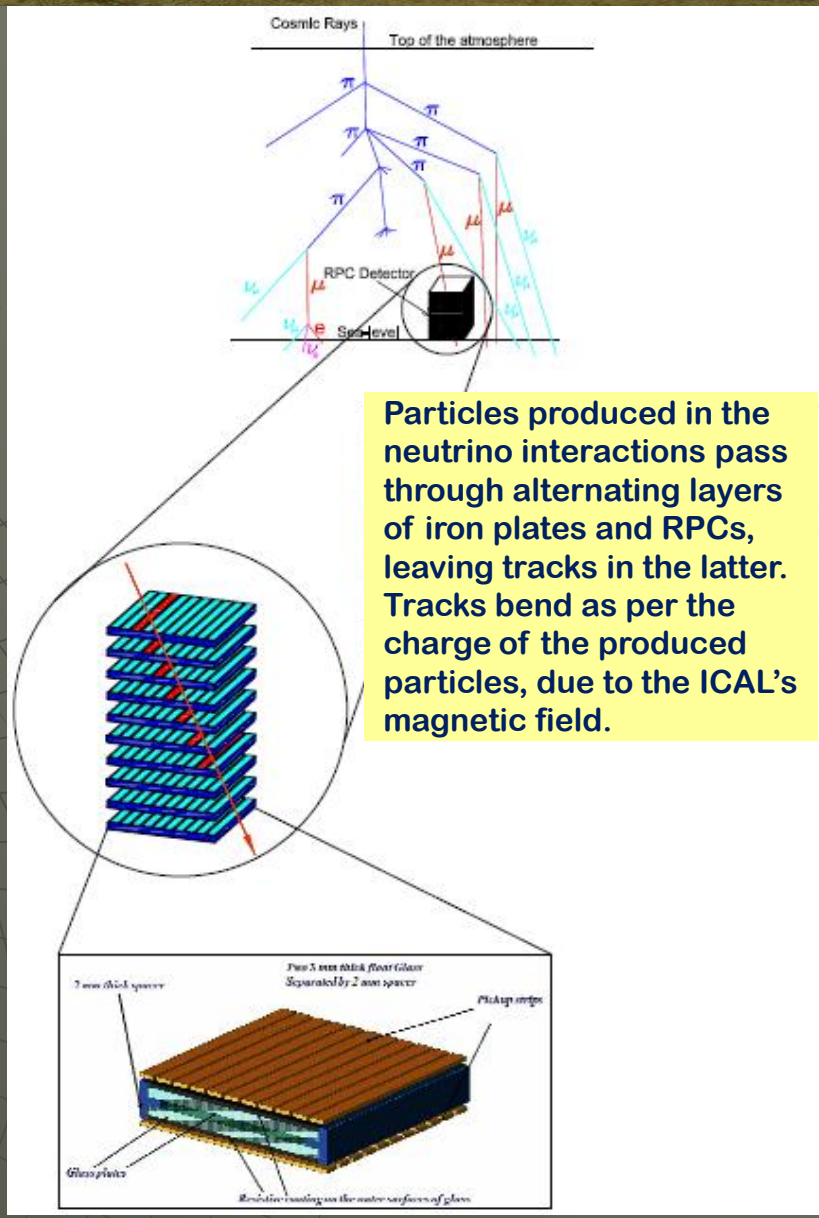


ICAL, e-ICAL and m-ICAL

Parameter	ICAL	e-ICAL	m-ICAL
No. of modules	3	1	1
Module dimensions	16.2m×16m×14.5m	8m×8m×2m (90:1)	4m×4m×1m (720:1)
Detector dimensions	49m×16m×14.5m	8m×8m×2m	4m×4m×1m
No. of layers	150	20	10
Iron plate thickness	56mm	56mm	56mm
Gap for RPC trays	40mm	40mm	45mm
Magnetic field	1.3Tesla	1.3Tesla	1.3Tesla
RPC dimensions	1,950mm×1,910mm×24mm	1,950mm×1,910mm×24mm	1,950mm×1,910mm×24mm
Readout strip pitch	30mm	30mm	30mm
No. of RPCs/Road/Layer	8	4	2
No. of Roads/Layer/Module	8	4	1
No. of RPC units/Layer	192	16	2
No. of RPC units	28,800 (107,266m^2)	320 (1,192m^2) (90:1)	20 (74.5m^2) (1440:1)
No. of readout strips	3,686,400	40,960 (90:1)	2,560 (1440:1)

Functions of ICAL electronics

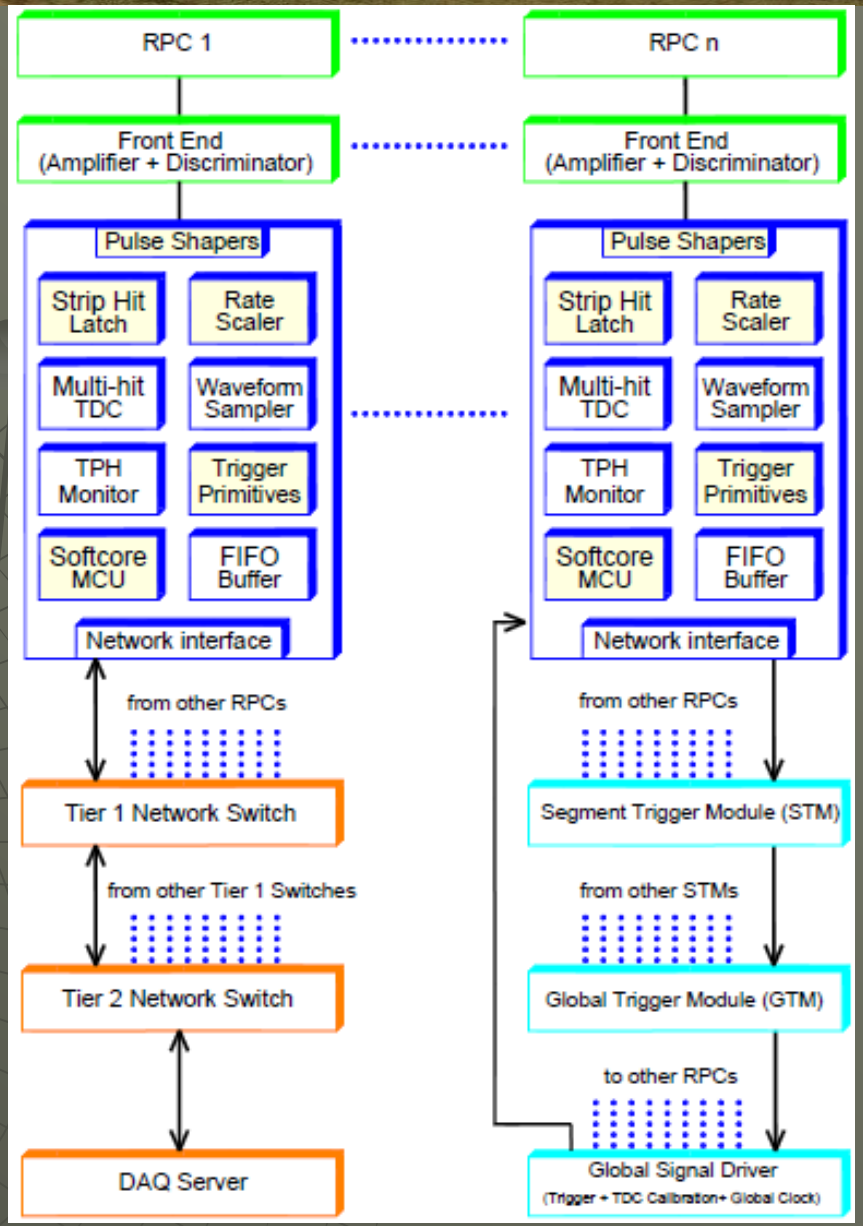
- Signal pickup and analog front-end
- Strip hit latch
- Pulse shapers, timing units
- Background noise rate monitor
- Digital front-end and calibration
- Data network architecture
- Multilevel trigger system
- Backend data concentrators
- Event building, data storage systems
- On-line data quality monitors
- Slow control and monitoring
  - Gas system, magnet, power supplies
  - Ambient parameters
  - Safety and interlocks
- Remote access to detector and data



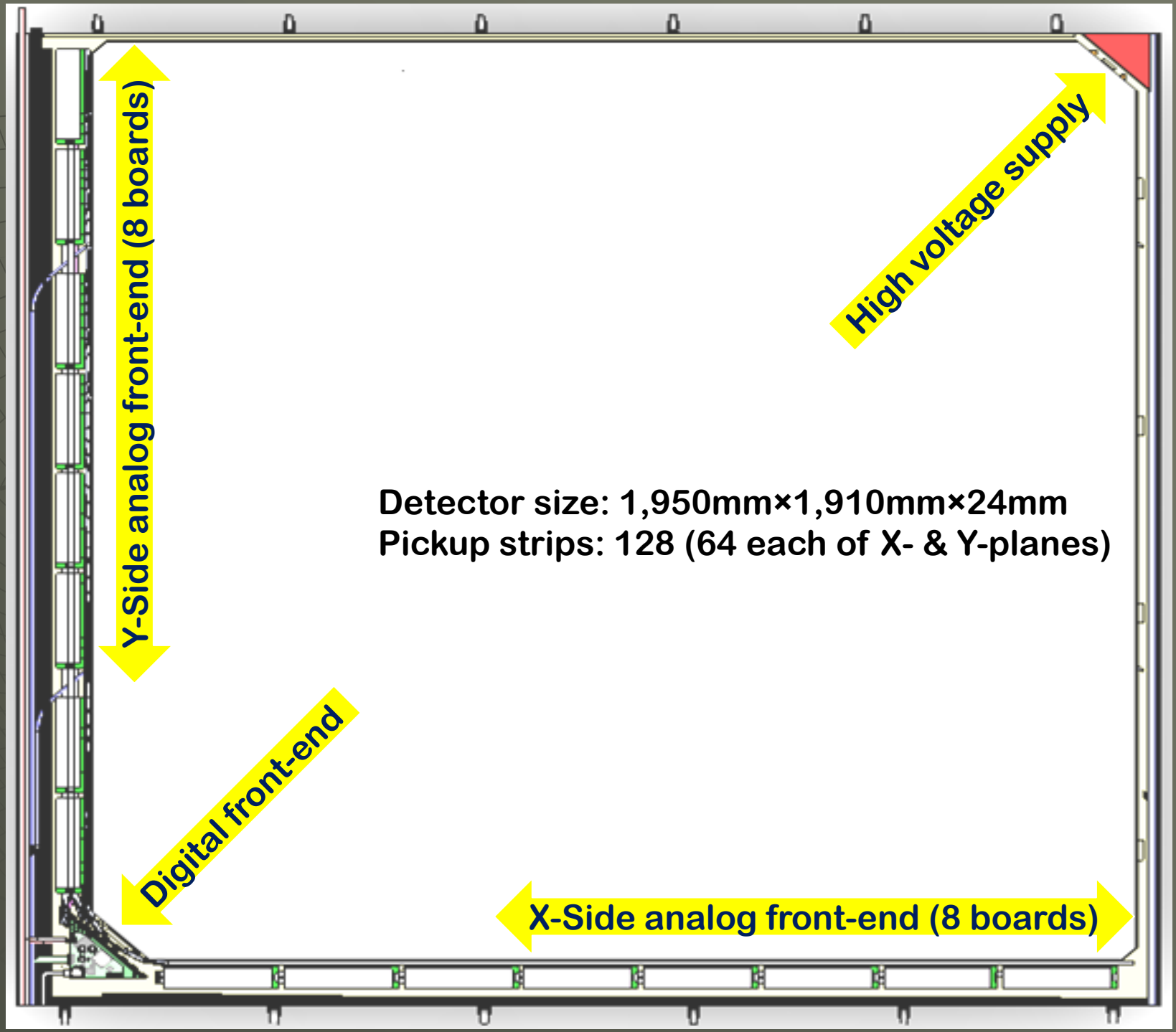
Particles produced in the neutrino interactions pass through alternating layers of iron plates and RPCs, leaving tracks in the latter. Tracks bend as per the charge of the produced particles, due to the ICAL's magnetic field.

Sub-systems of ICAL electronics

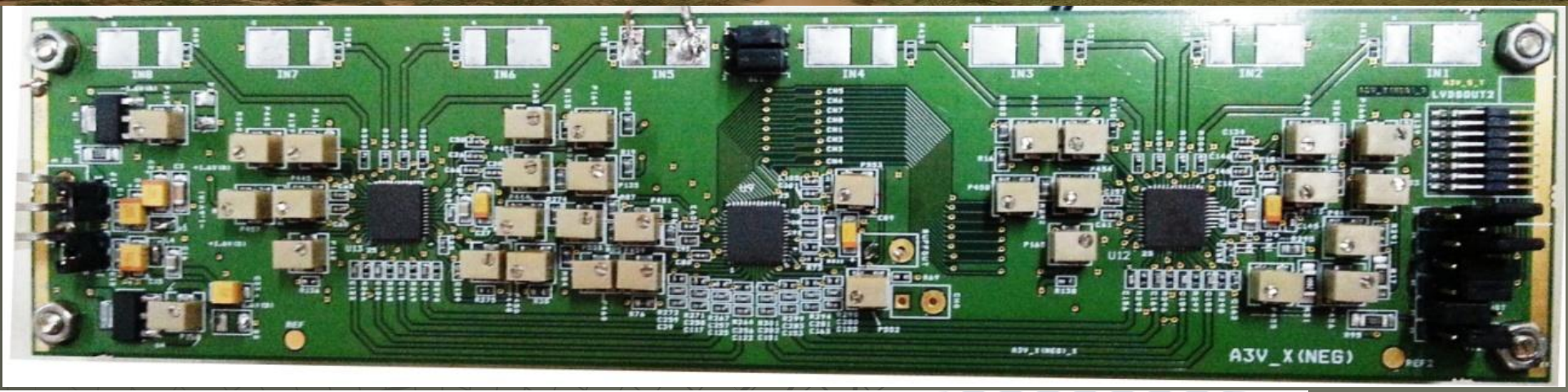
- Analog Front-ends
- TDC ASIC
- Digital Front-Ends
- Trigger System
- Global services, calibration and synchronisation units
- Data network and backend hardware
- Backend DAQ software
- Low voltage system
- High Voltage module
- Electronics integration



Outline of an RPC detector



Analog Front-End boards with Anusparsh ASICs



Fast Amplifier

Dynamically biased buffer

Voltage Amplifier
I/P terminated on 50Ω
Power ~12 mW/ch

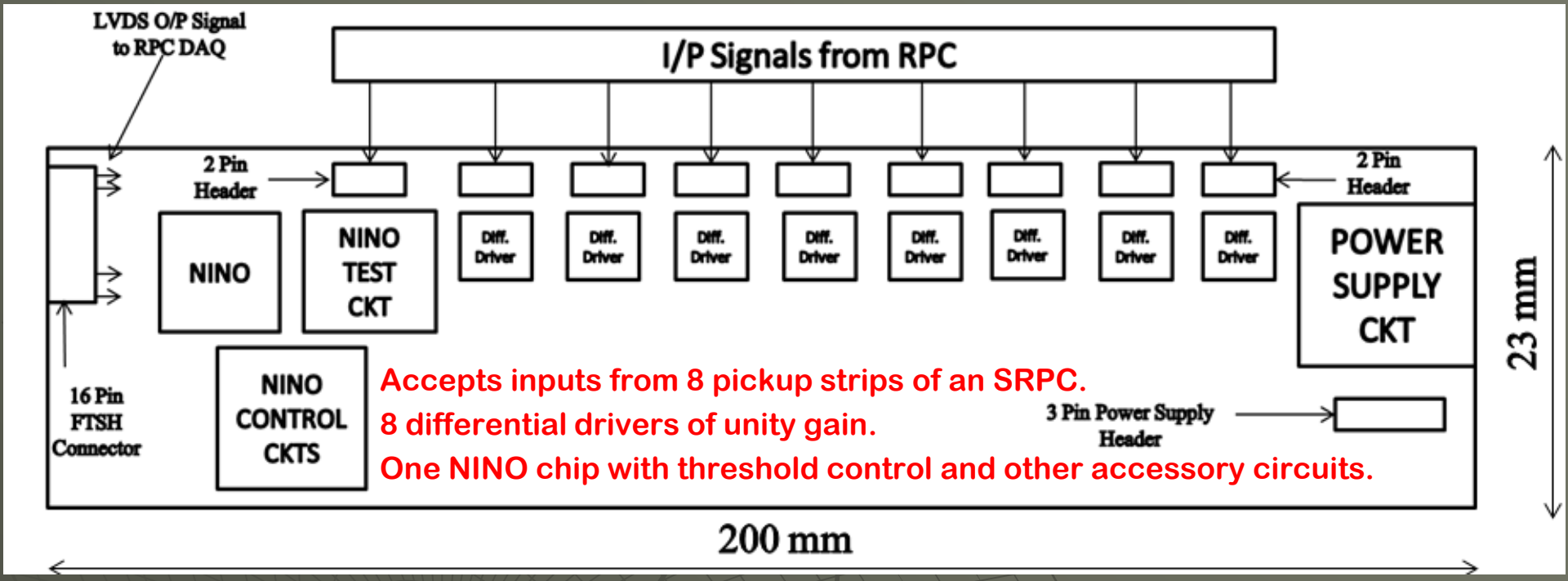
Fast Discriminator with LVDS driver
Power ~ 20mW/ch

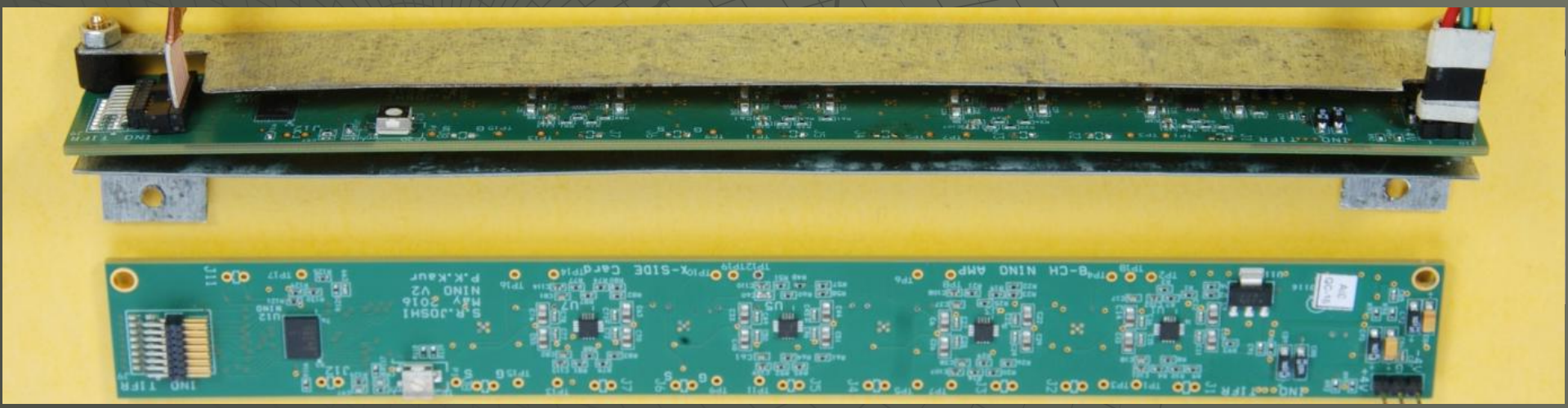
Multiplexed Analog buffer to drive 50Ω
Dynamically biased flipped voltage follower

ASICs designed using 0.35µm SiGe BiCMOS process and packaged in QFN-48.

Combined mask set for Amp and Disc ASICs. 15 wafers in production for 16,600 amp and 8,300 disc ASICs.

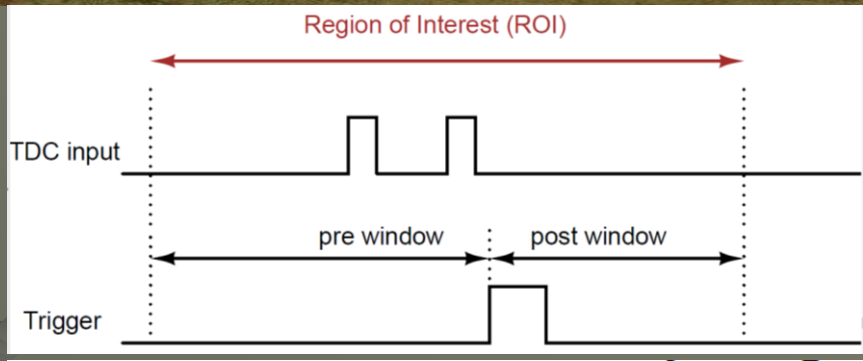
Analog Front-End boards with NINO ASICs

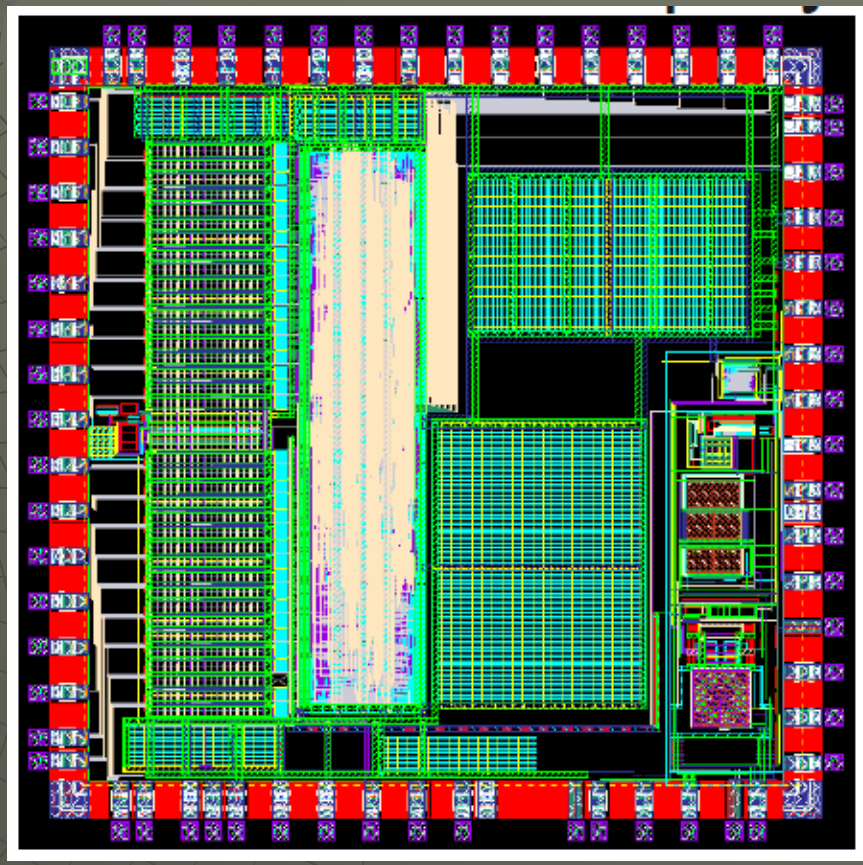




ICAL's TDC ASIC

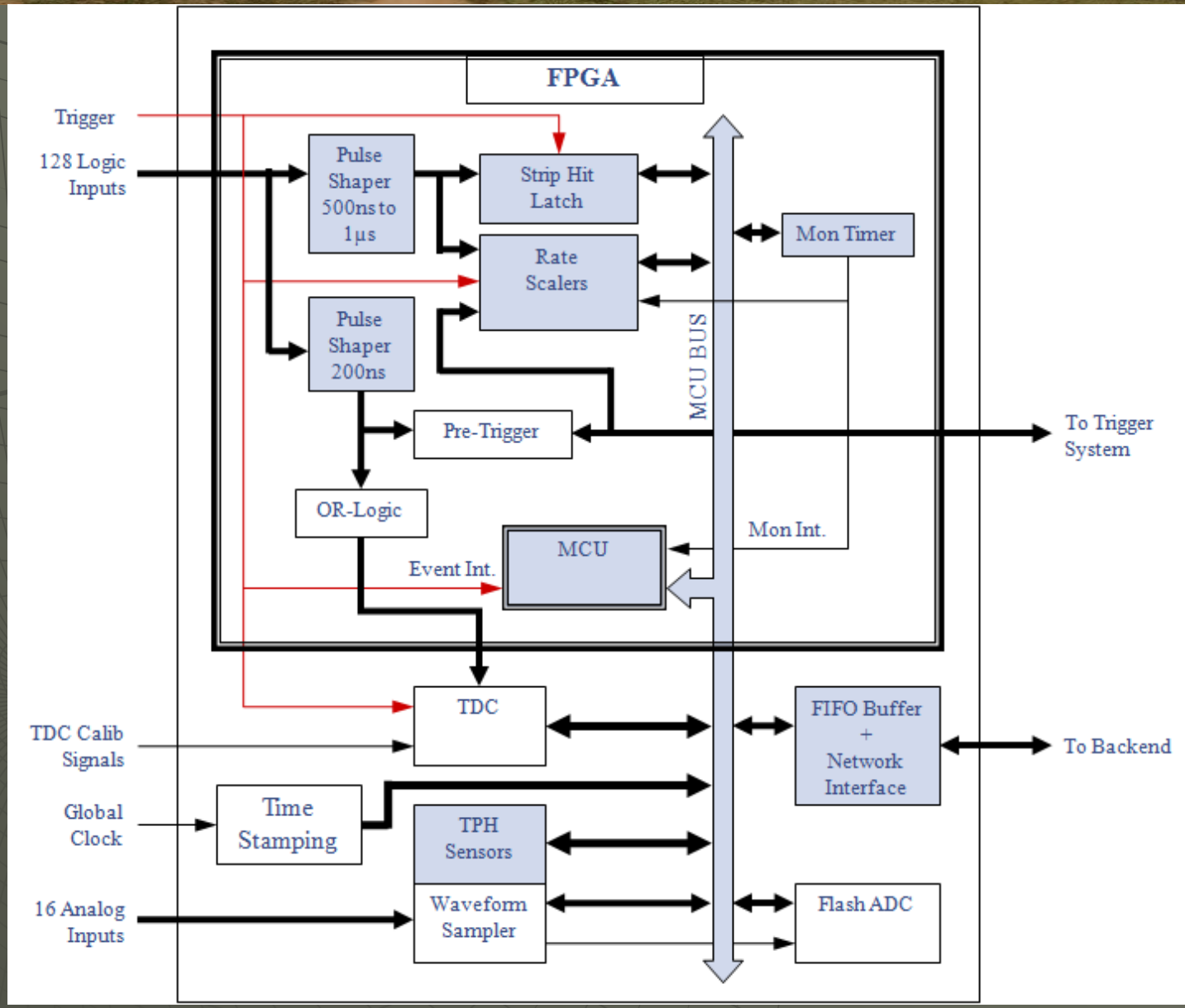
- **Principle**
  - Two fine TDCs to measure start/stop distance to clock edge (T1, T2)
  - Coarse TDC to count the number of clocks between start and stop (T3)
  - TDC output = T3+T1-T2
- **Features and specifications**
  - UMC 130nm technology, QFN64 package, 3.2mm×3.2mm in size
  - Input clock: 10MHz (250MHz to DLL internally generated by PLL)
  - 16 hit channels, 1 trigger and 1 calibration channel
  - Four paired time stamps: leading edge 65.5μs (125ps), pulse width 64ns (250ps)
  - Readout buffers: 91 locations
  - 32-bit/hit, data on 4-and 11-line SPI bus.
  - Self test features



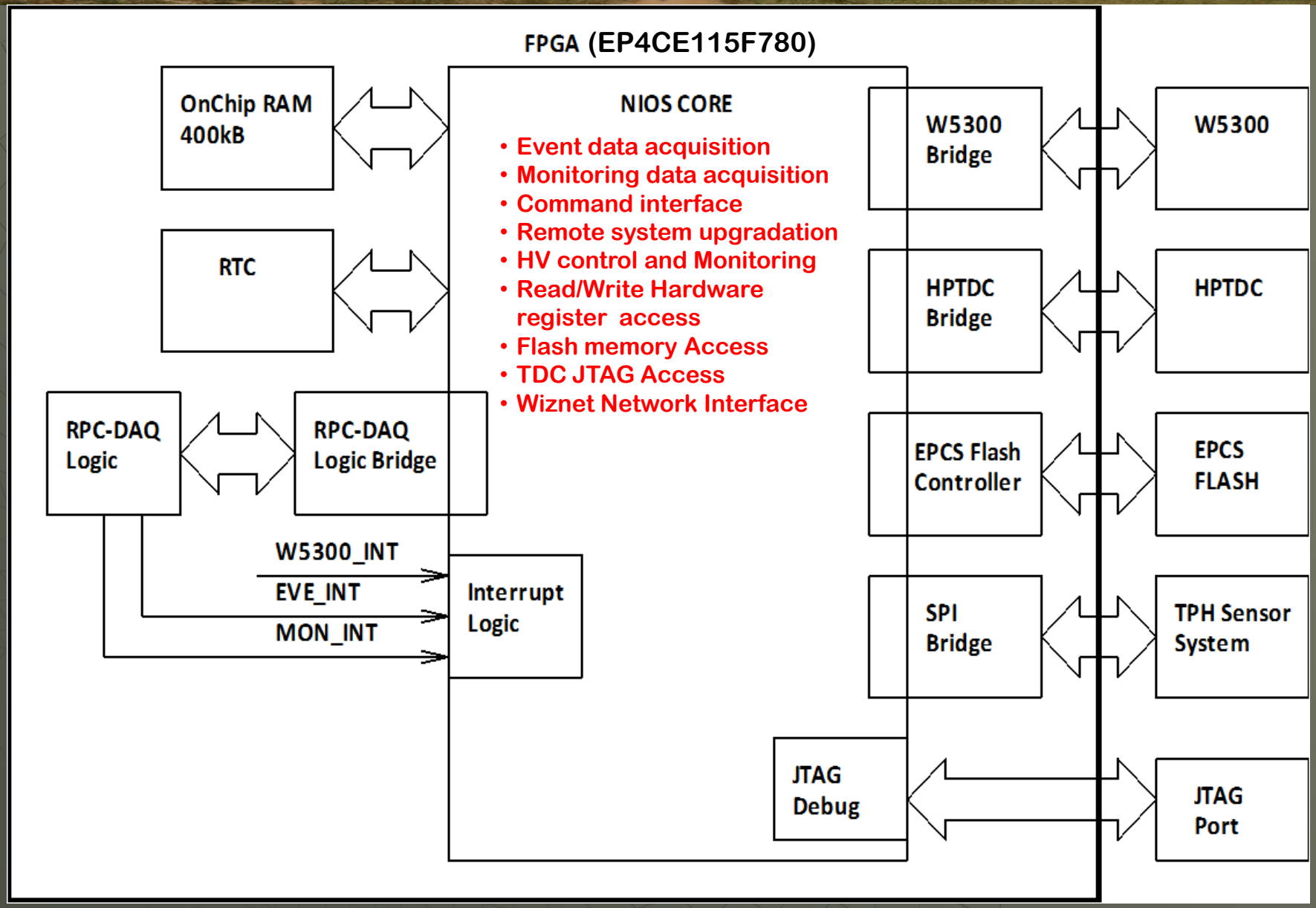


DFE module – the workhorse

- Unshaped, digitized, LVDS RPC signals from 128 strips (64x + 64y)
- 16 analog RPC signals, each signal is a summed or multiplexed output of 8 RPC amplified signals.
- Global trigger
- TDC calibration signals
- TCP/IP connection to backend for command and data transfer.

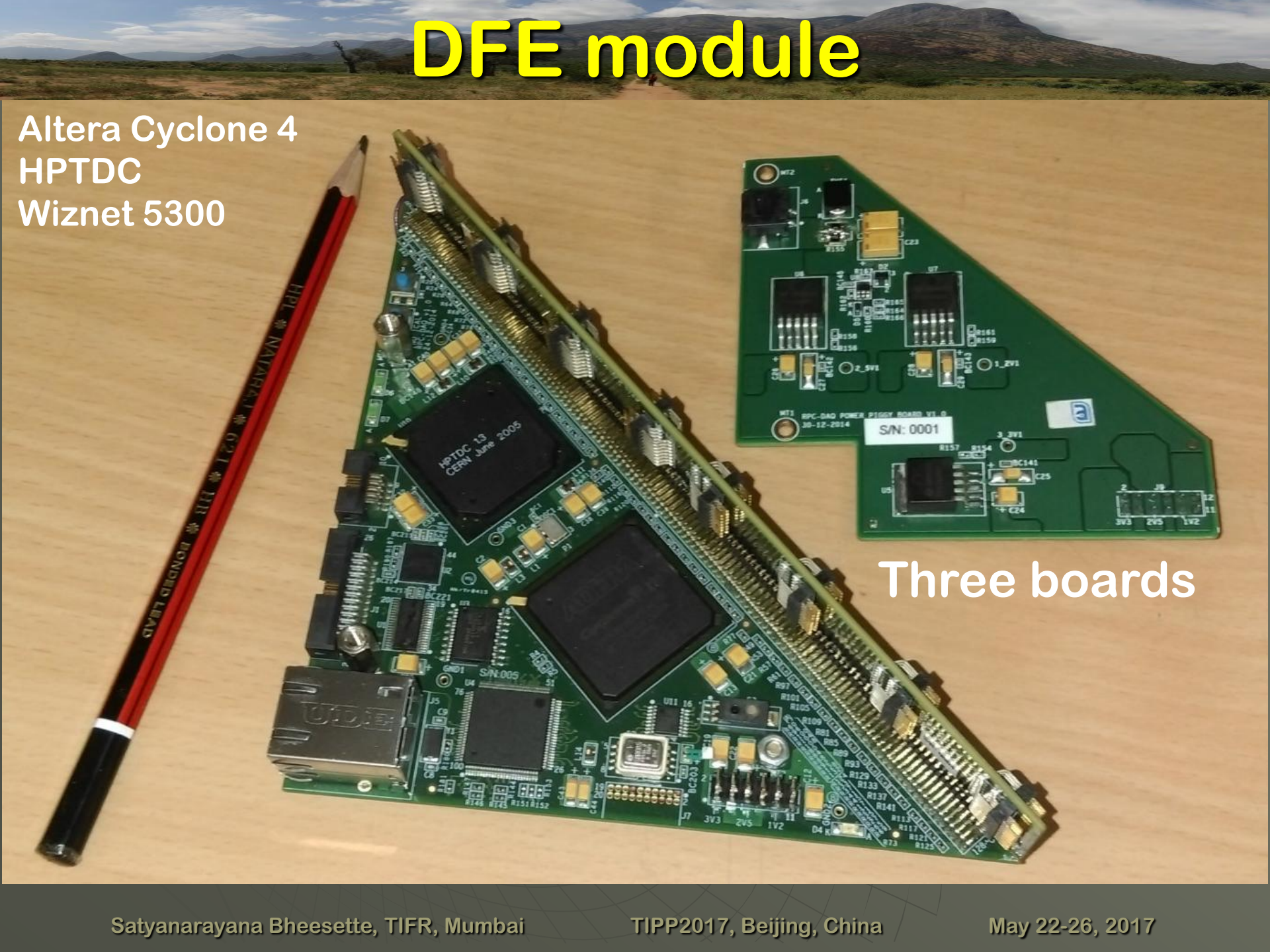


Soft-core processor



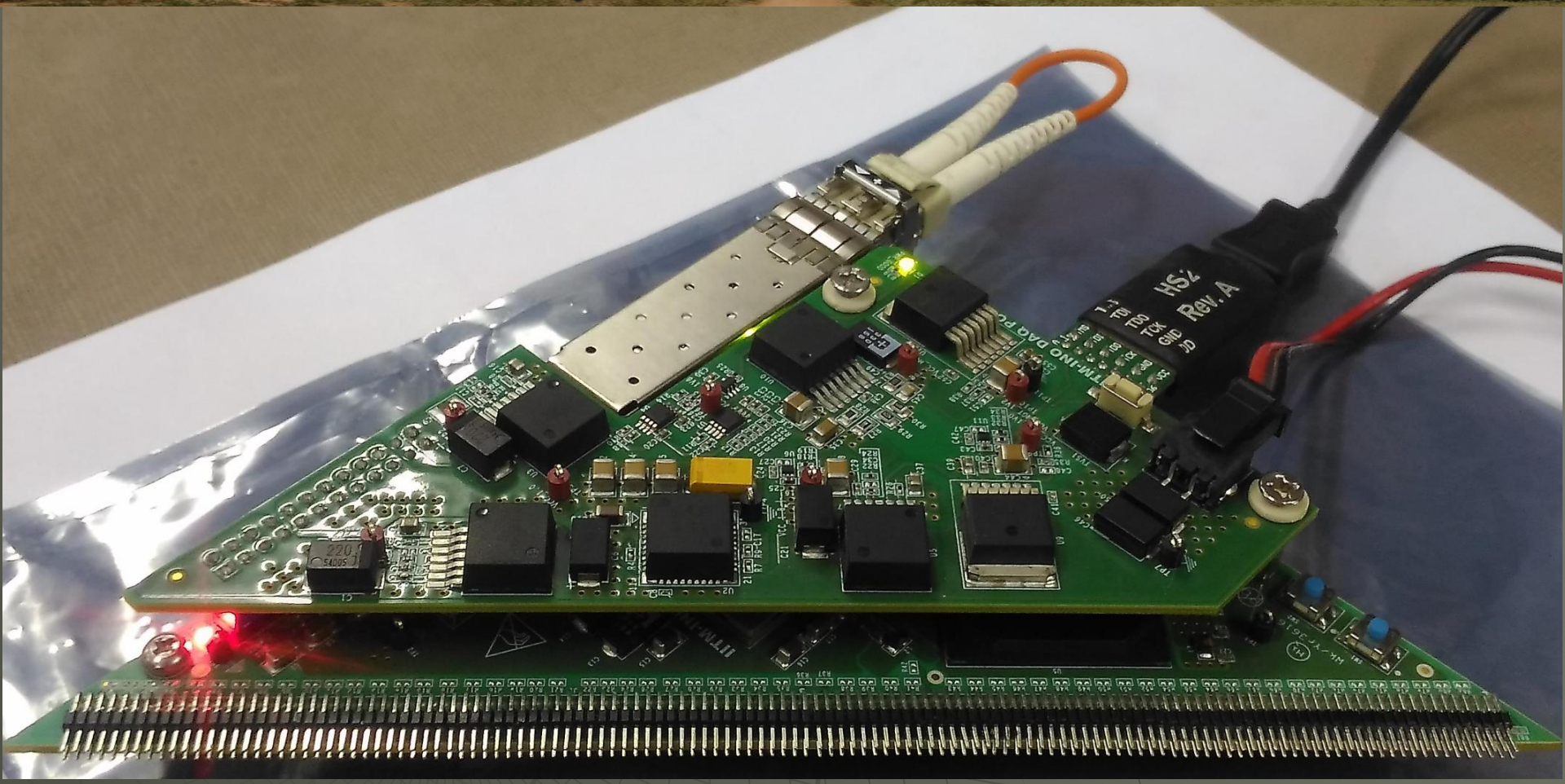
DFE module

Altera Cyclone 4
HPTDC
Wiznet 5300



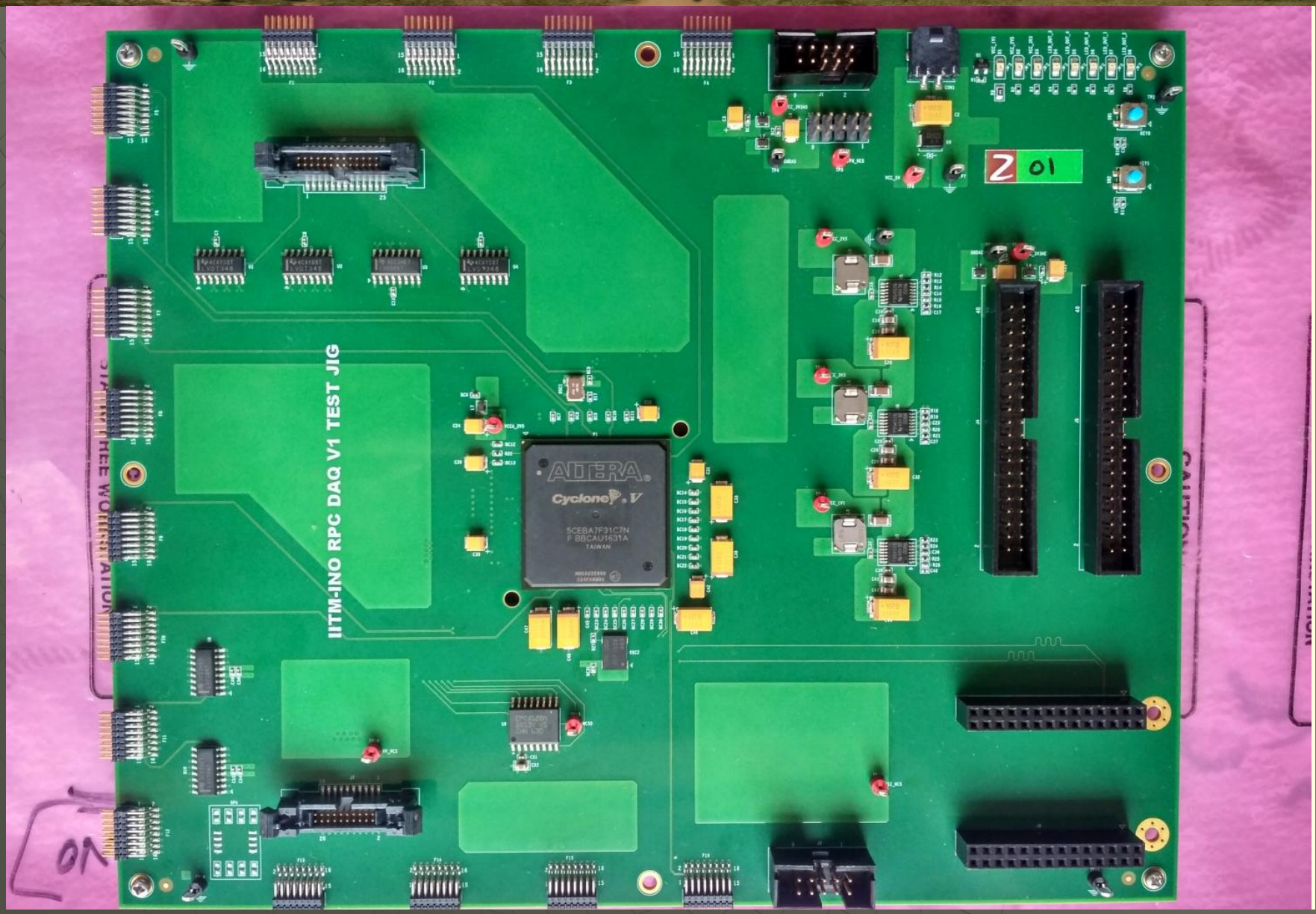
Three boards

DFE with optical data interface

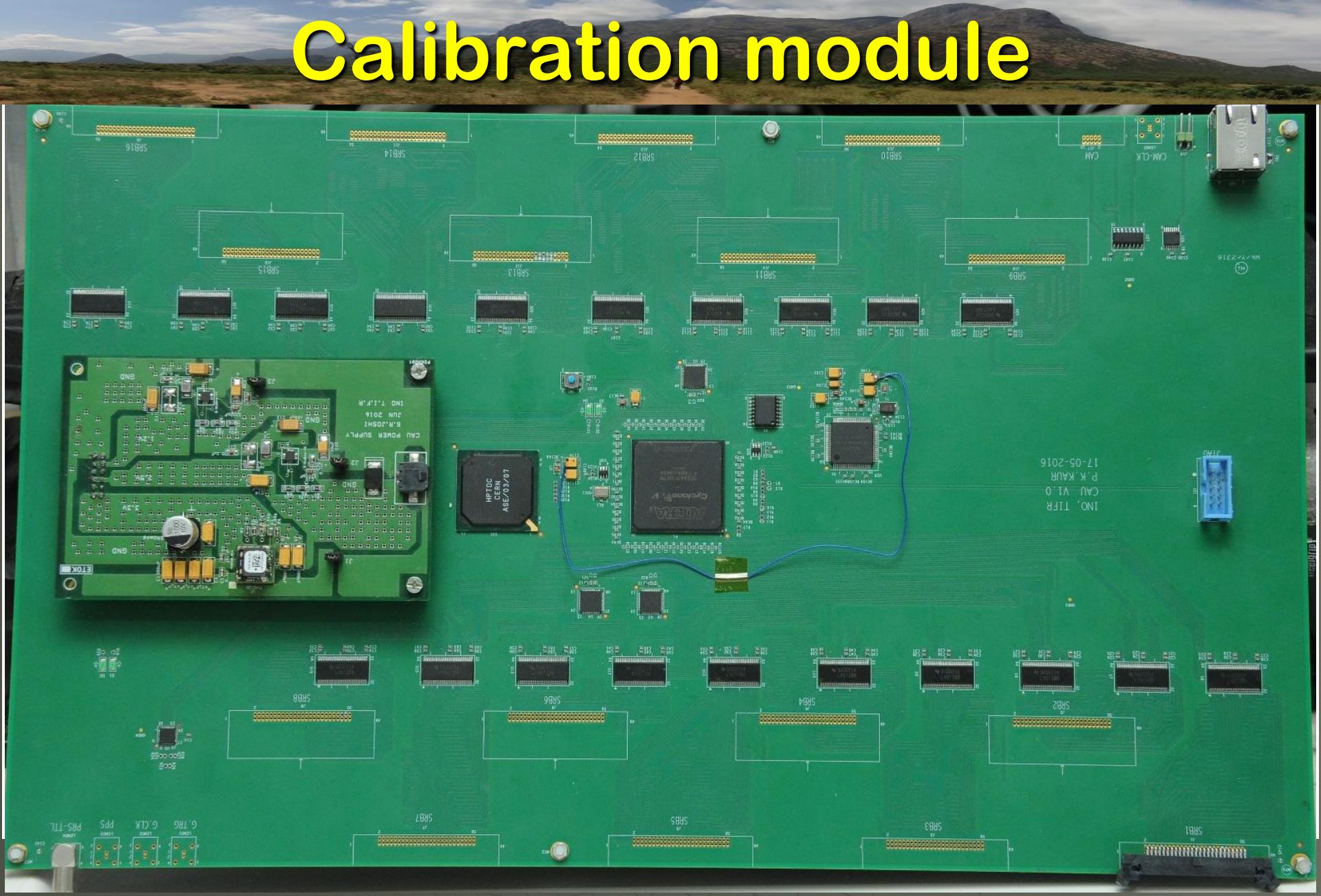


Xilinx Kintex-7 FPGA (XC7K160T-2FFG676I) and Aurora 64B66B IP core
SFP module (AFBR-709SMZ), 10Gb Ethernet, 850 nm, 10GBASE-SR/SW

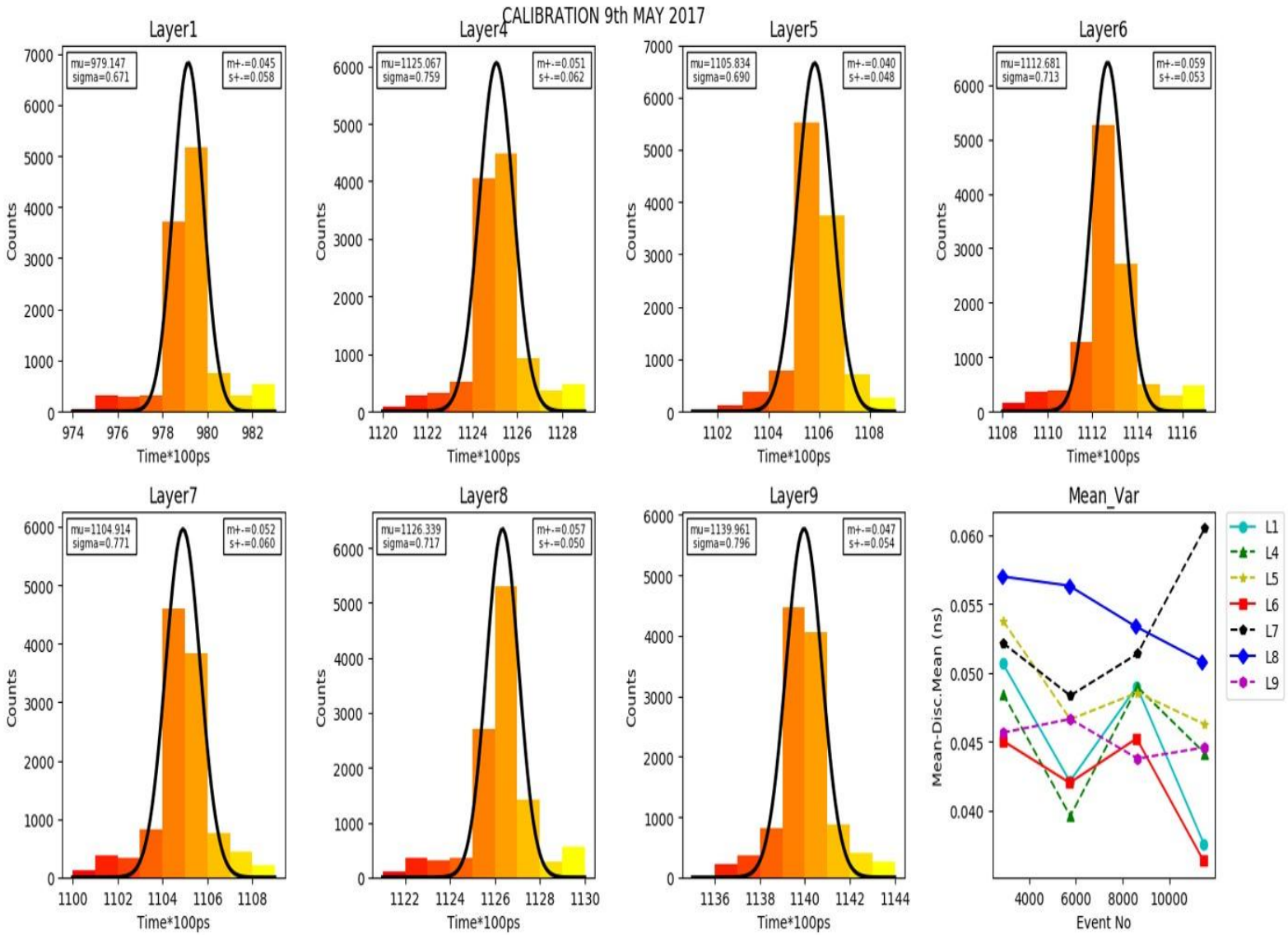
Test jig for DFE production QC



Calibration module

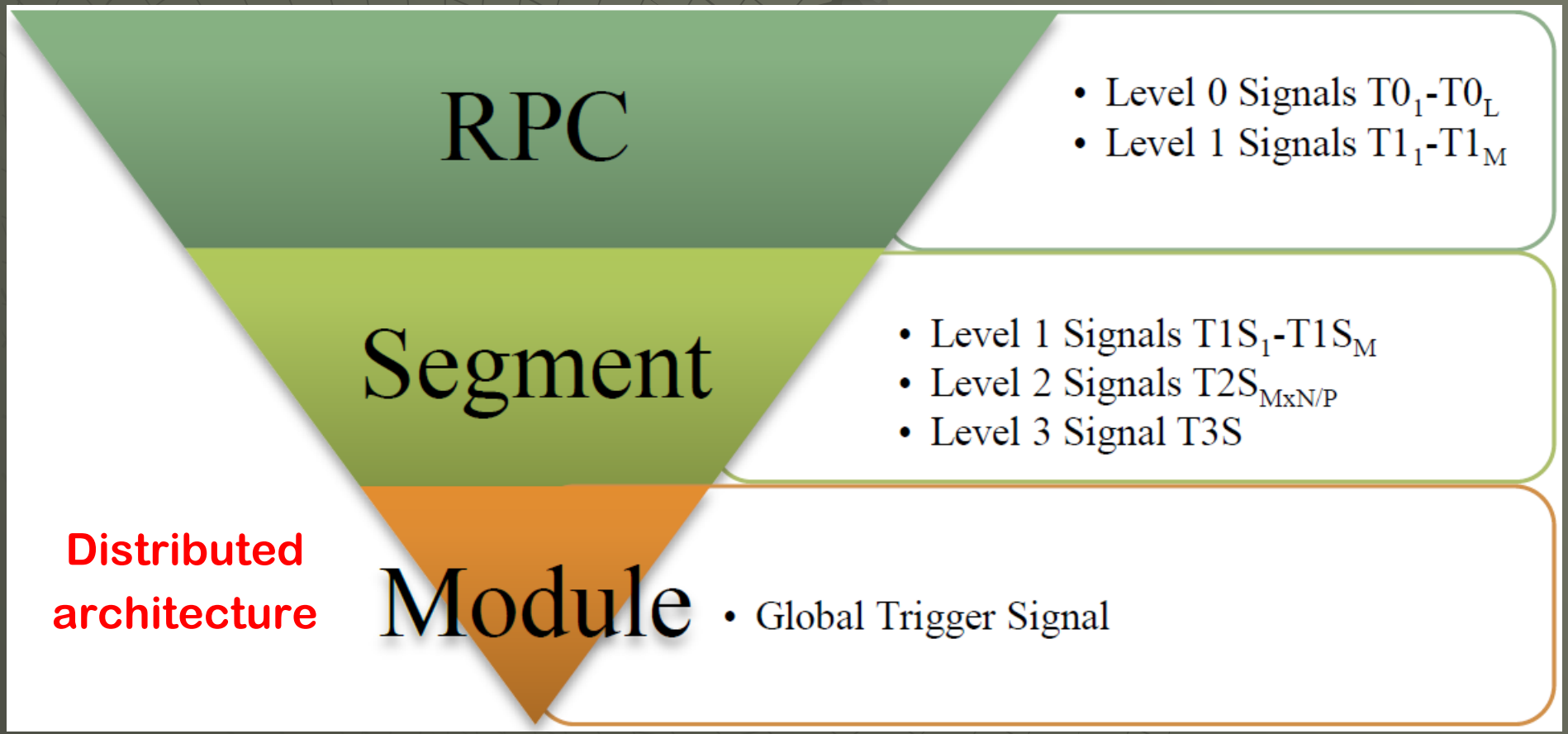


Performance of calibration module



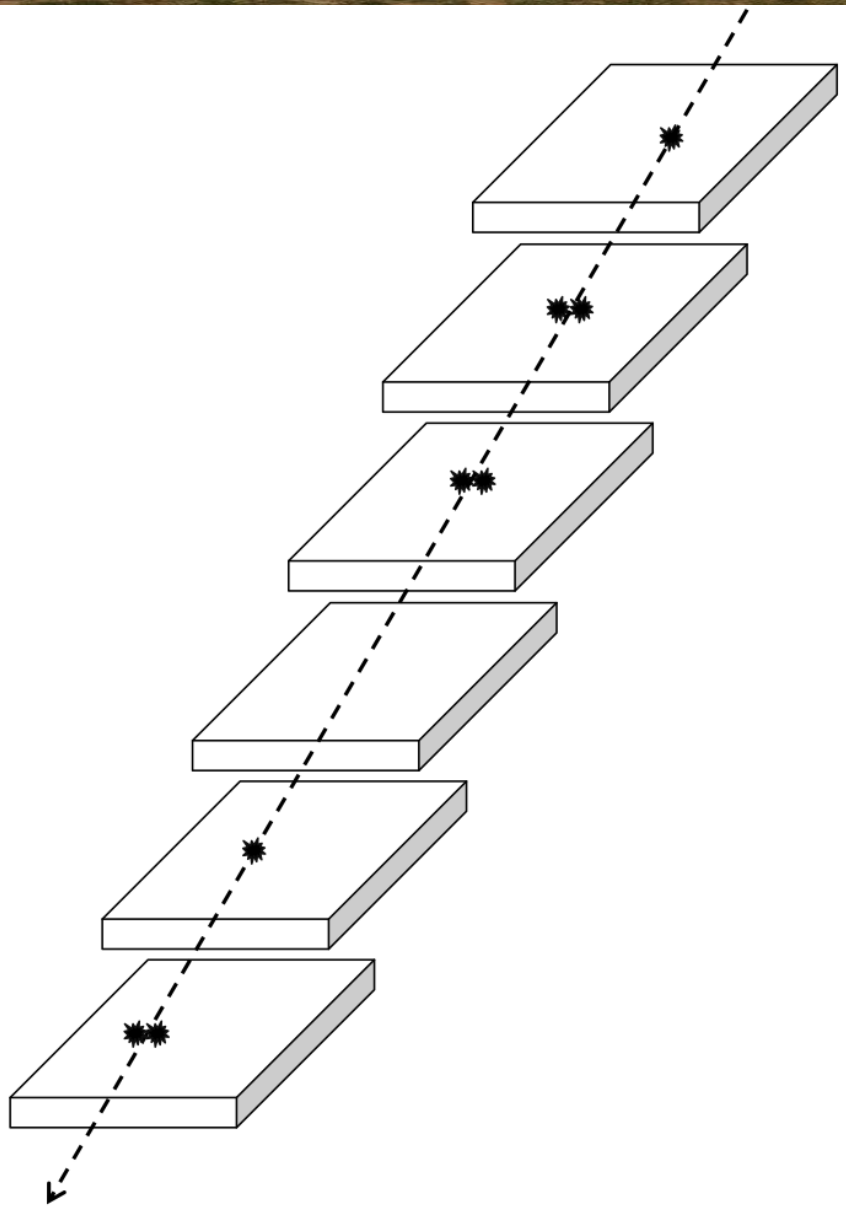
ICAL trigger scheme

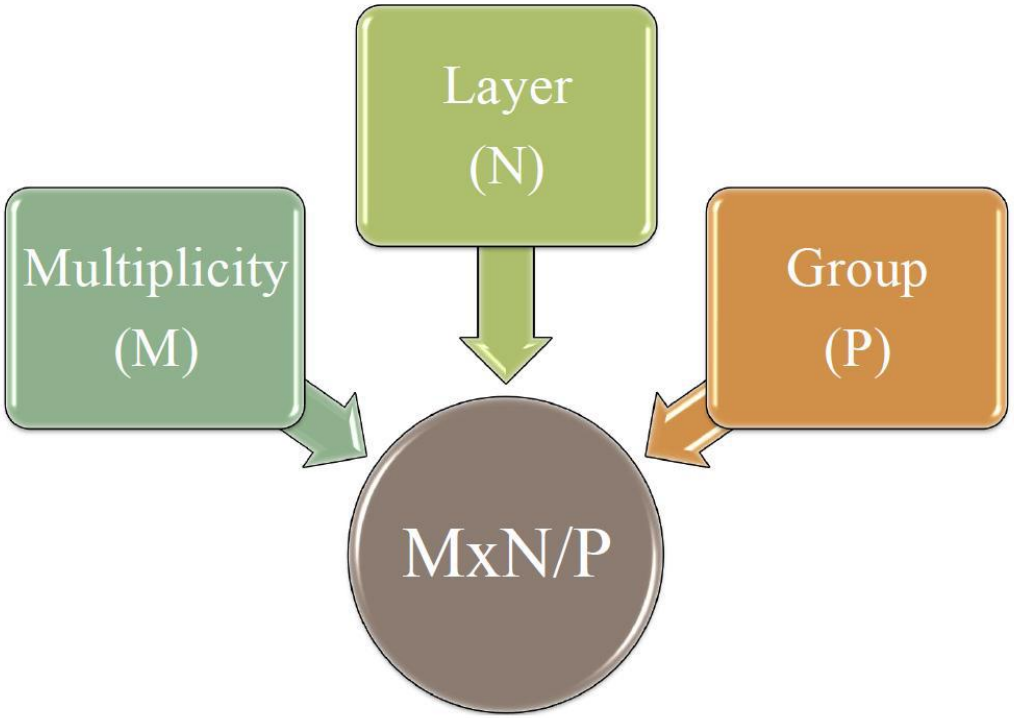
- *Insitu* trigger generation. Autonomous; shares data bus with readout system
- For ICAL, trigger system is based only on topology of the event; no other measurement data is used
- Huge bank of combinatorial circuits; Programmability is the game, FPGAs, ASICs are the players



Distributed architecture

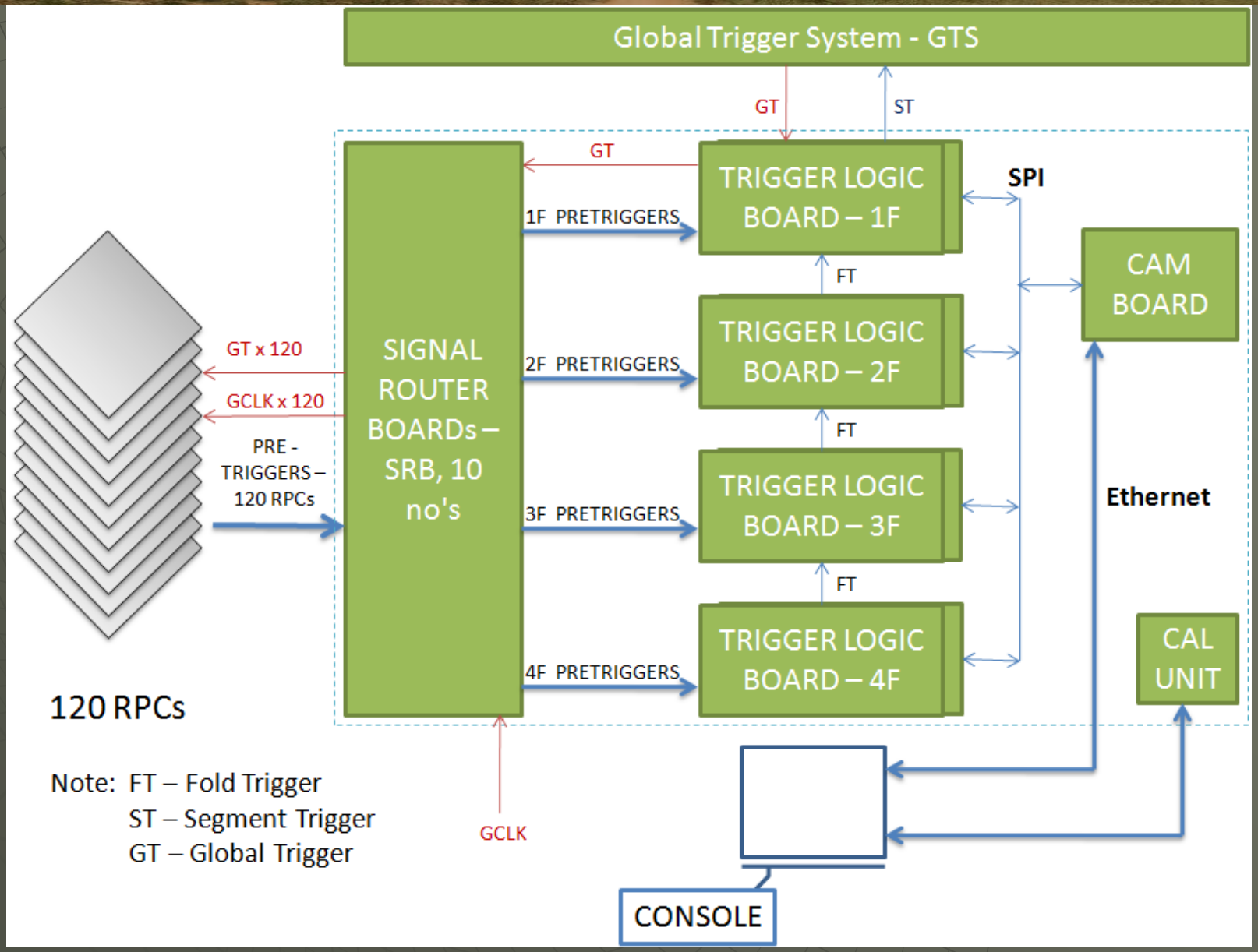
Trigger criteria



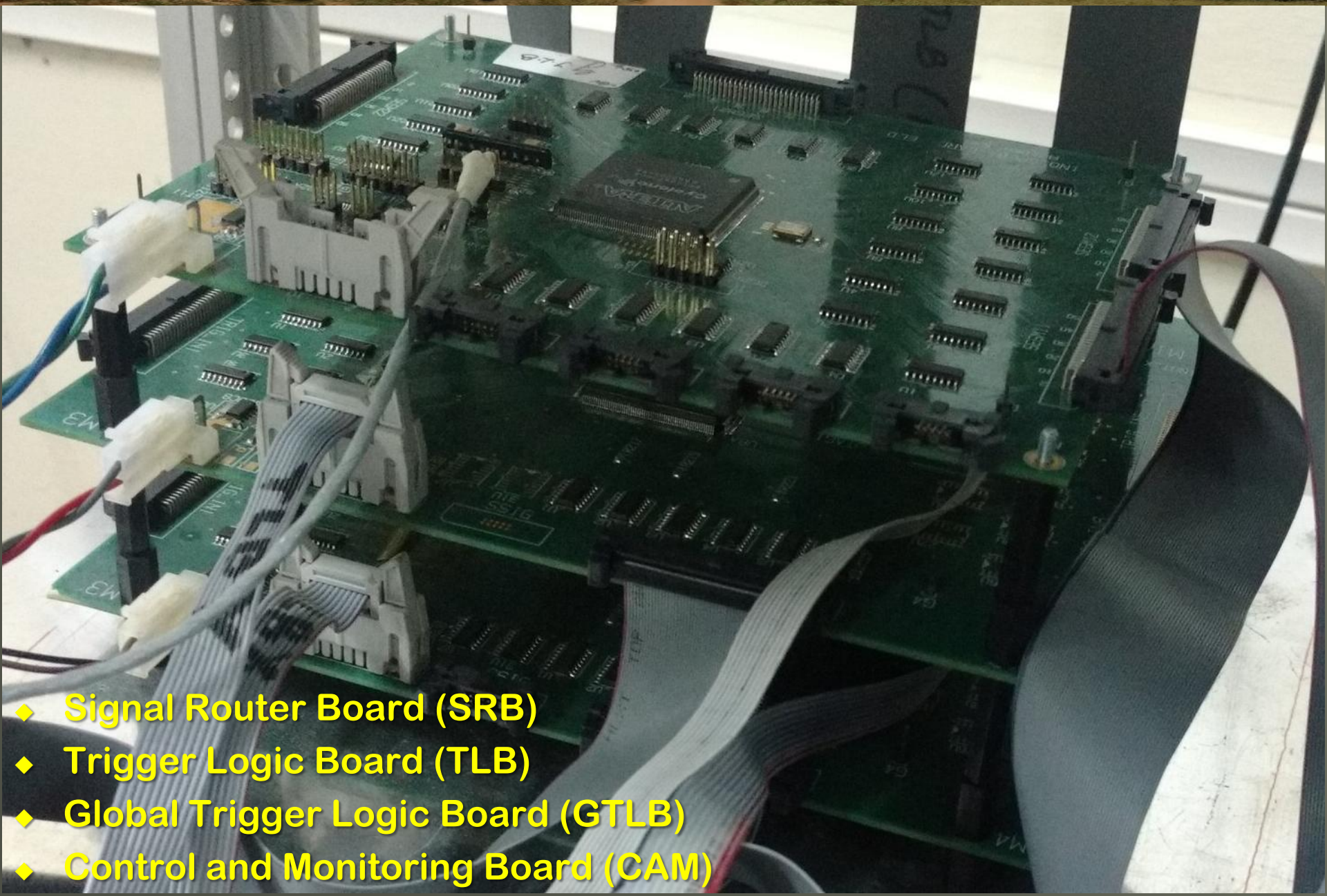


	Non-overlapped			Overlapped
RPC Strip Rate	Chance Rate for Full Trigger	Chance Rate for Partial Trigger	Total Chance Coincidence Rate	Total Chance Coincidence Rate
250 Hz	71 Hz	841 Hz	912 Hz	319 Hz
50 Hz	0.023 Hz	0.269 Hz	0.292 Hz	0.102 Hz

Trigger system for e-ICAL

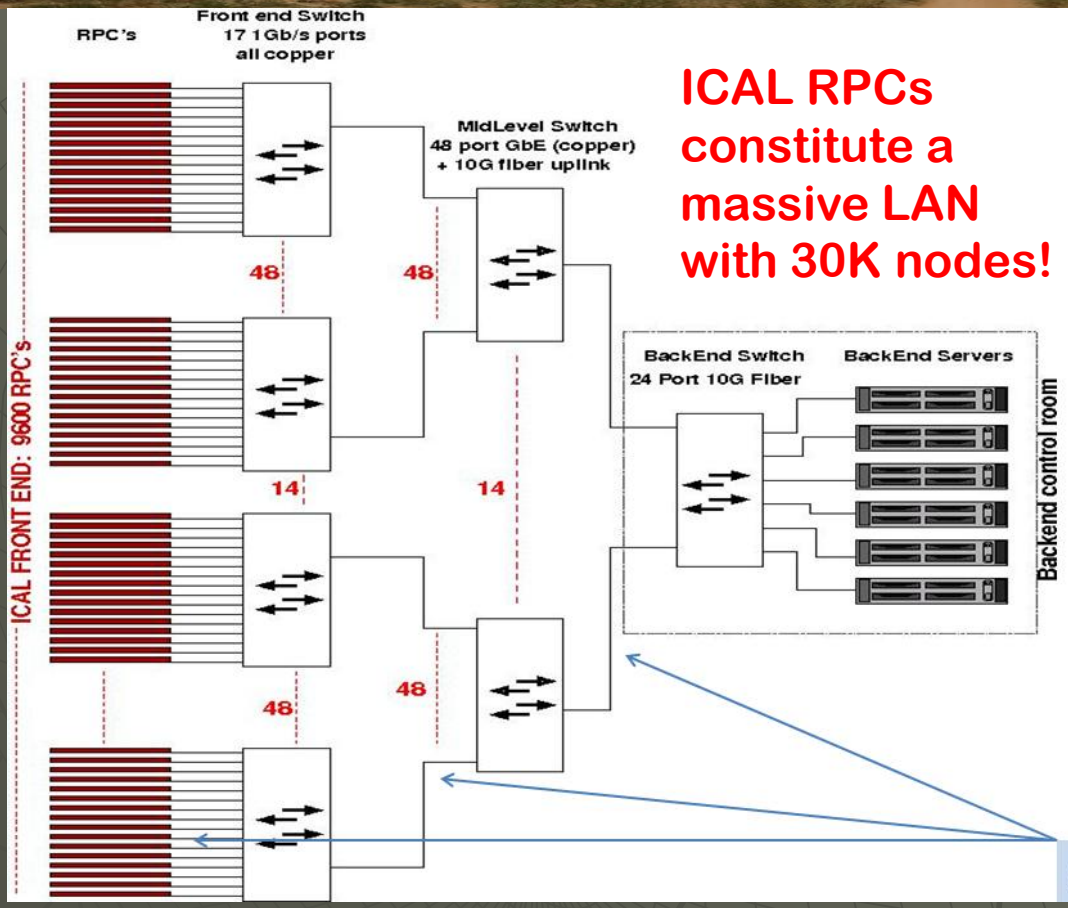


Trigger system with m-ICAL

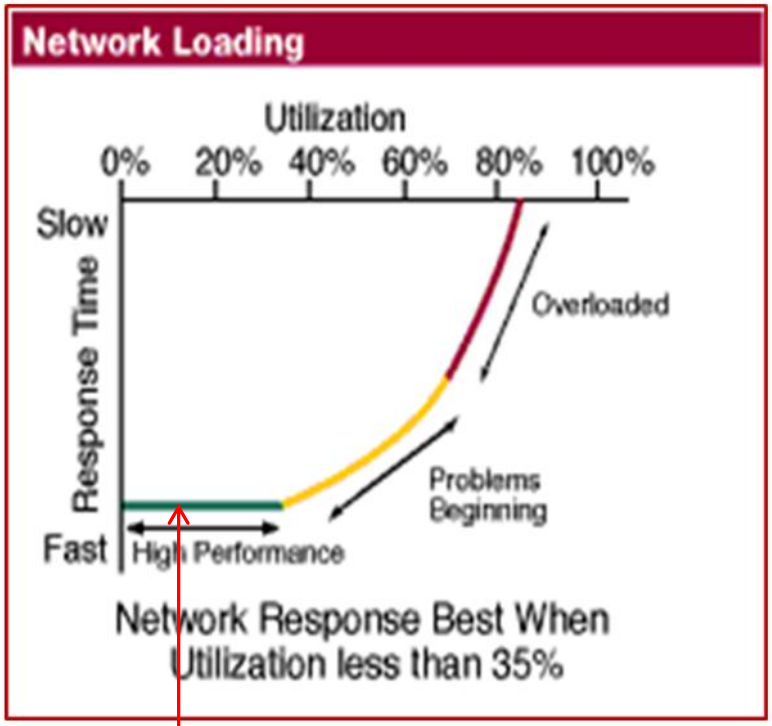


- Signal Router Board (SRB)
- Trigger Logic Board (TLB)
- Global Trigger Logic Board (GTLB)
- Control and Monitoring Board (CAM)

Overview of ICAL data LAN



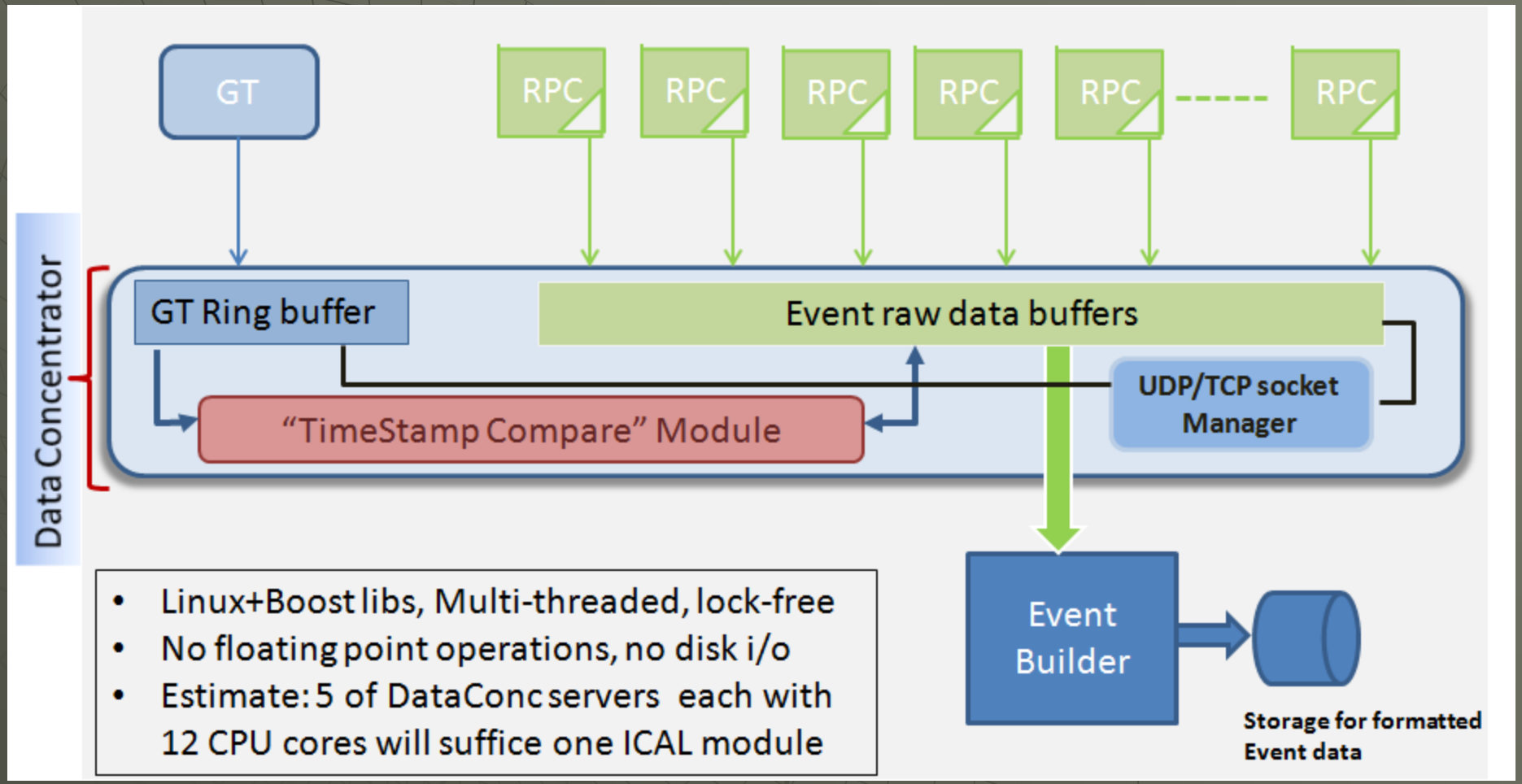
ICAL RPCs constitute a massive LAN with 30K nodes!



All cumulative traffic in high performance region

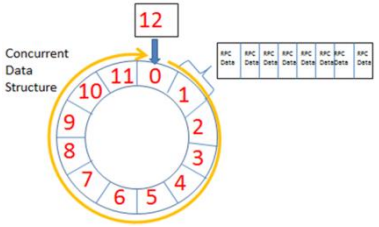
	Basic Data Size per RPC (Frond end)		Data Rate at backend	
	Without pulse profile	With pulse profile	Without Pulse Profile	With Pulse Profile
Event data (ICAL)	4384 bits	29984 bits	42.8Kbps (assuming 10Hz event rate)	292.8Kbps
Event data (ICAL-EM)	4384 bits	----------	1600Mbps (assuming 10KHz event rate)	----------
Monitor data (10s)	688 bits	3200688 bits	69 bps	312.6Kbps

Back-end data concentrator hardware



Back-end DAQ software

Data recording, DQMs, Visualization and Control



Long term Archival

Event Logger and Periodic Monitoring Node (EVENT BUILDER)

- Receives raw event (RPC) data that is pushed to it by the Data Concentrator.
- Combines raw data from various RPC's into a single chunk of "event data" based on Event Number.
- Writes into ROOT format files into short term high speed RAID based storage.

Remote Console-1

Remote Console-n

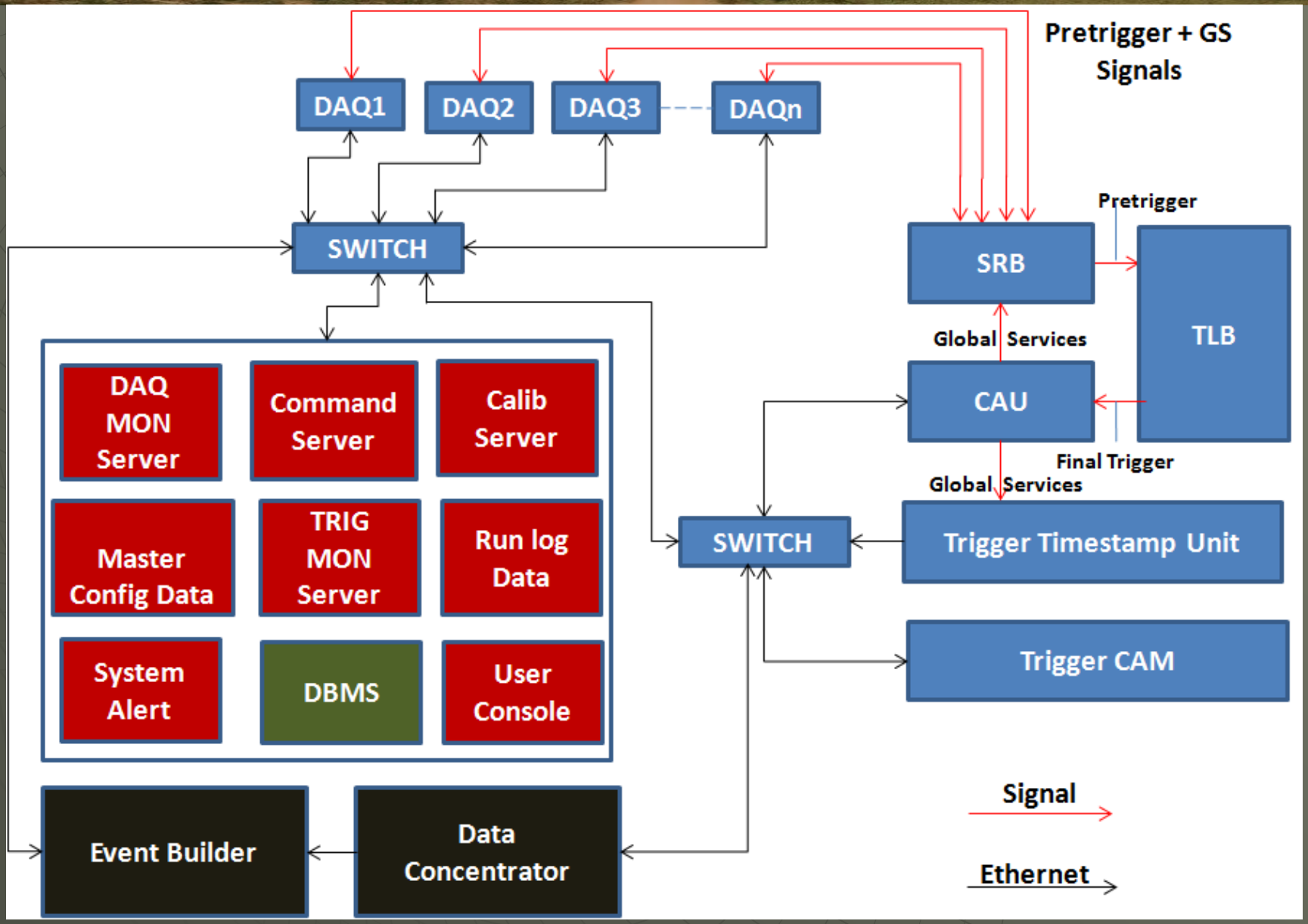
Local Consoles (1..n)

Run control And monitoring

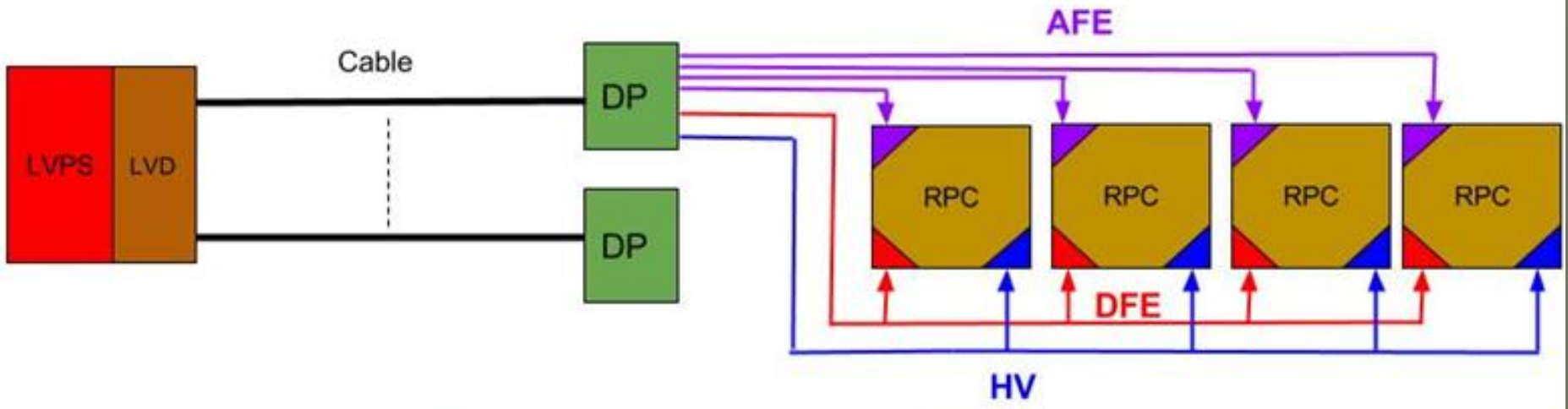
Configuration Console

Data Quality Monitor Console

System integration



LV Power Supply and distribution

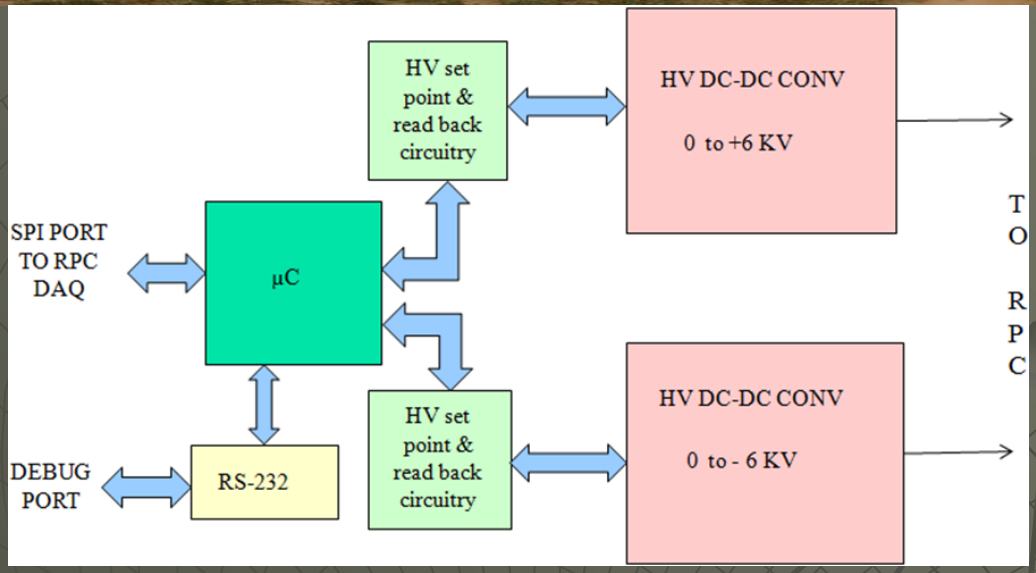


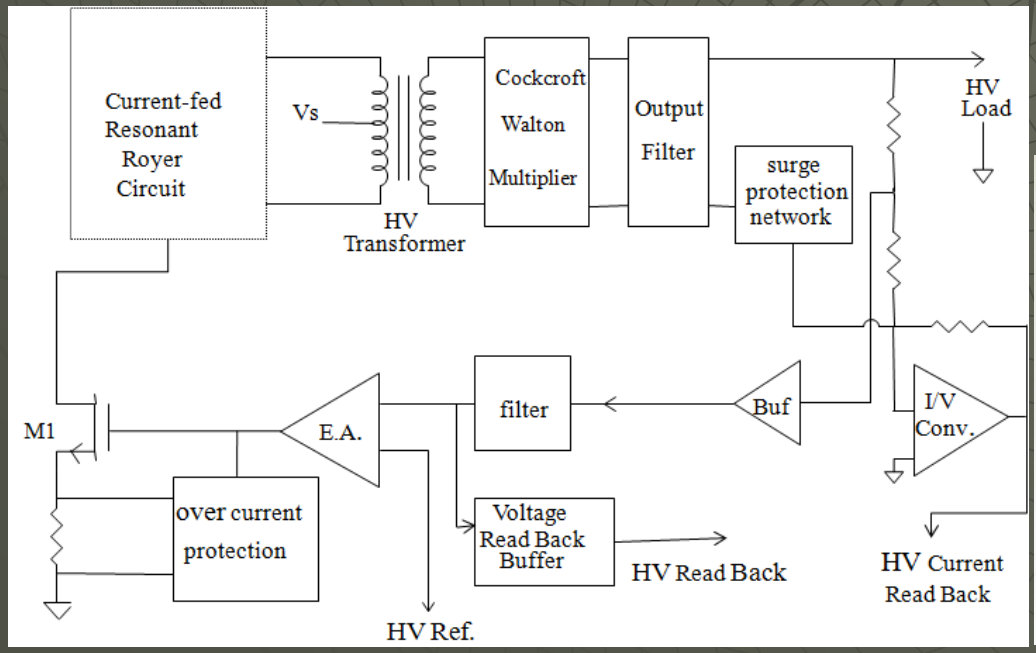
LVPS: Low Voltage Power Supply	RPC: Resistive Plate Chamber
LVD: Low Voltage Distributor	AFE: Analog Front-End
DP: Distribution Panel	DFE: Digital Front-End
	HV: High Voltage

Cables:- Each Cable will deliver power to four RPCs.
Cable Specification:-
DFE: 2 wires, +V and ground.
AFE: 12 wires; +V, -V and ground.
HV: 2 wires; +V and ground.

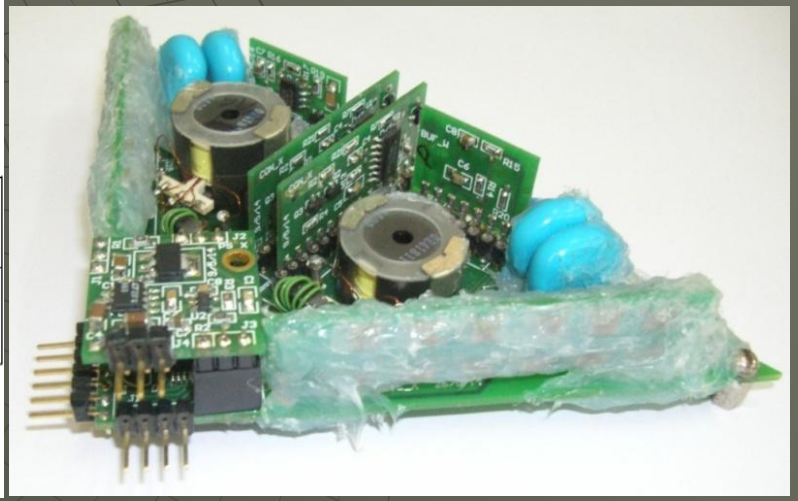
Design scheme is complete. Prototyping is in progress.

High voltage power supply

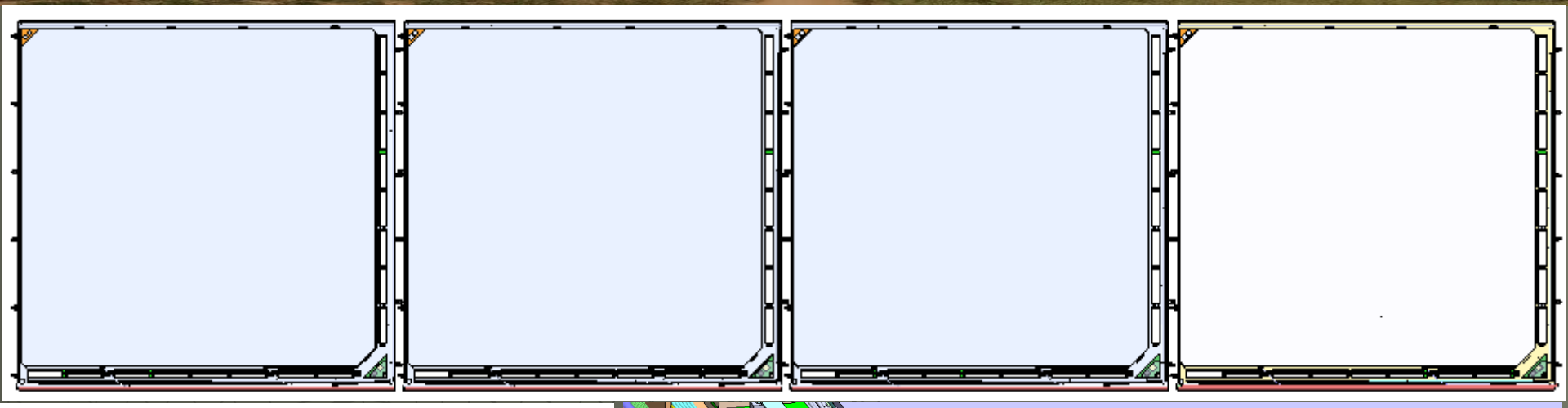


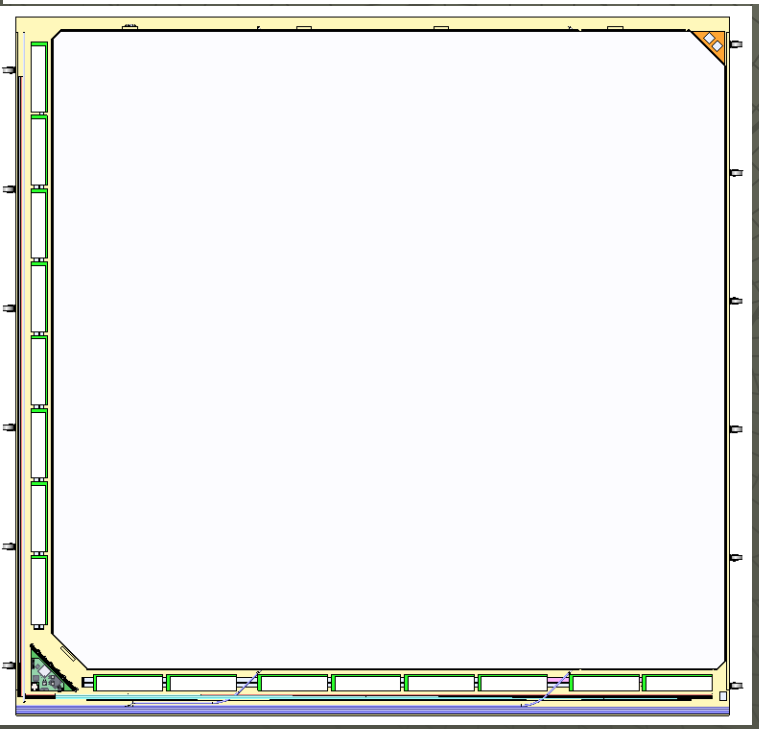


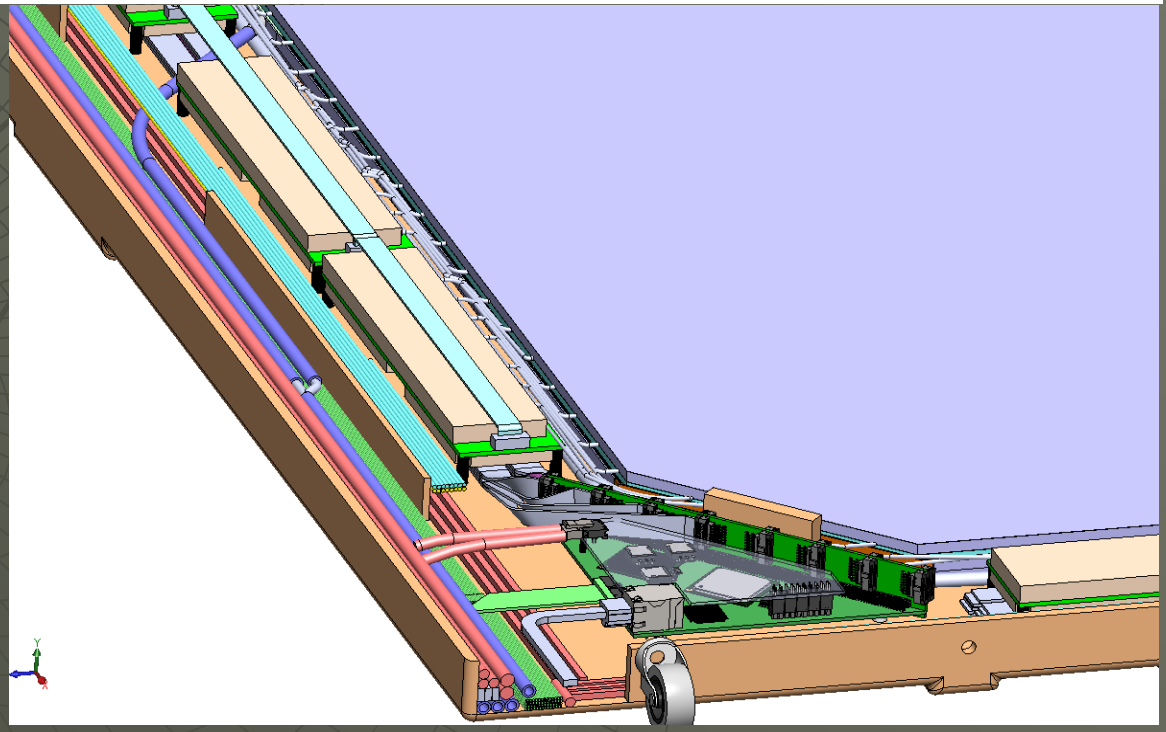
- Output voltage adjustable in the range ± 0-6KV (to generate 0-12KV) with output current up to 2µA.
- HV load regulation: better than 0.1% F.S
- Output ripple/noise voltage: within 200 mV (p-p).
- Adjustable HV Ramp rate 10-1000 Volts/ sec, HV on/off control, HV output read back facility.
- HV load current read back facility with a resolution of 5 nA.
- Required LV Input supply: 12V @200mA
- Ambient fringe magnetic field: 500 gauss



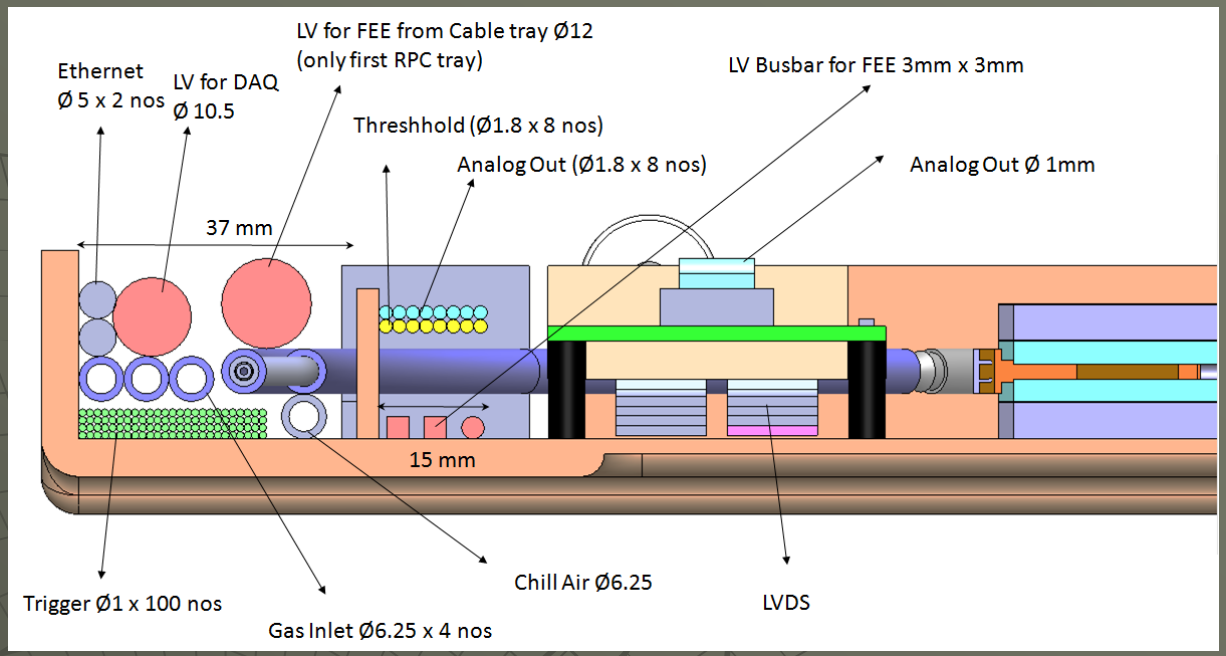
Integration of electronics in RPC

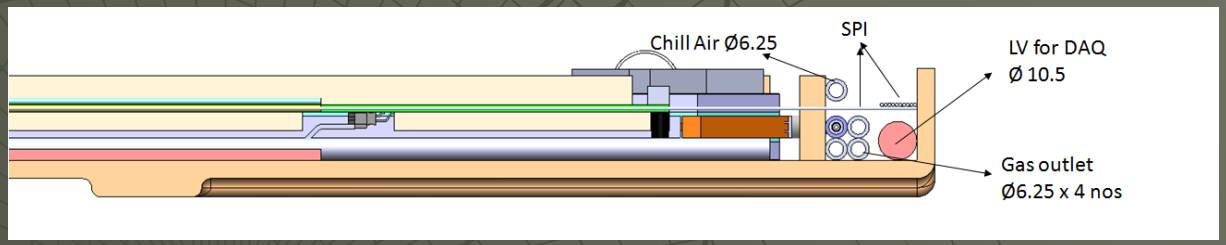


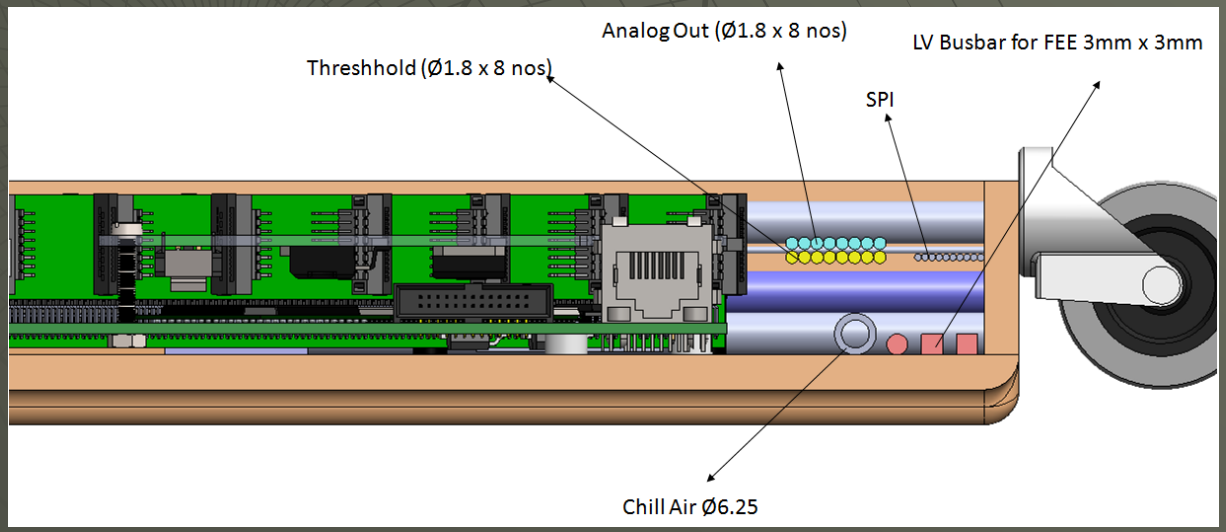




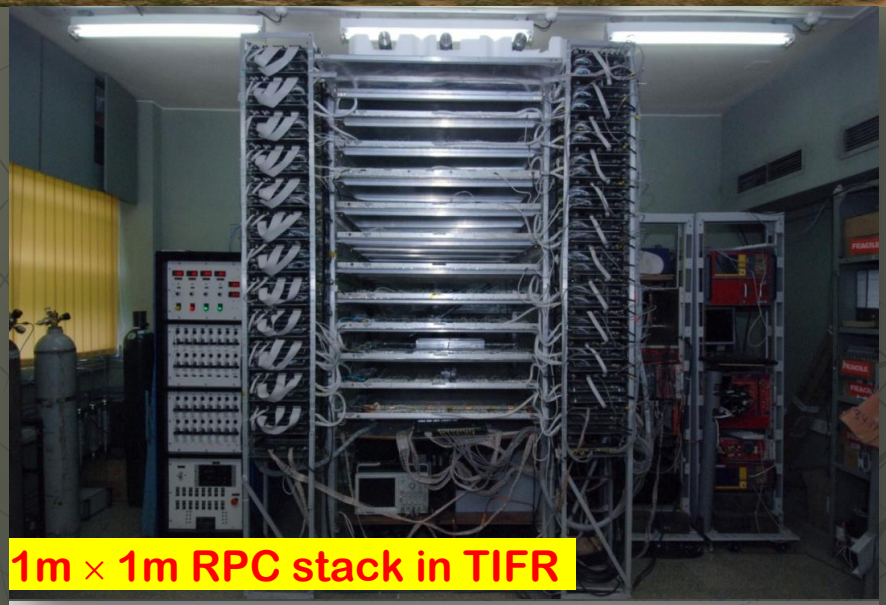
Side views of the RPC tray







ICAL Prototype detectors



1m × 1m RPC stack in TIFR

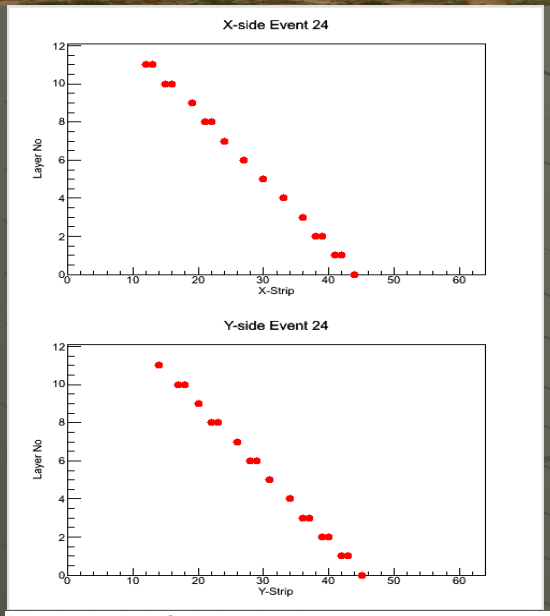
2m × 2m RPC test stand in TIFR

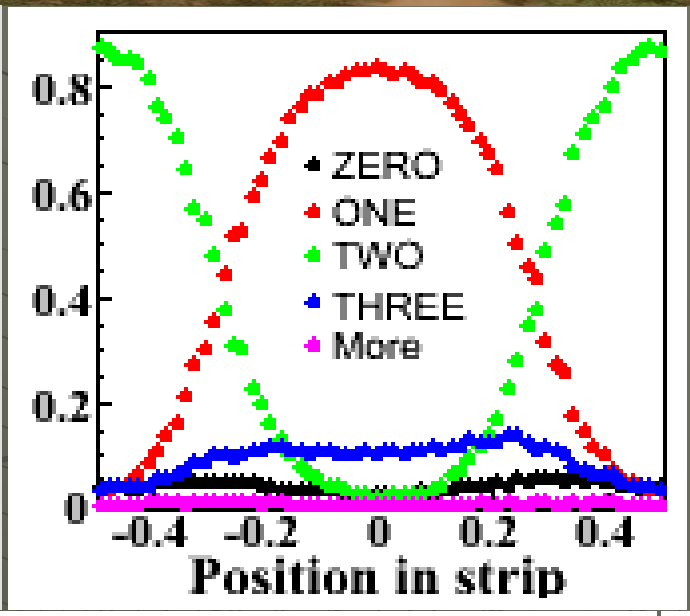
2m × 2m RPC stack in Madurai

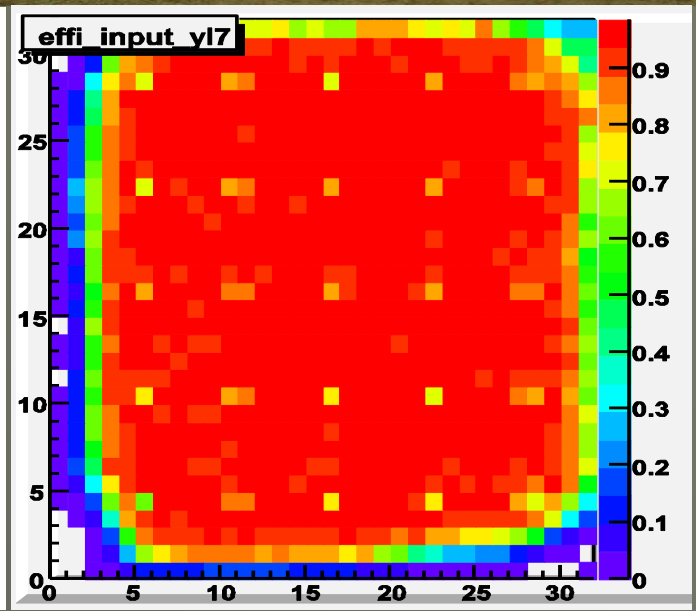
1m × 1m RPC stack in VECC

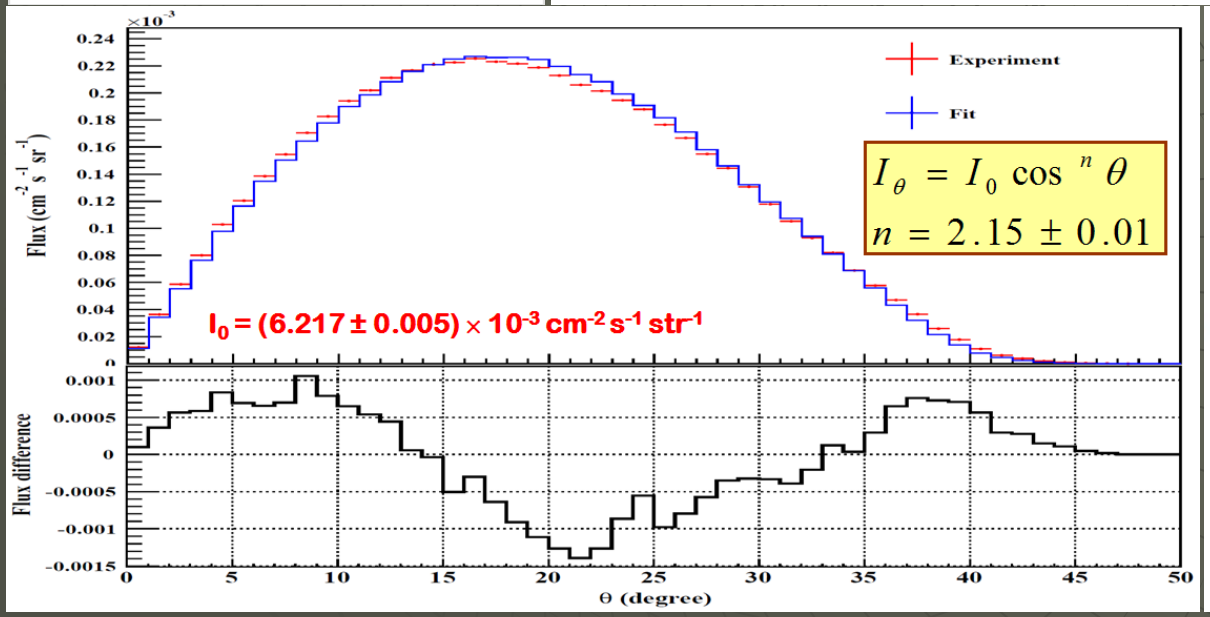
Operating 24×7 for many years

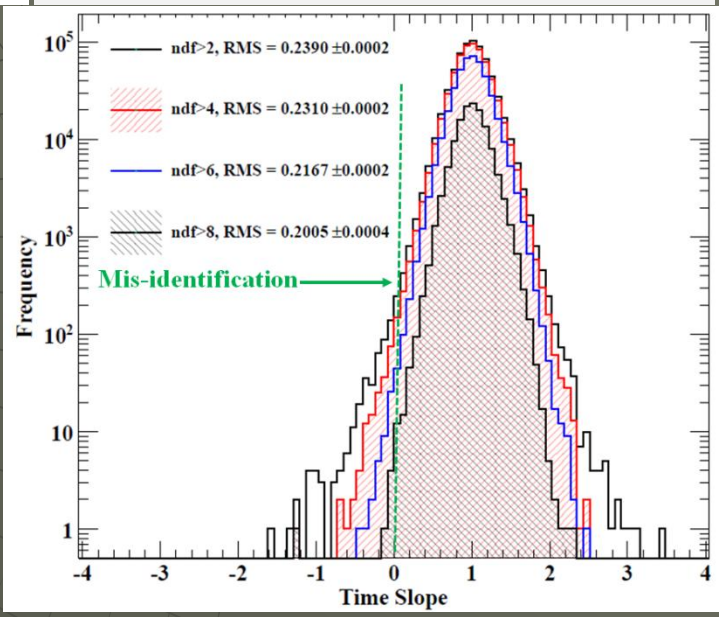
Some results from prototypes











Status and future outlook

- Design of baseline ICAL detector electronics completed, reviewed.
- Prototypes and limited quantities of various components and modules were produced, technologies and vendors identified.
- They are all tested, and are being used to read many ICAL prototype detectors, including the m-ICAL which is currently under construction.
- The project (ICAL) and the e-ICAL are delayed, hence large scale production of its electronics is put on hold.
- Meanwhile, revisions and upgrades – or even new architectures, of various components are being worked out.