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Electronics, trigger and data acquisition systems for the INO ICAL experiment

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India-based Neutrino Observatory (INO) has proposed construction of a 50kton magnetised Iron Calorimeter (ICAL) in an underground laboratory located in South India. Main aims of this, now funded project are to precisely study the atmospheric neutrino oscillation parameters and to determine the ordering of neutrino masses. The detector will deploy about 28,800 glass Resistive Plate Chambers (RPCs) of approximately 2m 2m in area.

About 3.6 million detector channels are required to be instrumented. The analog front-end comprises mainly of 4-channel preamplifier and 8-channel leading edge discriminator ASICs. The digital front-end is implemented using a high-end FPGA, a TDC ASIC and a network controller chip. The multi-level trigger system generates the global trigger signal based solely on event topology information. A dedicated sub-system handles distribution of global clock and trigger signals as well as measurement of time offsets due to disparate signal path lengths. The data, acquired on receipt of trigger signal by the digital front-end sub-system is dispatched to the backend data concentrator hosts via a multi-tier network. Finally, the event data is compiled by the event builder, which also performs various data quality monitors on the data besides archiving the same.

We will present the design of electronics, trigger and data acquisition systems of this ambitious and indigenous experiment as well as its current status of deployment.

Summary

Entire design and fabrication of ASICs, most of the circuit boards as well as firmware and software are now complete. Prototyping, benchmarking and limited production of various components are currently in progress.

The analog front-end (AFE) board mainly consisted of amplifiers and leading edge discriminators for eight RPC detector channels. Initially a couple of versions of 8-channel ASIC chips were designed using regulated cascode trans-impedance preamplifier stages. Subsequently we changed the design to two-chip solution - 4-channel voltage amplifier and 8-channel leading edge discriminators in QFN packages. The AFE boards designed using this chipset and produced in limited number were extensively tested on the actual detector stacks and are ready to be mass produced.

The digital front-end (DFE) board mainly consisted a high-end FPGA, a TDC ASIC, a network controller ASIC and processes 128 signals from the AFE. It interfaces with the back-end DAQ on Ethernet to receive commands and to transfer event and monitor data. Two iterations of 125ps TDC ASICs were designed by the collaboration and the design of the final version is submitted for production. A couple of DFE boards were produced and extensively tested on the RPC detector stacks. Final production required for the 320-RPC engineering module will be placed soon. Entire firmware for the FPGA as well as front-end software of the soft-core processor are complete. An alternate design of DFE with fibre data interface is also being looked at.

Trigger system is being implemented by a multi-board, crate mounted hardware interfaced to the DFE boards mounted on the detectors. The trigger system mainly consists of signal router boards (SRBs), segment trigger logic boards (STLBs), global trigger logic boards (GTLBs) and control and monitoring (CAM) units. All the boards are designed and limited production of most of them is now complete.

Calibration and auxiliary services sub-system mainly interfaces with trigger system and DFE boards and performs functions of distribution of clock and trigger signals as well as calibration of signal path delays. Design of this board as well as benchmarking of its elements is complete.

The multi-tier data network architecture along with various network elements is finalised. The back-end DAQ hardware involving multiple data concentrator servers is designed. Tests are being performed on its functional capabilities using data records in their the finalised packet format from the front-end. Various elements of event builder, data quality monitors, user consoles and other back-end software elements are already planned and most of them are even coded.

Integration of electronics, especially the analog and digital front-end onboard the RPC detector module posed a big challenge. This along with extensive cable routing spreading over the large detector of 48m x 16m x 16m in volume is being carefully addressed.

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