Upgrade of the ATLAS Thin Gap Chambers Electronics for HL-LHC

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on behalf of the ATLAS Muon Collaboration

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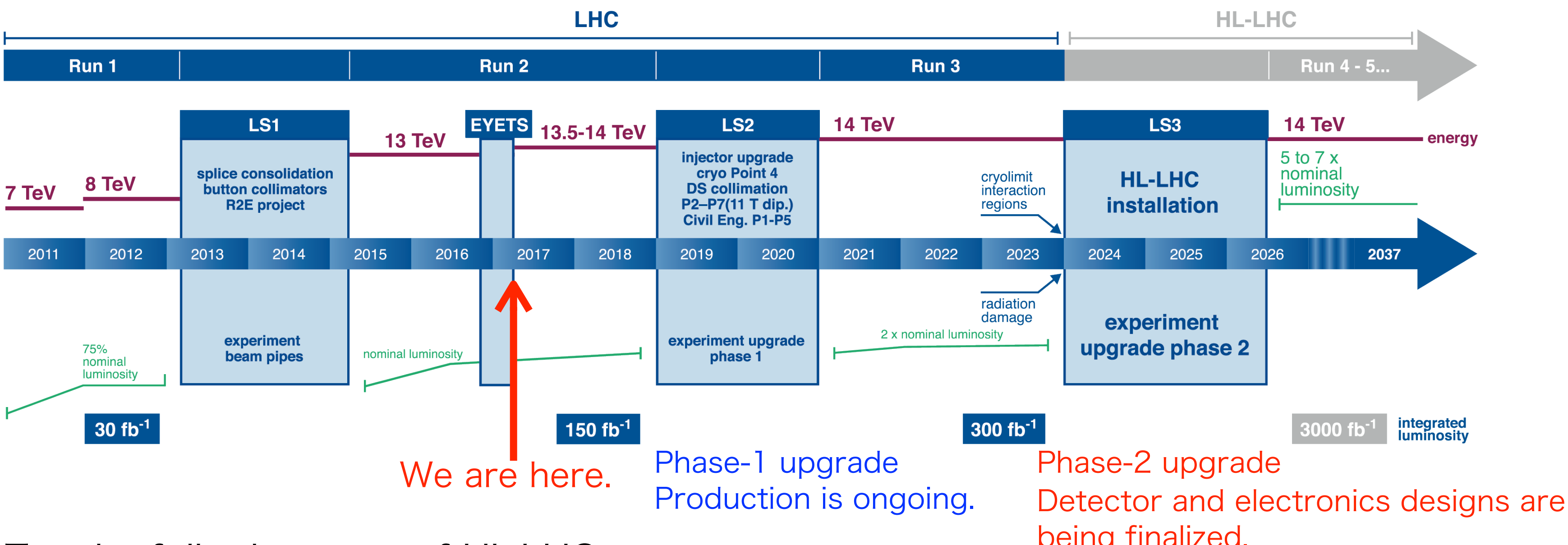
High-Luminosity LHC (HL-LHC)

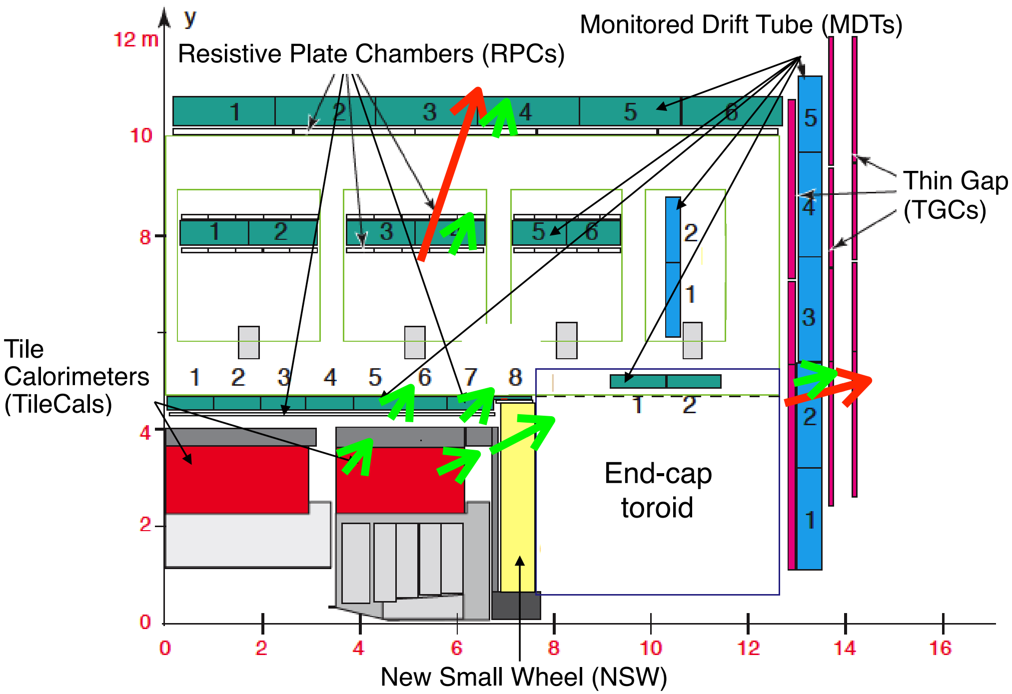
- HL-LHC experiment will start in 2026 to explore new physics by
  - the extension of the reach for new particles and
  - more precise measurements of Higgs couplings.

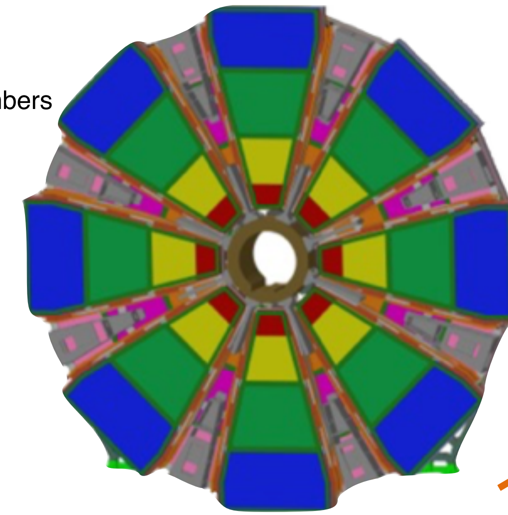


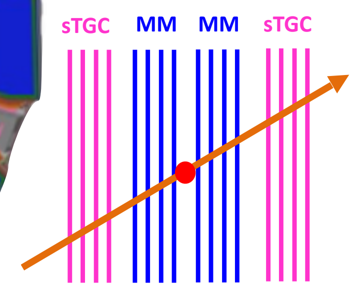
- To take full advantage of HL-LHC,
  - current trigger and readout electronics need to be replaced by new ones, and
  - sophisticated trigger algorithm will be introduced.

	Luminosity	First level trigger rate
ATLAS Run2	1.4×10^{34} cm^{-2}s^{-1}	100 kHz
ATLAS HL-LHC	7×10^{34} cm^{-2}s^{-1}	1 MHz

First Level Muon Trigger for HL-LHC ATLAS







NSW consists of MicroMegas (MM) and small-strip TGC (sTGC).

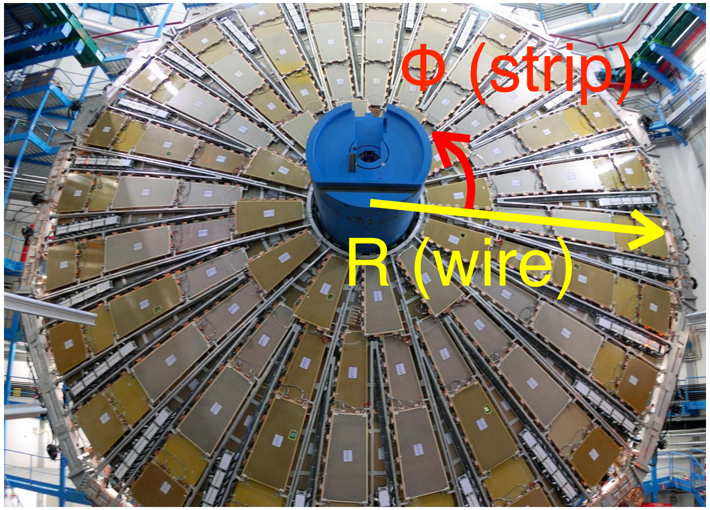
The ATLAS Collaboration, "ATLAS Phase-II Upgrade Scoping Document", CERN-LHCC-2015-020

- Multiple detectors will be used for muon reconstruction.
  - Barrel: RPC, MDT, TileCal (Additional RPCs will be installed in the inner layer.)
  - End-cap: TGC, RPC, MDT, TileCal, NSW (introduced at the Phase-1 upgrade)
- TGC and RPC trigger algorithms will be renewed to improve the momentum resolution.

End-cap First Level Muon Trigger Upgrade

Thin Gap Chamber (TGC)

- Multi-wire proportional chamber (MWPC) operated in a saturated mode
- Two-dimensional position measurements

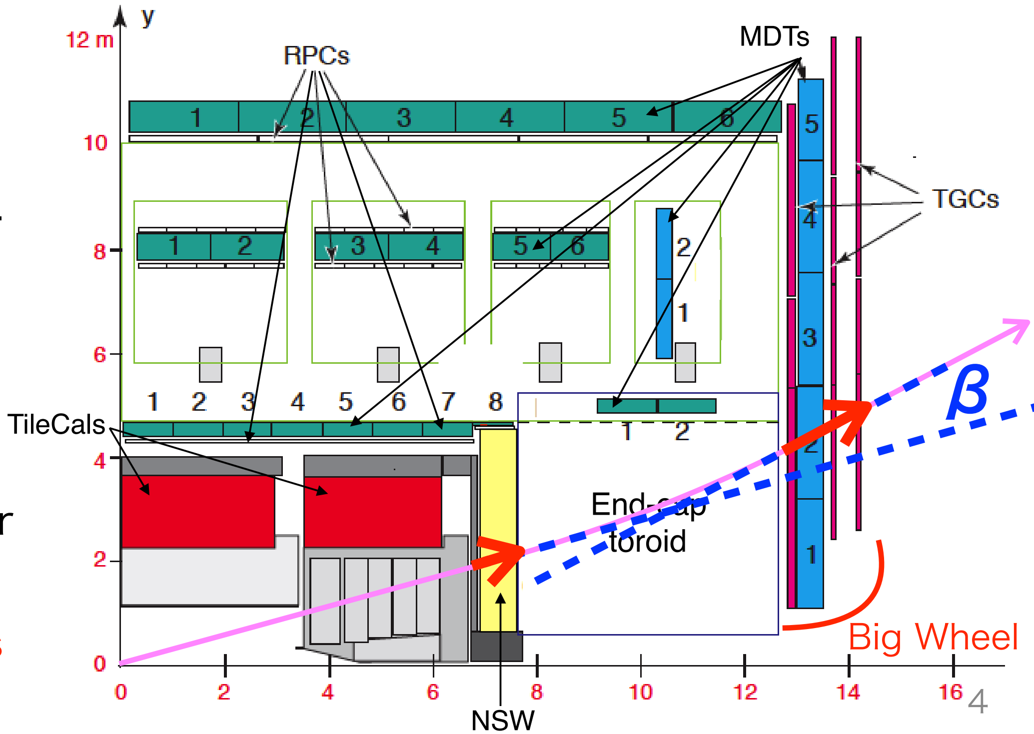


Current trigger system

- Take coincidence of the TGC hits among layers.

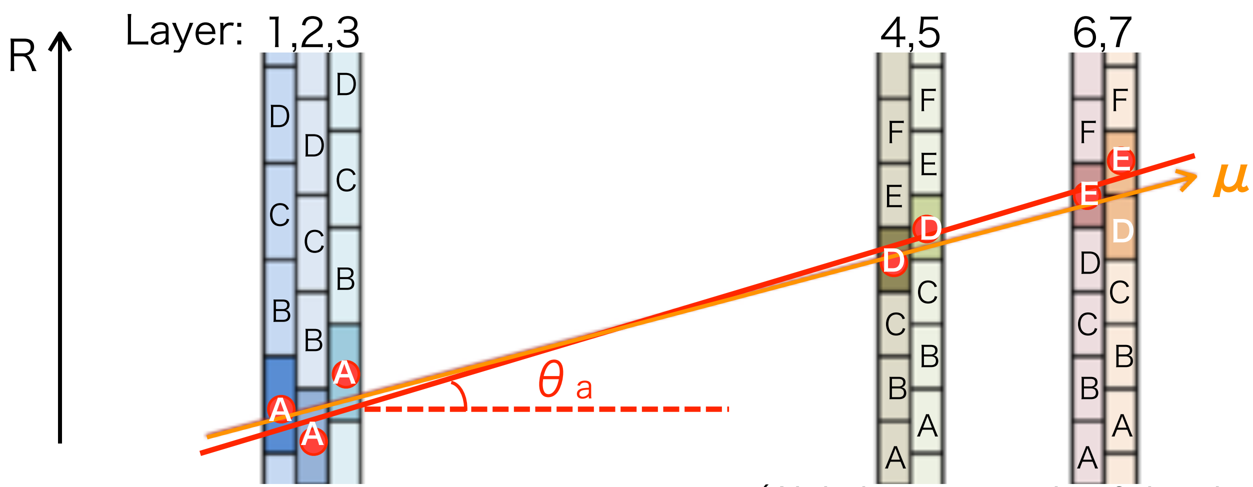
Trigger system for HL-LHC

- In addition to NSW, TGC provides the segments using track trigger algorithm.
- Make decision with the deflection angle β between the track segments before and after the magnetic field.
- Thanks to an improved p_T resolution for muons with β, the new trigger suppresses the events including muons with low p_T.



TGC Segment Reconstruction at HL-LHC

- In Run 2, the coincidence is taken but a segment is not reconstructed.
- Segment reconstruction with pattern matching is considered for HL-LHC.



(Alphabets: example of the channel number)

List ID: a	A	A	A	D	D	E	E	R_a	Φ_a	θ_a	$Quality_a$
List ID: b	A	A	A	D	D	E	D	R_b	Φ_b	θ_b	$Quality_b$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮

Channel identifiers of each layer — Position and segment angle, and quality

- Number of pattern lists in all region of TGC is roughly 4,800,000 (4,500,000) for wires (strips).
- TGC track trigger makes the decision by matching at least 5 hit out of 7 TGC layers with pattern lists.

Performance Study

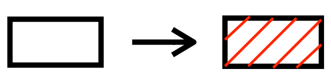
Performance is studied with the data sample collected in Run-1, $\sqrt{s}$ = 8 TeV, 25 ns bunch spacing.

TGC online track reconstruction

- TGC segment reconstruction is simulated with minimum χ^2 fit for the TGC hits (5 out of 7 layer coincidence is taken in advance) with a straight line.

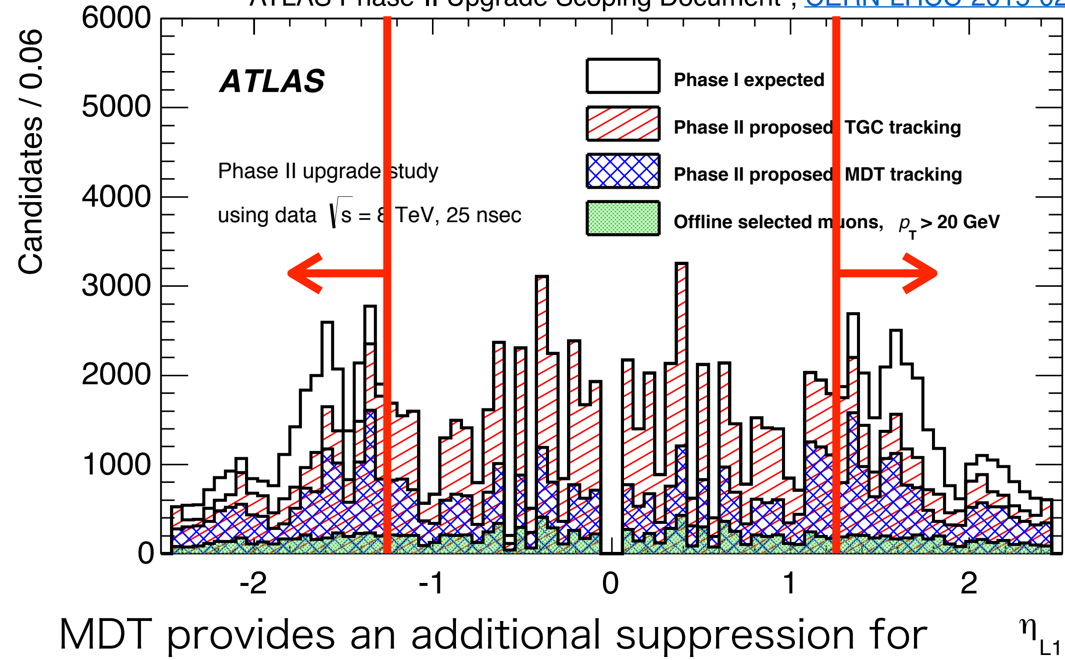
Requirement on the deflection angle

- The rate of a first-level single muon trigger with 20 GeV threshold is expected to be reduced by 25% with the polar angle difference between the TGC and NSW segments for the end-cap region (1.3 < $|\eta|$ < 2.4).



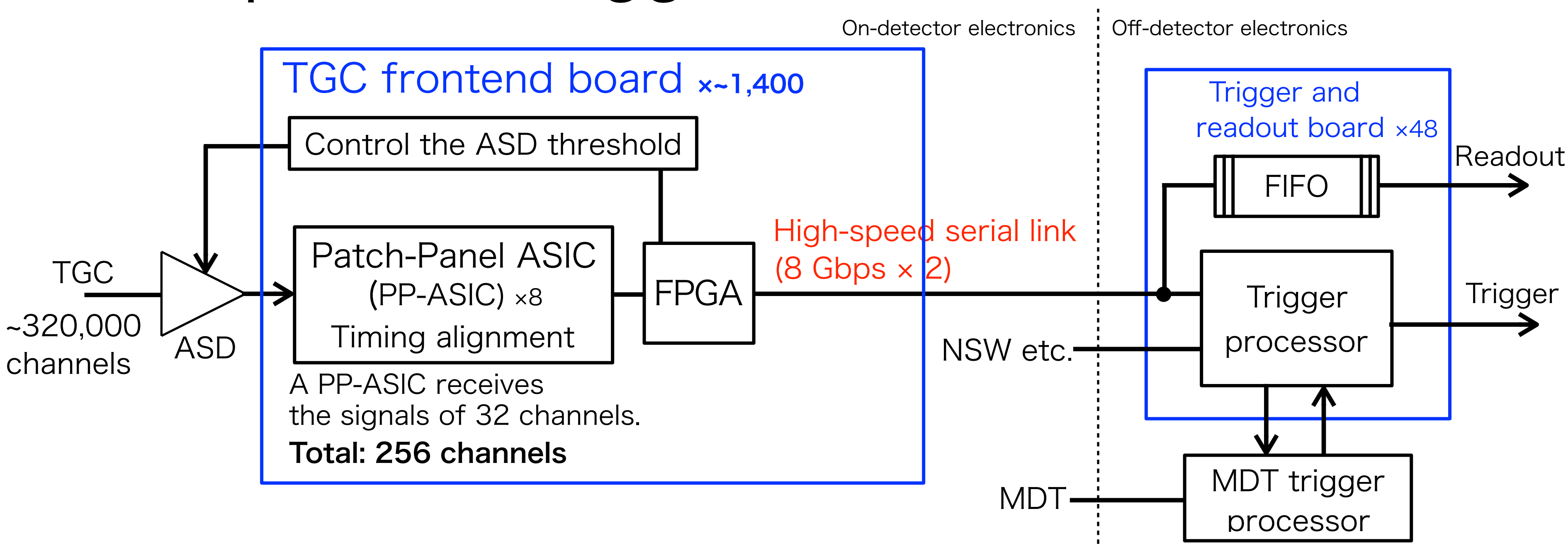
- Relative efficiency is 95% for 20 GeV threshold.

The ATLAS Collaboration, "ATLAS Phase-II Upgrade Scoping Document", CERN-LHCC-2015-020



MDT provides an additional suppression for low momentum muons.

End-cap Muon Trigger Electronics for Phase-2



- Signals digitized by amplifier/shaper/discriminator (ASD) boards are fed into the TGC frontend board.
- A TGC frontend board aligns the timing of the hits and transmits the data of 256 channels to the off-detector electronics at 16 Gbps (8 Gbps × 2) with fixed latency.
- Trigger and readout board reconstructs TGC segments using TGC track trigger algorithm and makes a preselection based on TGC and NSW segments.
- MDT trigger processor receives the information of preselection from the trigger and readout board and then makes a decision with an improved p_T resolution.
- Finally, trigger and readout board sends a trigger decision to central trigger processor.

Prototype of TGC Frontend Board

For the timing alignment

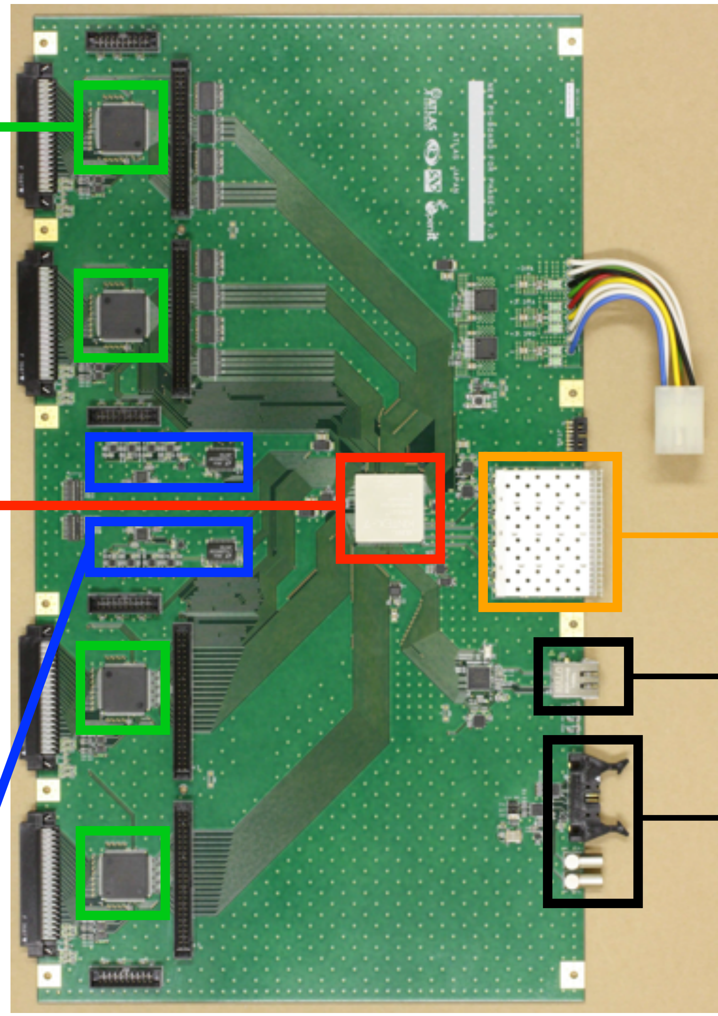
(old) PP-ASIC
4 on mother board
4 on daughter boards
32 × 8 = 256 channels

For hit data transfer and control

FPGA
Xilinx Kintex-7
XC7K325TFFG900-2
Data transmitter
PP ASIC control via JTAG
DAC control via I²C

For ASD threshold

DAC
DAC7578SPW
8 channels × 2
ADC
LTC1289CCSW



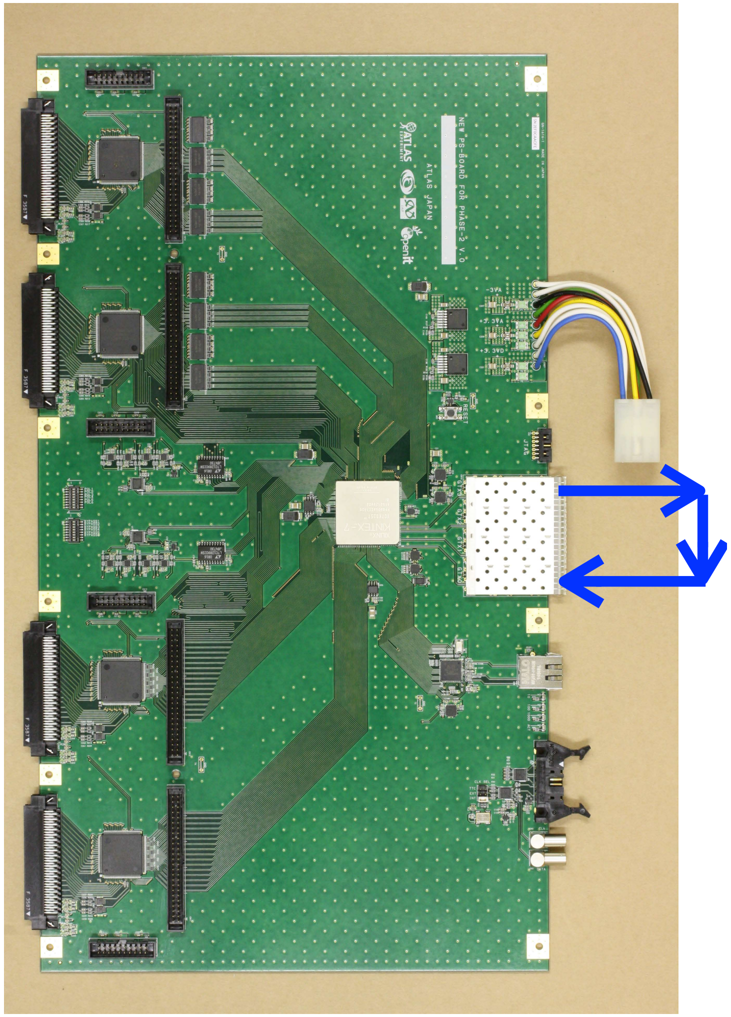
Optical receiver and transmitter
4 receiver and 4 transmitter
(up to 40 Gbps)

Ethernet interface
for debugging

Connecter for copper cable
LHC clock, reset, …

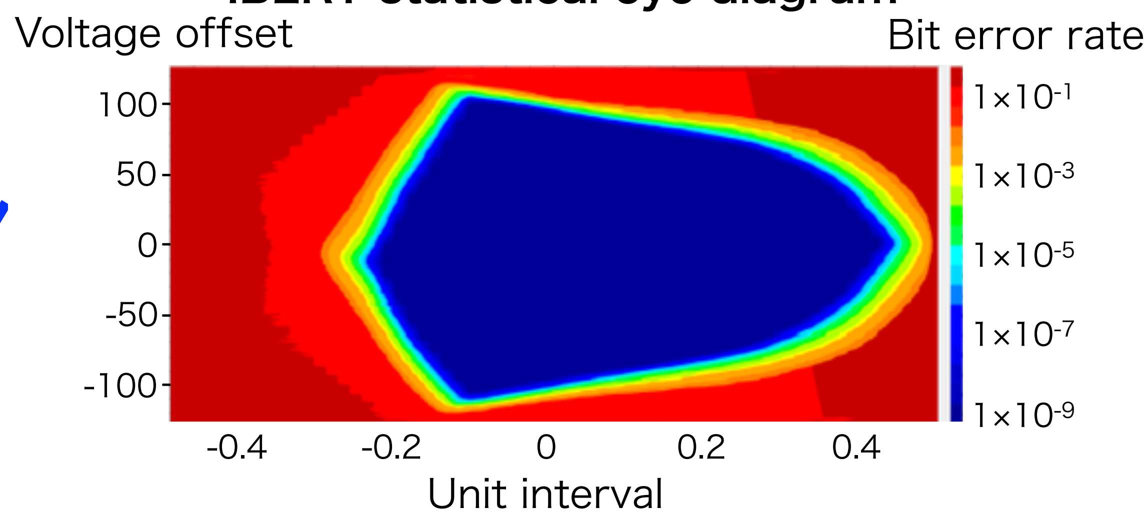
Prototype has all essential functions of TGC frontend board for phase-2!

Performance Test of the Data Transfer



- Measure the bit error rate with the loop back of Pseudo Random Bit Sequence (PRBS) using Xilinx's IBERT.
- Transfer rate: 8.0 Gbps for single lane

IBERT statistical eye diagram

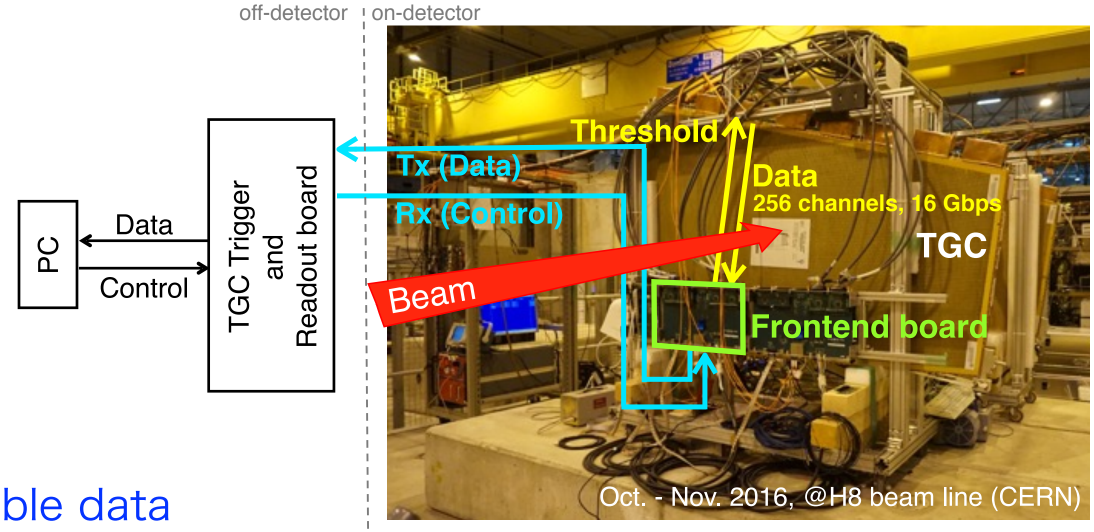


- Large open area is obtained.
- Measured bit error rate: < 1.3×10^{-16}
  (corresponding to < 1 errors for 5-day operation of single board)

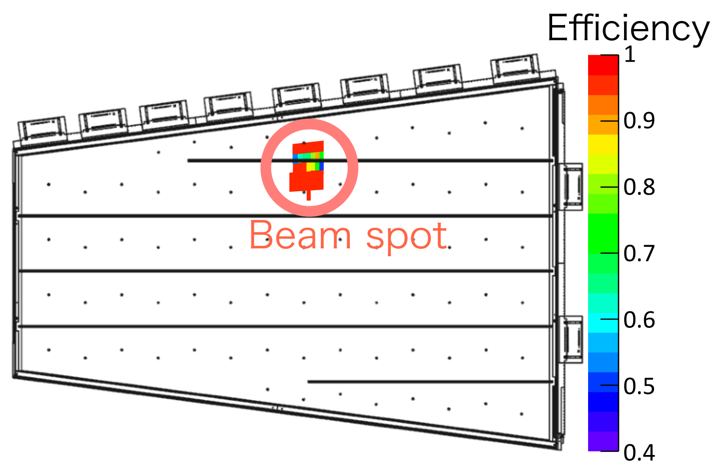
Beam Test

- The full TGC readout chain with the prototype of TGC frontend board has been demonstrated with charged particle beams at the H8 beam line in CERN.

- TGC trigger and readout board for phase-1 upgrade was used.
  (refer to “The Phase-1 Upgrade of the ATLAS Level-1 Endcap Muon Trigger” by Mr. Shunichi AKATSUKA (23 May))



- TGC frontend board provided stable data transfer with 2 × 8 Gbps in beam test period.
- The validity of the transferred data has been checked by evaluating the efficiency for each channel.
- ASD threshold controlling and monitoring based on FPGA have been demonstrated successfully.



Basic functionalities of the TGC front-end board are proven to work fine!

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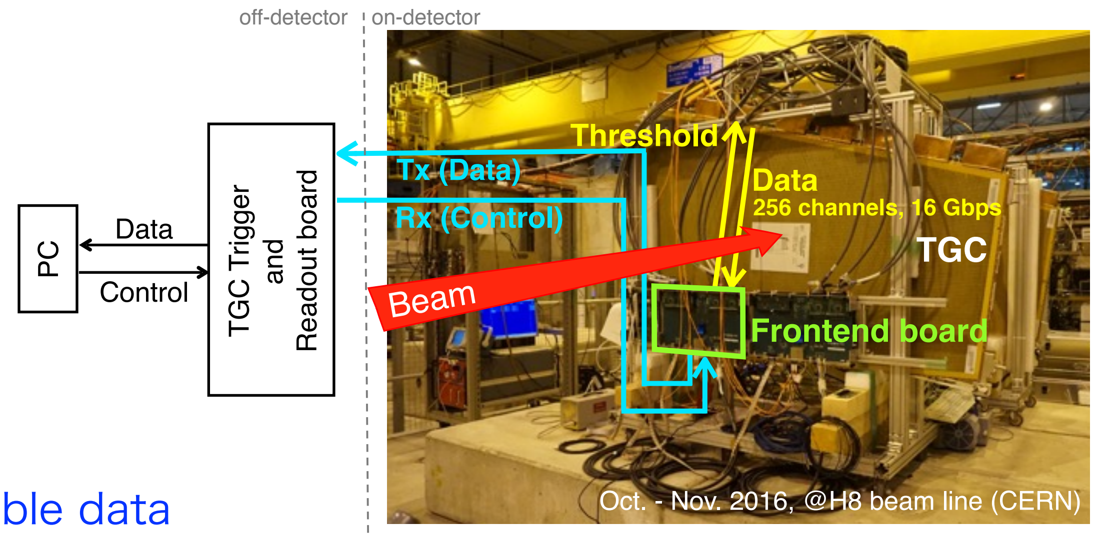

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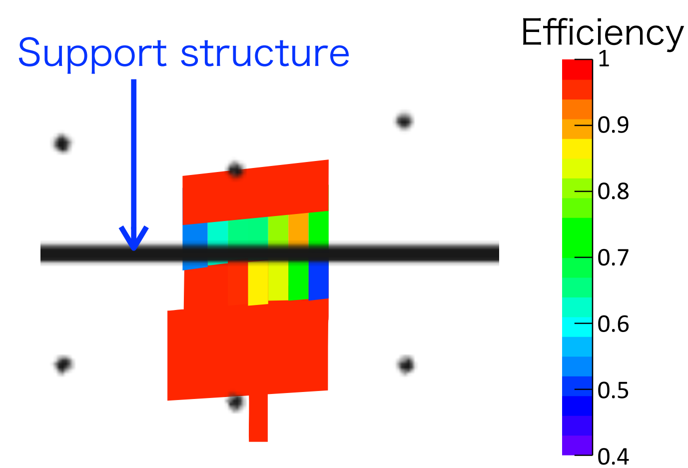

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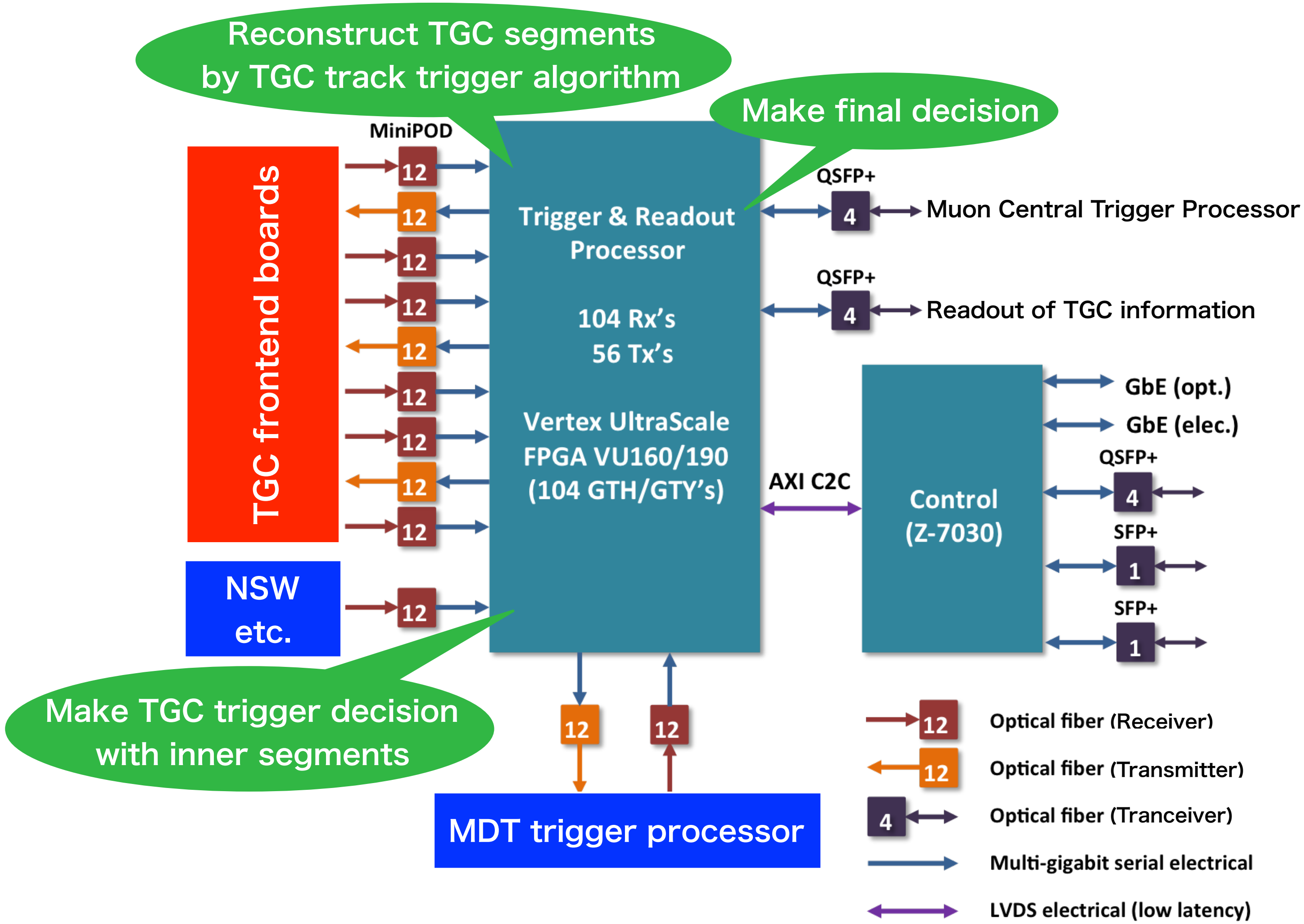
End-cap Muon Trigger Processor



- FPGA is required to have a large number of the high-speed transceivers and sufficient resources for trigger and readout algorithm.

The design of end-cap muon trigger and readout board in progress!

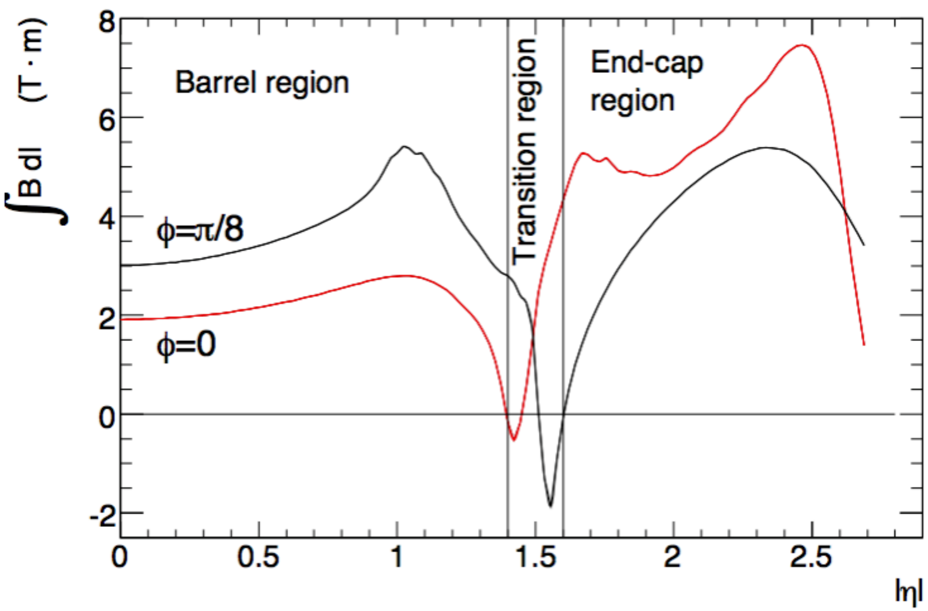
Conclusion

- In order to cope with a higher event rate in the HL-LHC operation, TGC trigger and readout electronics are planned to be upgraded.
- About 25% additional reduction of trigger rate is expected by an improved online momentum resolution with the new TGC track trigger logic in the end-cap region.
- A prototype of TGC frontend board has been developed with the concept of sending all hit data with 16 Gbps per board.
- The data transfer from TGC frontend board prototype has been successfully demonstrated with charged particle beam.
- Designing of the trigger and readout board is ongoing.
- Future tasks:
  - PP-ASICs need to be developed with a process of higher radiation tolerance,
  - Radiation tolerance of the devices (FPGA etc.) needs to be tested,
  - TGC track trigger algorithm needs to be tested with hardware, and
  - Trigger and readout board needs to be developed.

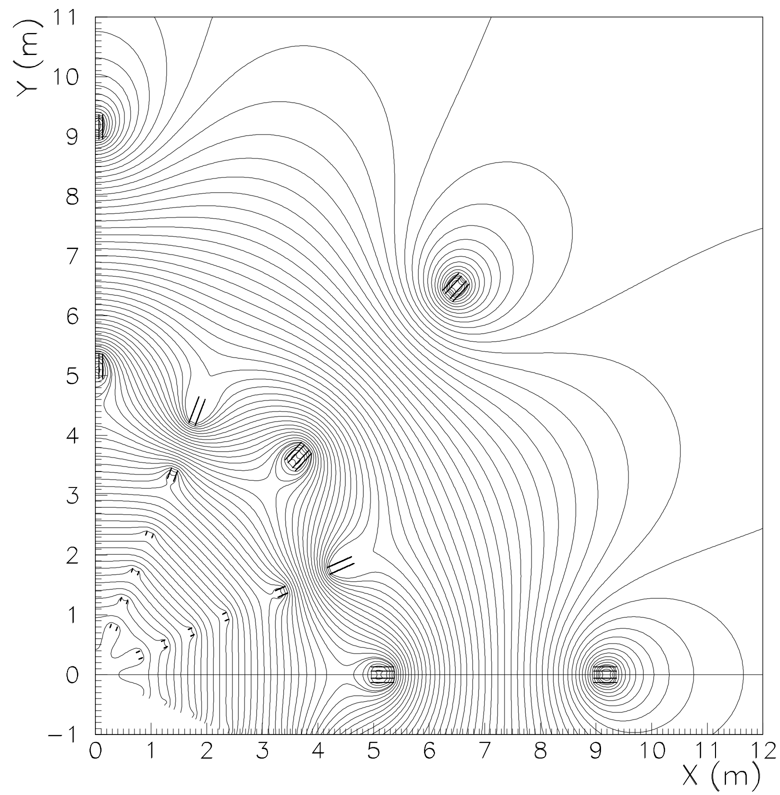
Backup

Magnetic Field

Distribution of toroidal magnetic field in beam axis direction



Distribution of toroidal magnetic field in the X-Y plane



- nonuniform magnetic field.
- arranged eight-fold symmetrical with respect to the Φ axis.

Radiation Levels

Radiation levels at LHC (@1x10^{34})

Location of TGC electronics

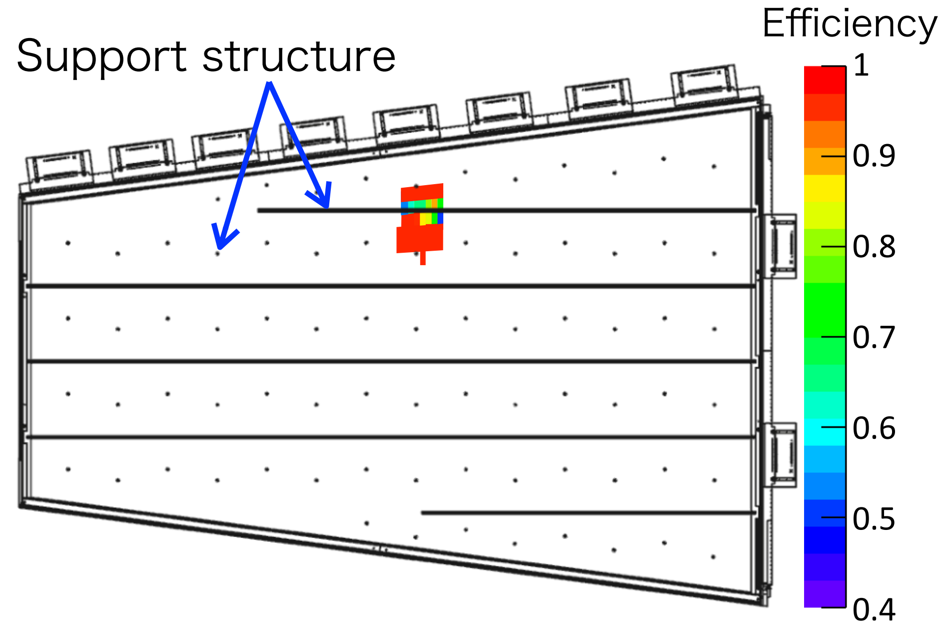
	Worst Location	Best Location
Neutrons, n/cm^2/yr	9.7×10^{10}	3.1×10^{10}
1 MeV equivalent neutron/cm^2/yr	2.0×10^{10}	3.6×10^{9}
Dose, Gy/yr	6.2×10^{-1}	2.1×10^{-1}

- Radiation levels are proportional to the luminosity, and a higher value is expected for HL-LHC.
- Position of the TGC front-end board is closer to the best location than the worst location.
- Electronic circuit of the TGC front end board should consist of devices with radiation resistant corresponding to this estimate.
- Soft error mitigation will be considered.

Efficiency of TGC hits

$$\text{Efficiency} = \frac{\text{number of events with a hit for interest and the other three layers}}{\text{number of events with a hit for each layer other than the layer of interest}}$$

- Most of the channels in the beam area has almost 100% efficiency.
- Efficiency is lower for some channels along the support structure of the wires inside the chamber.



The data transferred by the prototype of the TGC front-end board has been demonstrated!