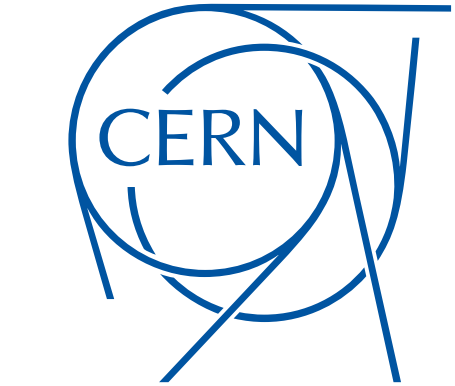


The ATLAS Level-1 Trigger System with 13TeV nominal LHC collisions

Louis Helary – CERN, on behalf of the ATLAS Collaboration

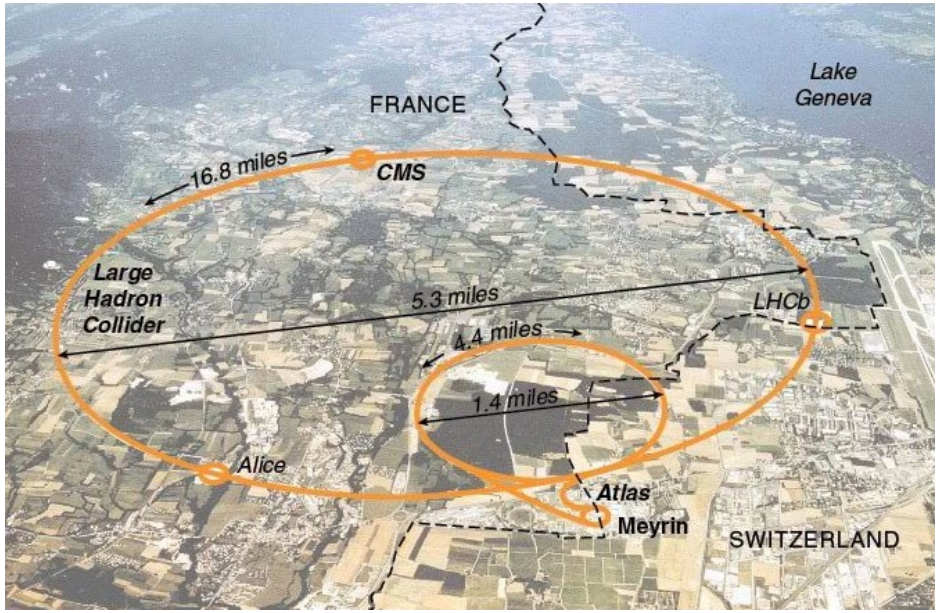
TIPP2017 – May 25th 2017

Introduction – LHC conditions

	energy [TeV]	bunch-spacing [ns]	$\mathcal{L}^{inst}$ [$cm^{-2}s^{-1}$]	average collisions / bunch-crossing
Run I (2012)	8	50	8×10^{33}	25-30
Run II	13	25	1.5×10^{34}	40-45

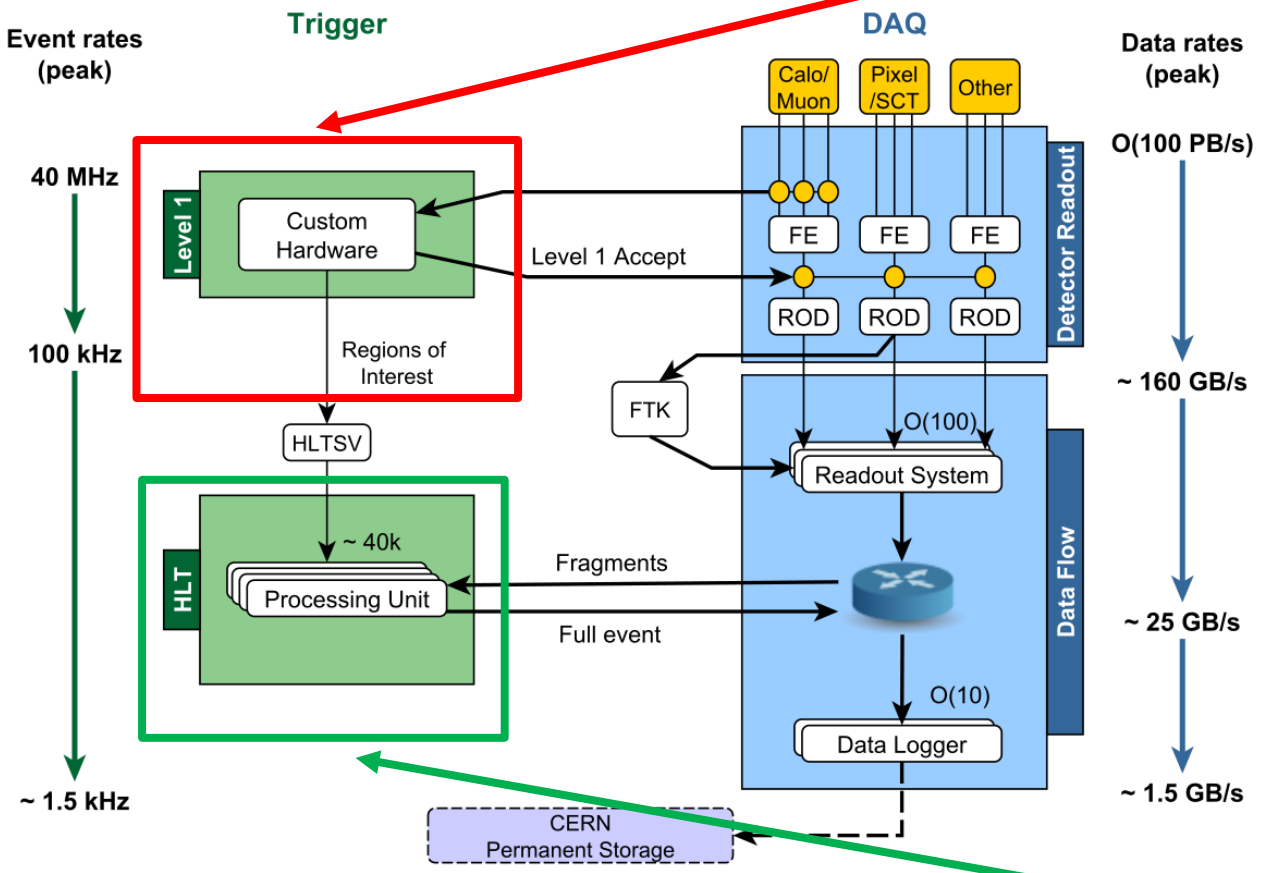
(or pileup)

- Large increase of interaction rate from Run1 to Run2 (~x5).
- Storage and CPU available increase by only a factor 2.
- Trigger strategy needs to be revisited to improve the event selection under in these conditions!



We will see how the L1 systems have been upgraded to cope with these conditions!

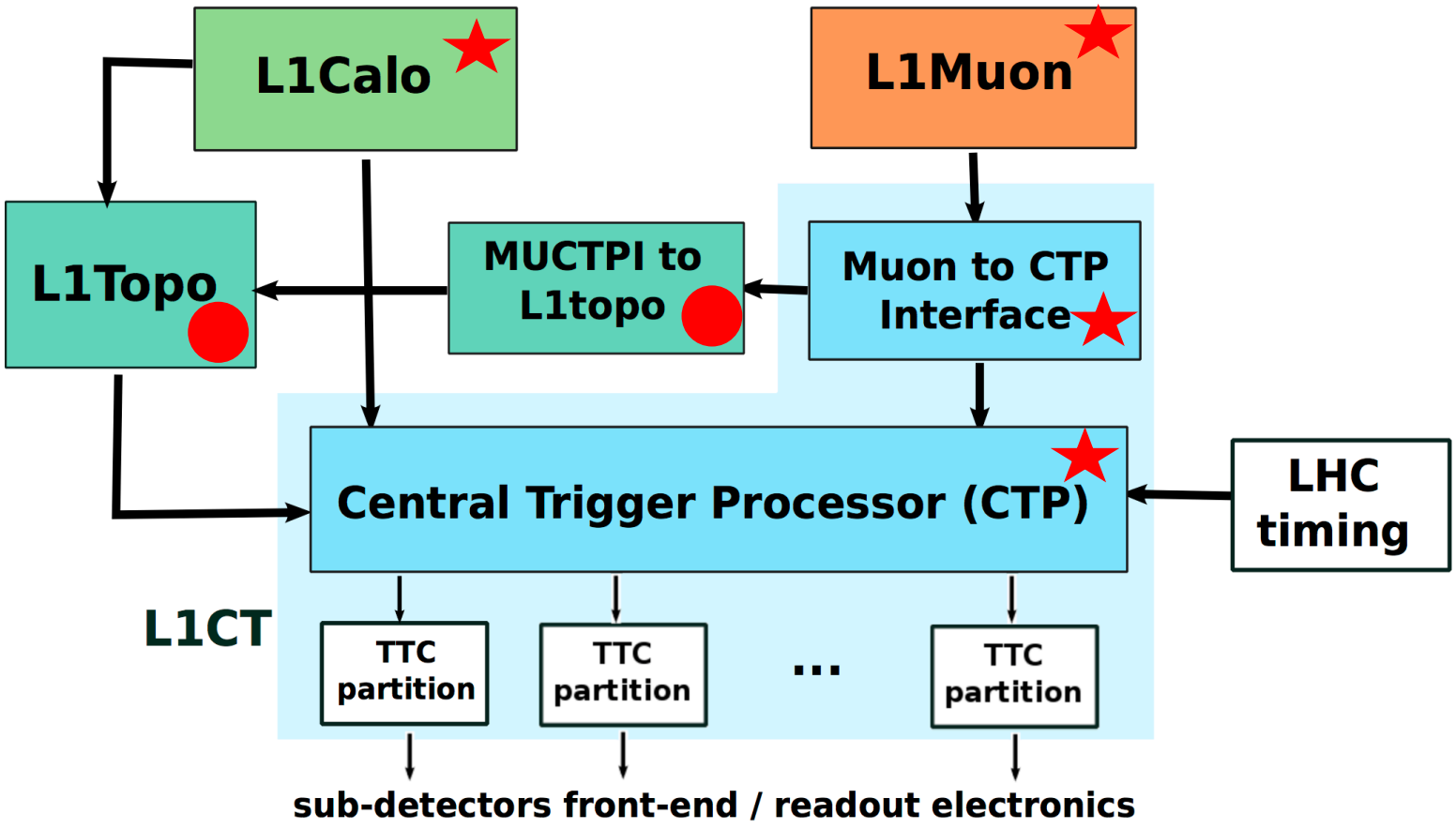
ATLAS trigger system



Level1:
- Logic done in dedicated hardware.
- Build regions of interest (RoI) based on coarse calorimeter and muon detector information.
- Topological selections between trigger objects.
- 40 MHz → 100 kHz
- Latency: 2.5 μs

HLT:
- Logic done in commercial computers.
- Fast algorithms running on RoIs or full events.
- Relies on object ID algorithms, calibration and detector granularity similar to those used offline.
- 100 kHz → 1 kHz
- Latency: 0.2 s

ATLAS L1 trigger systems

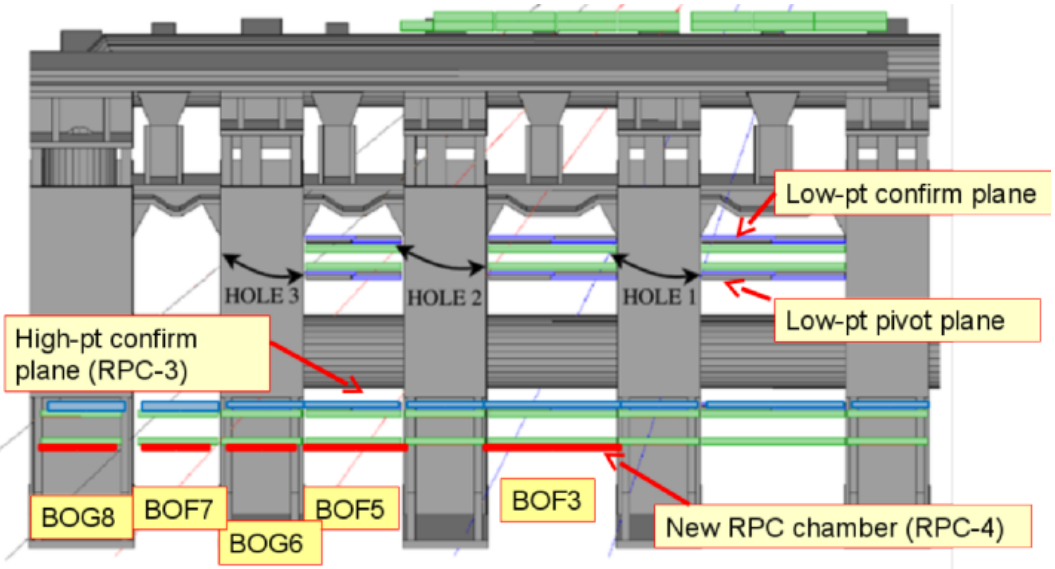


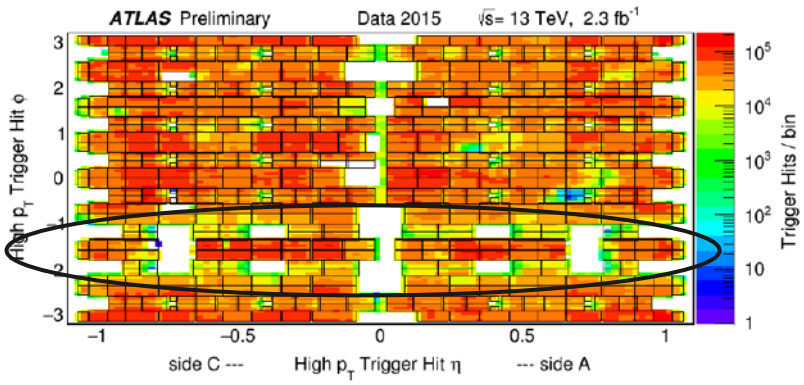
Upgrade compared to Run1:

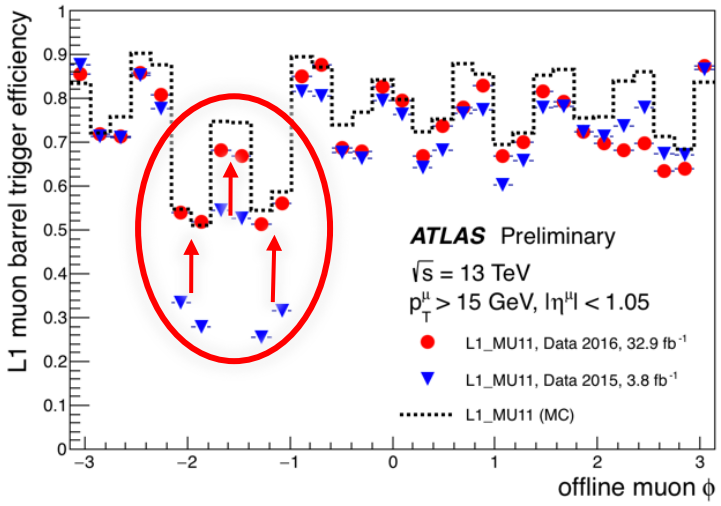
★ Upgraded hardware, firmware or software.

● New hardware.

L1Muon – barrel RPC upgrade

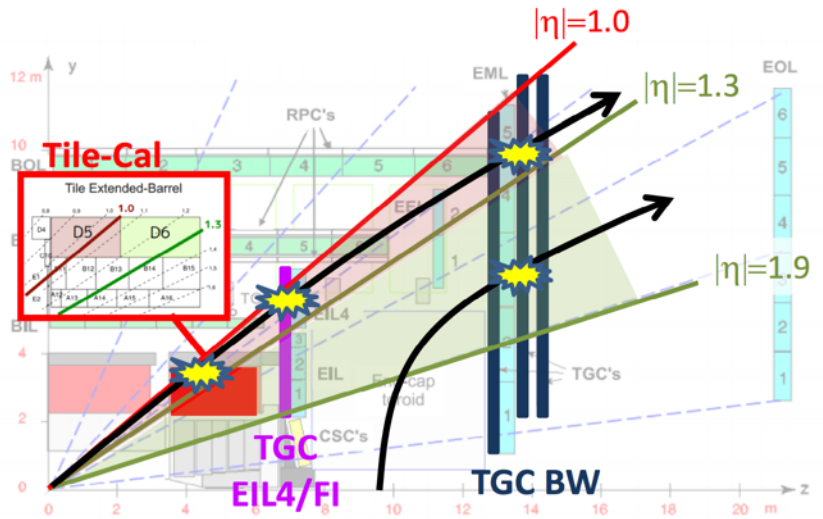


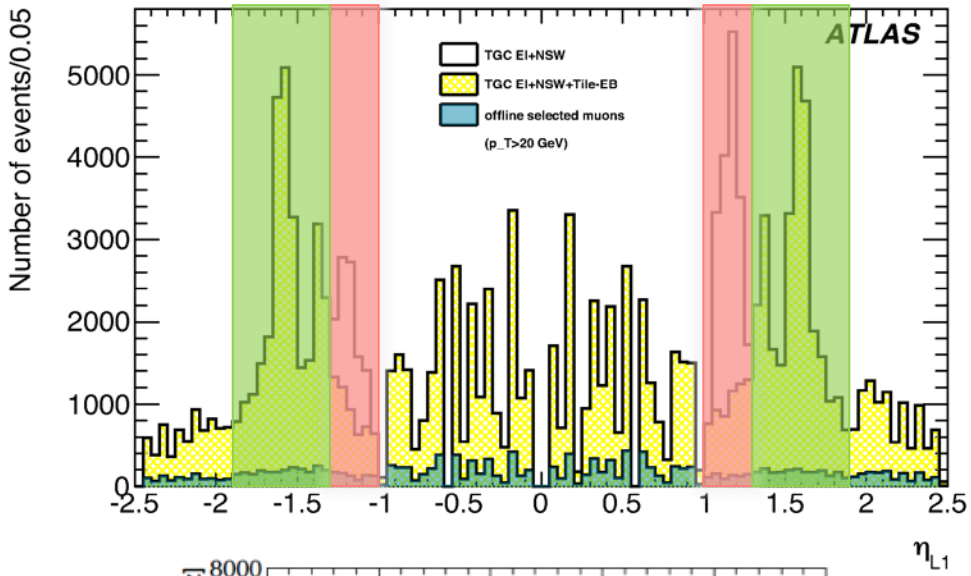




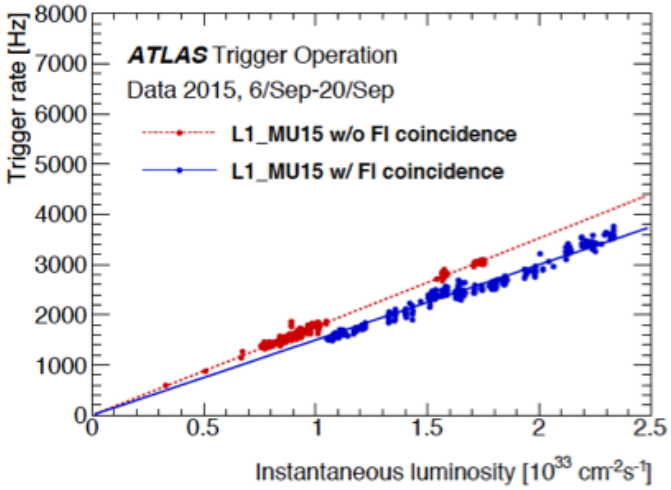
- Chambers installed during Long Shutdown1 (2013-2014).
- Cabling and commissioning during 2015.
- Active in data taking since 2016.
  →Increase acceptance by 3% in this region!

L1Muon – EndCap TGC upgrade

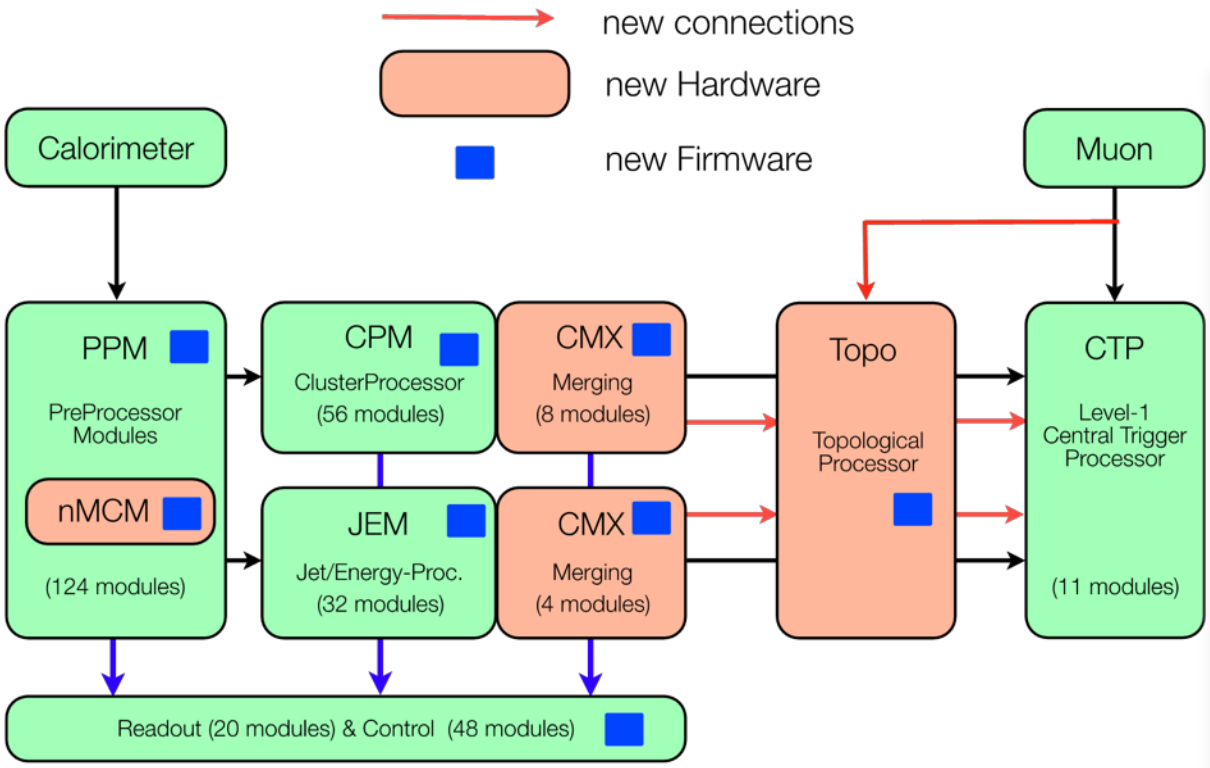




- Coincidence between Small Wheel and Big Wheel (1.3<|η|<1.9) is now working.
→Decrease rate of low p_T protons from beam by 15% for L1_MU15!
- Coincidence with Tile calorimeter (1.0<|η|<1.3) still under commissioning.
- Ask for 3 stations for low p_T item L1_MU4 instead of 2.



L1 Calo – Firmware and hardware upgrades



- nMCM: new Multi Chip Module.
- CPM: Cluster Processor Module.
- JEP: Jet Energy Processor.
- CMX: Common Merger Module EXtended.

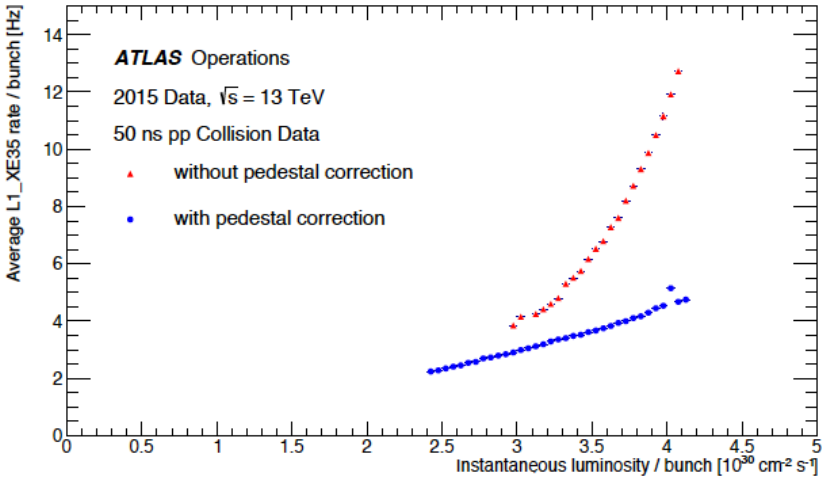
Improvements:

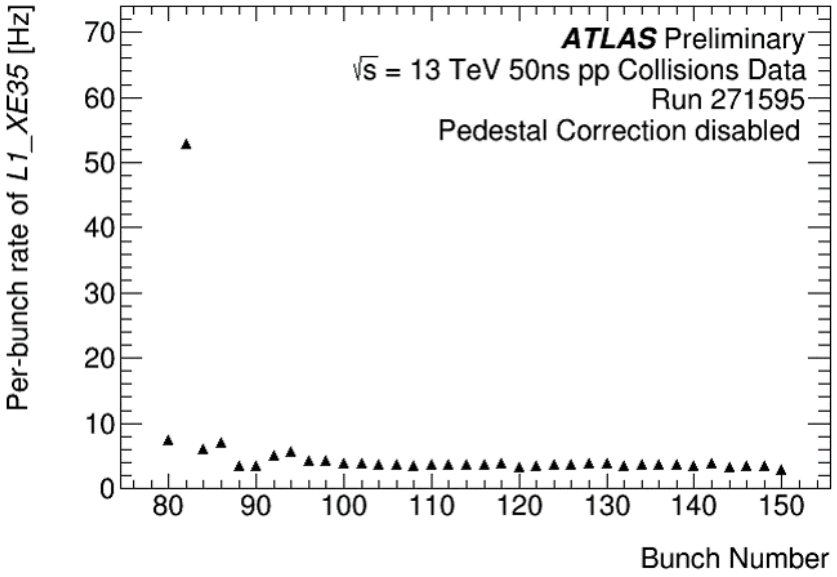
- Energy extraction performed in FPGA (was ASIC).
- Increase bandwidth (40→160 Mbit/s from JEM/CPM and between CMX modules).
- Provide position/energy of jets/electrons/taus for each trigger object.
- CMX sends objects to L1Topo and to CTP.

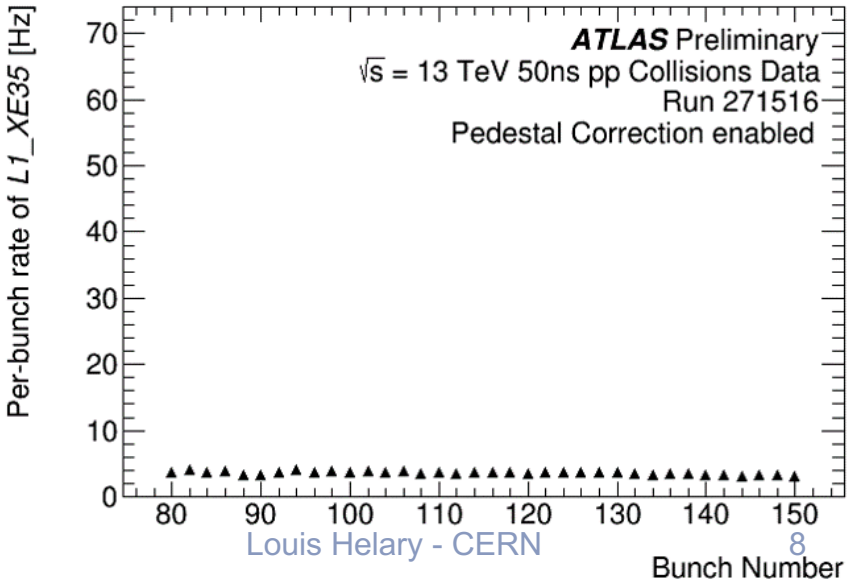
→Allow to run refined algorithms at L1

L1Calo – Pileup subtraction

- Observed significant rate effects of out-of-time pileup at high luminosity.
- Dominated by early bunch in train!
- Pileup suppression introduced at L1.
  →High rate reduction.







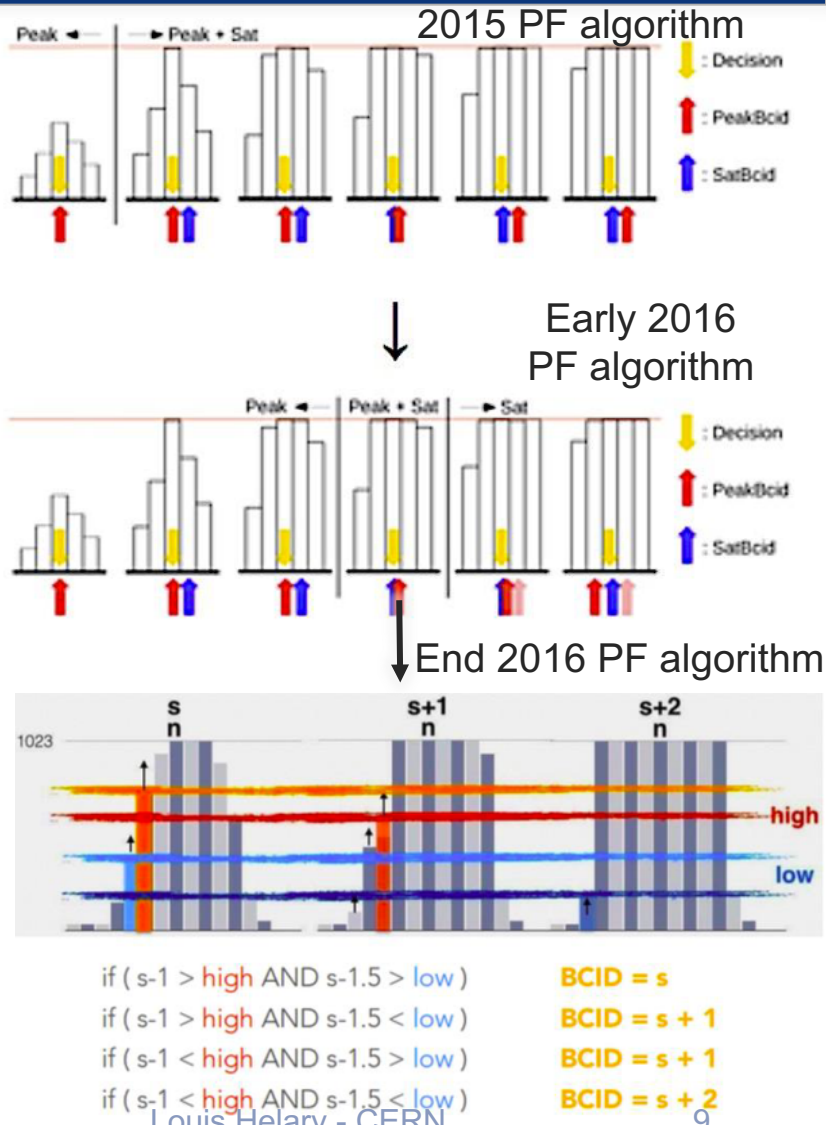
L1Calo – Improved Bunch Crossing ID (BCID) measurement

- Observed in 3.5 fb^{-1} of 2015 data (O(100)) mistimed events.
  - High p_T jet fired in too early BC.
  - Due to the interplay between PeakFinder, autocorrelation Finite Impulse Response (FIR) filters and saturated analogue signals.

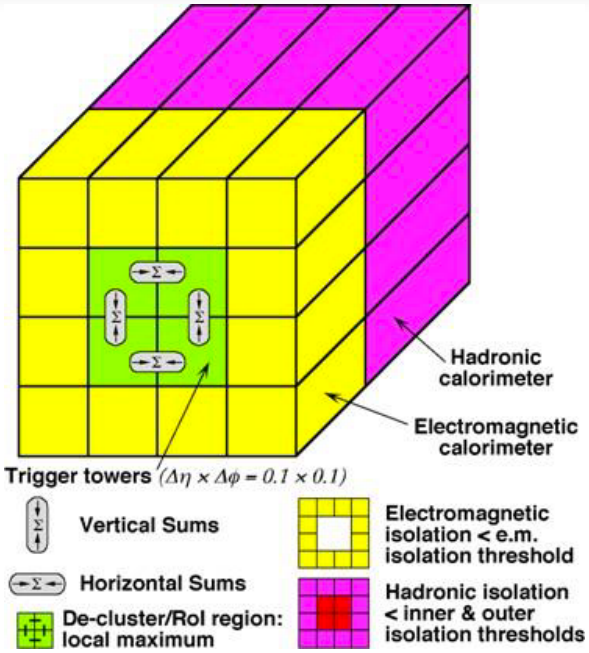
- Introduced a first solution early 2016:
  - Switched off PeakFinder after a certain number of saturated samples:
    PF3 (PF4) for 3 (4) samples.
  - Results in ~2 events per fb^{-1}.

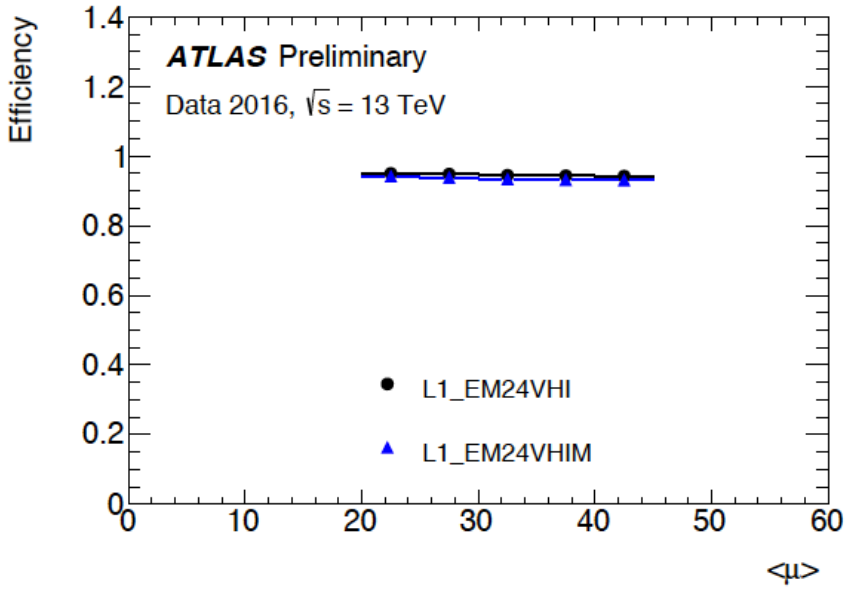
- New algorithm, taking advantage of the new 80 MHz digitization, was deployed at the end of 2016:
  - No mistimed events in 7fb^{-1} of 2016 data.

- Continue to extensively monitor this!



L1Calo – Improved EM isolation



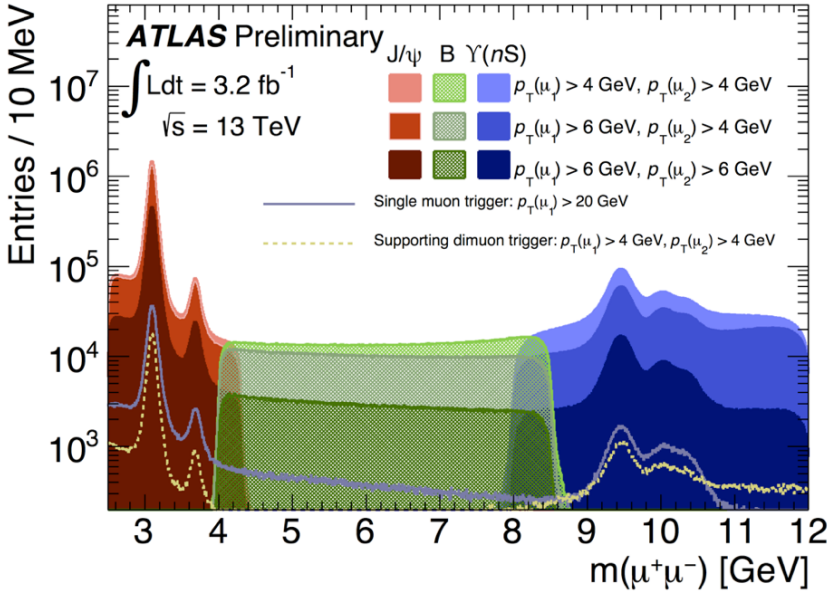


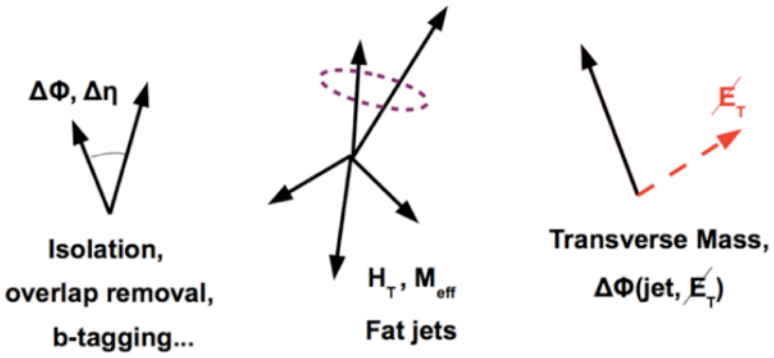
- EM isolation reoptimized using Z→ee events.
- Very useful to suppress QCD background.
- Allow to reduce the rate significantly with high signal efficiency.
  →therefore keep lower p_T items.
- Stable against pile-up increase.

Level-1 E_T	Efficiency loss	Rate reduction
22 GeV	1.3%	14.6%
24 GeV	1.0%	10.8%

L1Topo – motivation

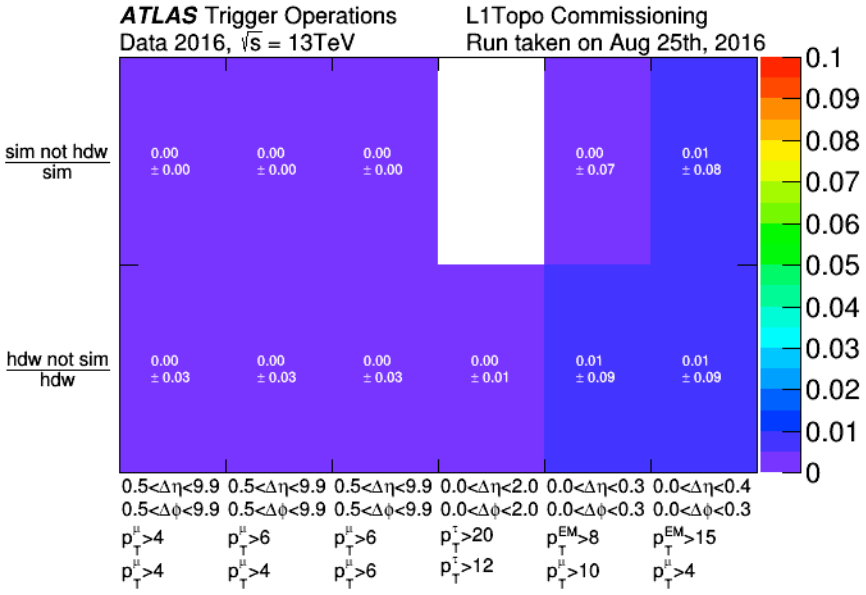
- In Run1, only possible to cut on the objects multiplicity and on their p_T.
  → Was already at the limit, impossible for certain signatures to cut harder on p_T!
- In Run2, introduce topological cuts, at L1 to select events and reduce the rate!
- Use dedicated FPGA-based modules to run algorithms in about 75 ns.
- Implement 107 new trigger Topo-items.

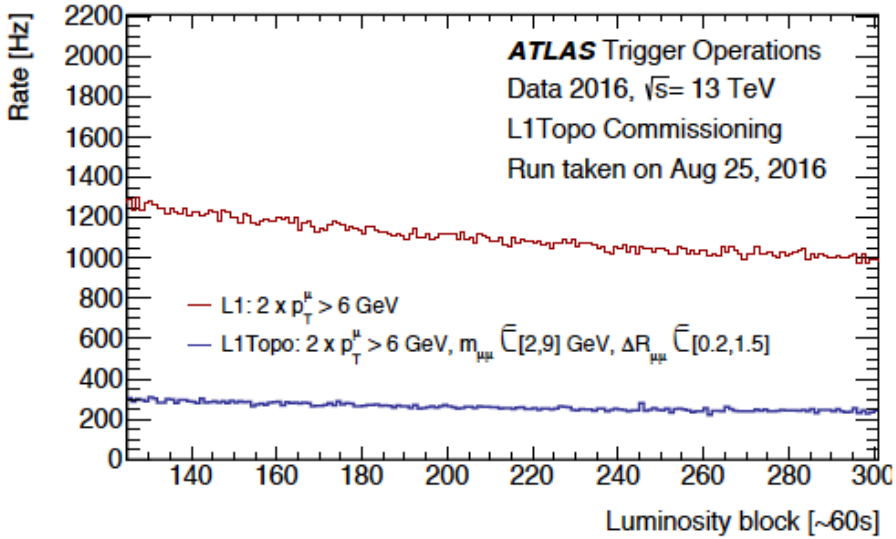




Purpose	Input objects	Algorithm
B-physics	muons	ΔR, Mass
H→ττ	tau_had, muons, electrons	Δη, Δφ, Mass
SUSY	Miss ET, jets	minΔφ, HT
W→eν	electrons, jets, Miss ET	Isolation, mT
Long lived Particles	late muons, Miss ET, jets	Muon in next bunch
etc		

L1Topo – validation and usage





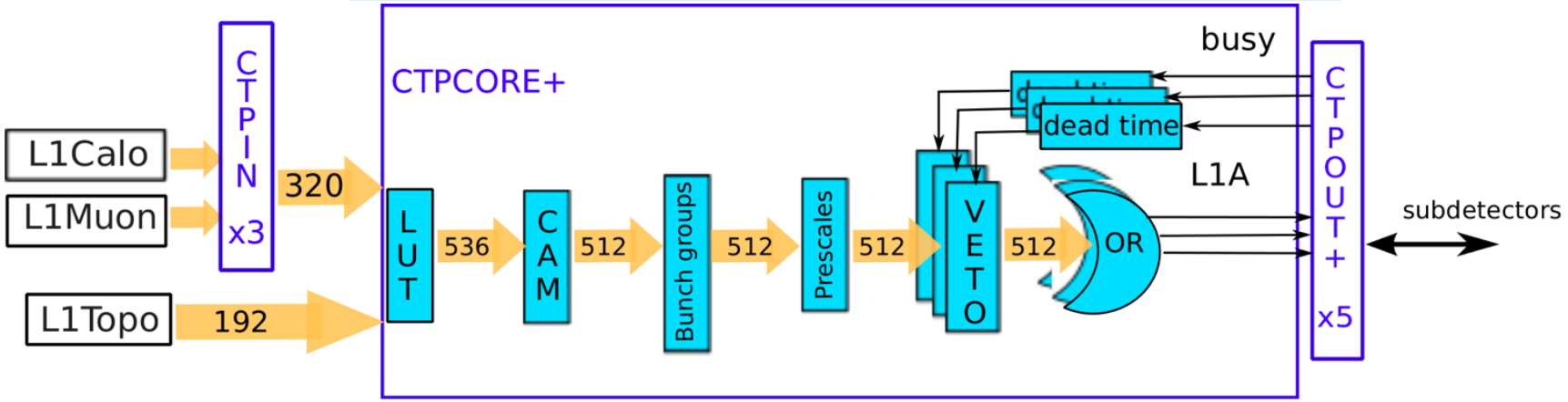
- Commissioning during 2015-2016 data-taking.
- Compare output of algorithm in simulation to actual trigger decision.

→Good agreement!

→Large rate reduction using topological selection, allow to keep low p_T items! Crucial for B-physics program (for instance, but not only)!

L1CTP – Introduction and motivation for upgrade

CTPCORE+:
- Form 512 triggers using LUT+CAM.
- Coincidence with LHC bunch pattern .
- Perform random prescaling.
- Generate dead-time, and monitor whole chain.

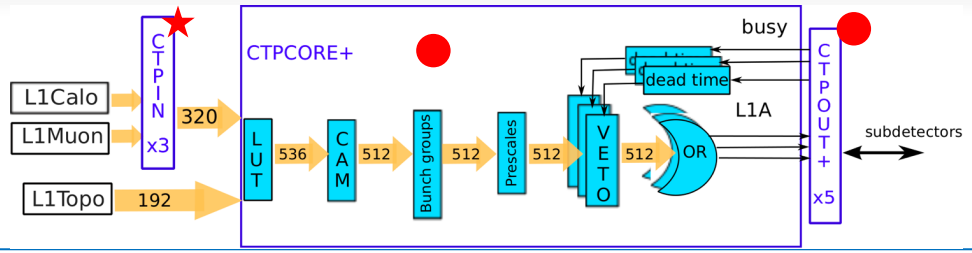


CTPIN:
Select and route trigger inputs from L1Calo and L1Muons.

CTPOUT:
Distribute trigger and timing to detectors, and receive BUSY signal.

Motivation for upgrade:
- CTP used to the limits of its capacity during the Run1.
- More inputs and trigger items needed to handle new L1Topo.

L1CTP – CTP upgrades



Upgrade compared to Run1:

★ Upgraded firmware .

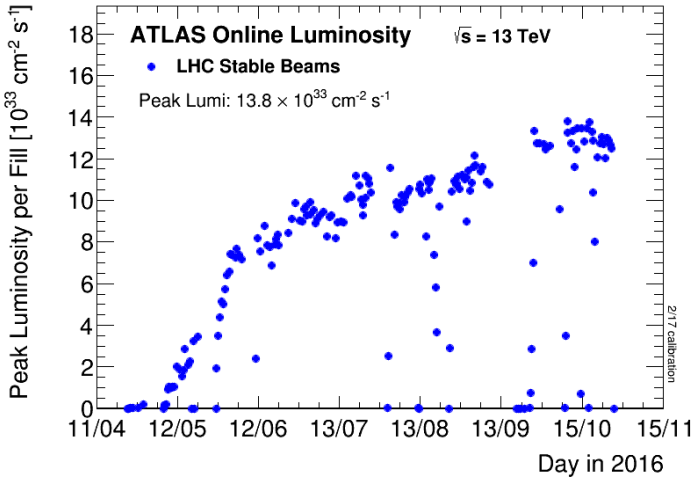
● Upgraded hardware.

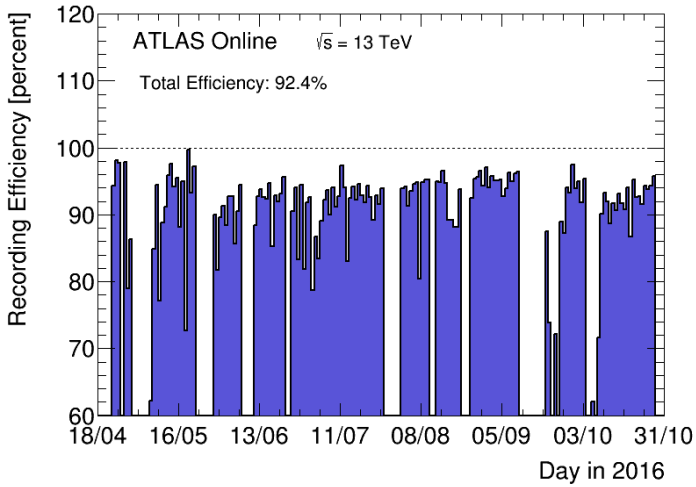
Upgrade compared to Run1:

- Upgraded CTPIN firmware: double data rate (80 MHz) allows up to 320 trigger inputs.
- Upgrade CTPCORE+ hardware module: additional 192 direct inputs (Run1: 0). 512 trigger inputs (Run1: 160), 512 trigger channels (Run1: 256), better monitoring
- Upgraded CTPOUT+ hardware module.
- Enable multi-partition mode (up to 3 running). Particularly important for commissioning of sub-detectors DAQ in parallel (in the past forced to use ATLAS partition).
- New L1CTP software architecture, designed to be more stable and robust.
- MUCTPI (Muon to CTP Interface) has received firmware upgrade to:
  - Provide L1Topo with (η,ϕ) coordinates (ΔηxΔϕ=0.3x0.1) of 2 leading muons p_T.
- New MuCTPIToTopo interface to communicate with L1Topo.

- $\eta = [1,1,1]$ means no muon
- $p_T = [1,1]$ means > 2 muons

Conclusions

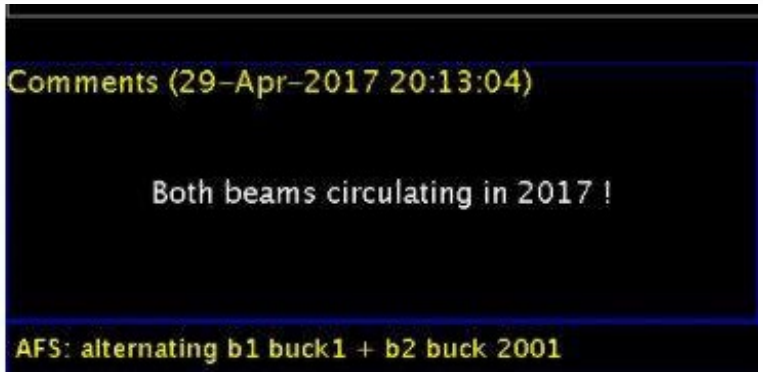


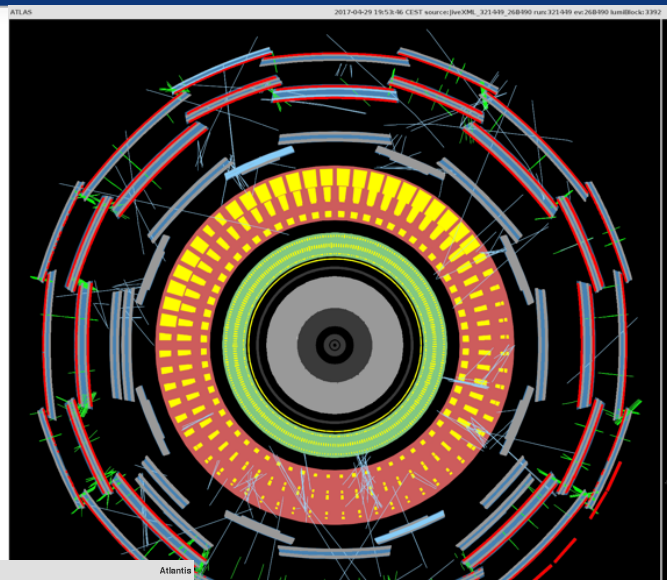


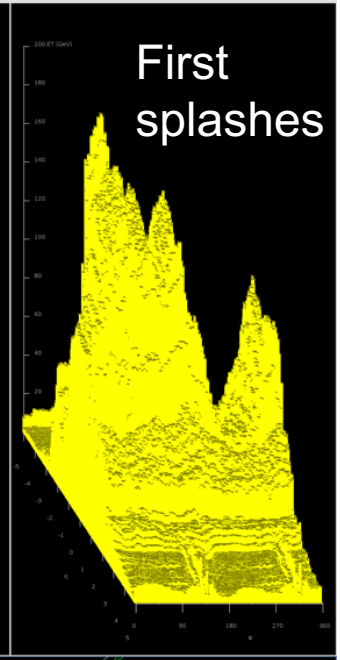
- After the LHC and ATLAS upgrades, despite the harshening of beam conditions, ATLAS took data with very high efficiency so far!

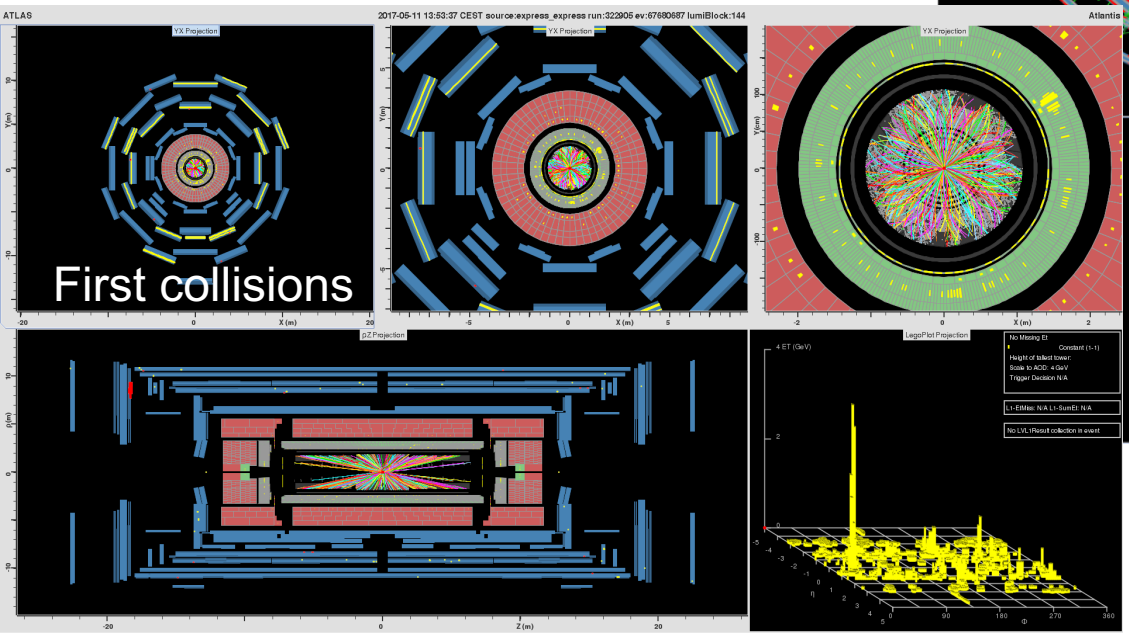
- We hope the best for end of Run2 data-taking!

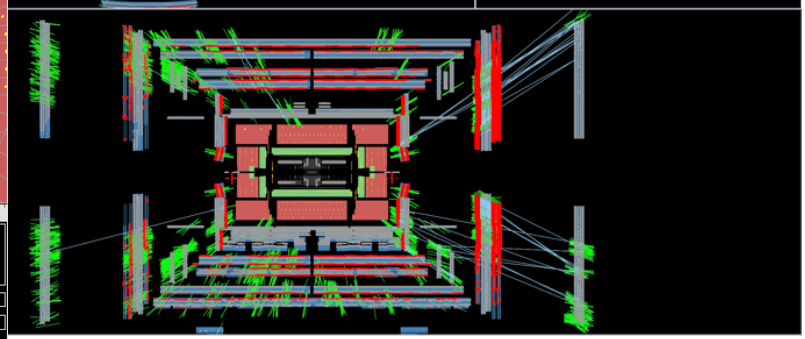
First beams in 2017 already there!





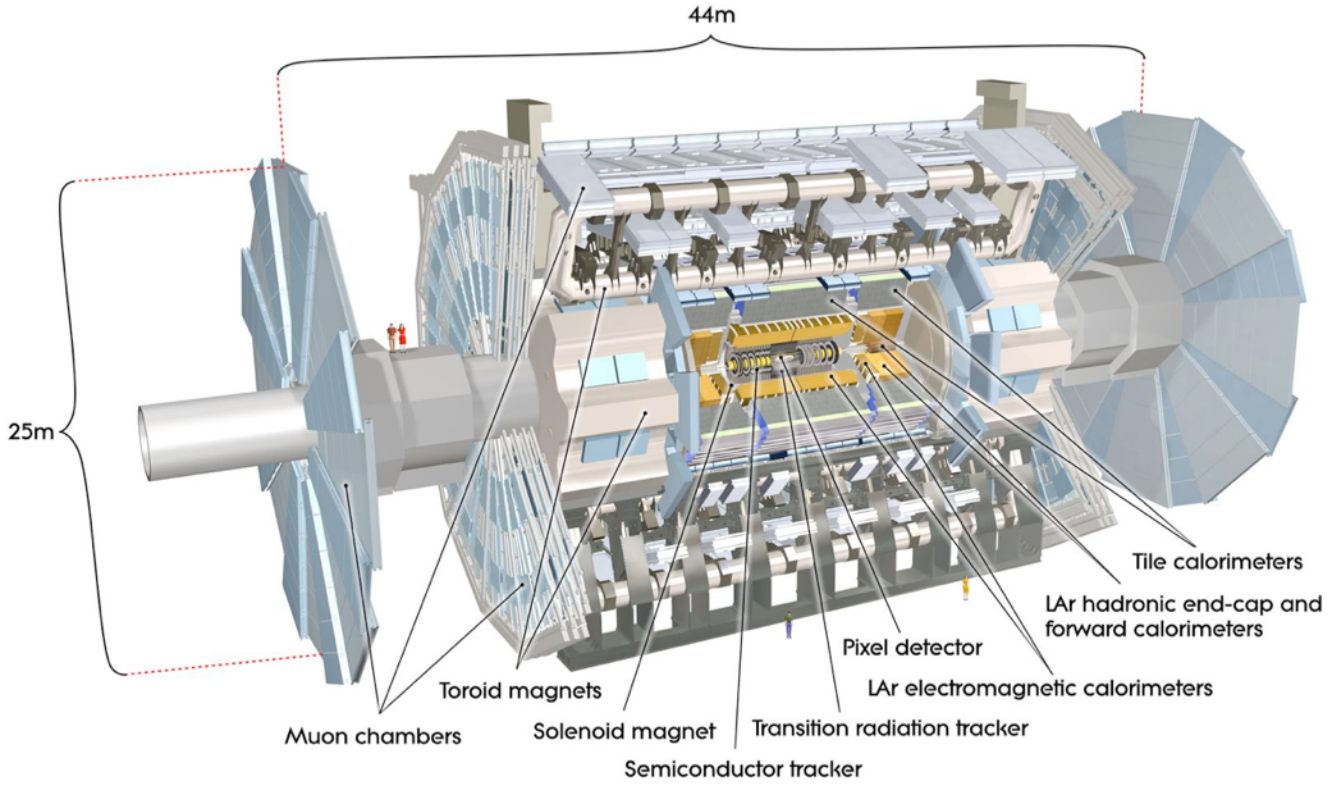




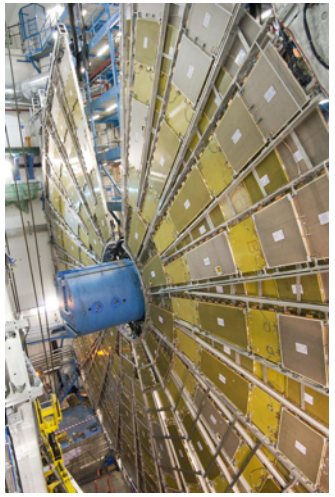


Back-up

Introduction – ATLAS and the four L1 detectors



Barrel L1 muon - RPC

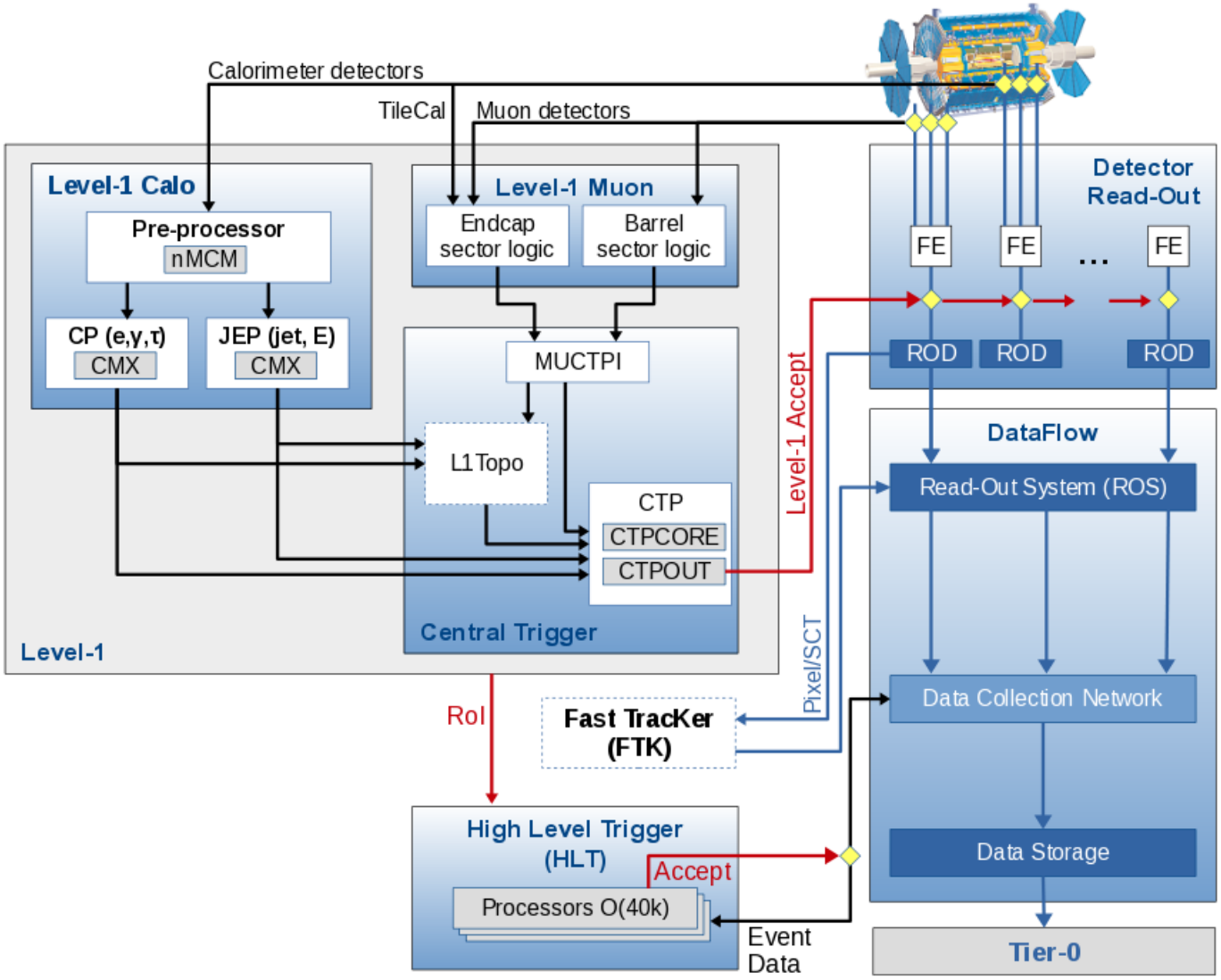


EndCap L1 muon - TGC

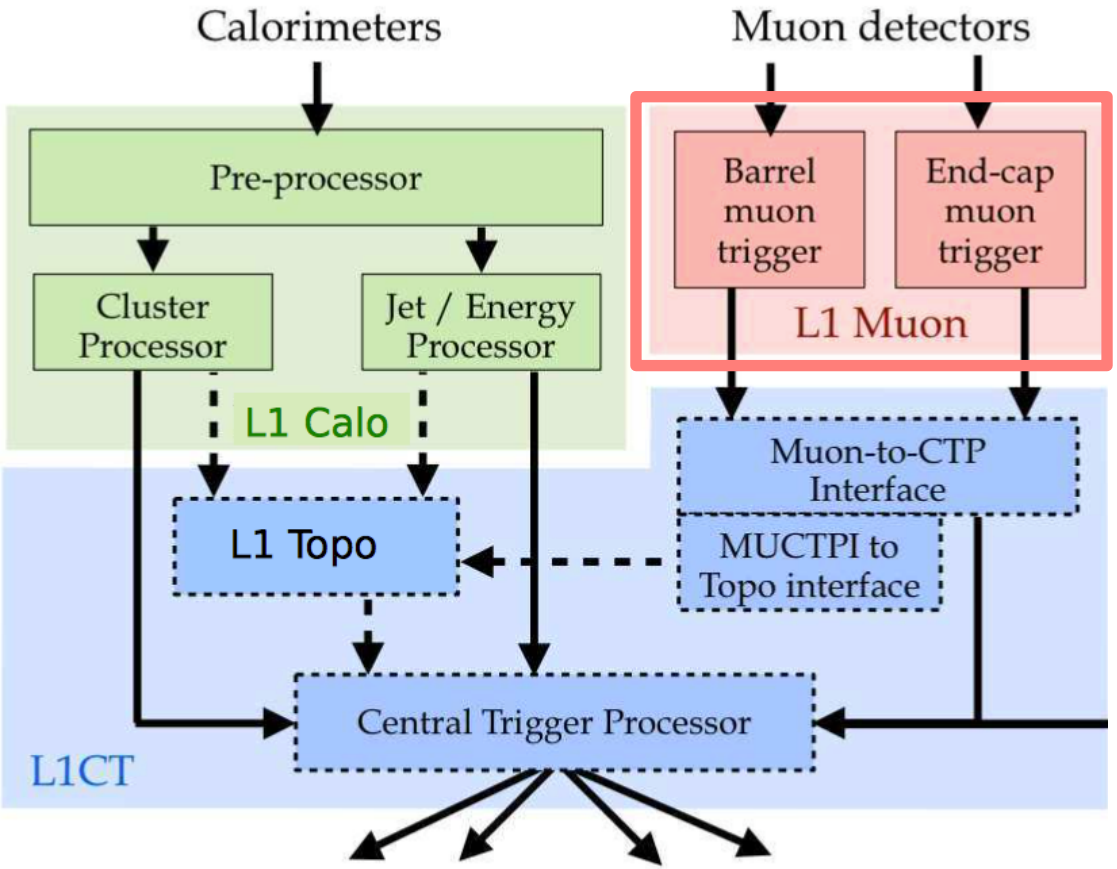
Tile Cal. - HCal barrel

LAr Cal. – ECal barrel, Cal Endcap

ATLAS L1 trigger



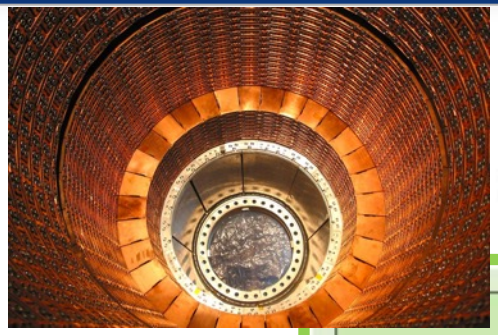
ATLAS L1 trigger – L1Muon



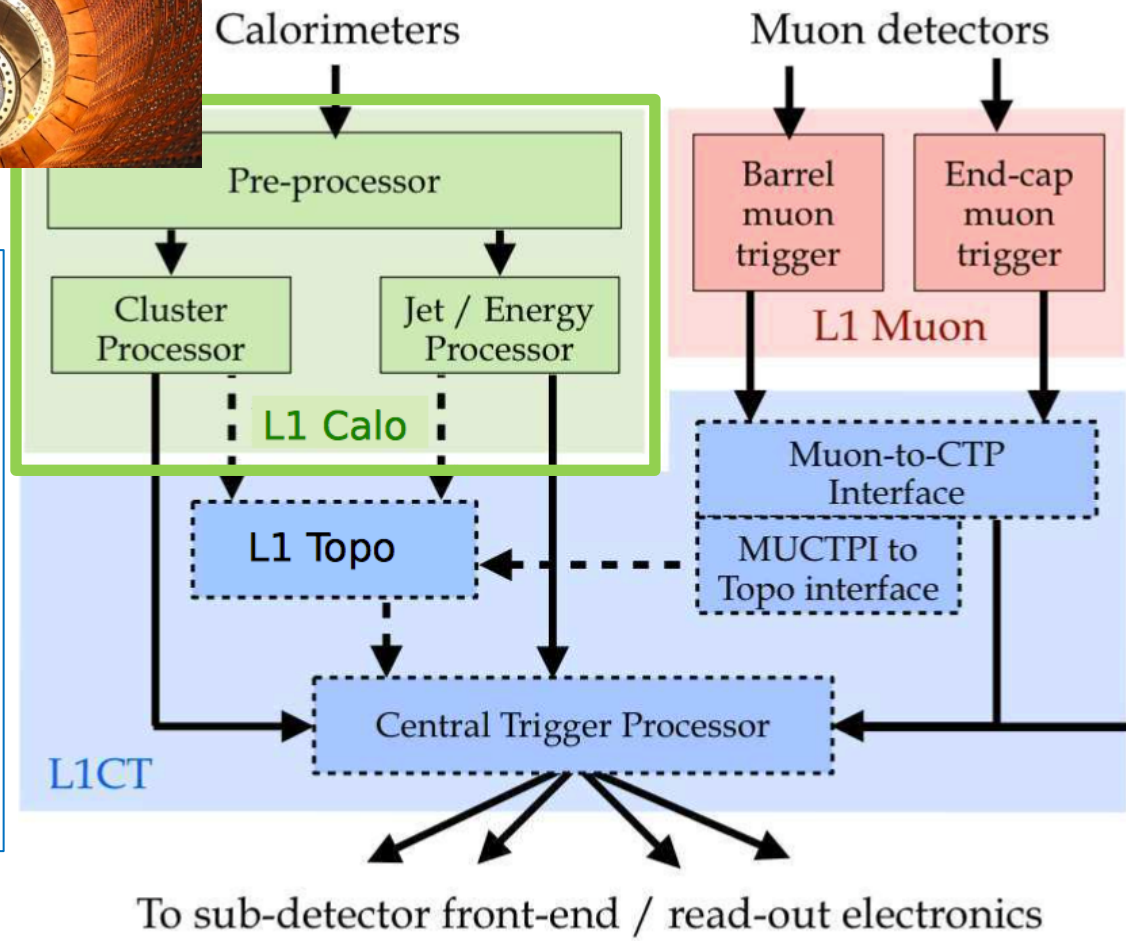
Upgrade compared to Run1:

- New RPC chambers installed in feet region(~3%) .
- TGC rate reduction using:
  - Coincidence between Small Wheel and big wheel (EI/FI).
  - Coincidence with TileCal barrel.
  - Low p_T items (MU4) requires 3 Stations instead of 2.
- New Muon to CTPI Interface firmware to provide muon p_T,η,ϕ to new MUCTPI to topo interface.

ATLAS L1 trigger – L1Calo

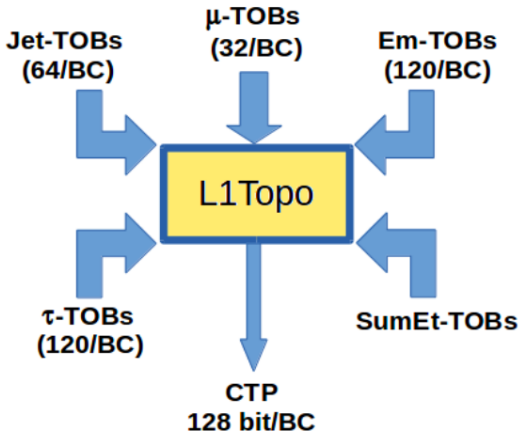


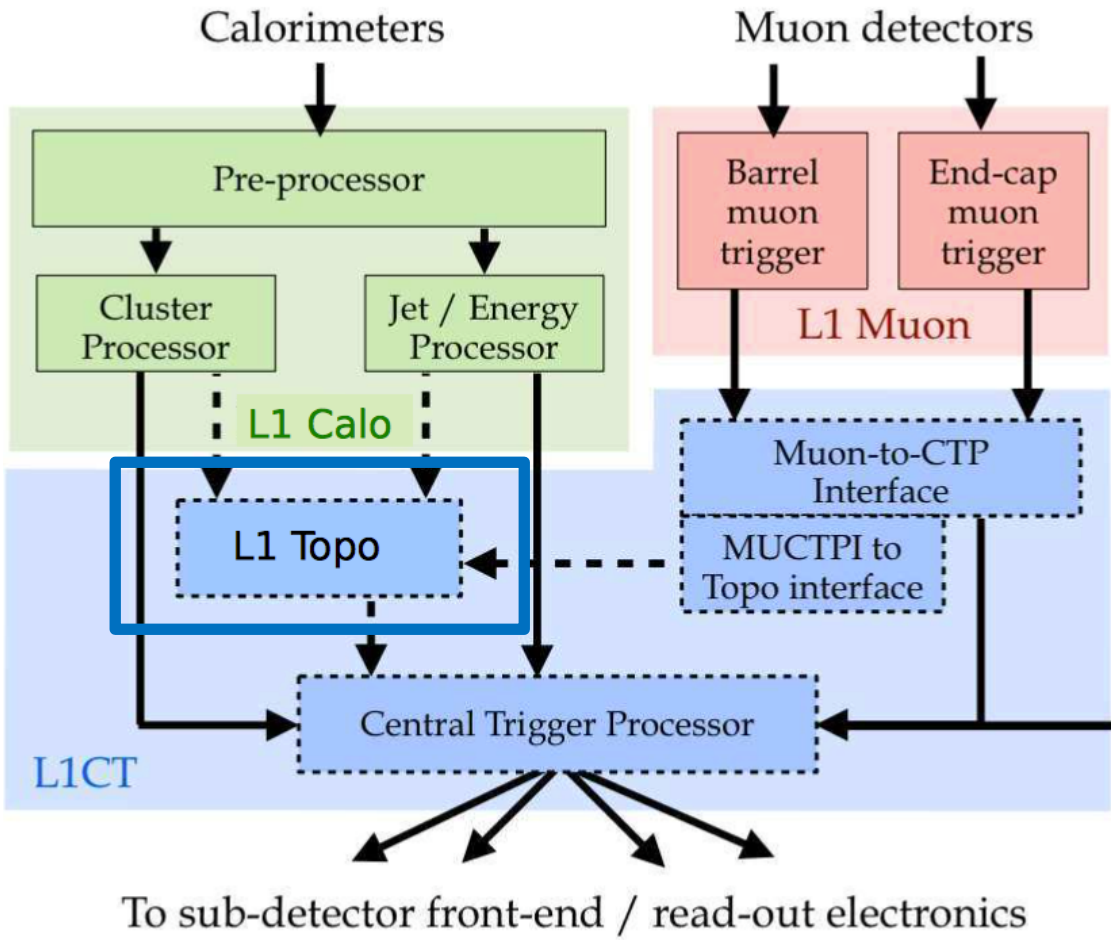
Upgrade compared to Run1:
- Replaced HW, and upgrade firmware in many L1Calo modules.
- Dynamic pedestal subtraction to reduce pileup dependence.
- Noise autocorrelation filters to improve energy resolution.
- ET dependent isolation.
- BCID measurement improvement.



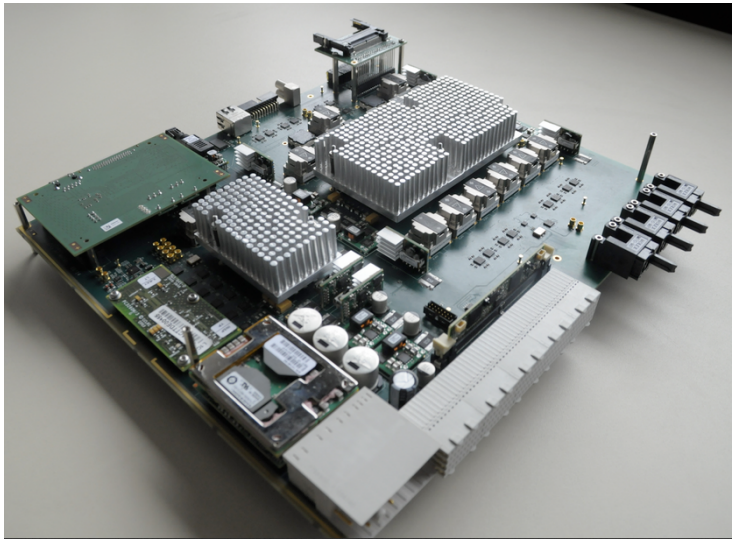
ATLAS L1 trigger – L1Topo

New in Run2!

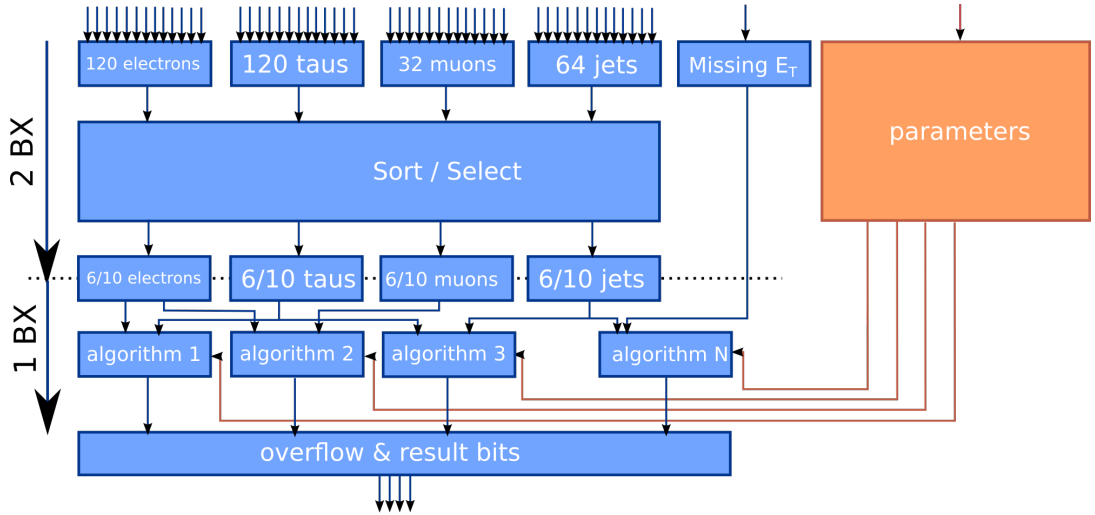




L1Topo specifications



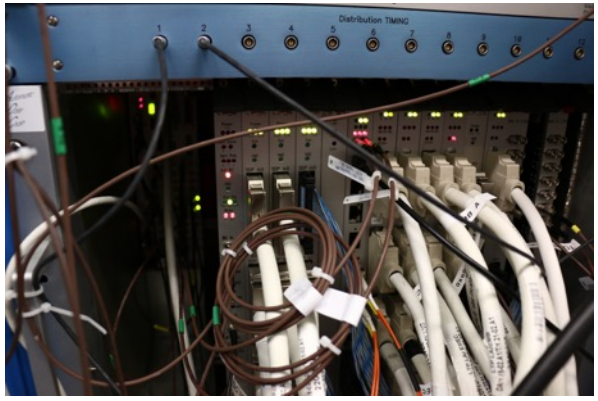
L1Topo - processing 1 Tb/s / module with latency budget of 150 ns
2 modules with 3 FPGAs each
(2 Xilinx Virtex7 XC7V690T for event processing and Kintex 7 for control and readout)
80 multi-gigabit receivers per FPGA (up to 13 Gbit/s)
dedicated boards converting input data into required format are also installed



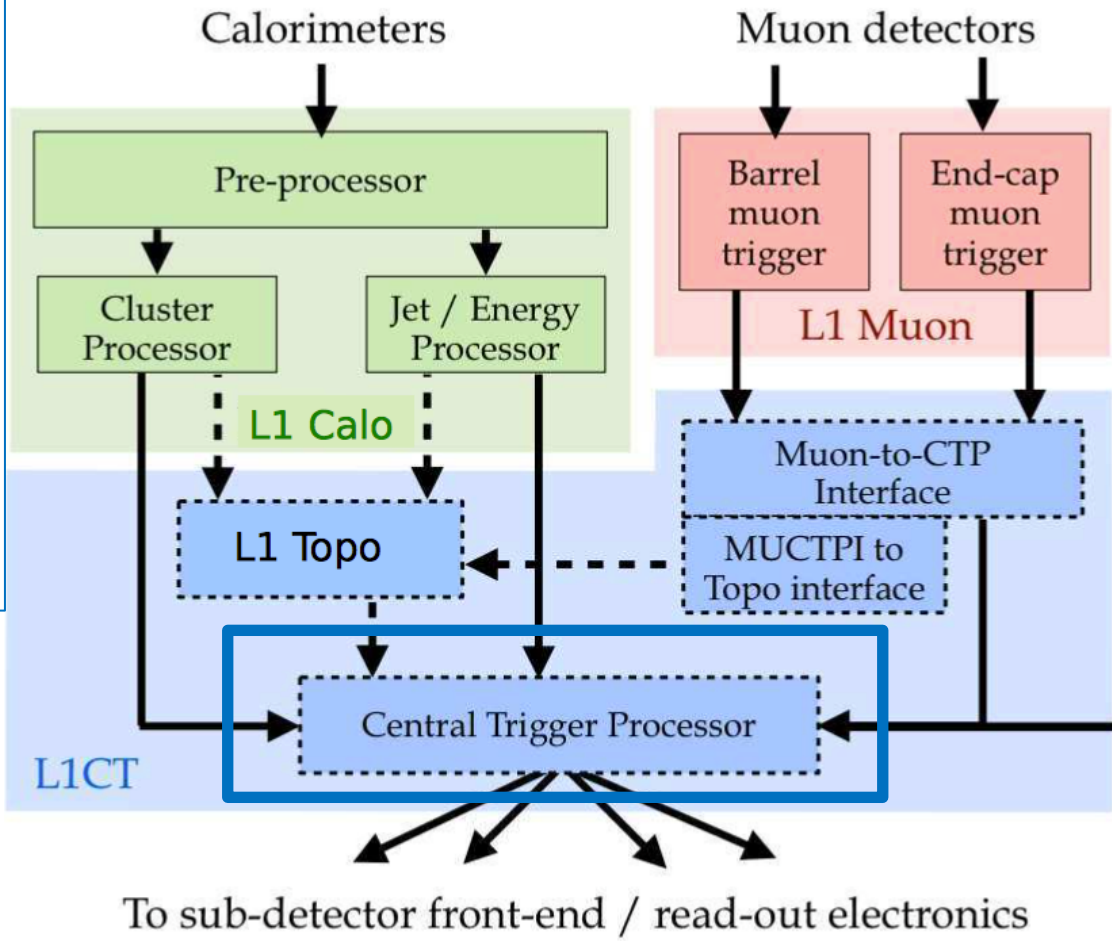
433200 look-up tables and 3600 digital signal processing slices
Execute algorithms in 75 ns (VHDL), decision is transmitted to Central Trigger Processor
Algorithms are configurable - up to 128 possible with 2 boards (107 are implemented)

ATLAS L1 trigger – L1CTP

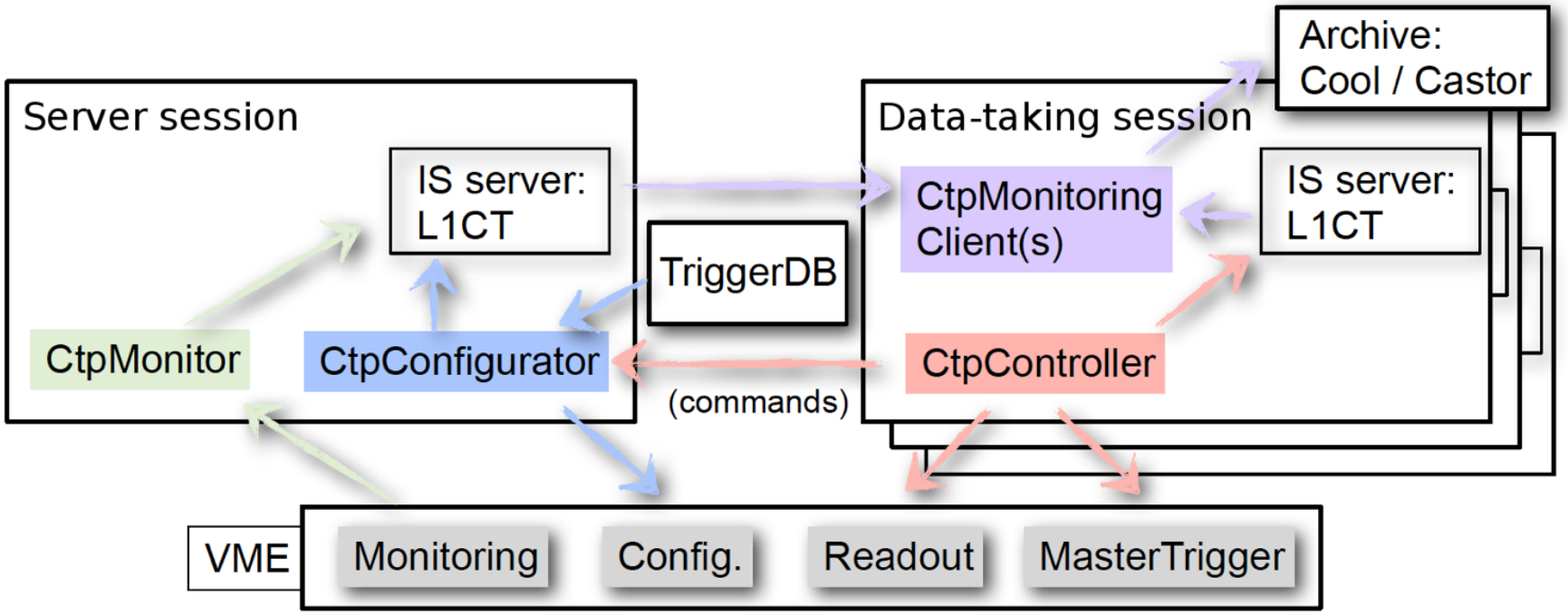
Upgrade compared to Run1:
- New hardware / firmware / software.
- More than 3 times the number of trigger inputs (160→512).
- Improved diagnostics and monitoring features.
- Double the number of triggers (256→512).
- up to 3 partitions running in parallel for calibration / commissioning.



CAM= content addressable memory



L1CTP – New software



Upgrades compared to Run1:
- New software architecture.
- More modular (allow MP running).
- Tested extensively in 2015-2016.

→Robust software important for reliable data-taking of central system such as CTP!

- CtpConfigurator : configure hardware.
- CtpController: control each partition.
- CtpMonitoring: Monitor info from hardware and publish to IS.
- CtpMonitoringClient: Display info from IS.