Contribution ID: **58** Type: **Poster**

Development of the slow control system for the Belle II ARICH counter

The Aerogel Ring Imaging Cherenkov (ARICH) counter is a particle identification device located in the endcap region of the Belle II detector, which is designed to discriminate charged pions from kaons. In total 420 of the Hybrid Avalanche Photo Detectors (HAPDs) are used in the ARICH counter to detect emitted photons. Therefore the management of power supplies and readout electronics of the HAPDs are critical in the ARICH operation.

Three kinds of power supply inputs are required in order to drive the HAPD module; negative high voltage for photo-electron acceleration (HV:˜7 kV), reverse bias voltage (Bias:˜300 V), and guard voltage (Guard:˜175 V). That means the ARICH slow control is required to have scalability up to 2520 input channels. We developed a network based control system of the power supplies to work collaboratively with other subsystems in the Belle II experiment such as SuperKEKB accelerator and environment monitors. Each of power supply crates has an Ethernet network connection to communicate with a control PC bridging between the crates and the Belle II global slow control system. The control system is based on common architecture of the Belle II data acquisition (DAQ) system for network communication, database access and graphical user interface. In order to protect the HAPDs, it is essential to keep the relations of voltages connected to the same HAPD gets down when the sensor is switched off. We have developed an automatic ramp up / down scheme for the same reason.

The readout of the HAPD module consists of two parts : Front-end boards (FEB) and Merger boards (MB). The FEB is connected to a HAPD, and several FEBs (up to six) are connected to a MB. FEB is developed based on an analog comparator in ASICs to extract signal and an FPGA for data transfer and configuration. In the second step, the MB connects several FEBs to merge and reduce data to send them out to the Belle II global DAQ system via a common protocol, called Belle2Link. The FEB needs three voltages (+2.0 V, -2.0 V, +3.8 V), and a MB needs two voltages (+1.5 V, +3.8 V). In total 420 FEBs and 72 MBs are used for the ARICH counter, therefore 1404 channels of the low voltages are required to be managed by the slow control system. In addition to readout electronics hardware, a control software is also developed based on the common framework of the Belle II DAQ system to manage parameters, such as threshold voltage of the comparators, in registers of FEBs and MBs. Since only the hit pattern is recorded, a dedicated technique of data taking for threshold and gain determination is developed. This threshold scan is a kind of noise measurement with changing the threshold voltage, and therefore requires to repeat the cycle of the threshold configuration and trigger start / stop. The readout control system realizes these procedure by synchronizing the trigger timing system and the readout electronics using the Belle II slow control protocol.

In this presentation, technical aspects of the ARICH control system are discussed and implementation in a detector operation test using cosmic ray during the detector construction and prospects of operation after installation into the Belle II detector.

Primary author: YONENAGA, Masanobu (Tokyo Metropolitan University)

Co-authors: KINDO, Haruki (SOKENDAI); KAKUNO, Hidekazu (Tokyo Metropolitan University); KAWAI, Hideyuki (Chiba University); ADACHI, Ichiro (KEK, SOKENDAI); OGAWA, Kazuya (Niigata University); HATAYA, Koki (Tokyo Metropolitan University); NOGUCHI, Kouta (Tokyo Metropolitan University); SANTELJ, Luka (KEK); TABATA, Makoto (Chiba University); MRVAR, Manca (Jozef Stefan Insutitute); MACHIDA, Masahiro (Tokyo University of Science); YOSHIZAWA, Morihito (Niigata University); KRIZAN, Peter (University of Ljubljana, Jozef Stefan Insutitute); DOLENEC, Rok (University of Ljubljana); PESTOTNIK, Rok (Jozef Stefan Insutitute); KORPAR, Samo (University of Maribor, Jozef Stefan Institute); OGAWA, Satoru (Toho University); NISHIDA, Shohei (KEK, SOKENDAI); SUMIYOSHI, Takayuki (Tokyo Metropolitan University); KUMITA, Tetsuro (Tokyo Metropolitan University); KONNO, Tomoyuki (KEK); YUSA, Yosuke (Niigata University)

Presenter: YONENAGA, Masanobu (Tokyo Metropolitan University)

Track Classification: Backend readout structures and embedded systems