Modules and Front-End Electronics Developments for the ATLAS ITk Strips Upgrade

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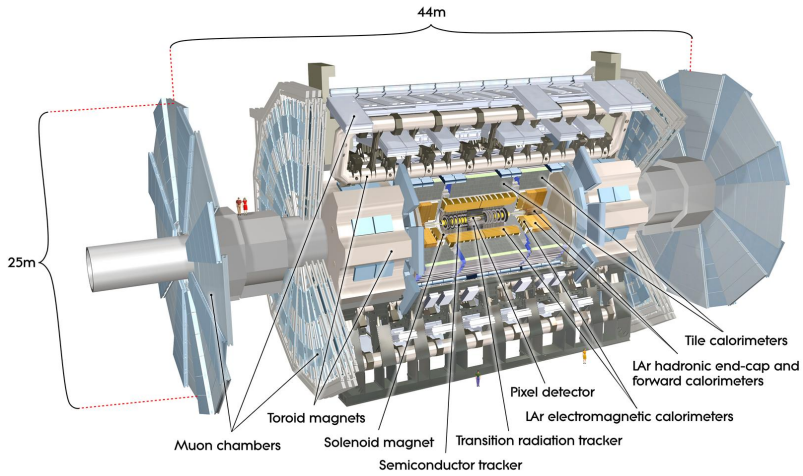
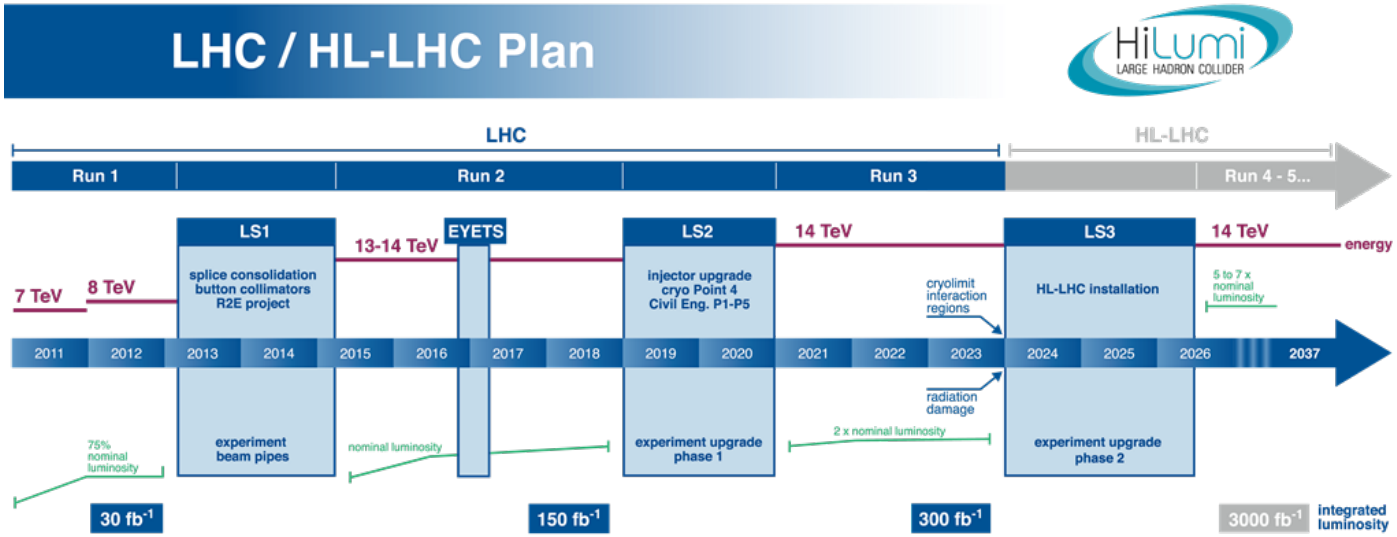
Outline

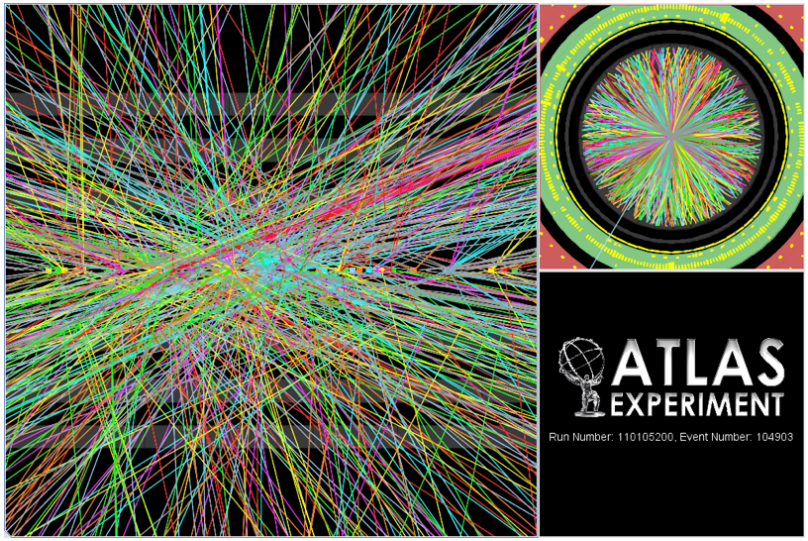
- ATLAS is a **general purpose experiment** at the Large Hadron Collider.
- It consists of:
  - Tracker (Inner Detector), built with **silicon pixels** layers, **silicon strips** (SCT) layers and a **Transition Radiation Tracker**.
  - Electromagnetic and hadronic calorimeters.
  - Muon chambers.
- Designed for $\mu = 25$ at 25 ns bunch crossings.



- The major upgrades will take place between 2024 and 2026.
- Increase in **pile-up and luminosity**.
  - $\mu \approx 200$.
- **Inner triplets** replaced due to radiation damage $\Rightarrow$ new designs for 4000 fb^{-1} by 2037.

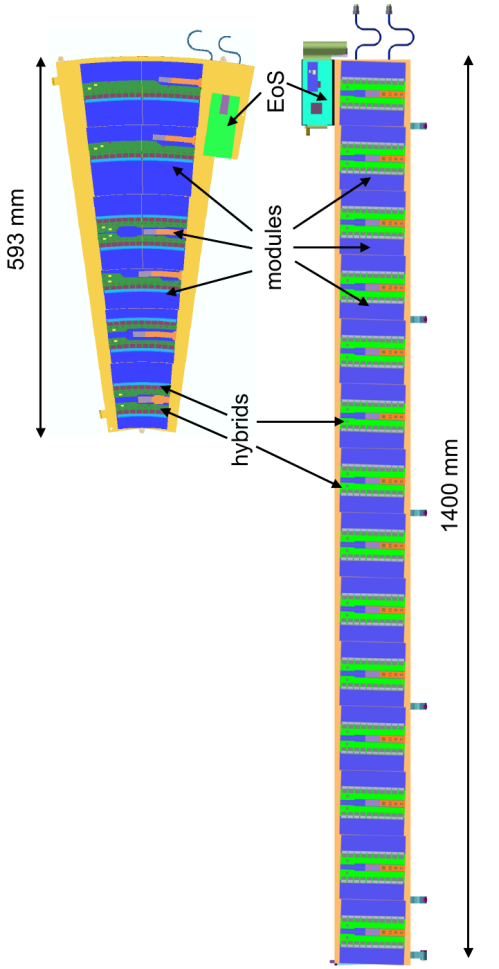


- ATLAS Tracker Upgrade:
  - **Increase sensitivity** for physics searches.
  - More **granularity** to counter the higher **pile-up and track density**, and to have more precise measurements.
  - New detector designs to cope with a **higher radiation** environment.
  - While **reducing power consumption** and keeping low **material**.



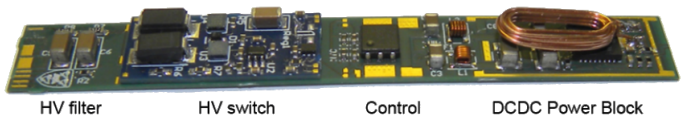
ATLAS simulated event with 140 pile-up

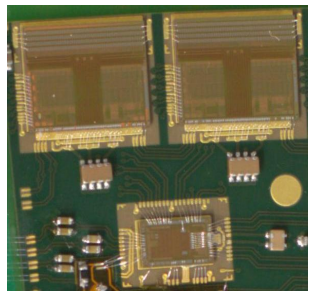
- ATLAS will replace the current tracker with an **all-silicon tracker**.
  - Channels: pixels $\approx 80 \rightarrow \approx 600$ million and strips $\approx 6 \rightarrow \approx 70$ million.
- Layout of the Strips Detector:
  - Four **barrel layers** and six **end-cap discs** per side.
  - Barrel layers are made from **staves**, end-cap discs from **petals**.
  - Staves and petals are an assembly of **modules**.
  - Modular with **integrated** cooling and electronics.
- **Radiation levels** in the HL-LHC require new **designs**.
  - Sensors: n-in-p, single sided. No bulk **type inversion**.
  - Read-out **electronics** in 130 nm process.



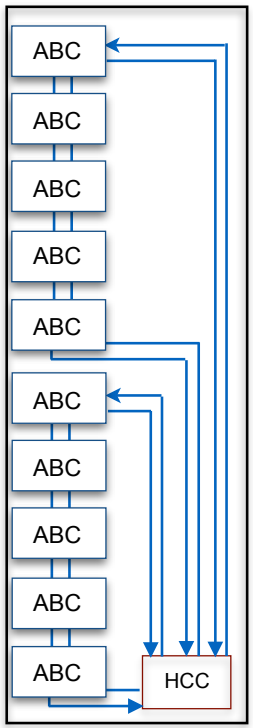
- Most results here from **Technical Design Report** (April 2017).

- Increased **power consumption**:
  - Tenfold increase in the number of channels, lower power consumption per channel.
  - Current SCT: $\approx 60\%$ **power lost** in cables.
  - No more space for **extra cables** (more material).
  - Higher voltage at PSU $\Rightarrow$ lower current $\Rightarrow$ **DC-DC conversion** at the modules.
- Sensor bias with **HV multiplexing**.
  - Single HV cable for multiple modules, **material reduction**.
  - **Radiation hard HV switches** required to isolate modules.
- **Power-board** with integrated DC-DC converter and HV multiplexer at the modules.
  - Control and monitoring: HV, LV currents, temperature.



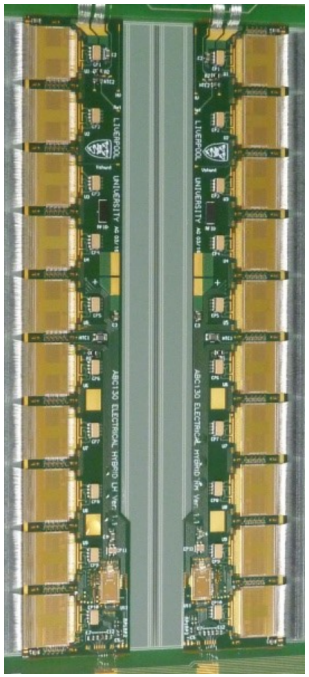


- Hybrid Control Chip **HCC130**:
  - **Interface** between the read-out chips and the End-of-Structure (stave/petal).
  - Two input data loops and one output data line.
- ATLAS Binary Chip **ABC130**:
  - IBM 130 nm CMOS process.
  - **Daisy chain** read-out architecture.
  - Reads out **256 strips** from a silicon sensor.
  - **Binary outputs** of the discriminators are sampled at 40 MHz rate and stored in a **pipeline**.
  - Shaping time of 20 ns.
  - **Gain** 85 mV/fC and **noise** $< 700\ e^-$ENC for $C_{in} = 6.4$ pF.

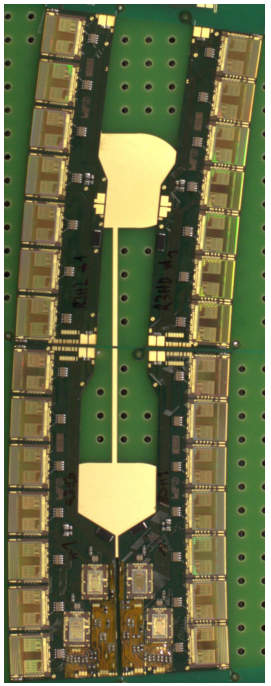


Hybrid Circuits

- The hybrid circuits for Strips Modules are **flex circuits** holding multiple read-out ASICs.
- **Polyimide base** with three or four copper layers.
- Multiple ABC130 read-out ASICs to connect to a silicon strip sensor.
- Different **shapes** for barrel and end-cap.



Barrel hybrids

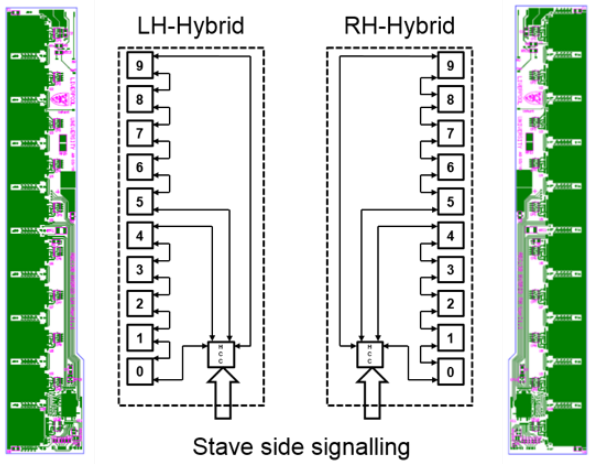


End-cap hybrids

Hybrid Circuits

Barrel Hybrids

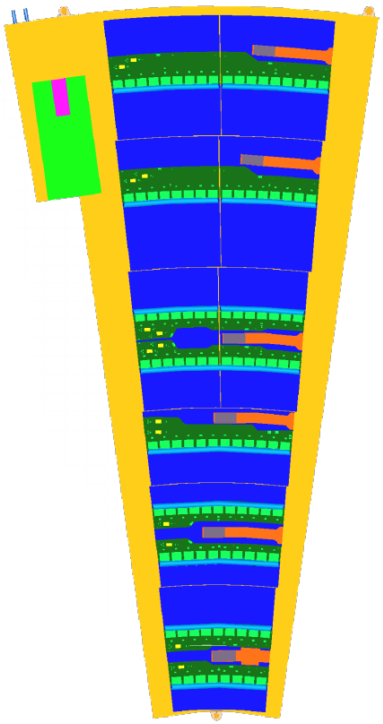
- Two types, mirrored: Left-Hand (LH) and Right-Hand (RH).
- Ten read-out ASICs and one HCC per hybrid.
- Reading out 2560 strips each.
- One type mounted on Long Strip (LS) modules, two on Short Strip (SS) modules.



Hybrid Circuits

End-cap Hybrids

- Several variations, with different dimensions depending on radius.
  - **13 flavours of hybrids** and 9 flavours of modules.
  - **Naming scheme**: "RxHy" where x is the ring and y is the hybrid position (0 to 3).
    - Position 0 is bottom/right, position 1 is top/left.
    - Position 2 is top-right and position 3 is top-left (only Ring 3).
- **Between 7 and 12 read-out ASICs** per hybrid (between 6 and 11 per HCC).
  - Split sensors/hybrids for higher radii.
  - Varying number of chips per HCC depending on occupancy and capability of the HCC (up to 11 chips).
  - Different power/DAQ requirements.



R5: split, 9 chips/hybrid

R4: split, 8 chips/hybrid

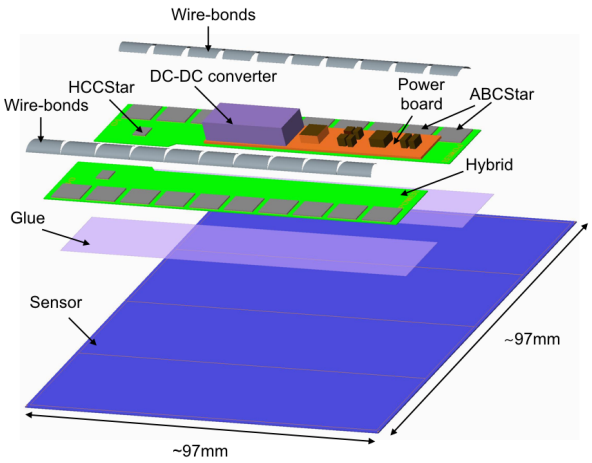
R3: split, 8 chips/hybrid

R2: 12 chips

R1: 11 and 10 chips

R0: 8 and 9 chips

- The **hybrid** is glued on sensor with non-conductive glue.
- **Power-board** glued on sensor next to the hybrid(s).
- **Wire-bonds** from ASICs to strips and from power-board to hybrid.
  - Power-board not needed for initial prototypes.
- **Read-out** from one side of the module to DAQ.
  - Power and data come from opposite sides of the module.

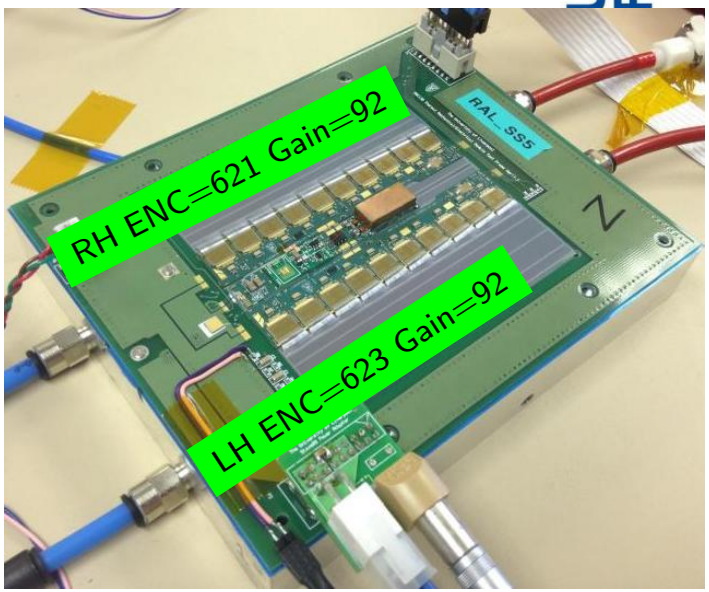


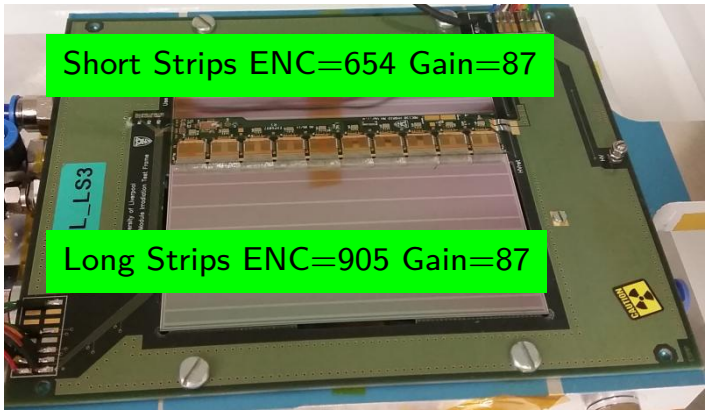
Modules

Barrel Long and Short Strips

- Two flavours of barrel module prototypes:
  - **Short strips (SS)**: two hybrids on a short strips (2.5 cm) sensor.
  - **Long strips (LS)**: one hybrid on a short strips sensor, strips segments connected together to have long strips.
- Initially built and tested on a single module test-frame.
  - Power and data come via IDC connectors.
- Now also tested on a bus-tape together with other modules.

[ENC (Equivalent Noise Charge) or noise is measured in electrons, Gain is measured in mV/fC.]



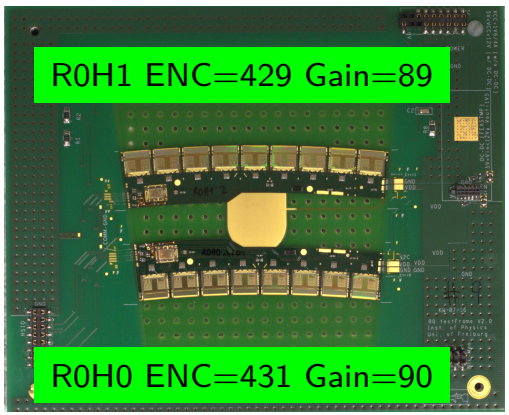


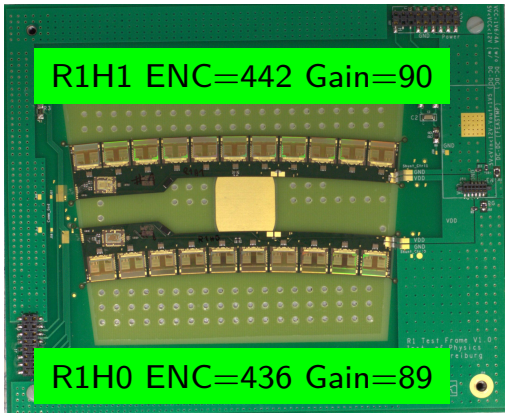
Modules

End-cap Modules

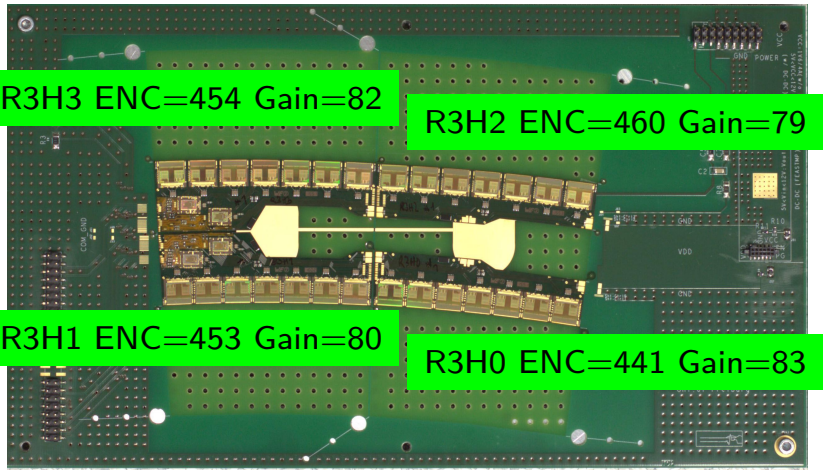
Noise and figures **without sensors** (averages of the whole hybrid):

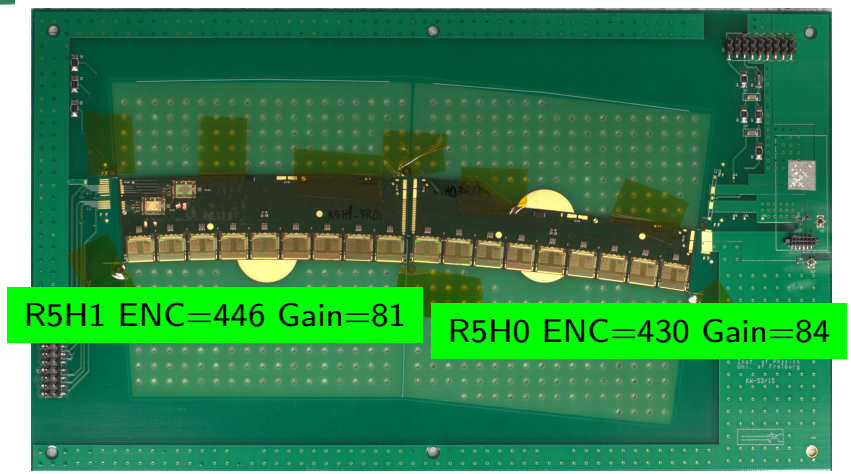
- First **Ring 0 sensors** received in February.
- We just produced the **first R0 modules**.





- **Multiple hybrid** assemblies already tested:
  - Rings 0, 1 and 5: two hybrids.
  - Ring 3: four hybrids.

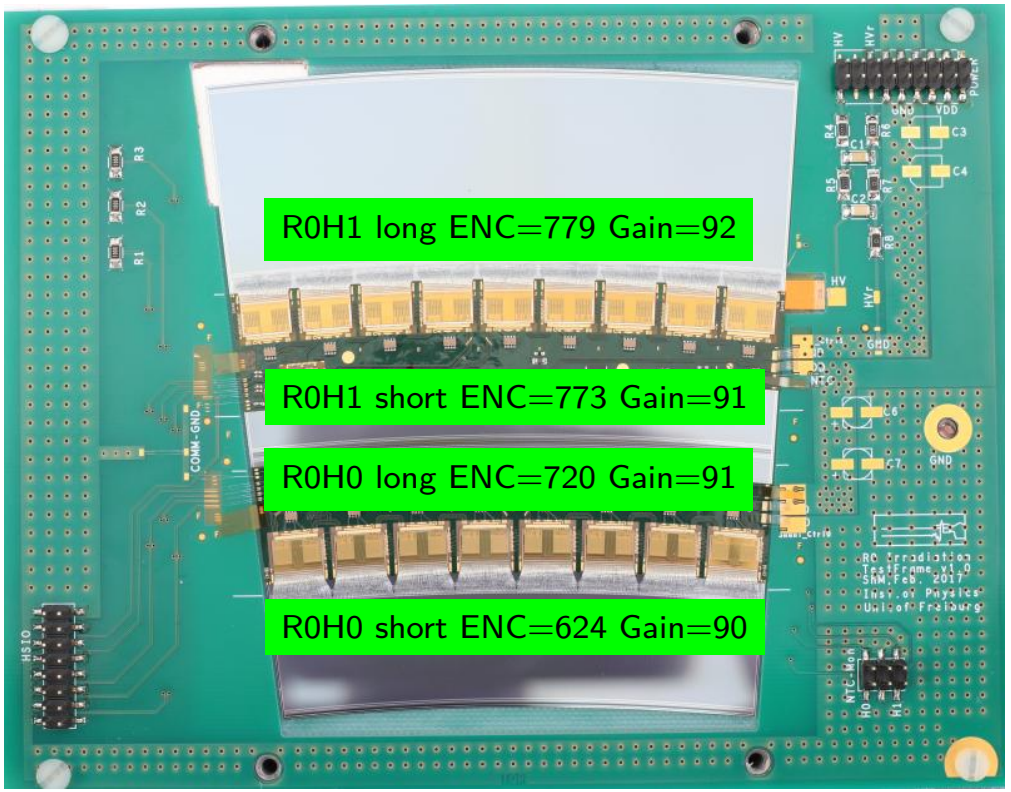




Modules

End-cap Modules

- First Ring 0 module.
- Currently in **test-beam** at DESY.
- Sensor has **4 strips segments** with different strip lengths:
  - First (top) is $\approx$ 30 mm, read out by R0H1.
  - Second is $\approx$ 27.5 mm, read out by R0H1.
  - Third is $\approx$ 22.5 mm, read out by R0H0.
  - Fourth (bottom) is $\approx$ 17.5 mm, read out by R0H0.

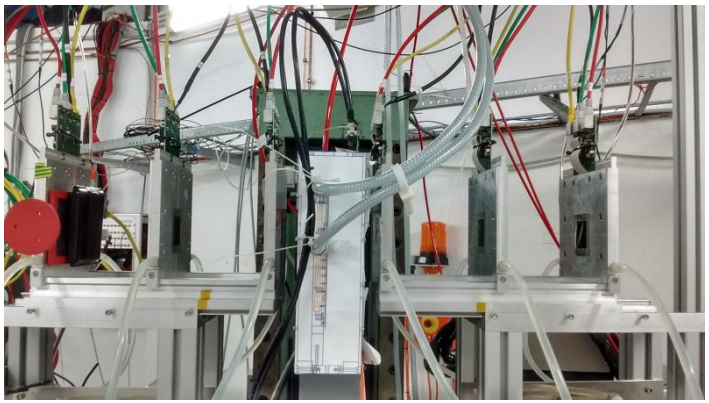


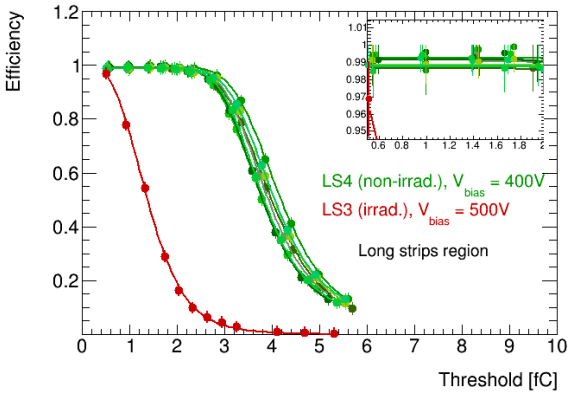
- **Noise and gain** are consistent with previous barrel prototypes.

Modules

Module Irradiations and Test-Beam

- Test-beams at DESY and CERN with full Long Strips **barrel modules** in 2016.
  - DESY with 4 to 4.8 GeV electrons, non irradiated module.
  - CERN with 120 GeV pions, a proton irradiated module to 8×10^{14} n_{eq}/cm^2 (end-of-life).
- Next: **end-cap** Ring 0 modules. Same as with the barrel modules, taking place this year.

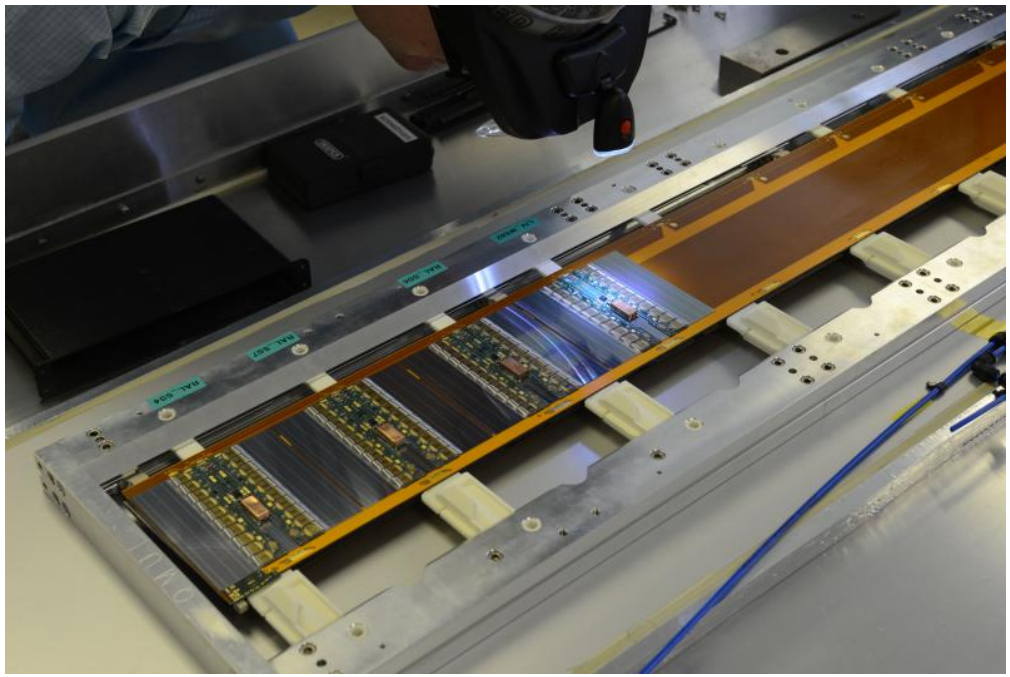




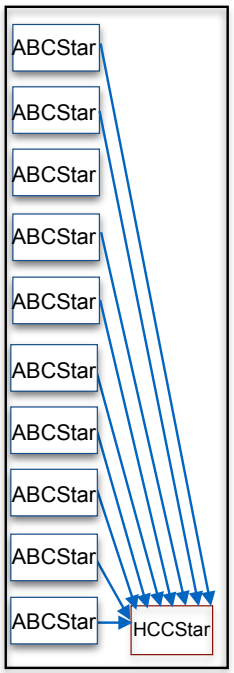
Modules

Stave of Modules

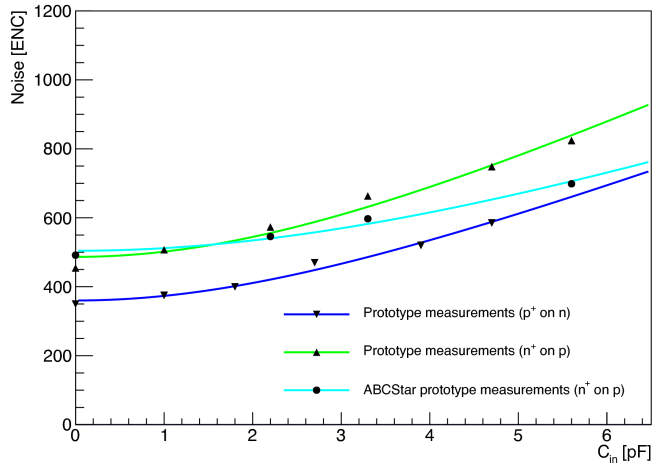
- **Four modules per side** of the stave (out of 13).
- **Power-boards** for LV and HV distribution.
- **Bus-tape** for data and power distribution from End-of-Stave.
  - Presented in the next talk.
- Noise **performance** is fair for all modules.



ABCStar and HCCStar



- **Evolution** of the current ABC130 and HCC130 chips, 130 nm process.
- Final read-out chip design for the ITk.
- Change in the **read-out architecture** to point-to-point links between each ABCStar and the HCCStar.
- Modifications in the **front-end**.
  - Prototype of preamplifier-shaper-discriminator with 32 channels.
  - Higher initial **noise** than ABC130, lower noise with irradiation.
- First **production**: 2017Q4.



Noise measurements for different input capacitance, ABC130 and ABCStar prototypes.

Conclusions

- ITk strips detector design and R&D well advanced.
- **New Front-End** development almost finished and preparing for pre-production.
- First **barrel modules** have been tested and show good end-of-life performance.
- The first **multi-module** structure (stave) is being built and tested.
- The **first end-cap module** is about to be tested at DESY.
- And a second one will be **irradiated** and tested at CERN.