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Acceleration of an particle identification algorithm used for the LHCb Upgrade with the new Intel(r) Xeon(r)/FPGA

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The LHCb experiment at the LHC will upgrade its detector by 2018/2019 to a 'triggerless' readout scheme, where all the readout electronics and several sub-detector parts will be replaced. The new readout electronics will be able to read out the detector at 40MHz. This increases the data bandwidth from the detector down to the event filter farm to 40TBit/s, which also has to be processed to select the interesting proton-to-proton collisions for later storage. The architecture of such a computing farm, which can process this amount of data as efficiently as possible, is a challenging task and several compute accelerator technologies are being considered for use inside the new event filter farm.

In the high performance computing sector more and more FPGA compute accelerators are used to improve the compute performance and reduce the power consumption (e.g. in the Microsoft Catapult project and Bing search engine). Also for the LHCb upgrade, the usage of an experimental FPGA accelerated computing platform in the event building or in the event filter farm (trigger) is being considered and therefore tested. This platform from Intel(r) hosts a general Xeon(r) CPU and a high performance Arria 10 FPGA inside a multi-chip package linked via a high speed and low latency link. On the FPGA an accelerator is implemented. The used system is a two socket platform from Intel(r) with both sockets hosting an Intel(r) Xeon(r)/FPGA. The FPGA has cache-coherent memory access to the main memory of the server and can collaborate with the CPU.

A computing intensive algorithm to reconstruct Cherenkov angles for the LHCb RICH particle identification was successfully ported to the Intel(r) Xeon(r)/FPGA platform and accelerated. For this a Verilog and a OpenCL kernel were used, and compared in performance and development time. Also, other PCIe FPGA accelerators using the same FPGA were tested for performance. One important measurement is the performance per Joule, which will be compared to modern GPUs. The results show that the Intel(r) Xeon(r)/FPGA platforms, which are built in general for high performance computing, are also very interesting for the High Energy Physics community.

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