Development of ATLAS Liquid Argon Calorimeter Readout Electronics for the HL-LHC

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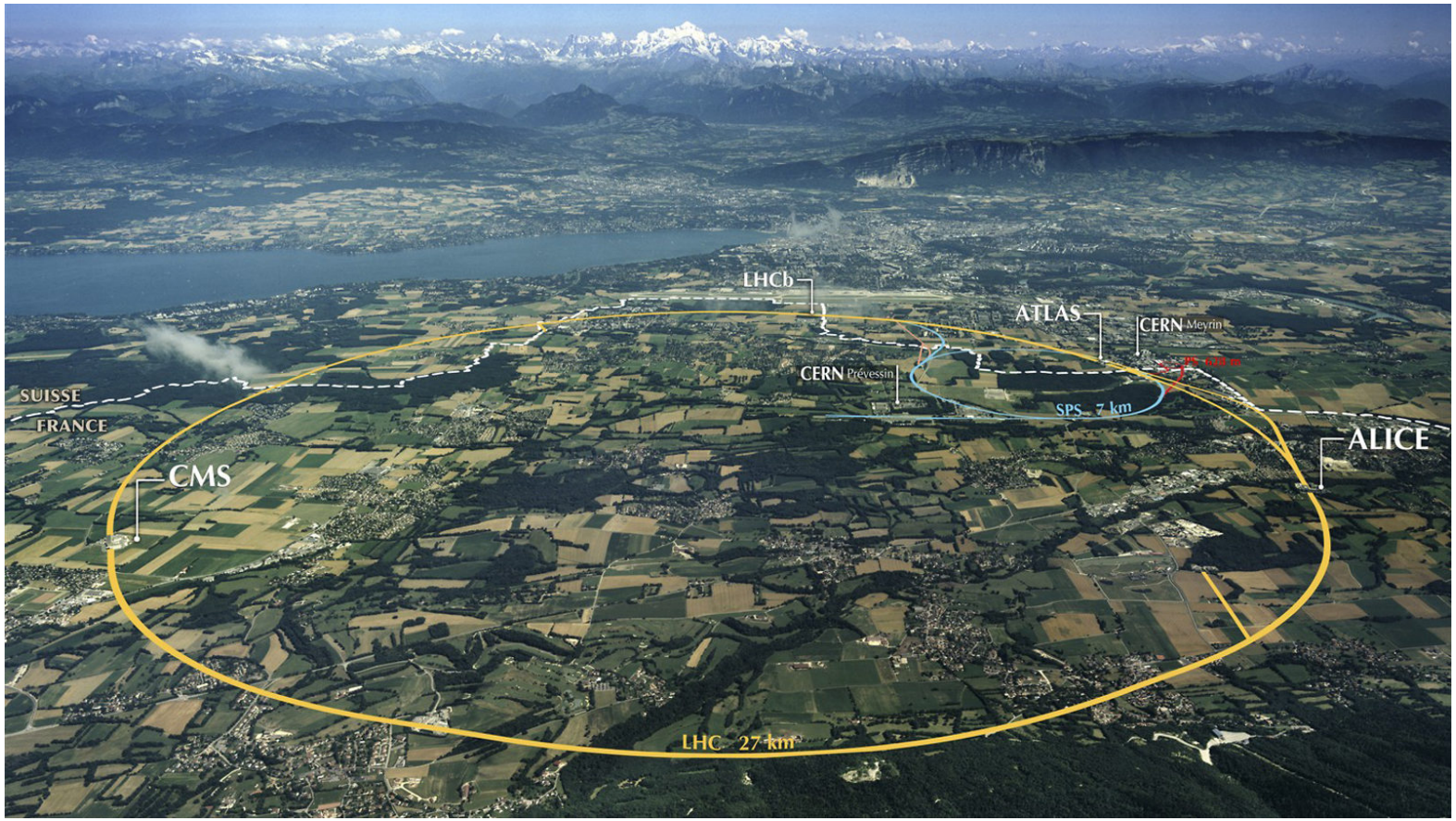
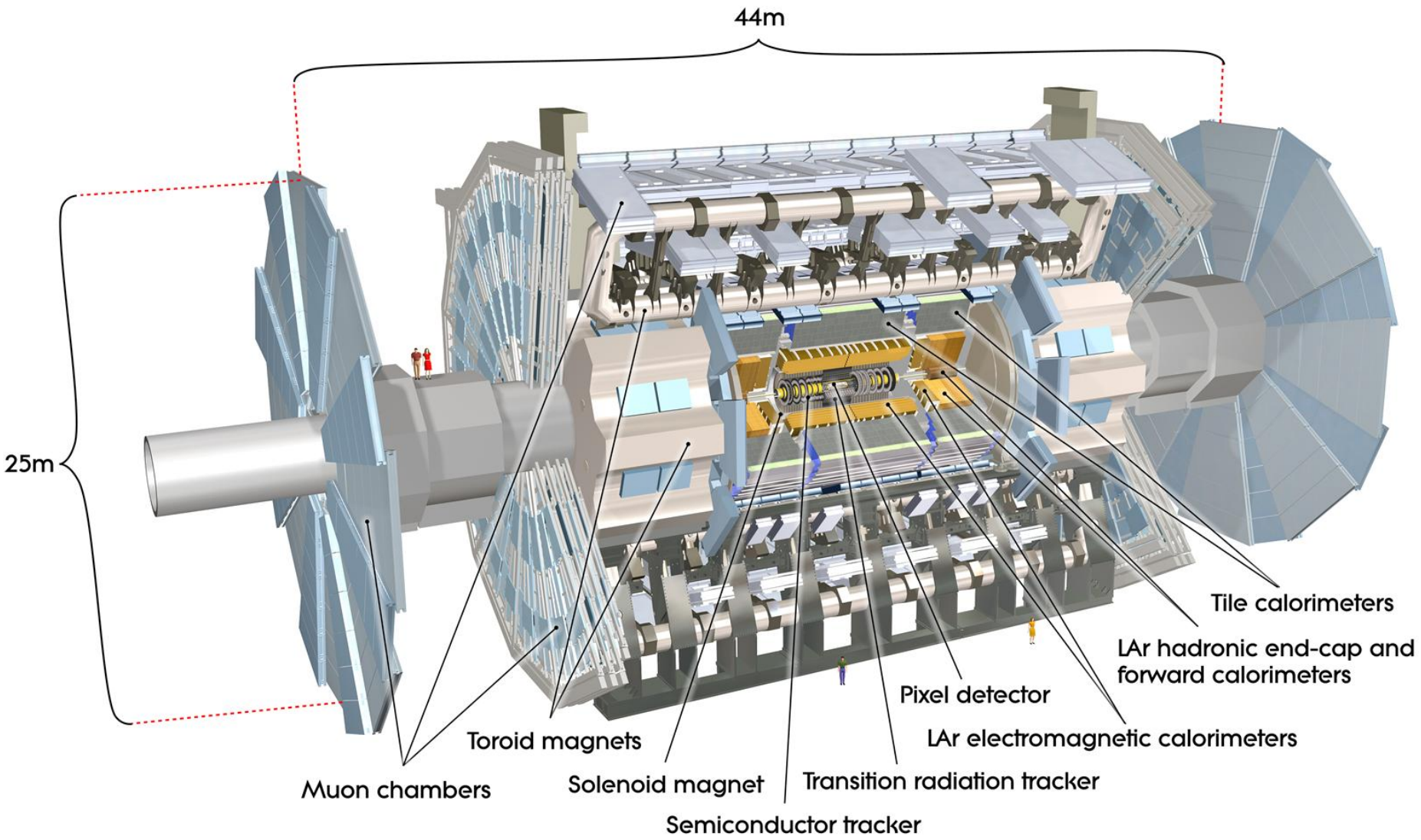
Large Hadron Collider

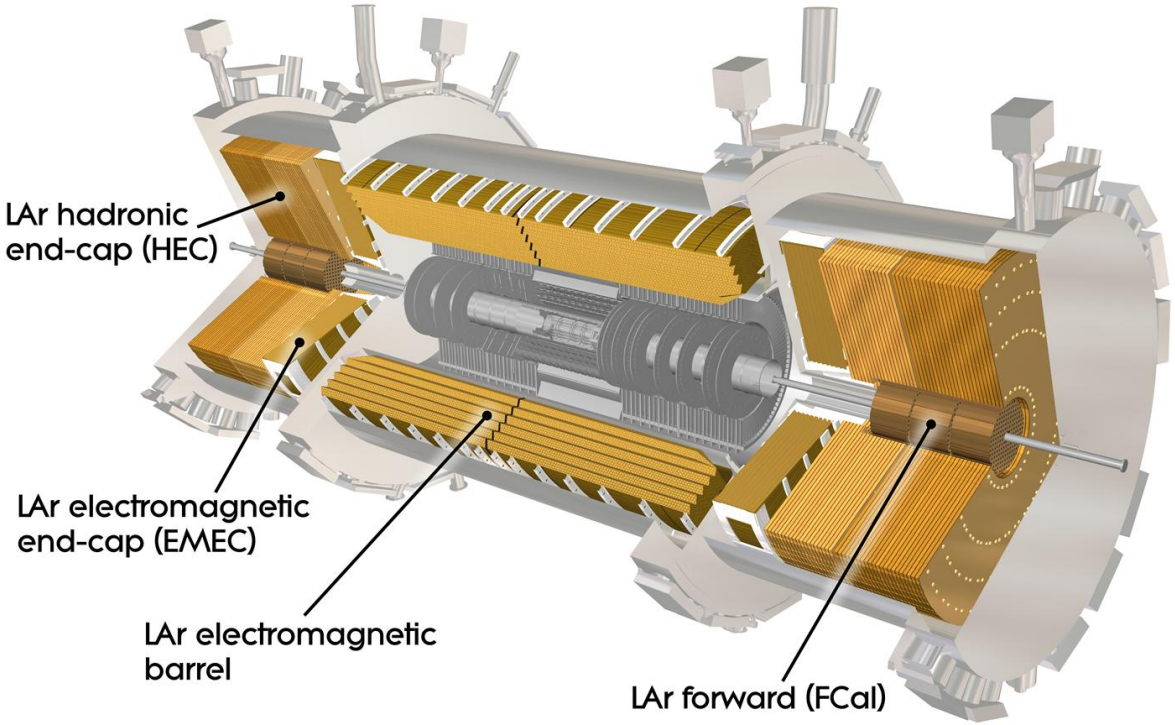


- Proton-proton collisions with $\sqrt{s} = 14\,\text{TeV}$ at a rate of 40 MHz
- About 10^{11} protons per bunch resulting in a design luminosity of $10^{34}\,\text{cm}^{-2}\text{s}^{-1}$

ATLAS Detector

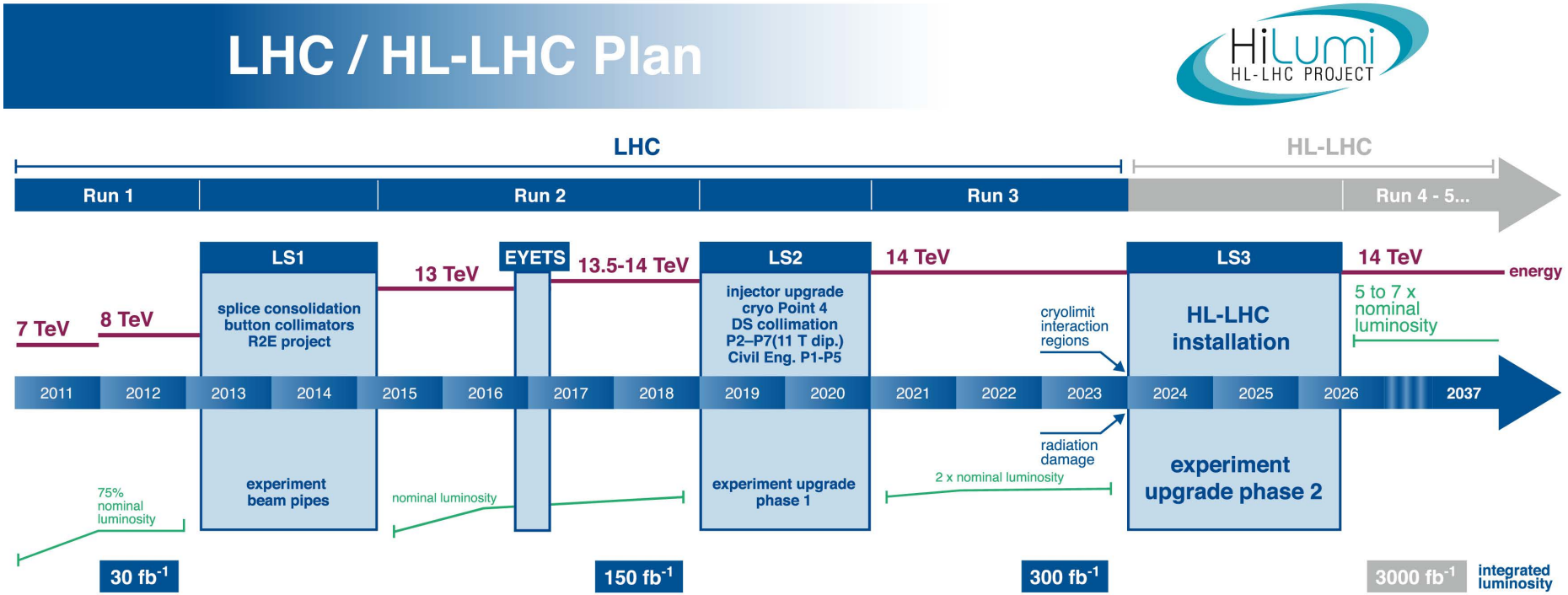


ATLAS Liquid Argon Calorimeter



- Sampling calorimeter (absorber: Pb, Cu, W; active: LAr)
- 182 468 detector cells arranged in layers

HL-LHC Upgrade Plans

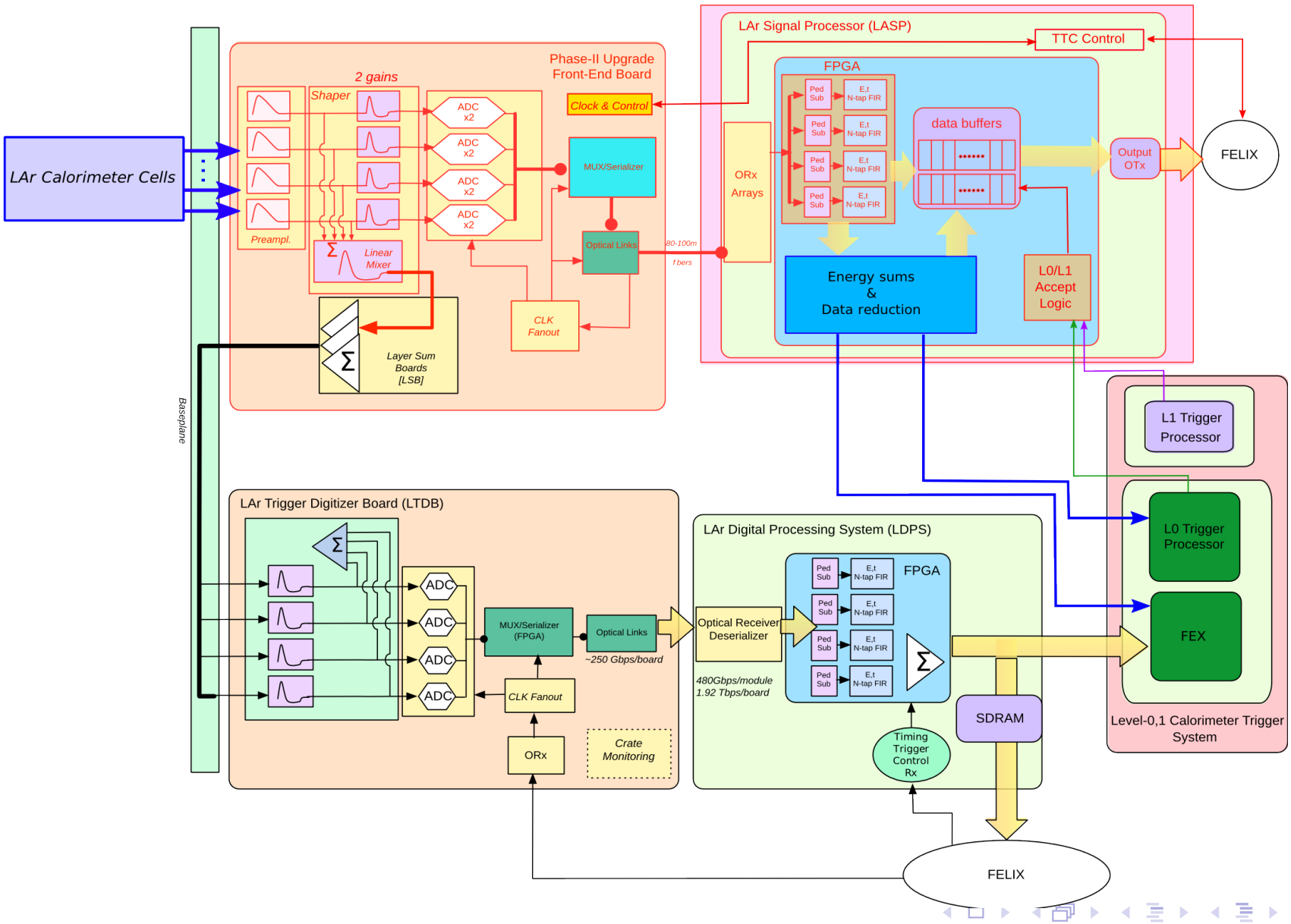


- Right now, the mean number of p-p collisions per bunch crossing is 20
- After the phase-2 upgrade (2024–26), up to 200 expected

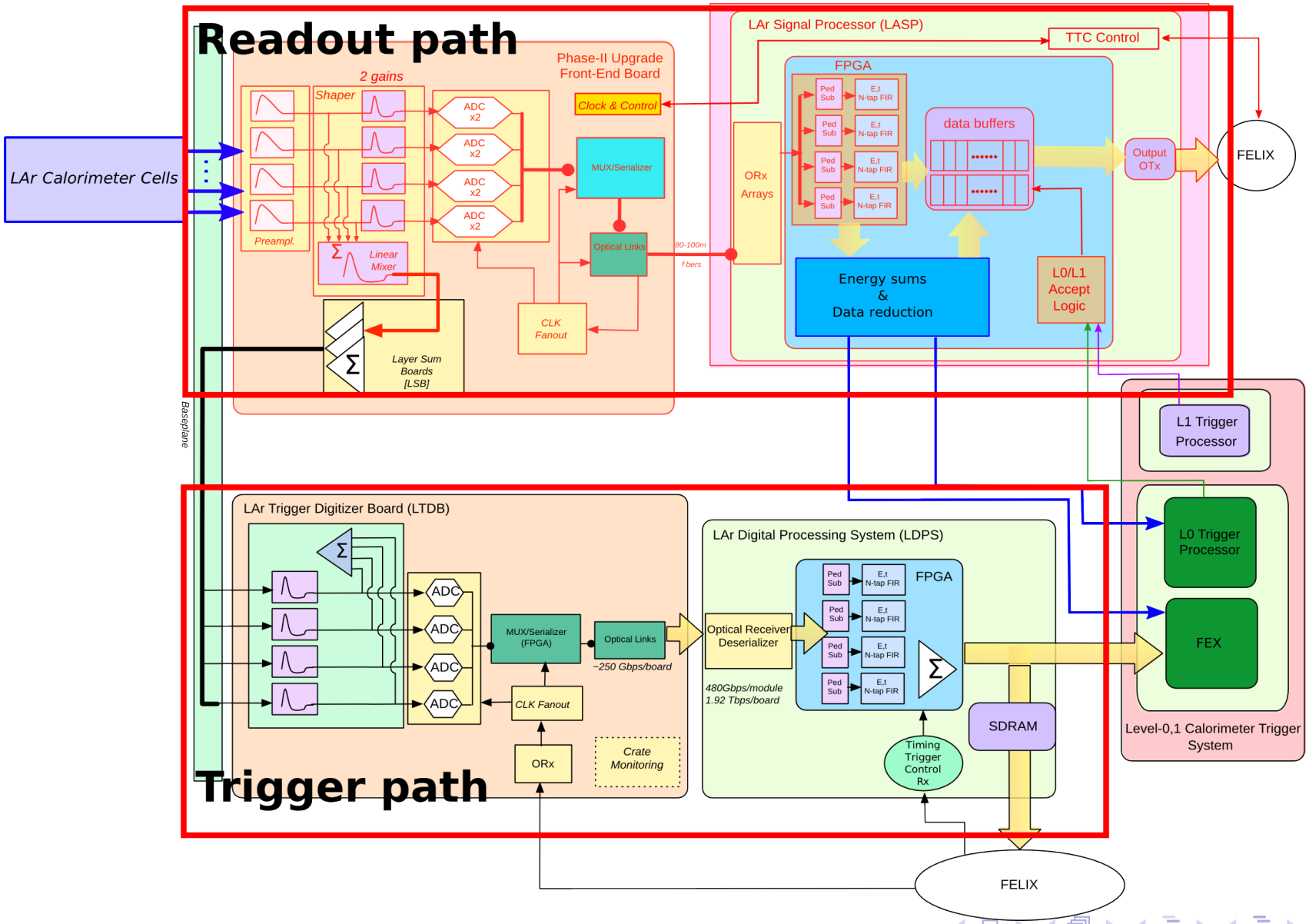
Performance Requirements on the Readout Electronics

- Currently installed readout is not ready for HL-LHC
- Large number of pile-up events will challenge the trigger system
  - Hardware trigger rate up to 1 MHz
  - 60 µs data buffering
  - Currently installed front-end electronics cannot provide that
- All 1524 front-end boards and the back-end electronics need to be replaced

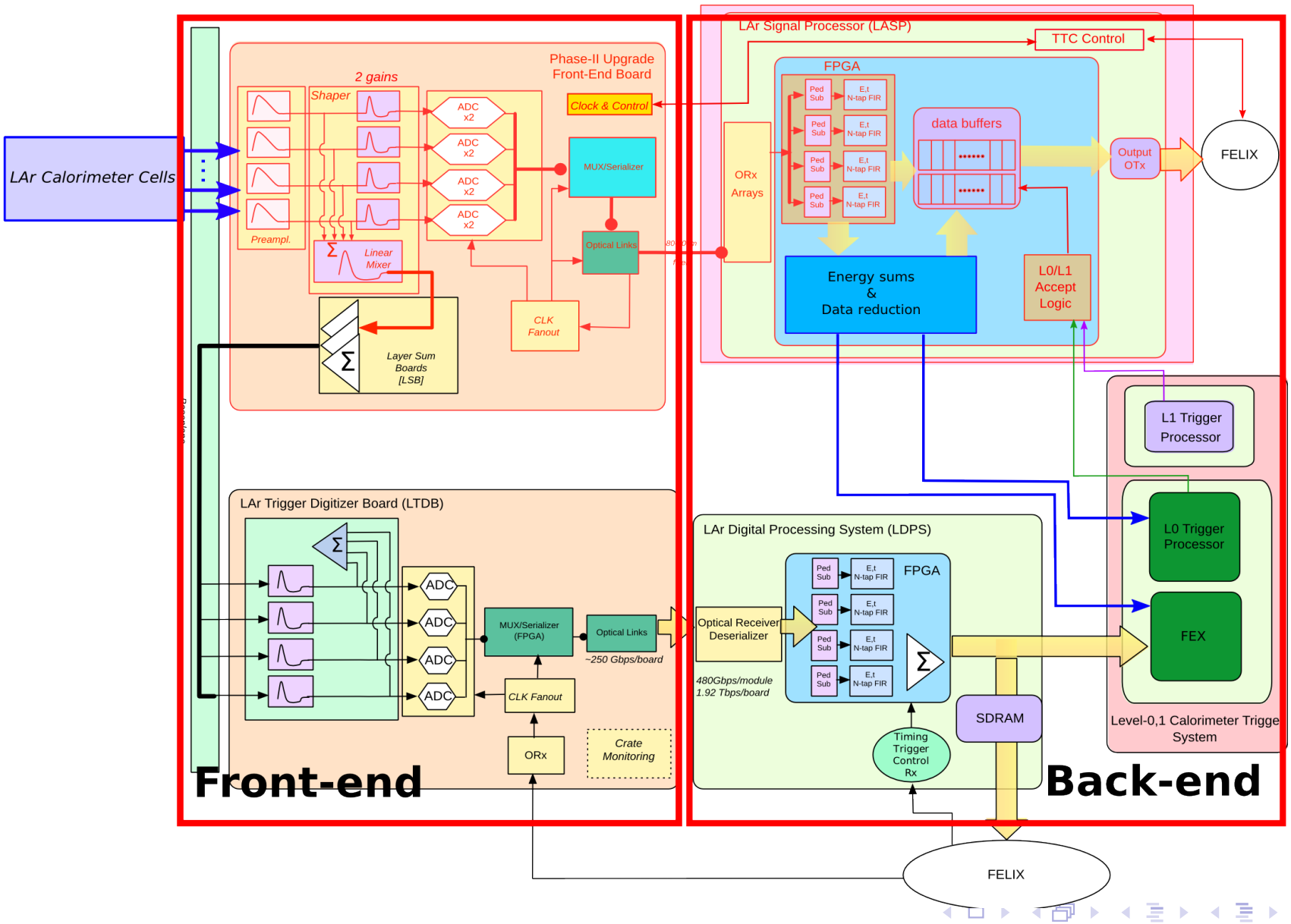
Upgrade of Readout Electronics



Upgrade of Readout Electronics

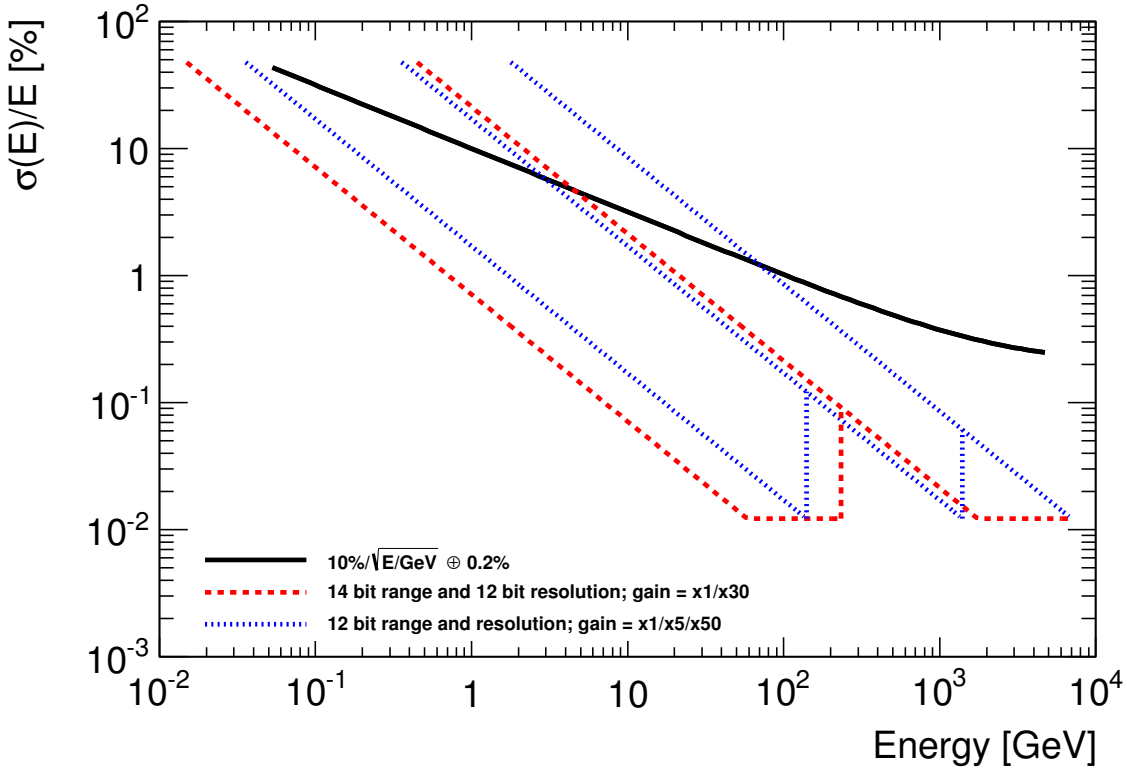


Upgrade of Readout Electronics



Specifications for the Front-end Electronics

- Preamplifiers have a finite dynamic range [30 MeV-4 GeV]
- Lineary of 0.1 % for energies up to 10 % of the dynamic range required
- Noise level below intrinsic calorimeter resolution
- Either two gains with 14-bit ADCs or three with 12-bit ADCs



Preamplifier & shaper

- Preamplifier and shaper will be implemented in a single ASIC
- Low noise required
- Low power required
- Two R&Ds paths on-going:
  - 65 nm CMOS, test chips submitted April 2017
  - 130 nm CMOS, tests chips submitted September 2016

- The 65 nm CMOS is a fully differential preamplifier

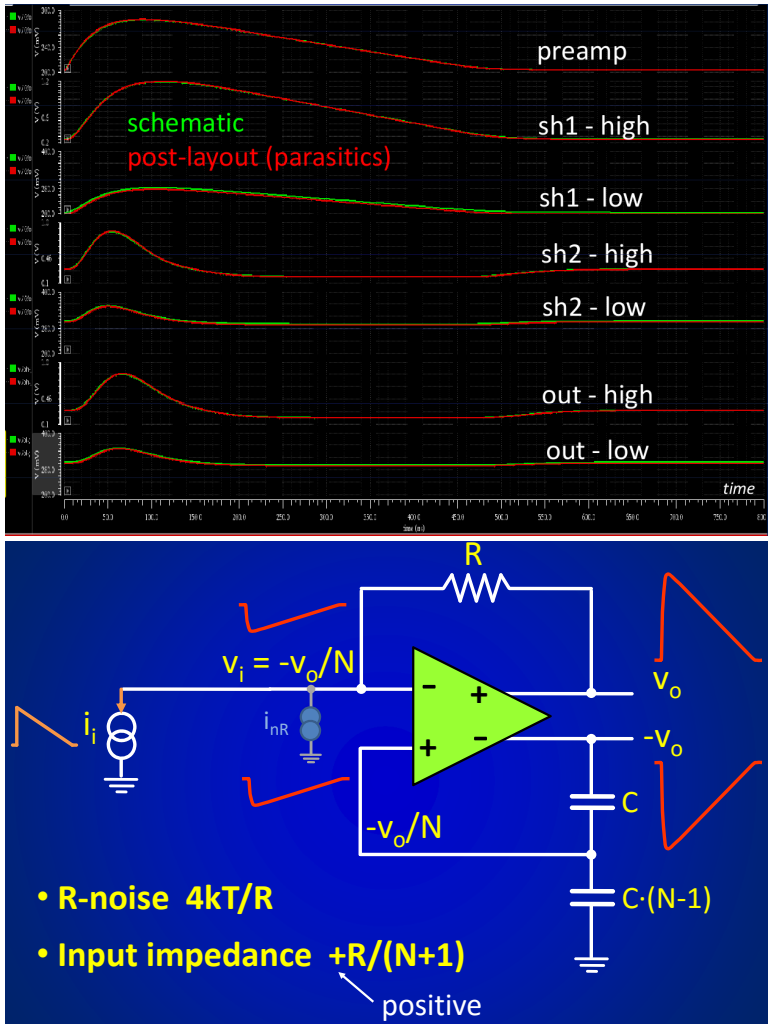
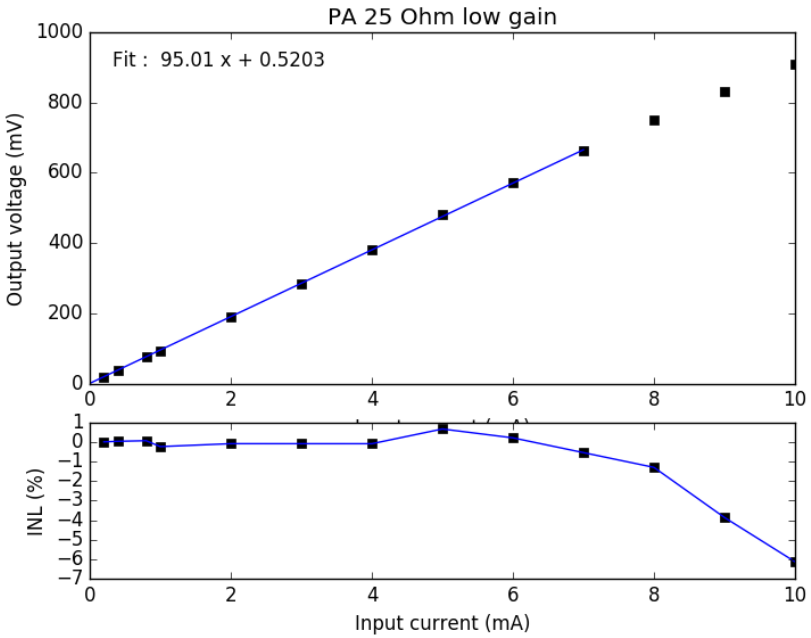
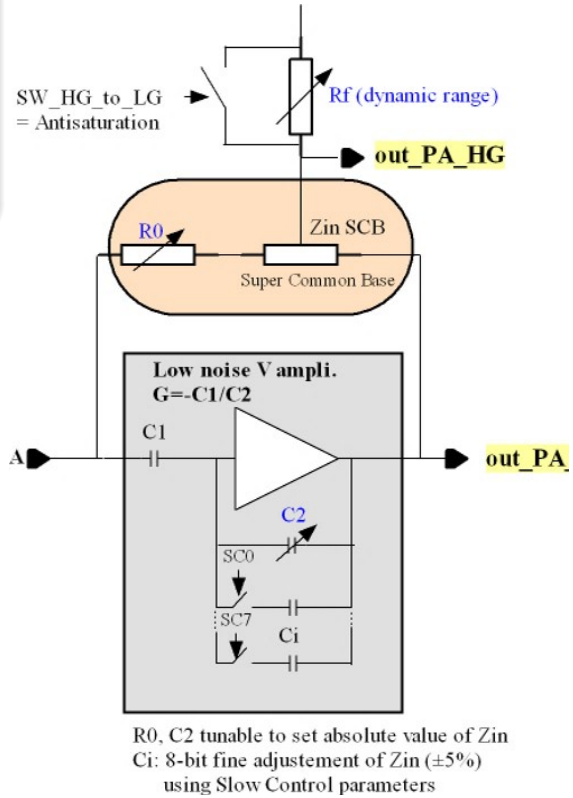


Figure: Post-layout simulations and architecture view of the 65 nm ASIC

Preamplifier & shaper: 130 nm Prototype

- New electronically cooled preamp design
- Linearity $\sim 0.1\,\%$, within $1\,\%$ up to $7\,\mathrm{mA}$
- In general, good agreement with simulations, except noise
- Issue understood, new prototype in 2017

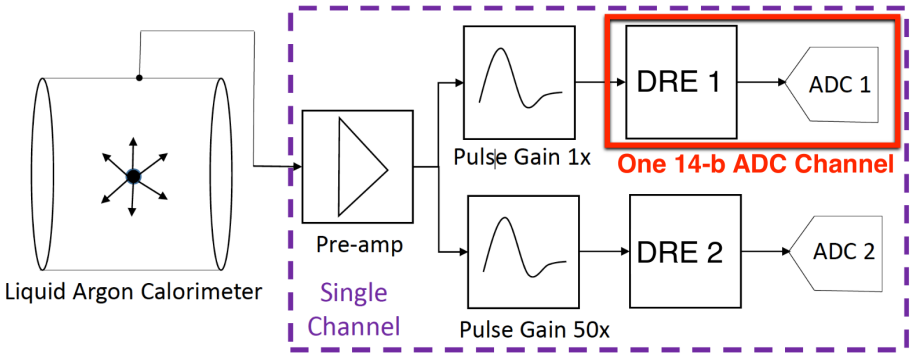


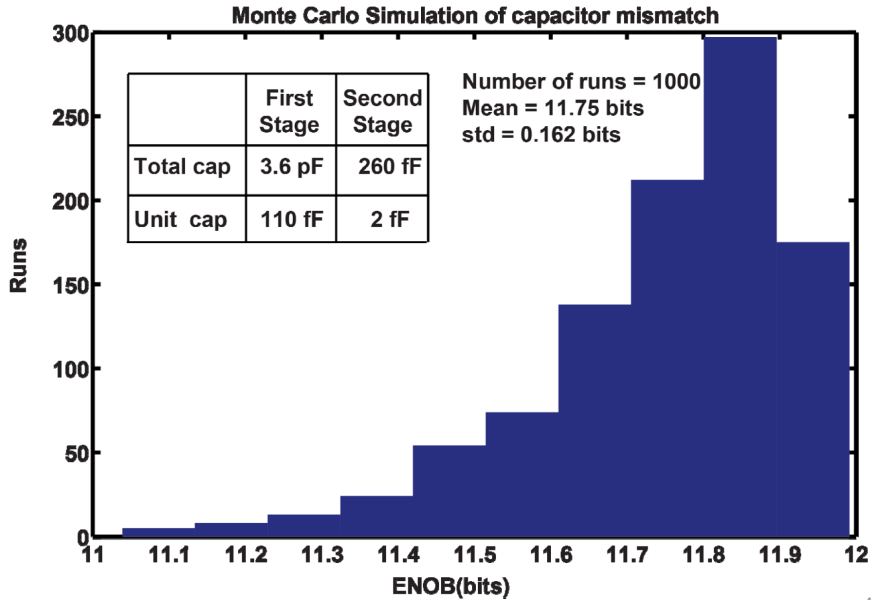


R0, C2 tunable to set absolute value of Zin
Ci: 8-bit fine adjustement of Zin (±5%)
using Slow Control parameters

Analog-to-digital Converter

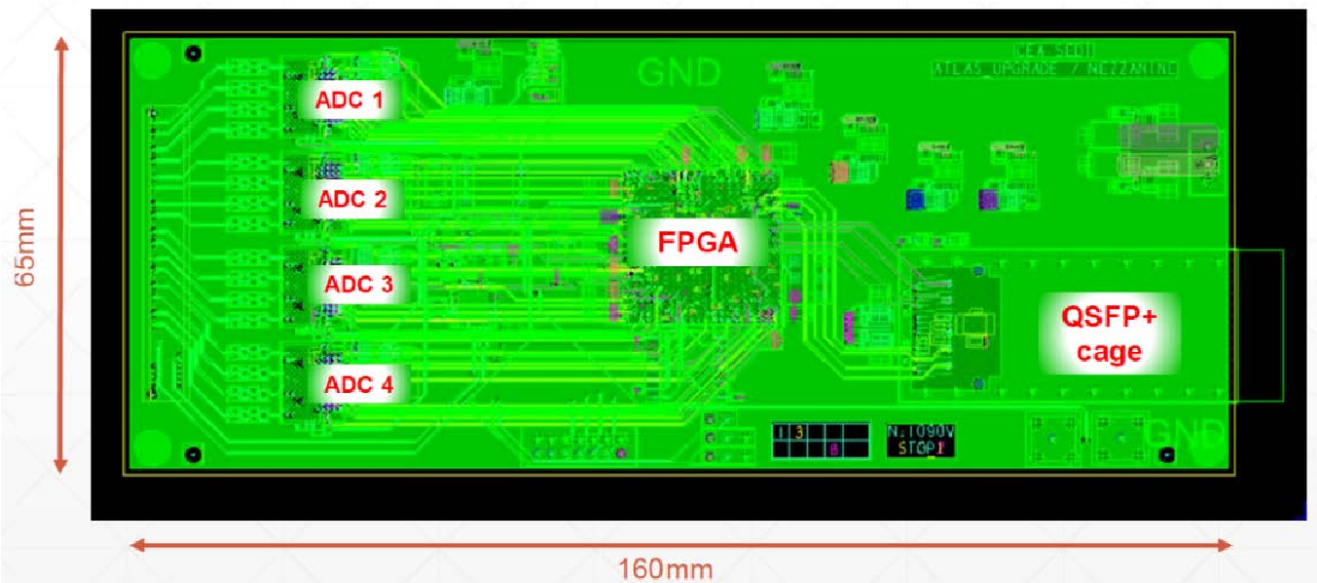
- Commercial and custom solutions
- ADC needs to be interfaced to CERN lpGBT serializer
- Custom design in 65 nm of a 14-bit ADC:
  - 12-bit Successive Approximation Register (SAR) and Dynamic Range Enhancer (DRE)





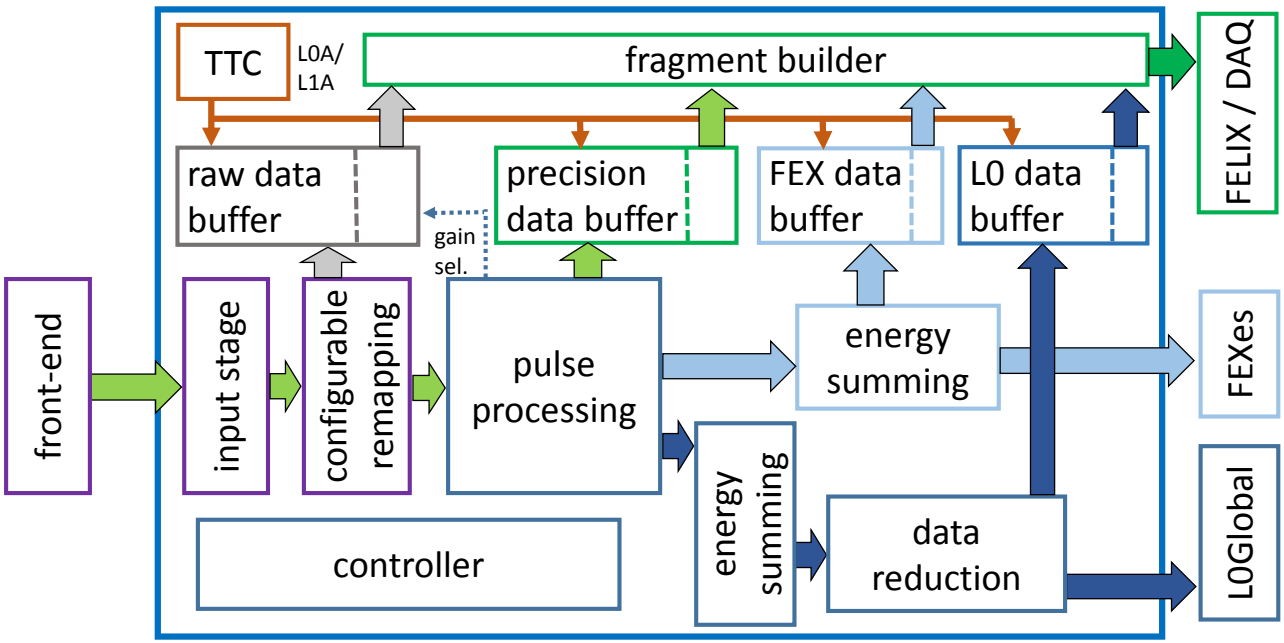
Analog-to-digital Converter

- Commercial off-the-shelf (COTS) ADCs:
  - Twenty 14-bit and seven 16-bit ADCs reviewed
  - 16-bit candidate ADCs identified (based on performance and cost)
  - Irradiation tests planned for 2017



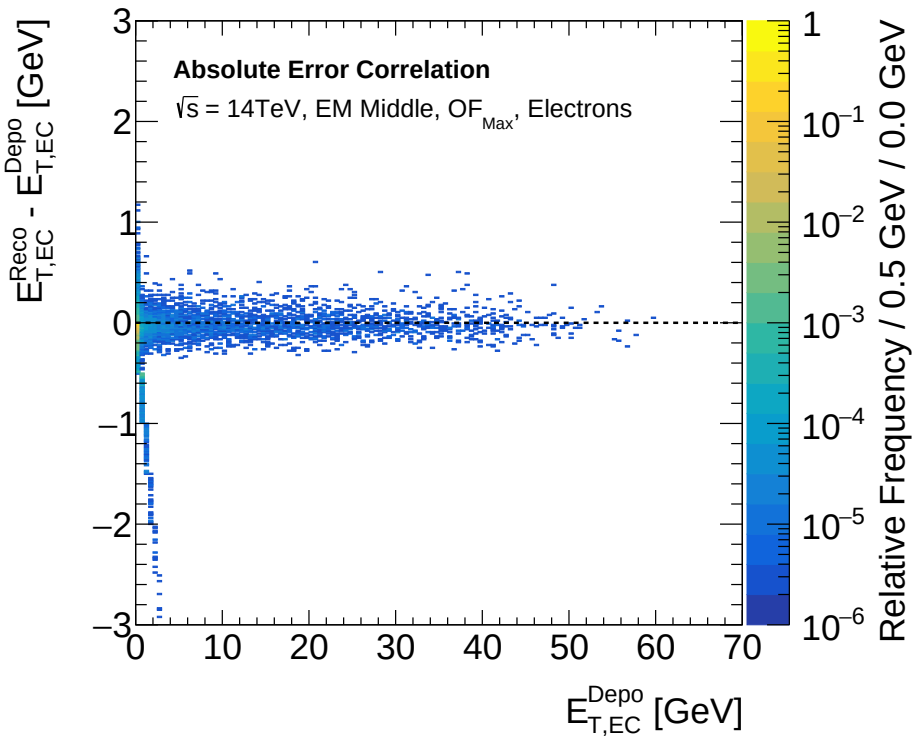
Back-end Electronics

- About 35 000 optical links from the front-end
- Input data rate of 275 Tbps
- About 400 high-performance FPGAs are needed



ATLAS Readout Electronics Upgrade Simulation

- Optimization of the readout chain with AREUS
- Comparison of e.g. deposited and reconstructed energies



Summary

- Front-end and back-end electronics need to be replaced due to higher pile-up
- Investigating different architectures for the preamplifier & shaper, test chips already submitted
- Studies of custom and commercial ADC designs
- Simulation studies for the readout electronics on-going

Backup

Radiation tolerance requirements for the front-end electronics

Table 5: Radiation tolerance requirements for the LAr front-end electronics for operation at HL-LHC for a total luminosity of 4000 fb^{-1}, including safety factors given in brackets.

	TID (kGy)		NIEL (n_{eq}/cm^2)		SEE (h/cm^2)	
ASIC	1.00	(2.25)	2.7×10^{13}	(2)	5.1×10^{12}	(2)
COTS (multiple lots)	13.2	(30)	10.9×10^{13}	(8)	2.0×10^{13}	(8)
COTS (single-lot)	3.3	(7.5)	2.7×10^{13}	(2)	5.1×10^{12}	(2)
LVPS (barrel and endcap)	0.77	(30)	12.3×10^{12}	(8)	3.2×10^{12}	(8)
HEC LVPS	0.23	(2.25)	6.3×10^{12}	(2)	3.6×10^{11}	(2)

Backup

AREUS