

Belle-II Silicon Vertex Detector

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The Belle II experiment at the SuperKEKB collider in Japan will operate at an unprecedented luminosity of $8 \times 10^{35} \text{ cm}^{-2} \text{ s}^{-1}$, about 40 times larger than its predecessor, Belle. Its vertex detector is composed on two-layer DEPFET pixel detector (PXD) and four layers double-sided silicon microstrip detector (SVD). To achieve a precise decay-vertex position determination and excellent low-momentum tracking under a harsh background condition and high trigger rate of 10 kHz, the SVD employs several innovative techniques. In order to minimise the parasitic capacitance in the signal path, 1748 APV25 ASIC chips, which read out signal from 224k strip channels, are directly mounted on the modules with the novel Origami concept. The analog signal from APV25 are digitised by a flash ADC system, and sent to the central DAQ as well as to online tracking system based on SVD hits to provide region of interests to the PXD for reducing the latter's data size to achieve the required bandwidth and data storage space. Furthermore, the state-of-the-art dual phase CO₂ cooling solution has been chosen for a combined thermal management of the PXD and SVD system. In this talk, we present the key design principles, module construction and integration status of the Belle II SVD.

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