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Development of Radiation-Hard ASICs for the ATLAS Phase-1 Liquid Argon Calorimeter Readout Electronics Upgrade

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The new trigger readout electronics system for ATLAS Liquid Argon (LAr) Calorimeter aims to improve granularity of the calorimeter information for the L1 trigger, essential for physics research goals after the phase-1 upgrade. The major R&D activities for front-end readout electronics upgrade include designing a new radiation-hard ADC and a data multiplexing and serialization ASIC to send the data off-detector via optical links.
The NevisADC is a radiation-hard four-channel 12-bit 40 MS/s pipeline ADC, which consists of four 1.5-bit Multiplying Digital-to-Analog Converters, with nominal 12-bit resolution, followed by an 8-bit Successive-Approximation-Register analog-to-digital converter to reach an optimization on performance and power consumption. The LArTDS ASIC multiplexes 16 channels of ADC data, then scrambles and serializes the data for transmission over two optical links each with a data transfer rate of 4.8 Gbps.
The custom design chips, fabricated in the GF 130 nm CMOS 8RF process, are extensively evaluated and tested. The NevisADC achieves an ENOB of 11 at 40 MS/s target sampling rate, with a latency of 112.5 ns while consuming 45 mW/channel and exhibits no performance degradation after irradiation. The LArTDS has passed the entire design function test with test pattern data and real ADC data. A 48-hours long term stability test shows the bit error rate is bellow 1.2x10ˆ-15 for both high speed serial channels. The ASIC chips architectures and detailed performance results will be presented.

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