The Global Control Unit for the JUNO front-end electronics

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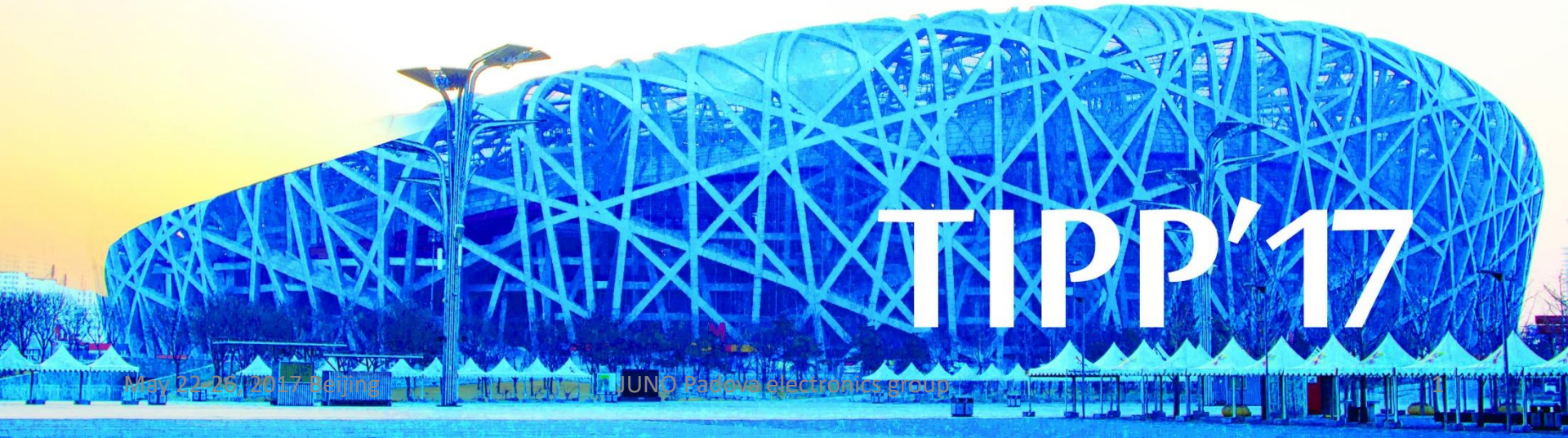
On behalf of

JUNO Padova Electronics Group & JUNO Collaboration



Outline

- The JUNO experiment.
- An overview of the electronics readout architecture.
- An intelligent PMT.
- Electronics requirements.
- The Global Control Unit (GCU) architecture and main features.
- GCU design and prototyping.
- Electronics integration and first data acquisition.
- Conclusions.

The JUNO Experiment

JUNO is a multipurpose neutrino experiment designed to determine neutrino mass hierarchy and precisely measure oscillation parameters by detecting reactor neutrinos from the Yangjiang and Taishan Nuclear Power Plants, observe supernova neutrinos, study the atmospheric and solar neutrinos.

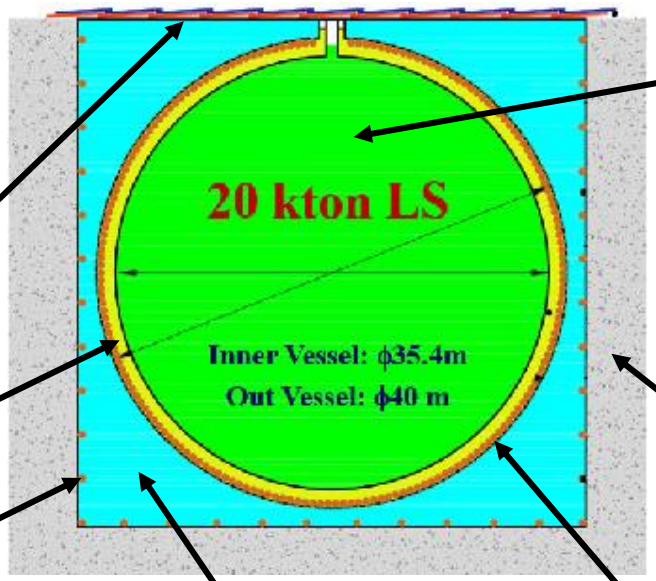
The Central Detector

The energy of incident neutrinos and the interaction vertex can be reconstructed based on the charge and time information coming from the PMTs. Energy resolution 3% @ 1MeV.

Top Tracking: muon tracking system.

Buffer inactive liquid: LAB or mineral oil. 4kton

VETO Photomultipliers: muons, cosmogenic and neutron background rejection.

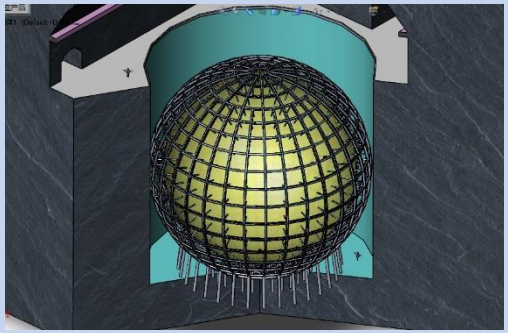


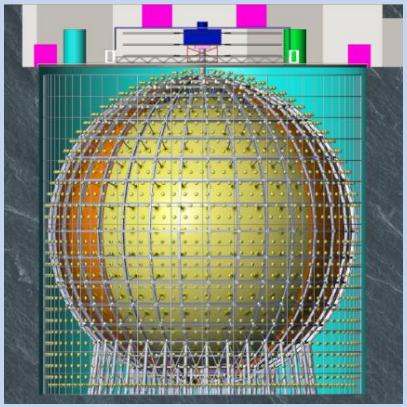
Acrylic sphere holds 20kton of scintillator liquid.

Rocks

The detector is located deep into a hill. The overburden will be 700m rocks.

How it will look like:





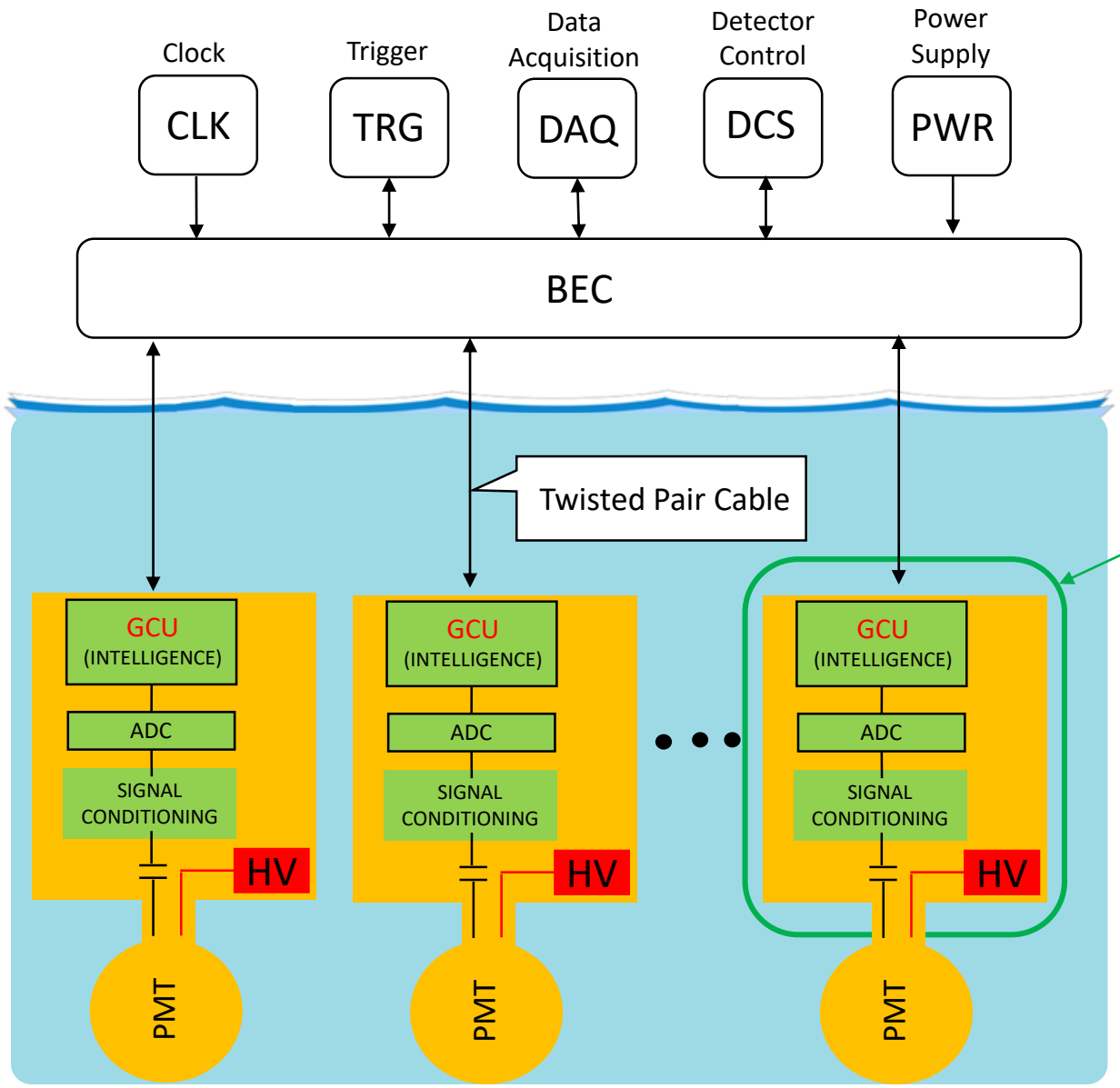
Water Pool.

- Heat dissipation
- Water Cherenkov detector
- ~21°C

Photomultipliers

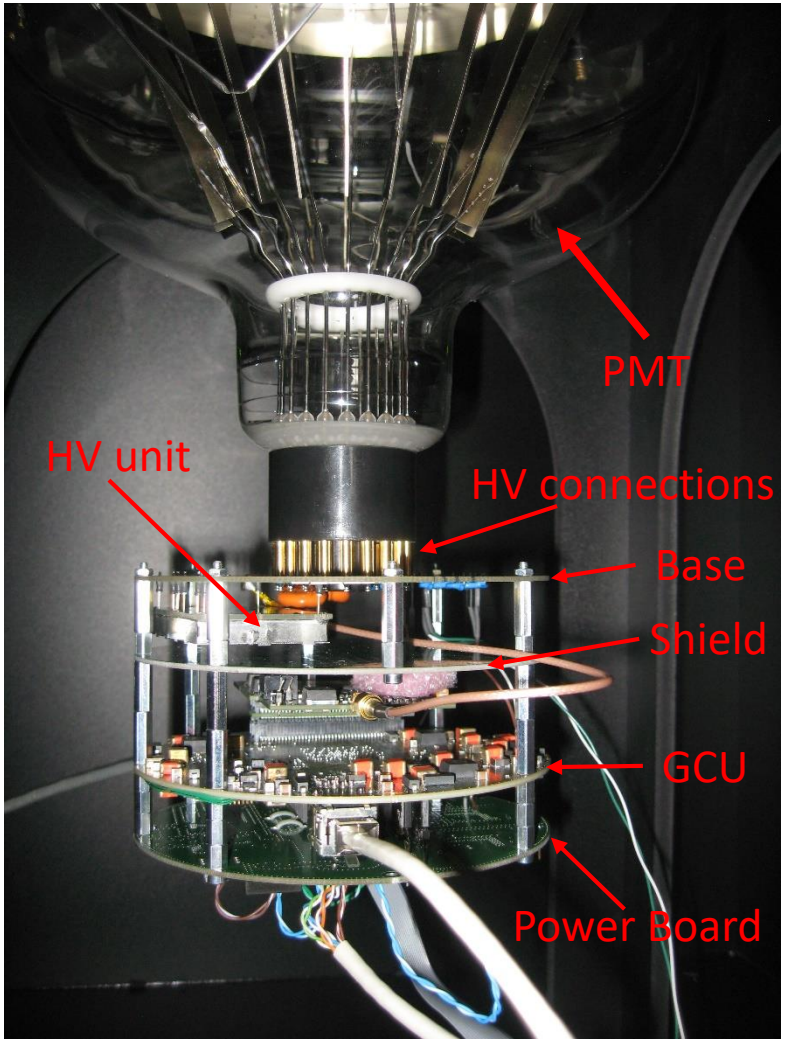
~20000 PMTs
Optical coverage ~ 80%

Electronics BX Scheme

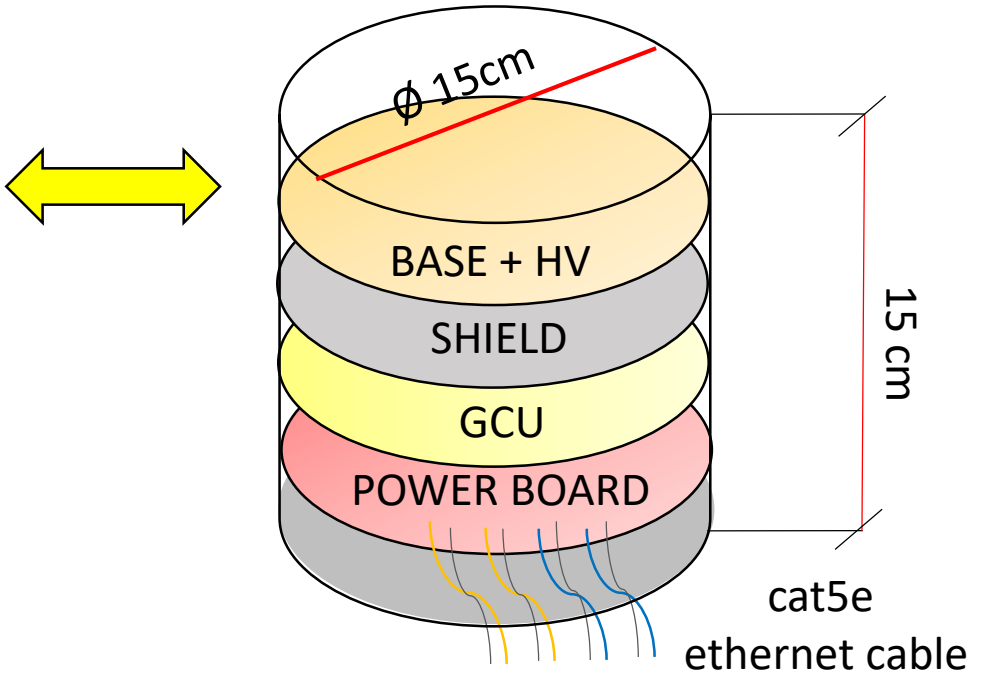


The JUNO collaboration foresees a basic readout structure in which PMT readout, trigger primitive generation, fragment buffering, baseline control, selective data readout and HV interface take place in a watertight box sealed together with the PMT. Each readout electronics box communicates with the external world via 4 pairs of copper cable CAT5e with an estimated length of ~ 100m.

An Intelligent PMT



- Best performance in terms of SNR.
- Onboard system test and calibration.
- Lower the data rate on the 100m cable.
- Modularity and flexibility; complex tasks and programmable digital signal pre-processing can be done locally.
- Facilitate the local data storage in case of supernova.
- Minimize the number and cost of waterproof connectors and cables to outside water world.



Underwater Electronics Guidelines 1

Physics/Installation Requirements	Electronics Requirements
Performances: • *High resolution*: noise level should be below 0.1pe for single photoelectron detection. • *Wide input range*: ➢ Signal range: 1 – 100pe with a charge resolution growing linearly from 0.1 to 1pe. ➢ Background range: 100 – 4000pe with a charge resolution of 1pe. • Bandwidth: 400MHz. The rise time of a single p.e. is about 2.5ns.	• Analog Digital Unit: two ASICs under development: ➢ Vulcan Chip (Forschungszentrum Jülich Institute). ▪ 3 x 8 bit @ 1Gsps ▪ Overshoot compensation ➢ Tsinghua Chip (IHEP Beijing) ▪ 2 x 14 bit @ 1Gsps • Highly linear over a wide range and low noise receiver. • Optimal ground strategy. • Signal and power integrity and low jitter clock concerns. • Provide support for precise system calibration and synchronization, channels alignment. • Baseline correction (Vulcan or firmware).

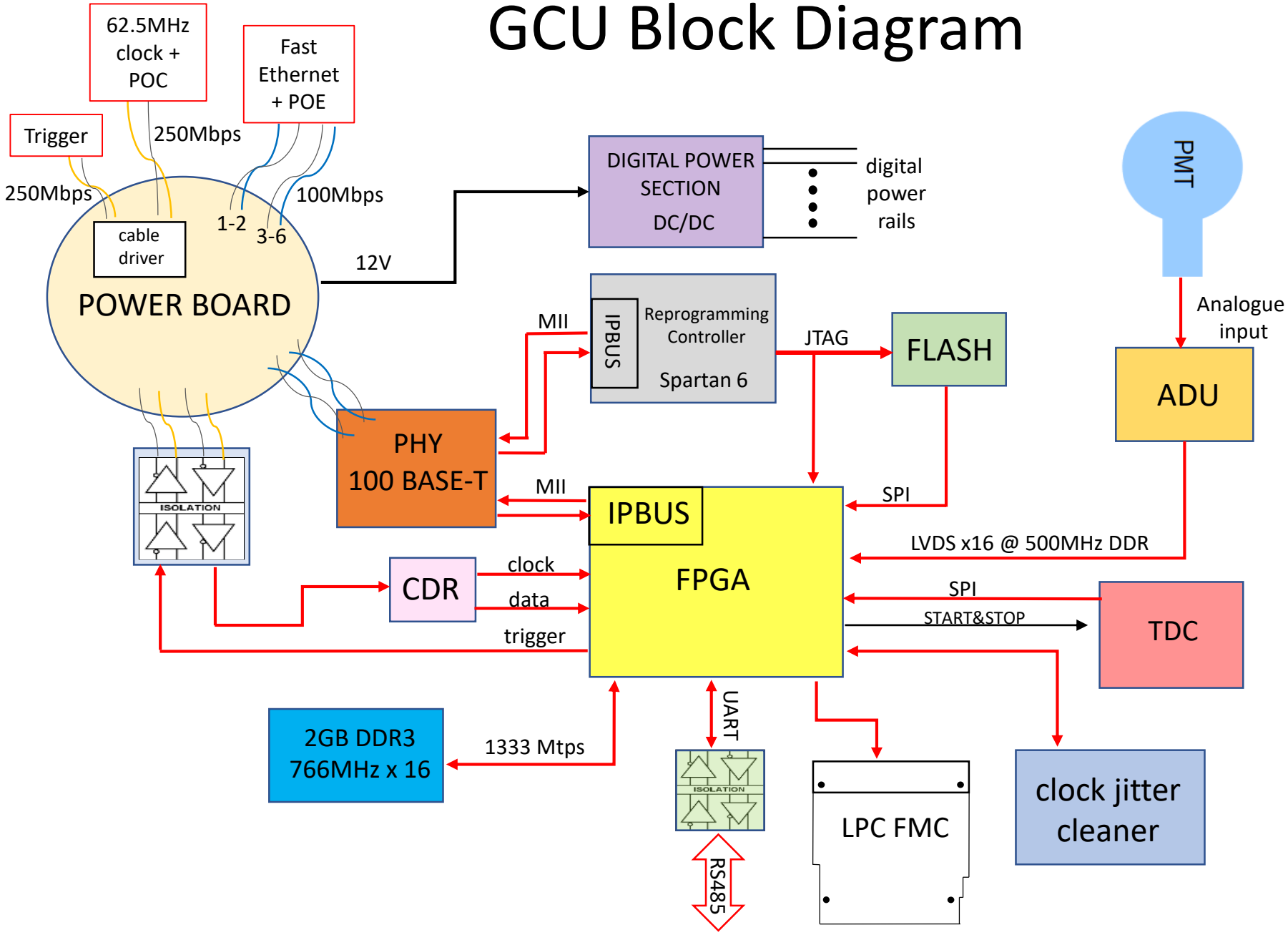
Underwater Electronics Guidelines 2

Physics/Installation Requirements	Electronics Requirements
Inaccessibility after installation	• Reliability. The goal is 1 % failures in 6 years: 0.5 % PMT 0.5 % underwater electronics • Remote FPGA reprogramming and debug tools.
Minimize the number of cables and waterproof connectors for each PMT	• Power, data readout, slow control, clock, trigger all rely in only one CAT5e connector.
Minimize the power consumption per channel. ➢ facilitate the heat dissipation from the PMT. ➢ best performances at lower temperature. ➢ Increase the reliability.	• Use very low power devices. • Efficient DC/DC conversions. • Minimize voltage drop & power losses in the cable. • Try to avoid the usage of DDR3 memory. • The FPGA should run only the strictly necessary algorithms.
Try to minimize the cost of the electronics of each channel.	• We are talking about ~20000 channels…

GCU Features

- GCU hosts the ADC ASIC; 1Gsps @ 14 bits.
- Readout the ADC input stream of 1Gsample/s (input bandwidth 14Gbps).
- Handle data packaging and buffering and long term storage of 1s of raw data in case of supernova.
- Generation of trigger primitives and local event storage waiting for trigger validation.
- Auto-trigger mode.
- Provide support for the global synchronization process. The system clock is recovered on board and the timing system must guarantee that all the 18000 local clocks are aligned with the global time within a system clock period (16ns).
- Provide remote slow control and system monitoring via Fast Ethernet.
- High voltage regulation via a serial interface (1500V to 3000V).
- System monitoring.
- Guarantee remote FPGA reconfiguration and recovery.

GCU Block Diagram



FPGA

Tradeoff between:
- Power Consumption
- Cost
- Performance
- Number of I/O available

XC7K160T-2LI
FFG676

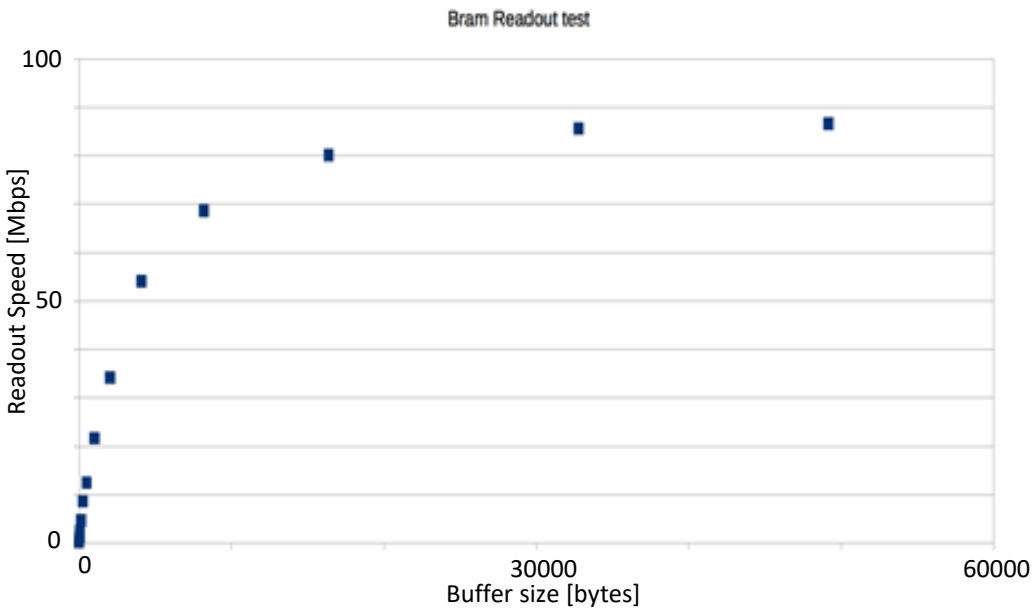
FFG676 package is compatible with three different devices of the Kintex-7 family:
1. **XC7K160T**
2. **XC7K325T**
3. **XC7K410T**

FPGA - only estimated power consumption:
- 4W best-case
- 8W worst-case

Power is strictly related to the algorithms that you foresee to run in the FPGA.

IPBUS Data Readout Test

- The raw data generated by the ADC is 16Gbps.
- In trigger validation mode we must be able to readout ~1KHz x 1000 x 16 = 16Mbps (well in the range of fast ethernet).
- L1 Cache inside the FPGA:
  Maximum trigger latency: 20us.
  Cache1 size = 16Gbps x 20us = 320kb.
- The available block RAM in the XC7K160T is 11700Kb.
- The DDR3 write bandwidth is ~766MHz x 2 x 16 x 85% (efficiency) = 20.84Gbps.
- In supernova mode (auto-trigger) ~1MHz x 300 x 16 = 4.8Gbps (well in the range of the DDR3).

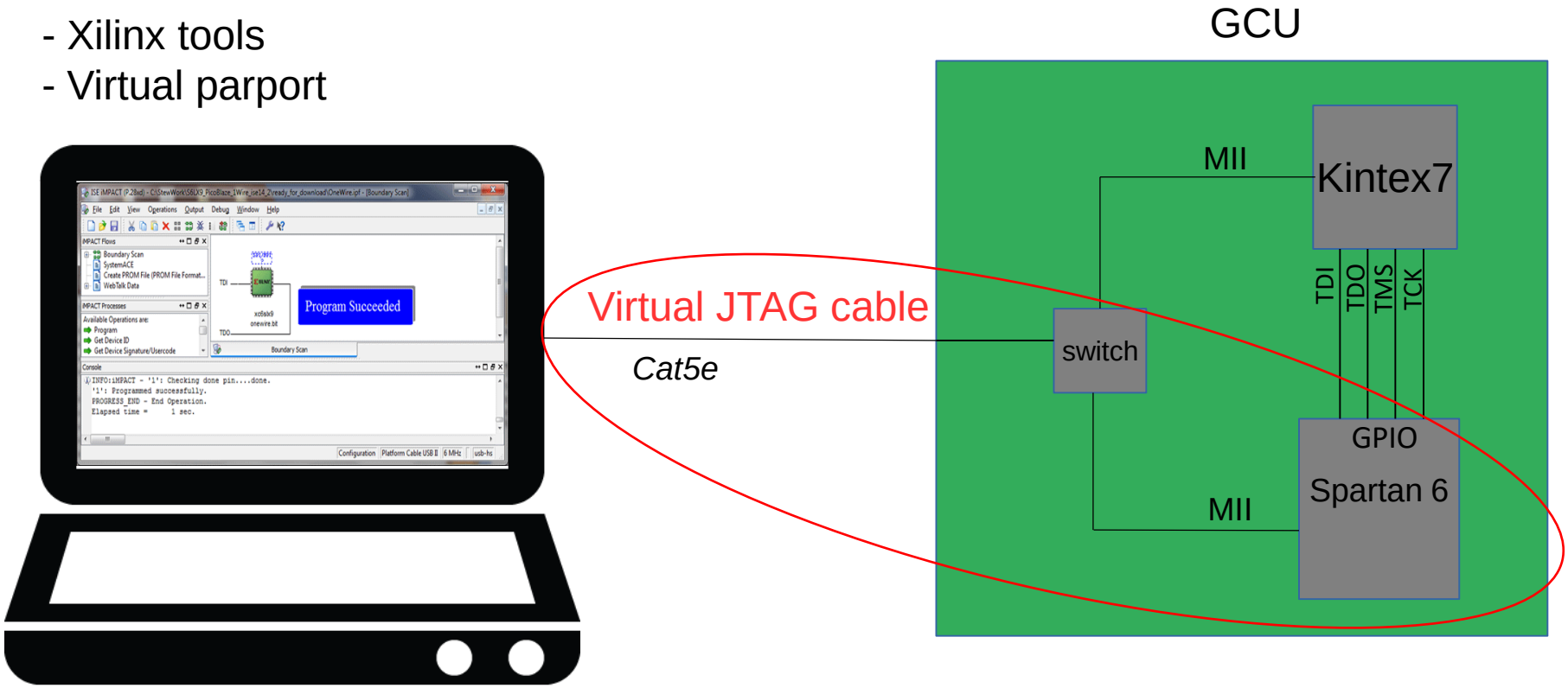


16Mbps << 90Mbps
320Kb << 11700Kb
4.8Gbps << 20.84Gbps

Without data compression algorithms!

Virtual JTAG over IPBus

- Xilinx tools
- Virtual parport



Configuration controller acts as a Xilinx remote cable.
Xilinx debug & programming tools (Impact, Chipscope, Vivado) are able to connect to a TCP port service named xilinx_xvc.

The PCB Design

	Subclass Name	Type
1		SURFACE
2		DIELECTRIC
3	TOP	CONDUCTOR
4		DIELECTRIC
5	L2GND	PLANE
6		DIELECTRIC
7	L3	CONDUCTOR
8		DIELECTRIC
9	L4PWR	PLANE
10		DIELECTRIC
11	L5GND	PLANE
12		DIELECTRIC
13	L6PWR	PLANE
14		DIELECTRIC
15		DIELECTRIC
16		DIELECTRIC
17	L7PWR	PLANE
18		DIELECTRIC
19	L8GND	PLANE
20		DIELECTRIC
21	L9PWR	PLANE
22		DIELECTRIC
23	L10	CONDUCTOR
24		DIELECTRIC
25	L11GND	PLANE
26		DIELECTRIC
27	BOTTOM	CONDUCTOR
28		DIELECTRIC
29		SURFACE

2

isola

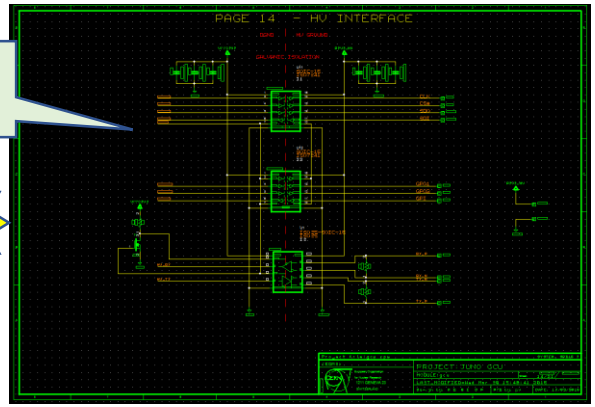
FR408HR

Tg190, Td 360

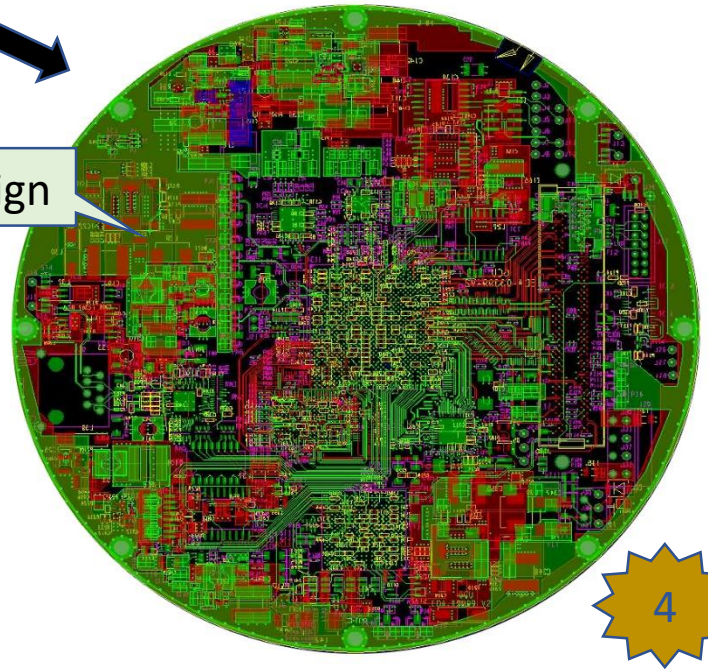
Dk 3.68, Df 0.0072

Allegro - Design Entry HDL

1



Allegro PCB Design



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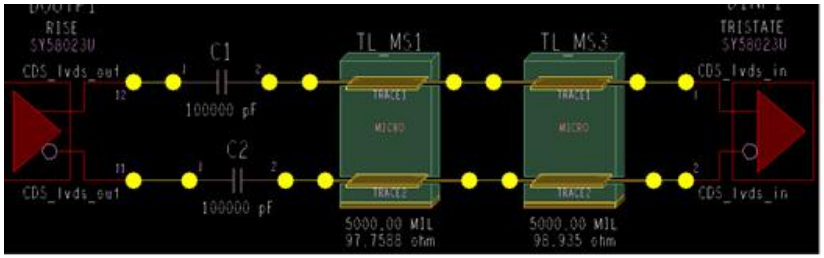
Pre-layout simulations



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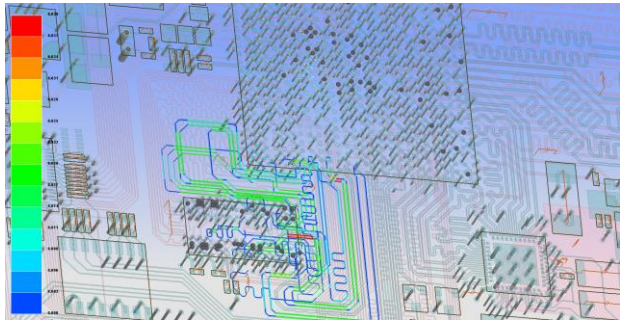
Cadence PCB Design environment version SPB16.6

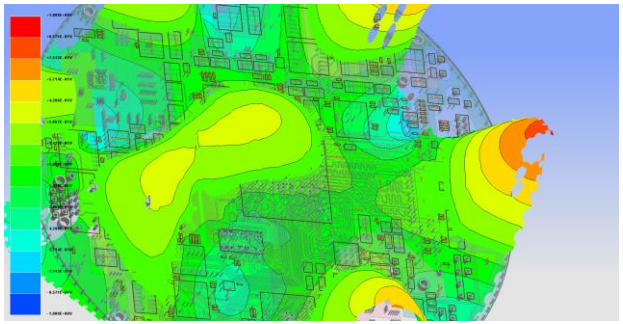
Post-Layout simulation



Signal integrity

ANSYS SiWave

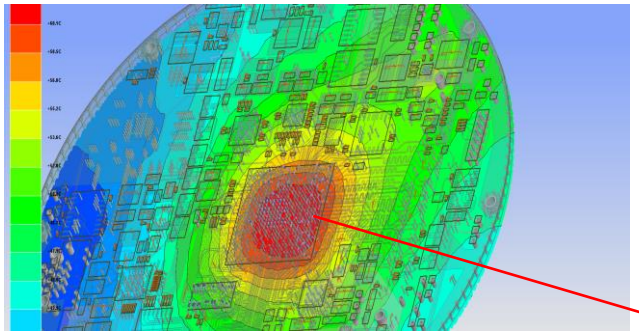
- Meet target impedances
- Crosstalk analysis
- Scattering Matices



(at 2.8 GHz on L9PWR - L11GND)

Power Integrity

- Meet target impedances
- SSN
- Planes Resonances

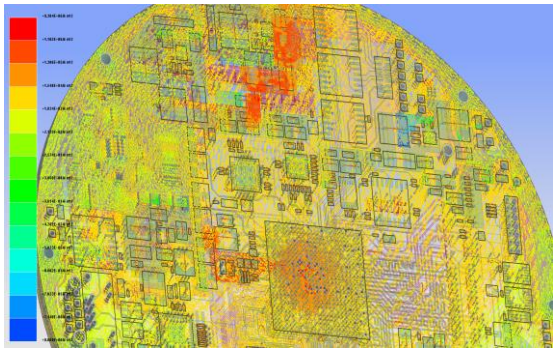


Thermal distribution

Thermal analysis

ANSYS ICEpack

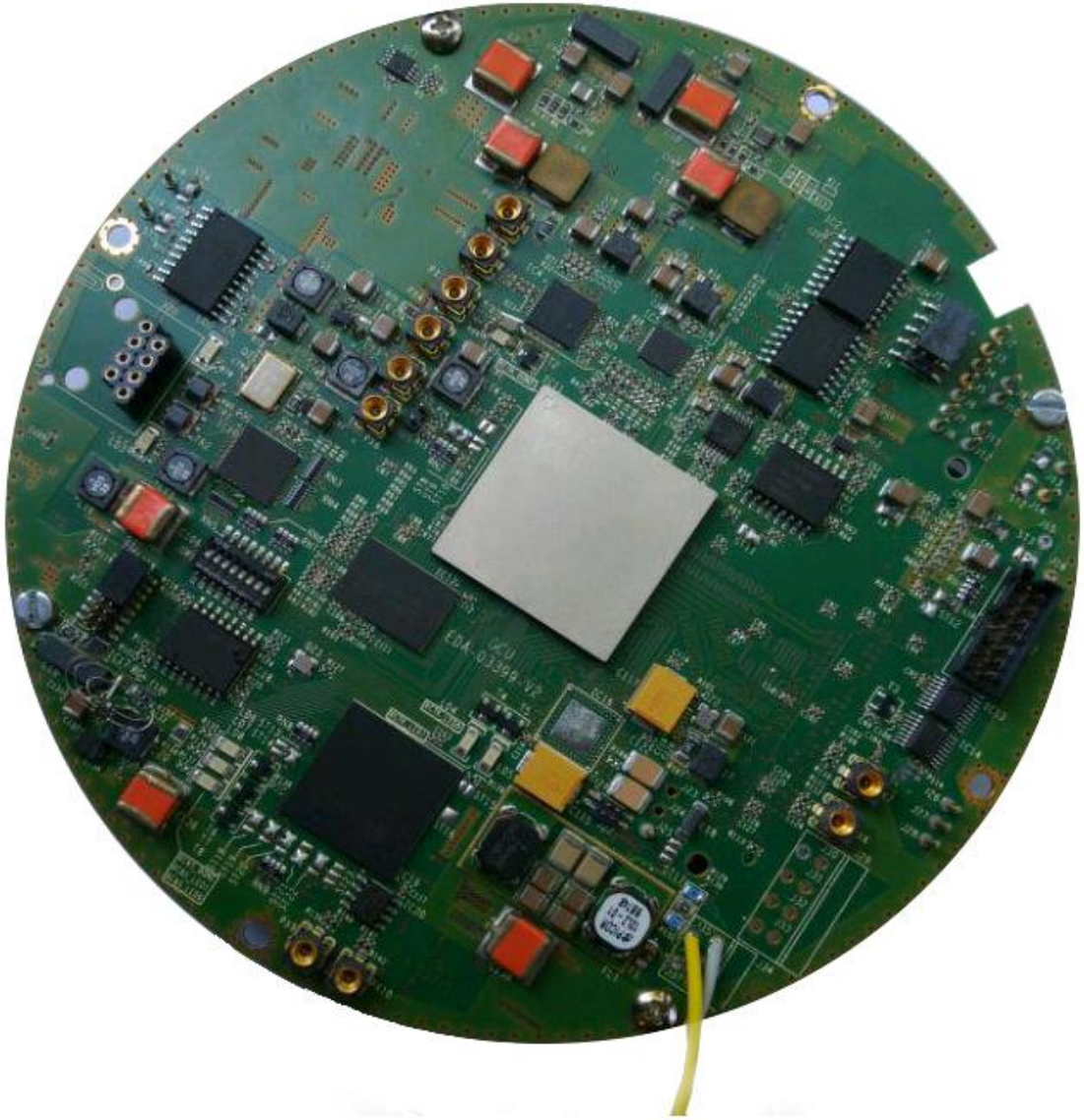
FPGA 60°C



Current density

Prototype V2

GCU measured power consumption: ~10.4W

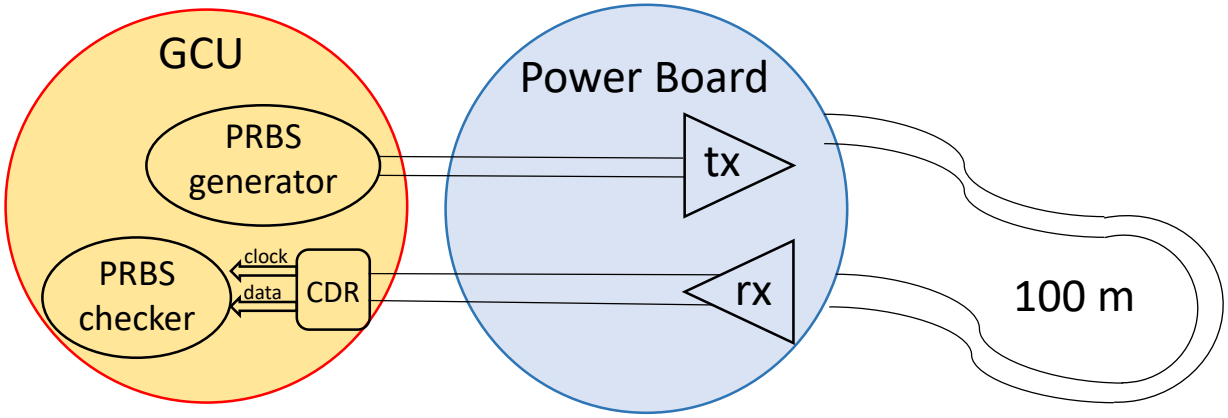


3 working prototypes:

- 1 at the present is in China for potting tests.
- 2 are in Padova to complete the hardware debug and for firmware developing.

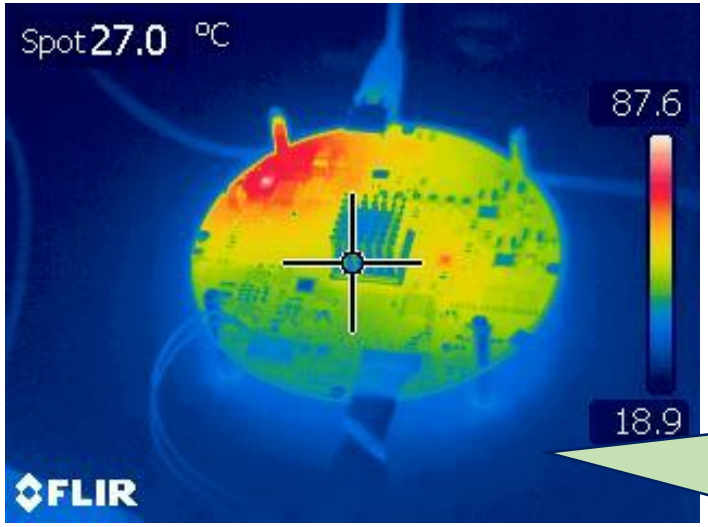
Debug and Performance Tests

Example of data integrity test on the synchronous links:



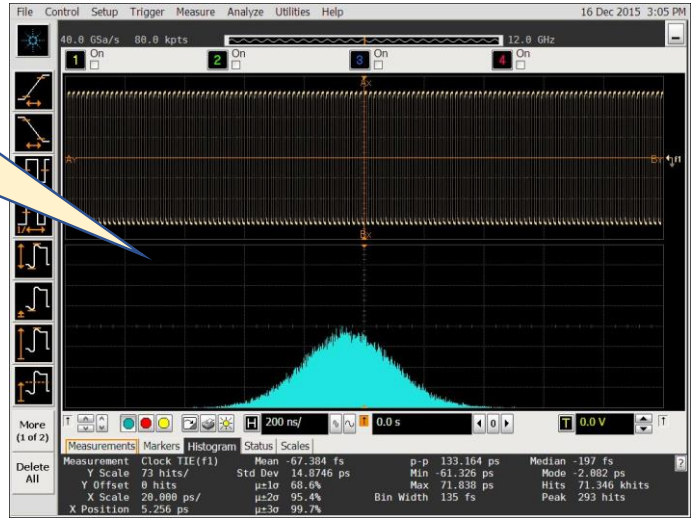
Xilinx xapp884 application note

Eye diagram 250 Mbps @ PRBS7
Data caught at the CDR input

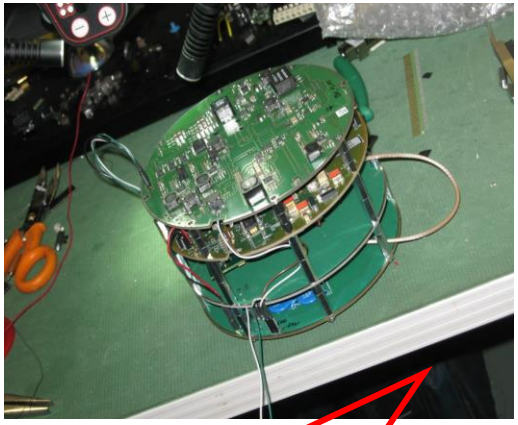


GCU prototype V1: thermocamera analysis: VCCO3V3 load switch to be replaced.

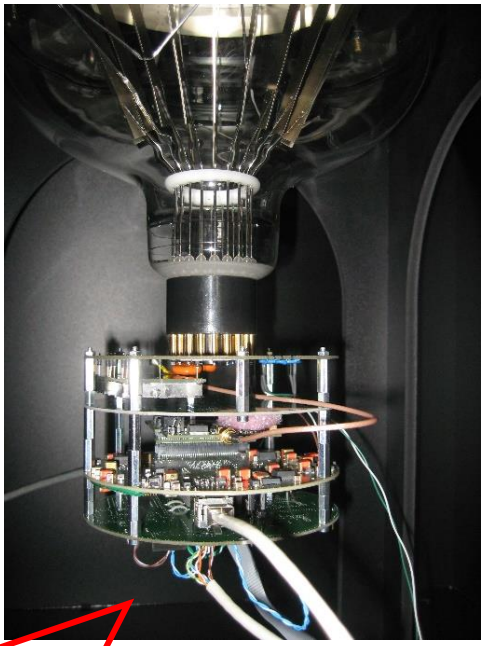
Jitter measurement; 62.5MHz system clock std dev = 14.87ps



Electronics Integration and First Data ReadOut



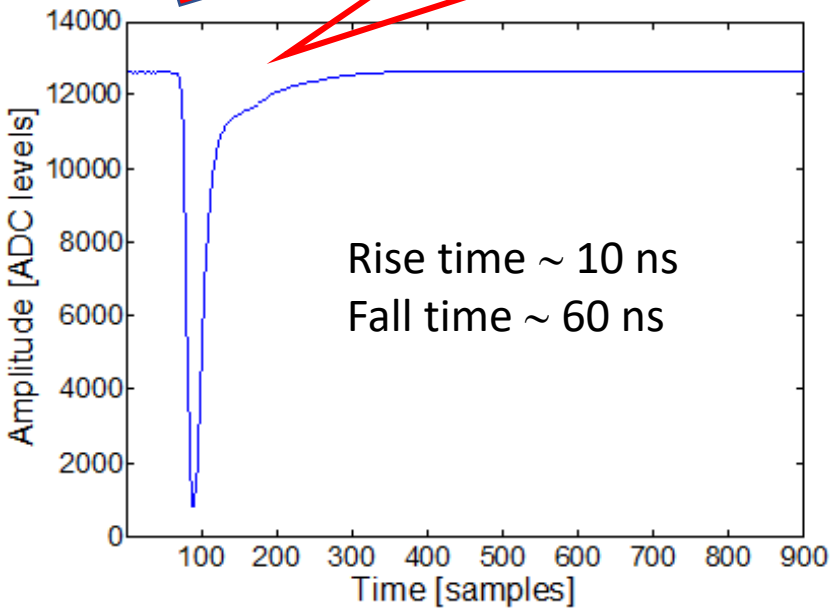
Mockup assembled on the desk and communication test between boards.



- PMT & electronics assembled.
- The light source was a LED.
- GCU in auto-trigger mode.
- Tsinghua ADC on LPC FMC mezzanine.

Padova 17th March 2017.
The aim was to test/qualify the first full-chain electronics and validate the intensive work done so far to develop the current electronics scheme.

Data readout via IPBUS. Python script.



Conclusions

- The GCU meets all the functional requirements.
- The integration tests and first data readout have been successfully performed.
- The mass production and test will be a huge challenge.
- The current readout scheme is a feasible solution but there are still difficulties and improvement to be done to meet all the underwater electronics guidelines:
  - Installation with a 100m cable without connector will be difficult and risky.
  - It would be better to split the potting and the electronics development. With the current scheme the electronics must be ready for the mass production before the potting starts (beginning 2019). Shorten R&D time.
  - Power consumption per channel is too high (17.4W measured in Padova). In turn this calls for high potting requirements and high cost of operation. To be improved.
  - Heat removal is key for good performances and long lasting operation.
  - Reliability. The overall readout electronics reliability is above 0.5%. To be improved.

The JUNO collaboration is evaluating new possible readout schemes. New architectures will be compared with the current scheme in term of performances, cost, power consumption, reliability, potting problems. The new proposals for electronics readout should take advantage of all the effort done so far since no schedule changes are admitted: the first run of the experiment is foreseen for 2020.

Thanks!

Questions