Recent Updates on Trigger and DAQ System of PandaX-II Experiment

Qinyu Wu

Shanghai Jiao Tong University

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Outline

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  - PandaX Experiment
- FPGA-based Trigger System
  - Motivation
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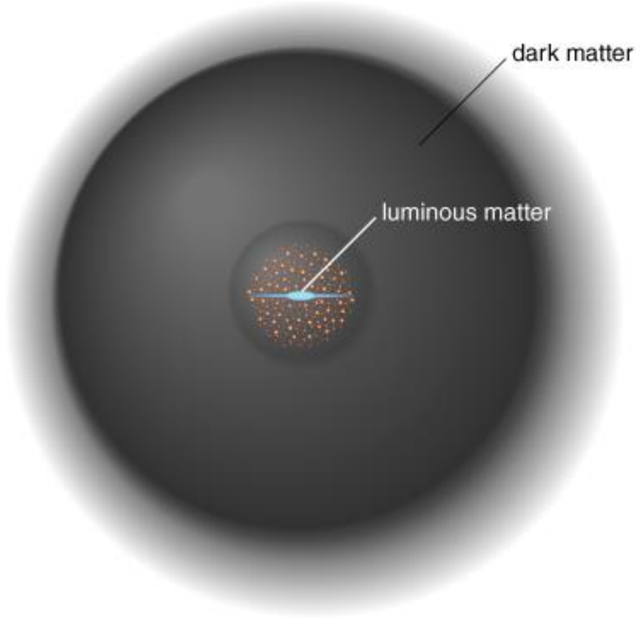
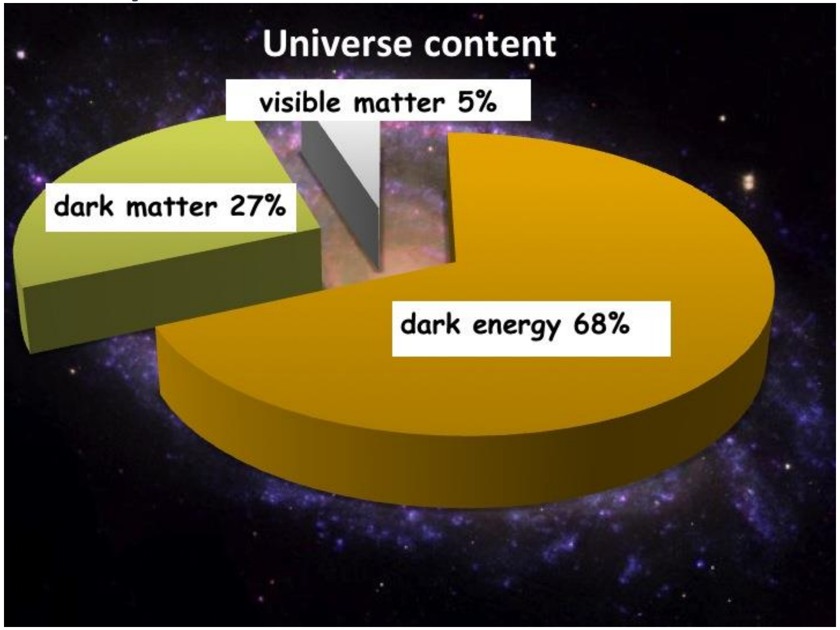
- Future: Multithread Readout
- Summary & Outlook

Dark Matter

- Important part of the universe.
  - Strong evidences from indirect detection of astrophysics.
  - About 27%. Much larger than visible matter.
- Dark Matter Direct Detection
  - Complementary with indirect detection and collider search
  - Xenon detectors leading sensitivity for WIMPs.



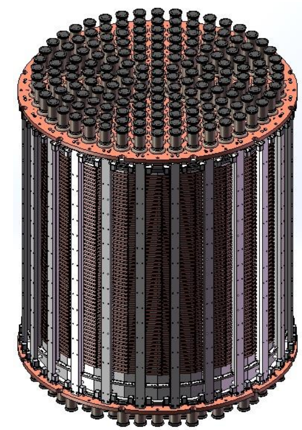


The PandaX Experiment

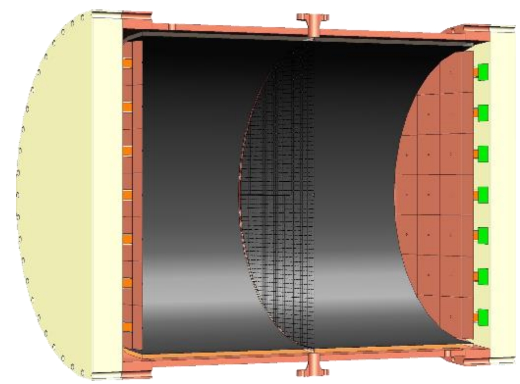
- PandaX = **Particle and Astrophysical Xenon Experiments**

PandaX-I: 120 kg DM experiment
2009-2014

PandaX-II: 500 kg DM experiment
2014-2018



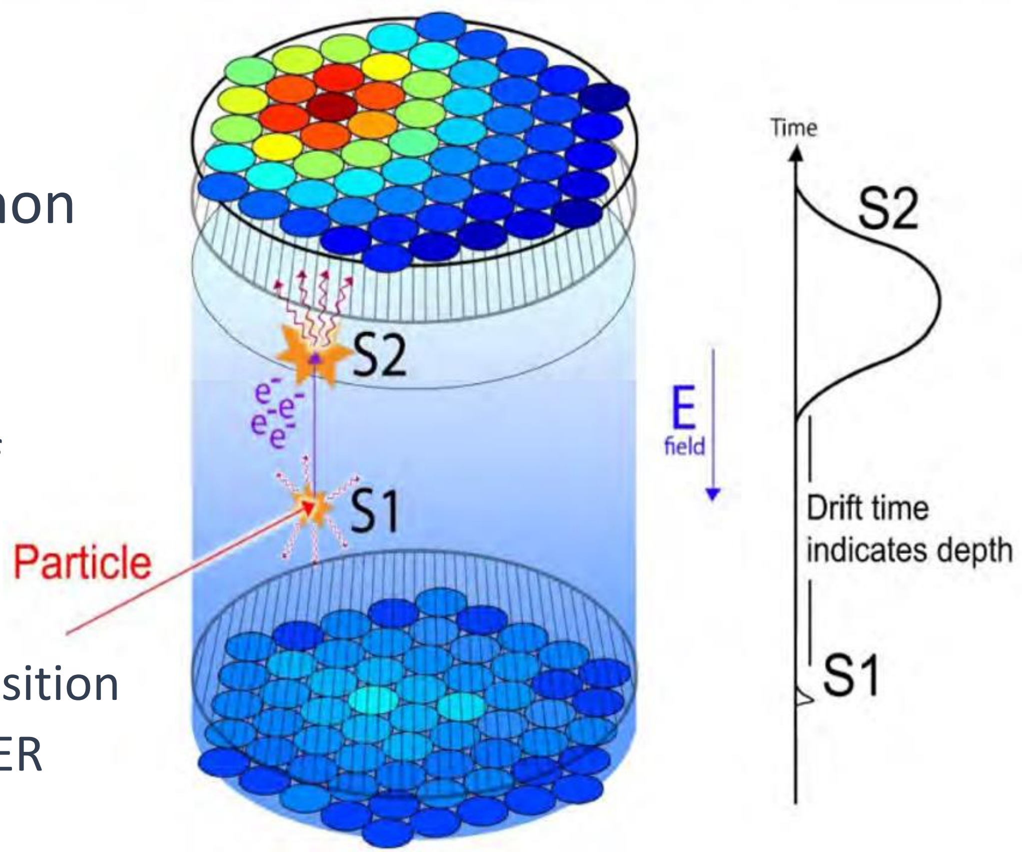
PandaX-xT: multi-ton DM experiment
2016 -



PandaX-III: 200 kg to 1 ton ^{136}Xe 0vDBD
2016 -

Dual Phase Xenon TPC

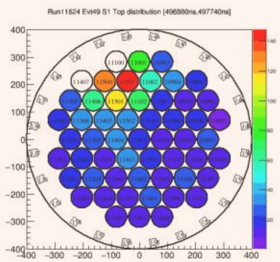
- Incoming DM collide with Xenon
- Two signals:
  - S1: Scintillation light in LXe
  - S2: Proportional scintillation of ionization electrons
- Advantage
  - Reconstruct energy and 3-D position
  - Discriminate between NR and ER



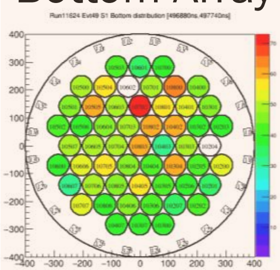
Typical Single Scattering Event

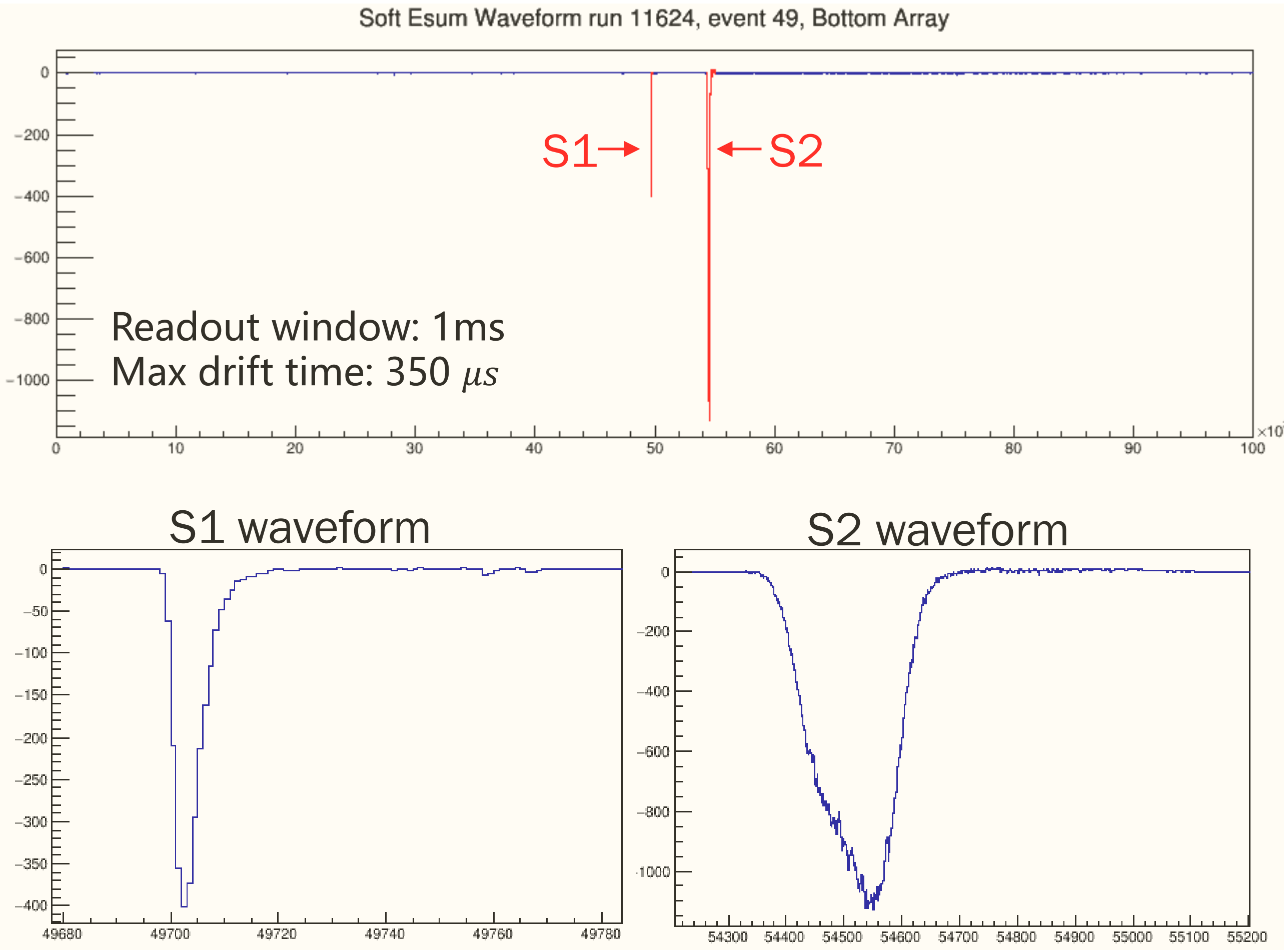
S1
$1\sim 100PE$
$\sim 100ns$

Top Array



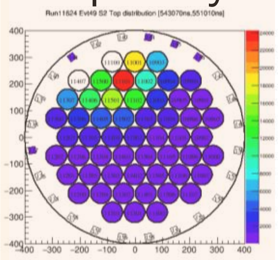
Bottom Array





S2
$100\sim 10000PE$
$\sim \mu s$

Top Array



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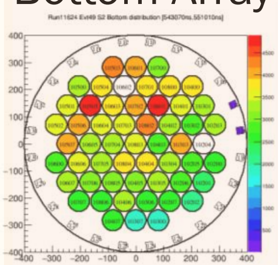
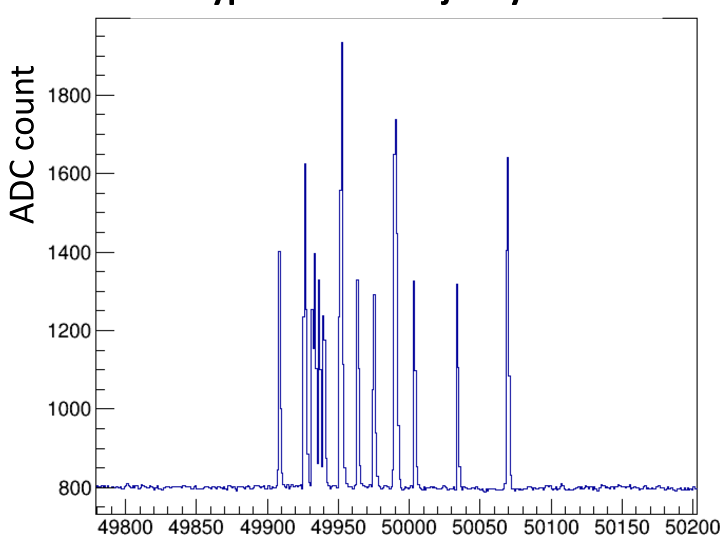


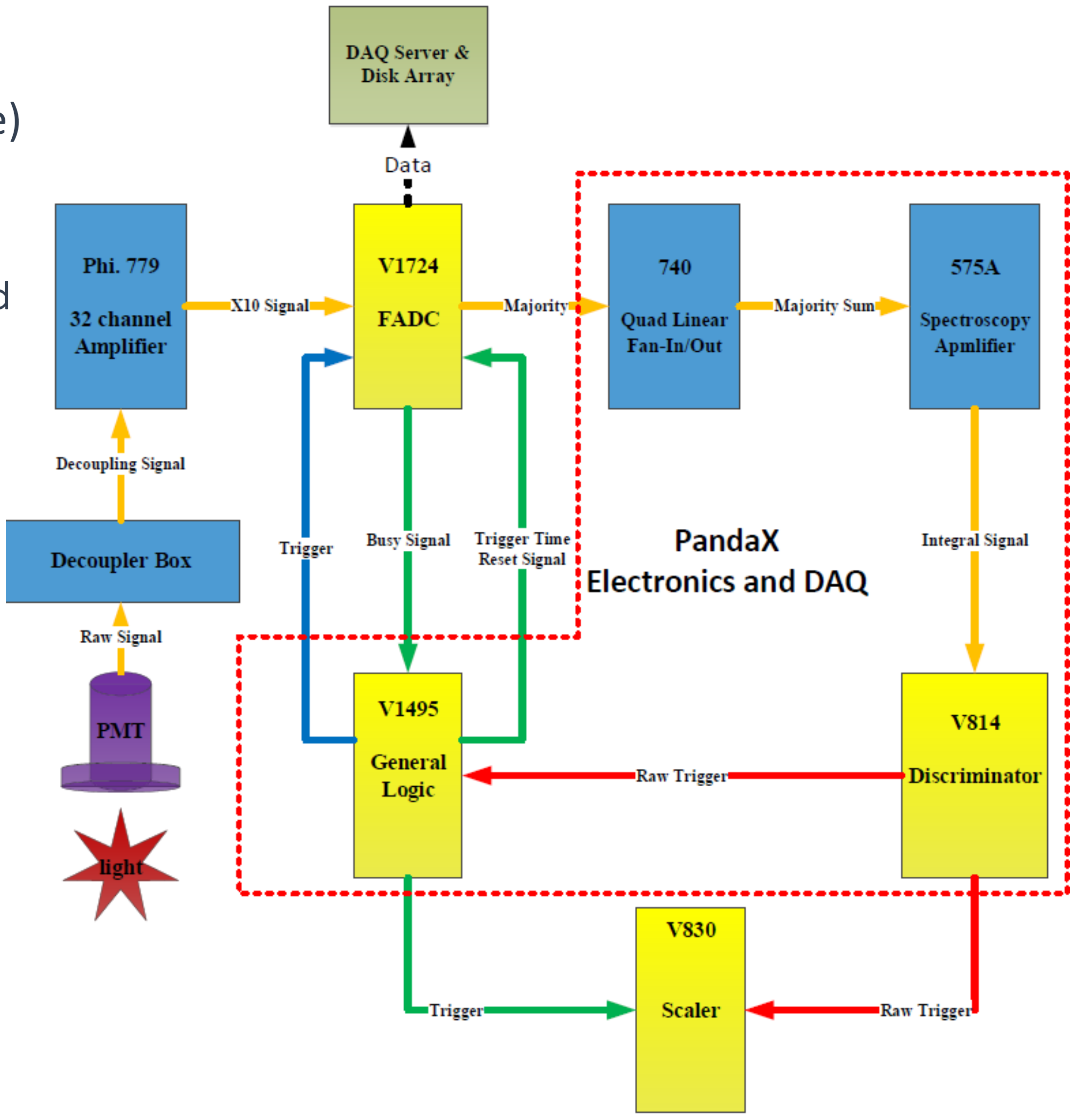
Motivation

- Old Trigger System(red dashed line)
  - Based on analog electronics
  - Not flexible
  - Meet its limit on trigger threshold

Majority Sum: Sum of 110 channels of time-over-threshold signals

Typical S2 in Majority Sum

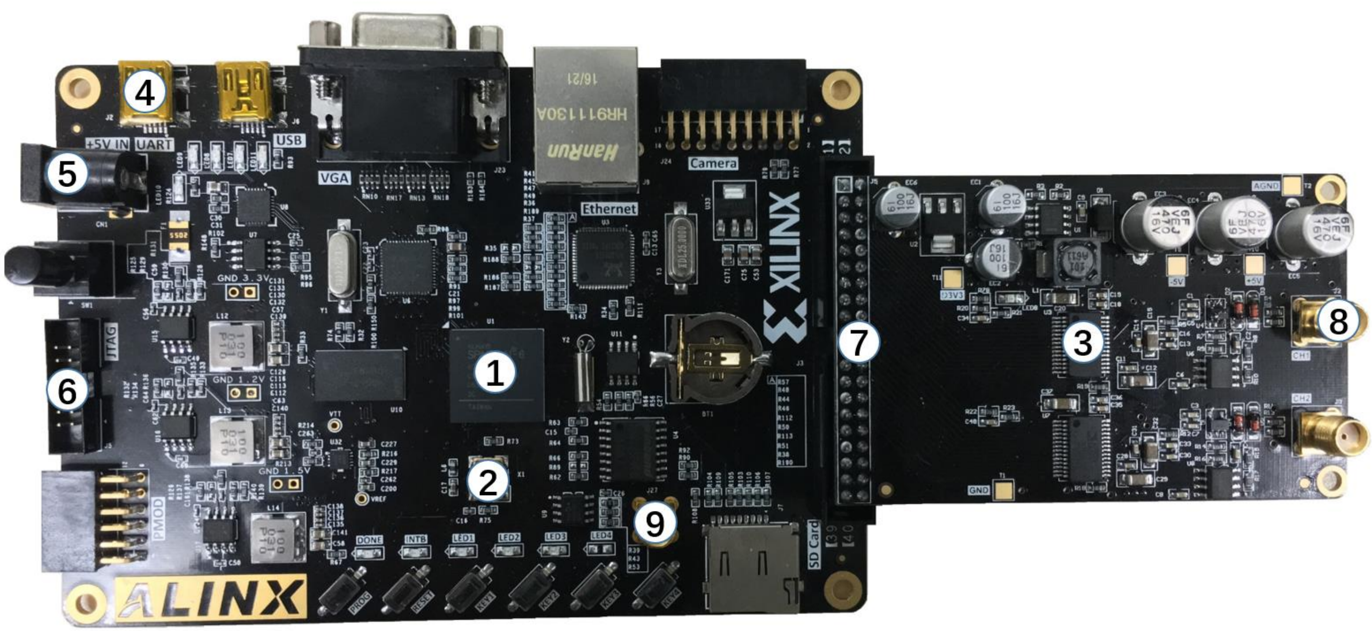




PANDA X
PARTICLE AND ASTROPHYSICAL XENON TPC

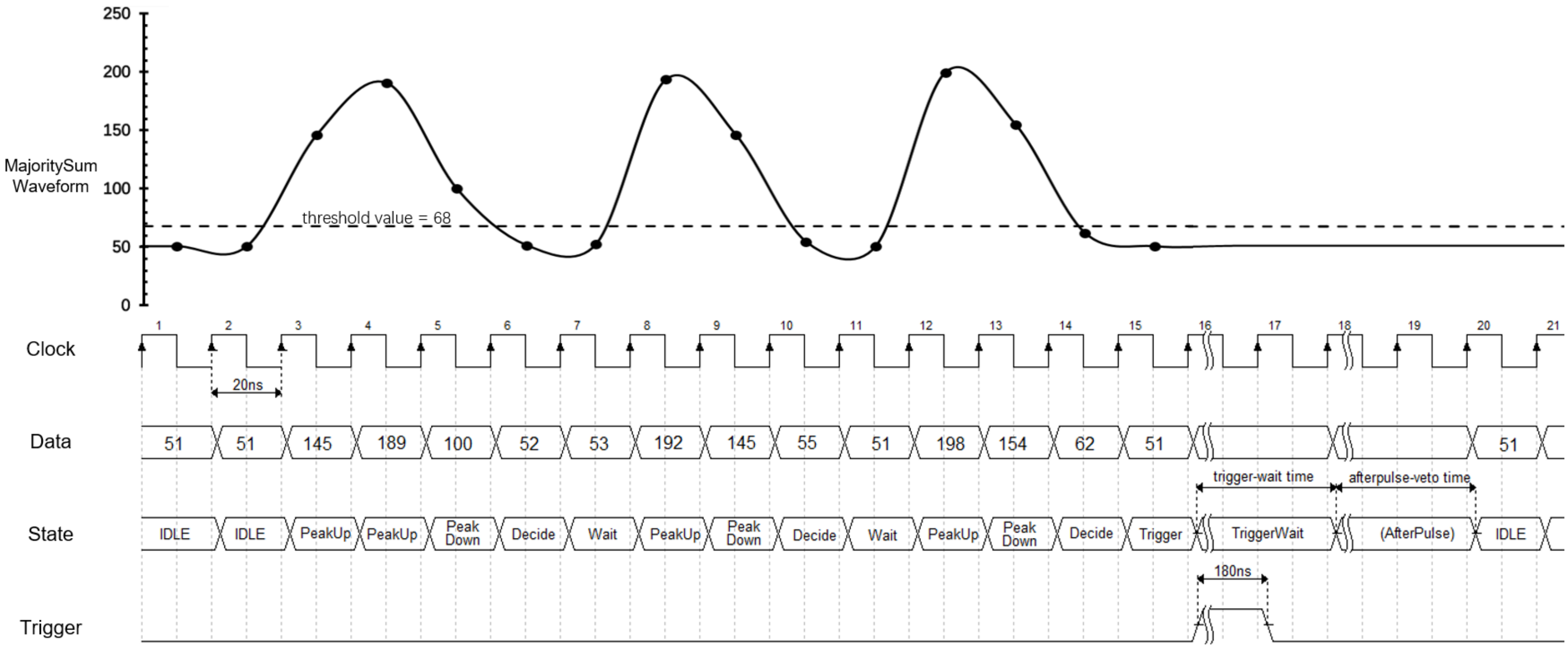
Step One: Hardware

- Commercial FPGA board with ADC subboard
  - Input: Majority Sum through Port 8
  - AD9226: 50MHz, 12bit; Digitize Majority Sum
  - FPGA: Xilinx Spartan-6; Deal with the digits with pre-programmed algorithm
  - UART: Enable simple monitor and control function.



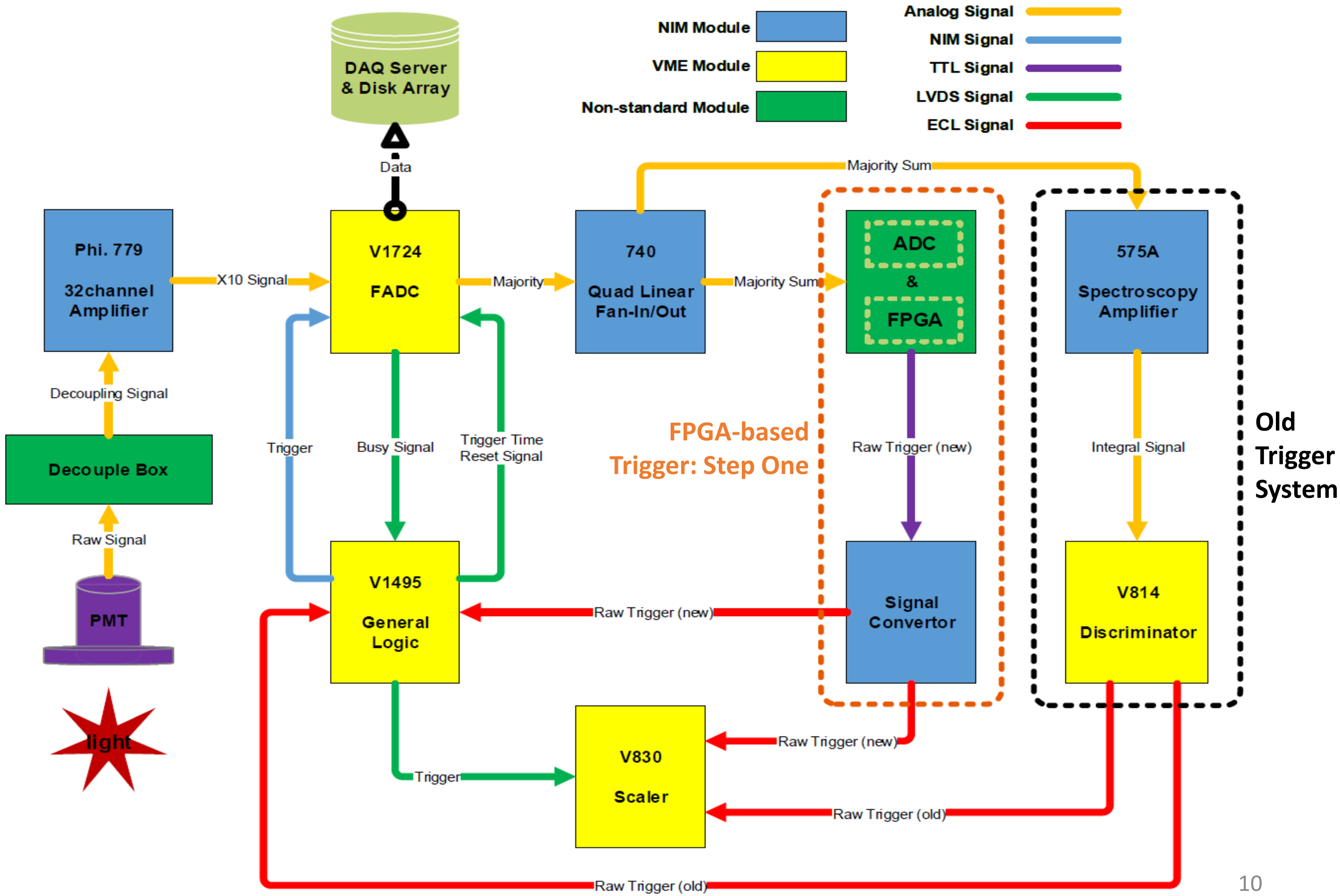
1 – FPGA(XC6SLX16)
2 – 50MHz Oscillator
3 – AD chip(AD9226)
4 – UART Connector
5 – Power(+5V)
6 – JTAG Connector
7 – 40-pin Connector
8 – Analog Input
9 – TTL Output

Step One: Main Algorithm



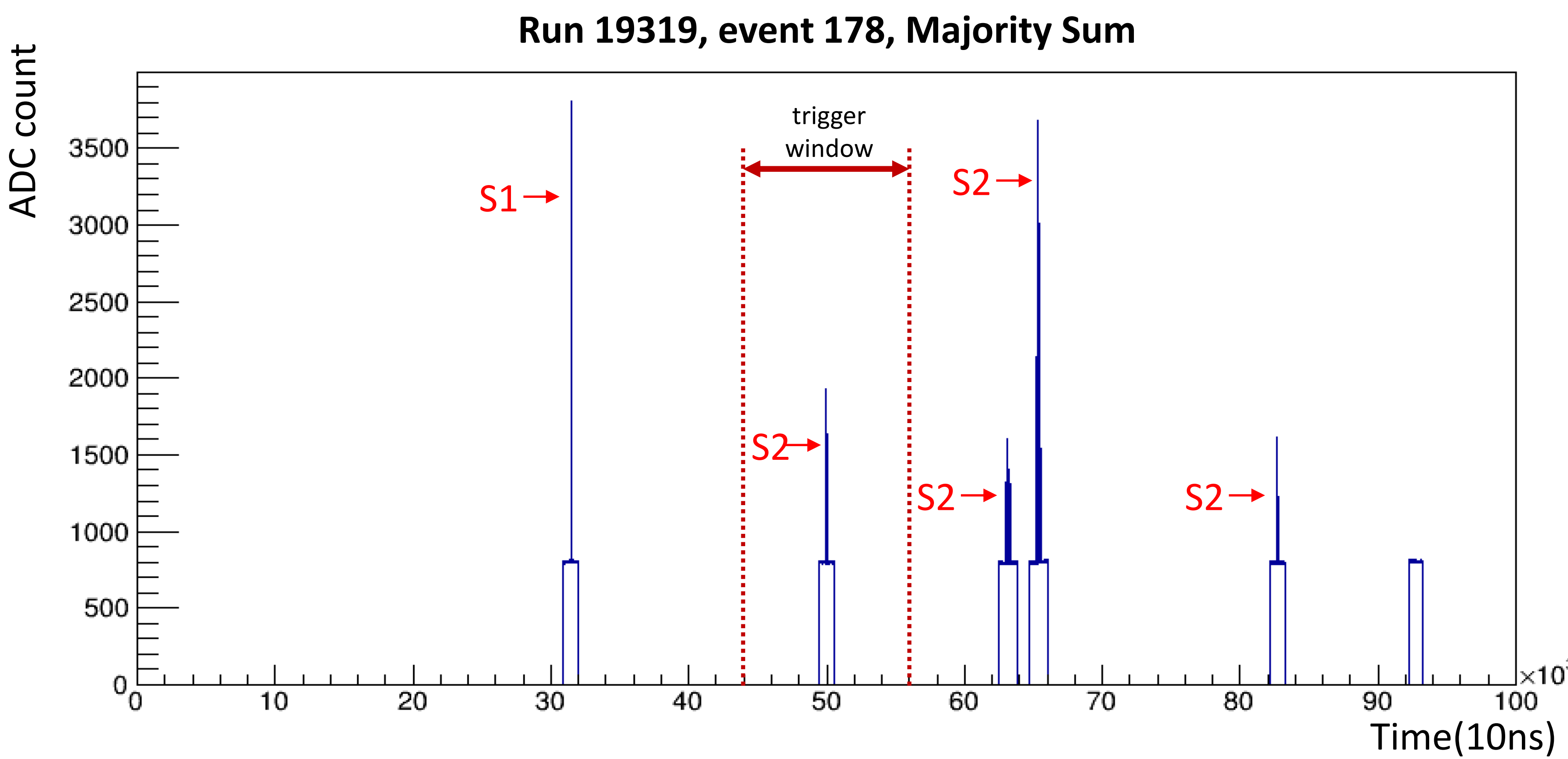
- Structure: Finite State Machine(FSM).
- Trigger Conditions: compare width, amplitude and number of peaks with adjustable parameters, separately.

Step One : TDAQ Scheme

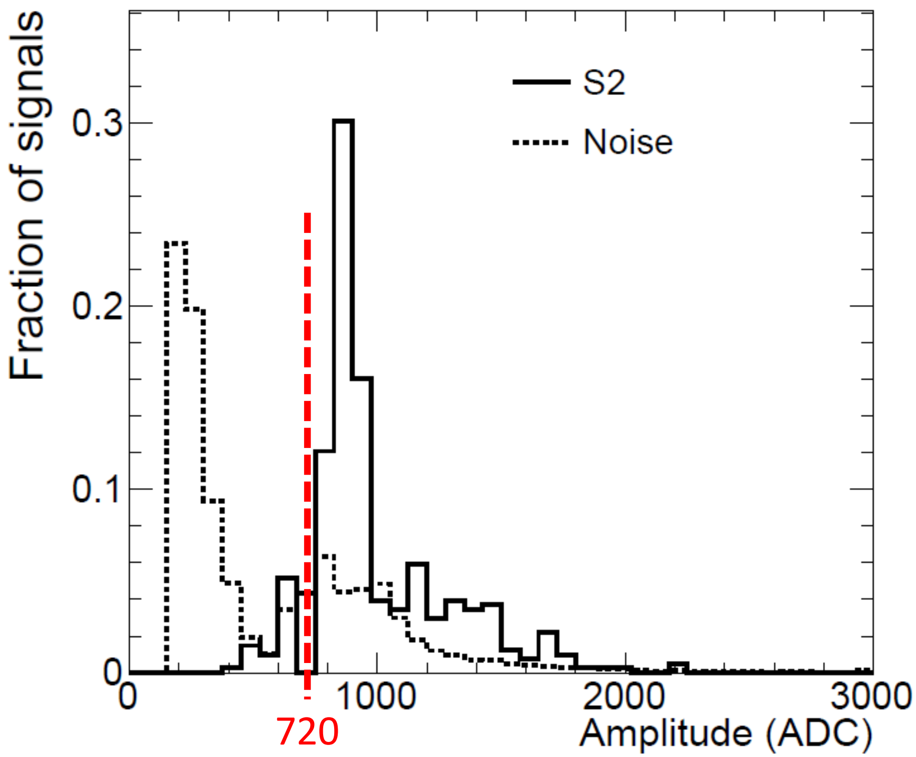


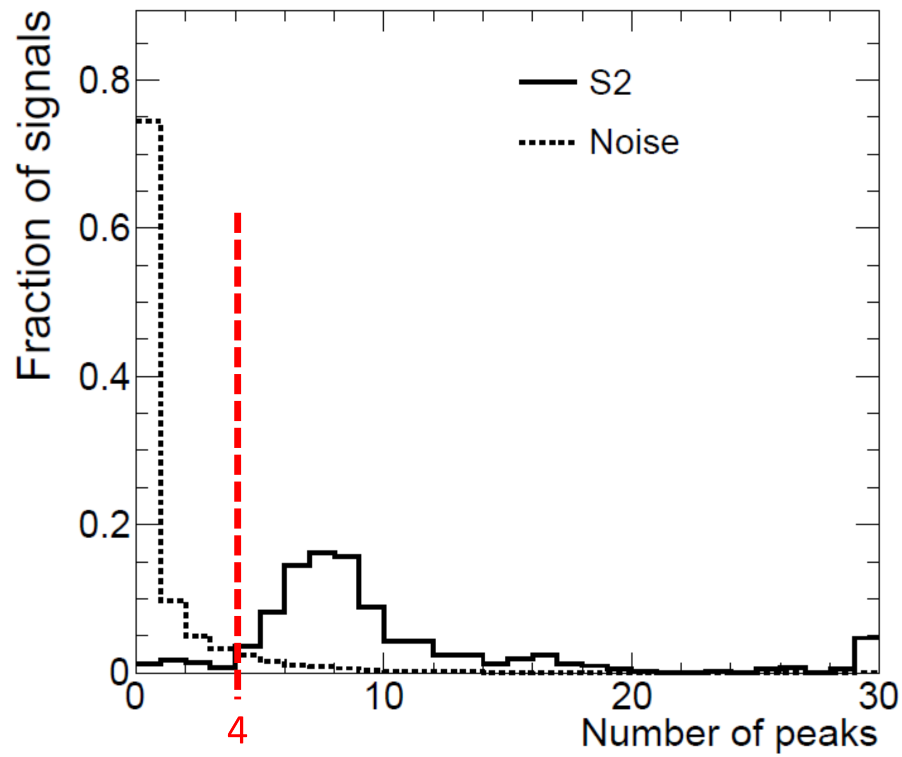
Step One: Multi Scattering

- Neutron Calibration: AmBe source.
  - Multi scattering: mean free path of neutron in LXe is about 12cm.
  - Several S2 in one event (1ms length).



Step One: Parameters

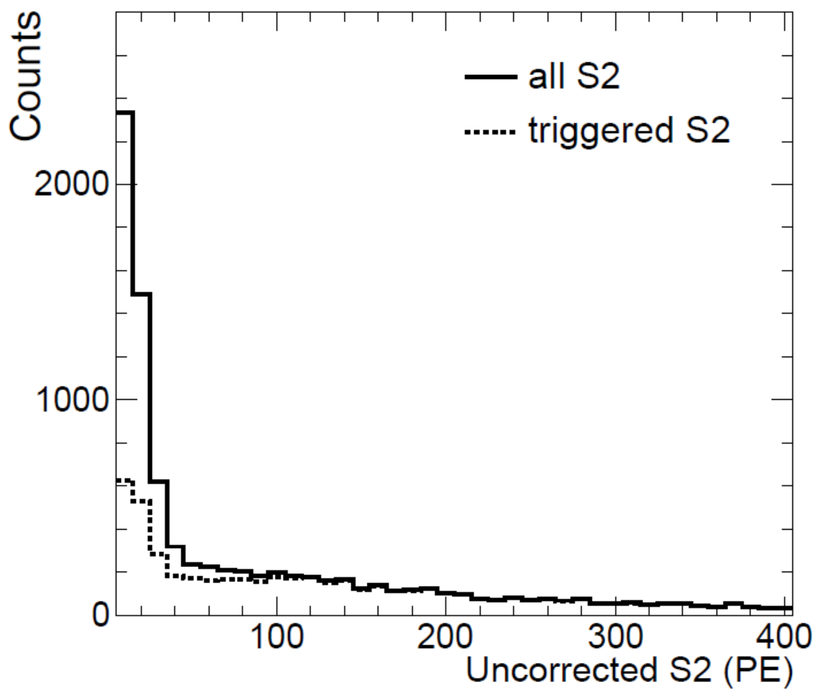


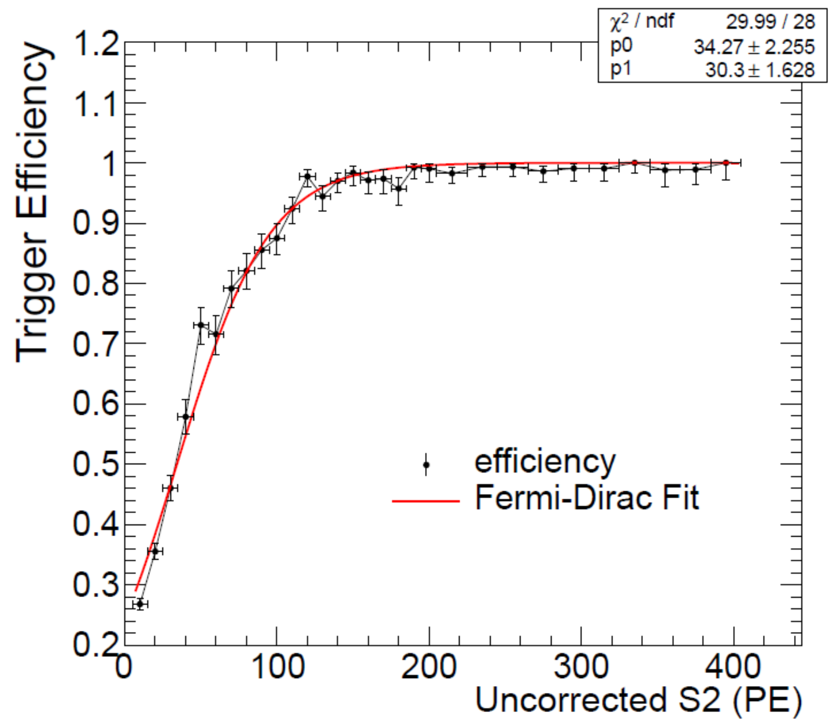


- Use real data: off-trigger-window S2 from multi scattering.
- Used for determining the threshold of parameters.

Step One: Performance Test

- Check the trigger efficiency: selected off-trigger-window S2 segments.



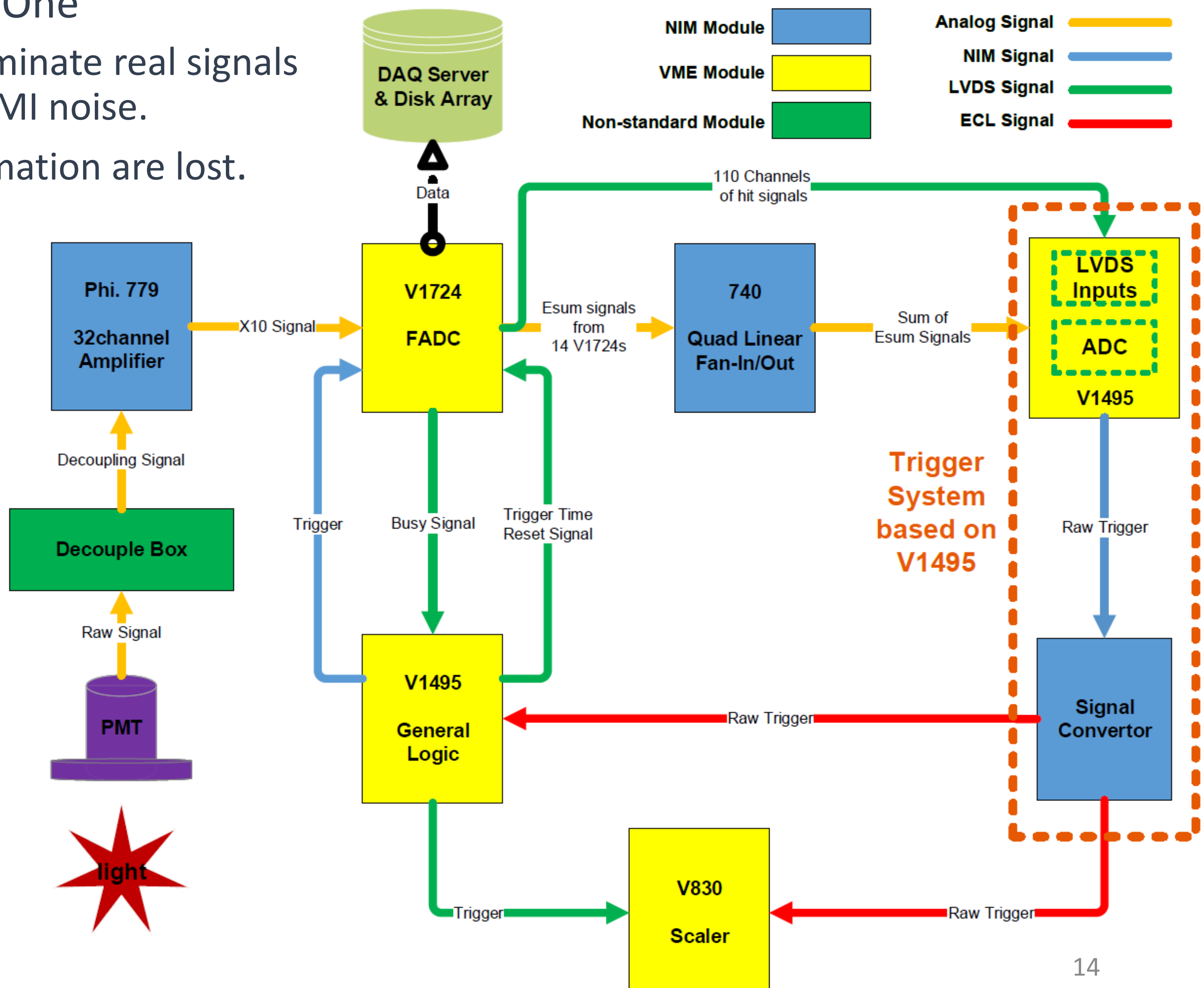


- We obtained trigger threshold at about 35PE, which is much lower than the old trigger system (80PE).
- This system is now being used for PandaX-II's data taking.

Future: Step Two: TDAQ scheme

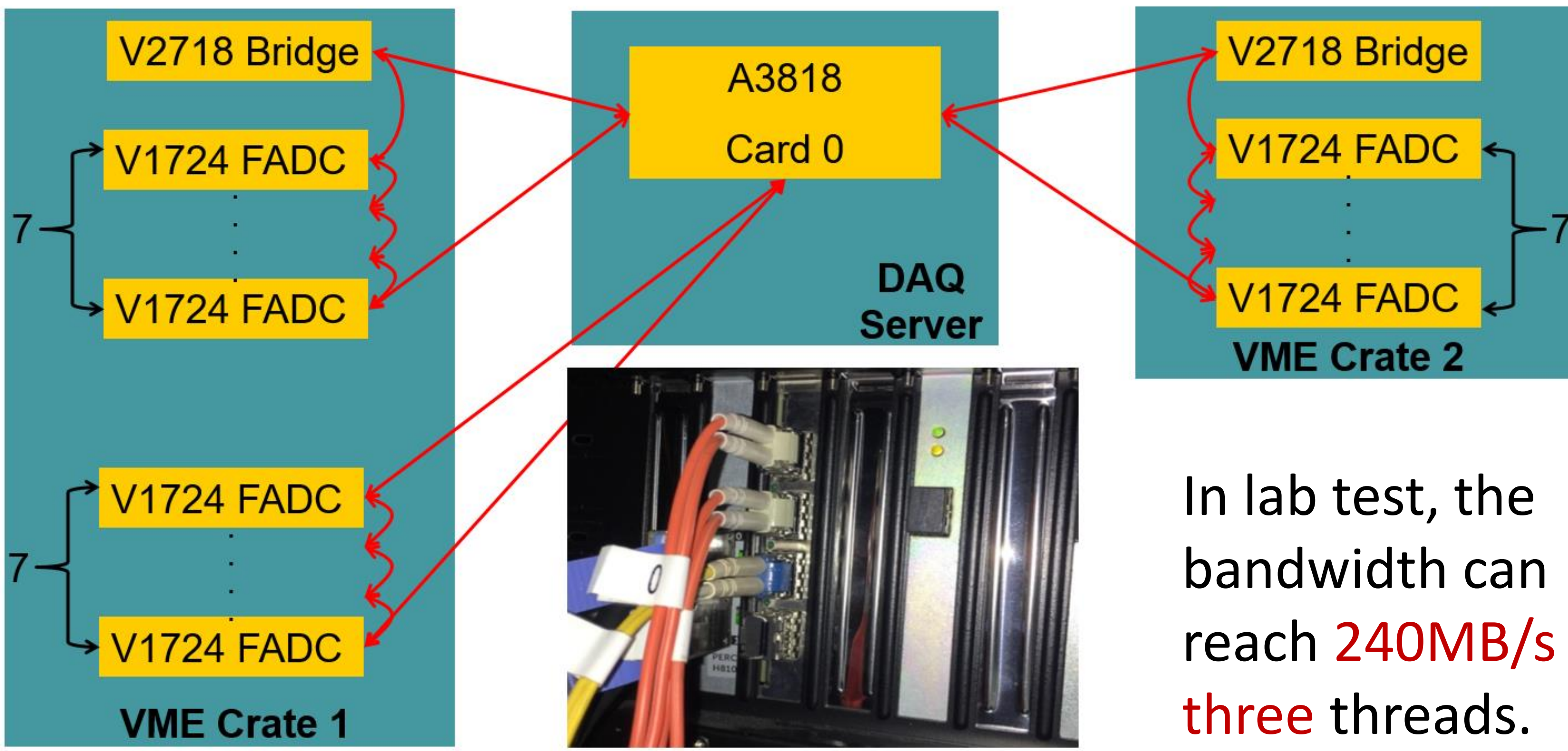
- Problems with Step One
  - Difficult to discriminate real signals with the 80kHz EMI noise.
  - Hit pattern information are lost.

Total ESum: proportional to the sum of 110 waveforms.



Future: Multithread Readout

- Daisy Chain: Every 7 V1724s share one optical fiber
- A3818 PCI Express × 8 card: manage the readout
- C++ projects for multithread readout



In lab test, the bandwidth can reach 240MB/s for three threads.

Summary & Outlook

- We developed a FPGA-based trigger system.
- Achieved lower trigger threshold, compared to previous analog-based trigger.
- The FPGA-based trigger system has been used for PandaX-II.
- Future upgrades of the readout system:
    1. FPGA Programming board V1495.
    2. Multithread readout.

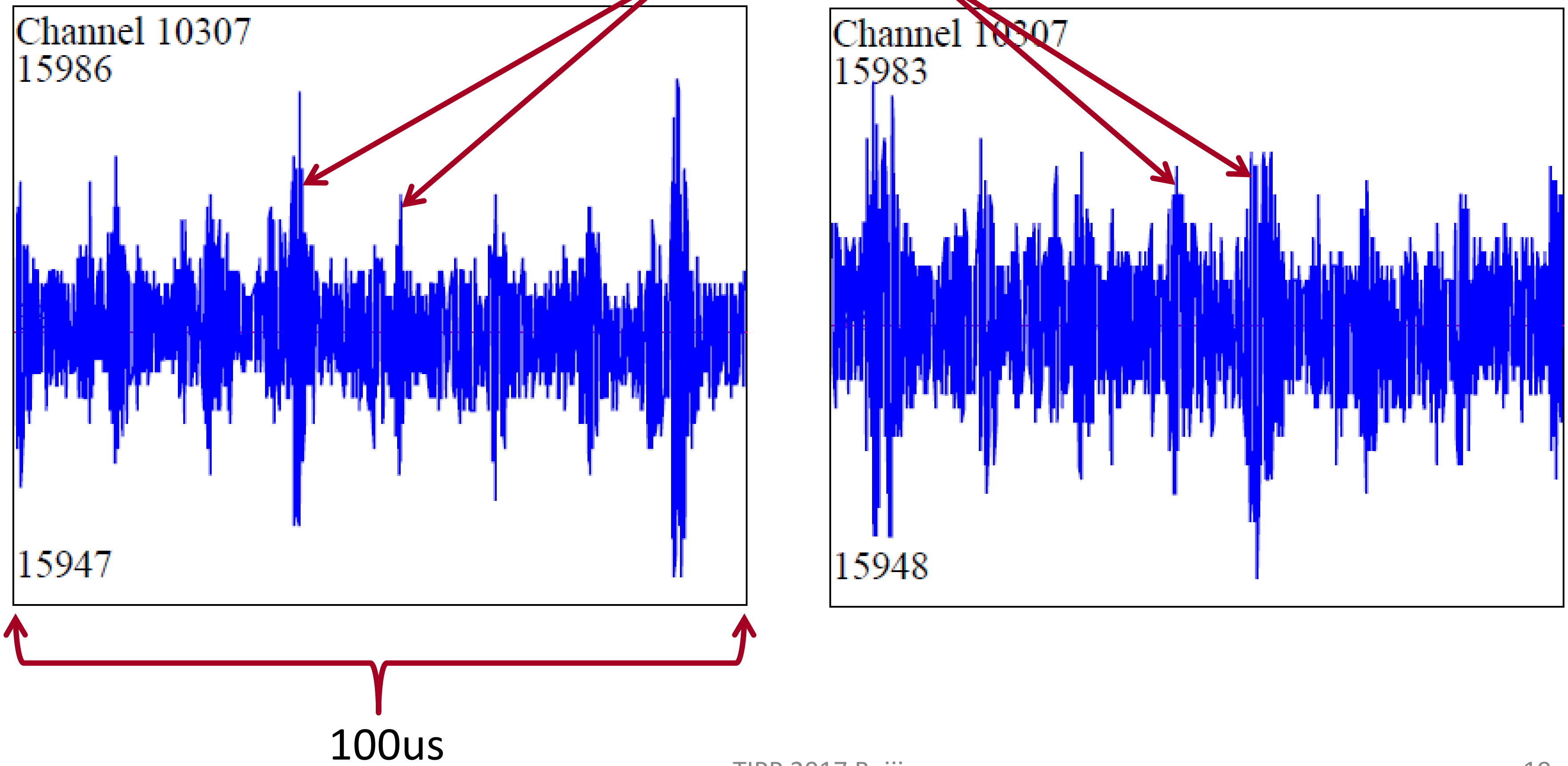
Thanks!

Backup Slides

80kHz EMI Noise in CJPL

- Coupled from the ground

Main Noise: $\sim 13\mu s$;



Step One to Step Two

- Problems with Step One
  - With Majority Sum only, there's no way to discriminate real signals with the 80kHz periodic noise from the ground.
  - Hit pattern information are lost
- Solutions in Step Two
  - Change the output of every V1724 from Majority to Esum signal. Esum is the proportional sum of all 8 waveforms.
  - Use the front panel of V1724 to send hit signal to V1495 channel by channel.

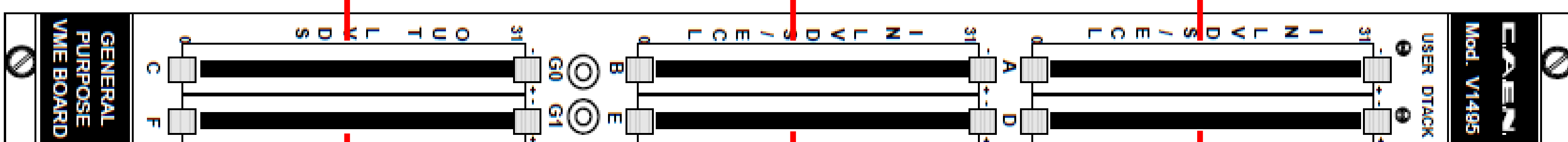
FPGA-based Trigger System: Step Two

- CAEN V1495 General Logic Module
  - Two Cyclone FPGA chips. One for Communication, one for user define.
  - Easy monitor and control through VME crate
  - Expandable with subboards

C: 32 channel LVDS outputs

B: 32 channel LVDS inputs

A: 32 channel LVDS inputs



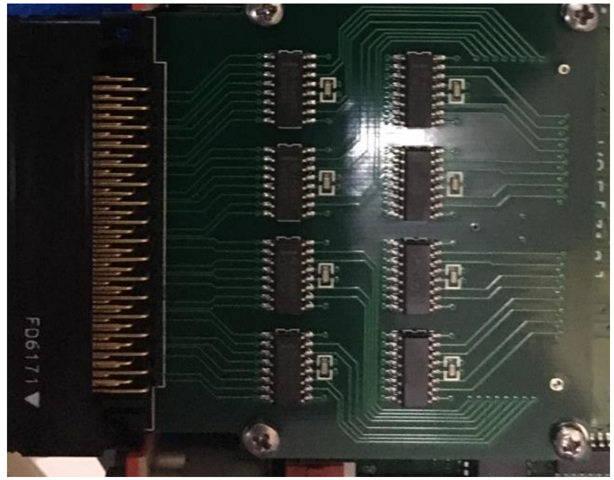
F: 32 channel LVDS input(self-made)

E: 32 channel LVDS input(self-made)

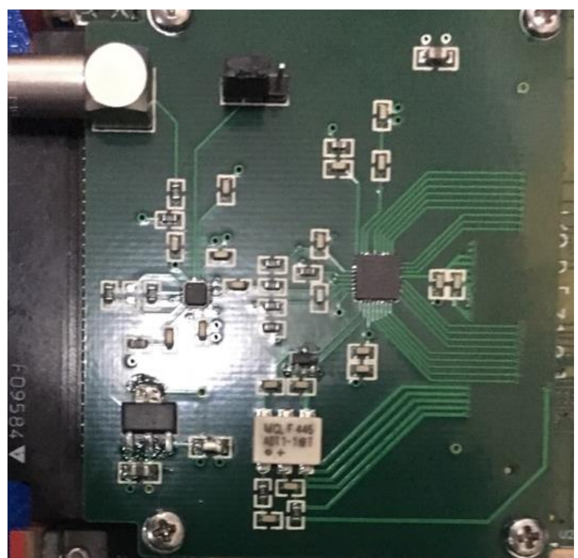
D: One channel AD convertor

Step Two Hardware: self-made subboard

- 32-ch LVDS input subboard: finished



- 14-bit ADC subboard: under debugging and new version in progress



Step Two: Software

- Sliding Window Trigger
  - A window sliding on the 110 hit signals and check how many hits are there in the window
- NHit Trigger
  - Add up all 110 hit signals to one signal digitally
  - Then the same main algorithm as Step One: To check the width, amplitude and number of peaks
- Periodic Noise Killer
  - To check the vibration of the Esum waveforms. Symmetrical height of peaks are the symbol of the noise.
- Final trigger = SWT “AND” NHT “ANDNOT”PNK