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CATIROC, a multichannel front-end ASIC to read out the Small PMTs (SPMT) system of the JUNO experiment

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CATIROC (Charge And Time Integrated Read Out Chip) is a complete read-out chip designed to read arrays of 16 photomultipliers (PMTs). It finds a valuable application in the content of the JUNO experiment, the largest Liquid Scintillator Antineutrino Detector ever built, currently under construction in the south of China. A double calorimetry system will be used for the first time ever combining about 18k 20" PMTs and around 36k small PMTs (3"). The CATIROC will be used to read out the small PMTs system and provide the charge measurement up to 400 photoelectrons (70 pC) on two scales of 10 bits and a timing information with an accuracy of 200 ps rms. It is composed of 16 independent channels that work in triggerless mode, auto-triggering on the single photo-electron (p.e.). It is a SoC (System on Chip) that processes analog signals up to the digitization and sparsification to reduce the cost and number of cables. The ASIC performances will be detailed in the paper.

Summary

JUNO is a Liquid Scintillator Antineutrino Detector currently under construction in the south of China (Jiangmen city). It aims at detecting reactor antineutrinos at a baseline of 53 km, with the primary goal of determining the neutrino mass ordering and performing a sub-percent measurement of the solar mixing angle and of the two mass-squared differences. Once completed, JUNO will consist of 20k tons of liquid scintillator monitored by roughly 18 thousands 20" PMTs.

A challenging total energy resolution of ˜3% at 1MeV is required to achieve these physics goals. For this purpose a large photo-coverage and quantum efficiency needs to be addressed and a double calorimetry system comprising an additional set of 36k Small PMTs (3") has been proposed. The sPMTs will provide a complementary systematic budget and will allow a combined, more precise and more accurate energy scale definition. The readout of the sPMT needs to fulfill optimum charge and time resolutions (< 1 ns). The proposed ASIC, named CATIROC, is being tested to study its performance with the sPMT models under evaluation for JUNO and to design the readout card, the DAQ system and the test-bench needed in the production phase.

CATIROC is an AMS SiGe 0.35 µm technology chip that integrates 16 identical channels. It auto-triggers on the single p.e. and sustains a dark noise rate of 20 kHz/channel. It provides a charge measurement over a dynamic range from 160 fC (1 p.e. at PMT gain of 106) up to 70 pC (˜ 400 p.e.) and a timing measurement with an accuracy of 500 ps (200 ps rms) per channel, both measurement on 10 bits. A gain adjustment per channel (over 8 bits) allows to compensate the non-uniformity of the 16 PMTs operated at the same high voltage. Only one line of digital data running at 160 MHz comes out.

The chip architecture is made of two main paths: a slow and a fast channel.

The slow channel is obtained by two input voltage preamplifiers with high and low gain respectively. The gain of each channel can be set individually and can be adjusted on 8 bits thanks to a preamplifier feedback variable capacitor. Each preamplifier is followed by a slow shaper and two Track-and- Hold (T&H) stages in order to provide a charge measurement. The two T&H work in a "ping-pong mode" : while the first value is digitized, a second slow shaper signal can be stored in a second capacitor. The charge analog value is then converted by the internal 10-bit Wilkinson ADC operated at 160 Hz.

The fast channel is made by the high gain preamplifier followed by a fast shaper (5 ns) and a low offset discriminator to auto-trigger down to 50 fC (1/3 p.e.). Its threshold is set by an internal 10-bit DAC common for the 16 channels. The discriminator output signal (or trigger) is delayed to hold the shaper signal at its maximum value into the T&H. It is also used to manage two TDCs (Time to Digital Converter) that convert the time in a voltage using two ramps of 25 ns. The time measurement is classically obtained by two paths: a "time stamp" performed by a 26-bit counter at 40 MHz and a "fine time" obtained thanks to two TDC ramps per channels converted by another 10-bit Wilkinson ADC.

All channels are handled independently by the digital part and only channels that have created triggers are

digitized, transferred to the internal memory and then sent-out in a data-driven way.
The ASIC characterization shows a good overall behavior and that the chip has fulfilled the requirements of the JUNO SPMT system. The ASIC architecture, the test-bench and the PMT measurements will be presented.

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