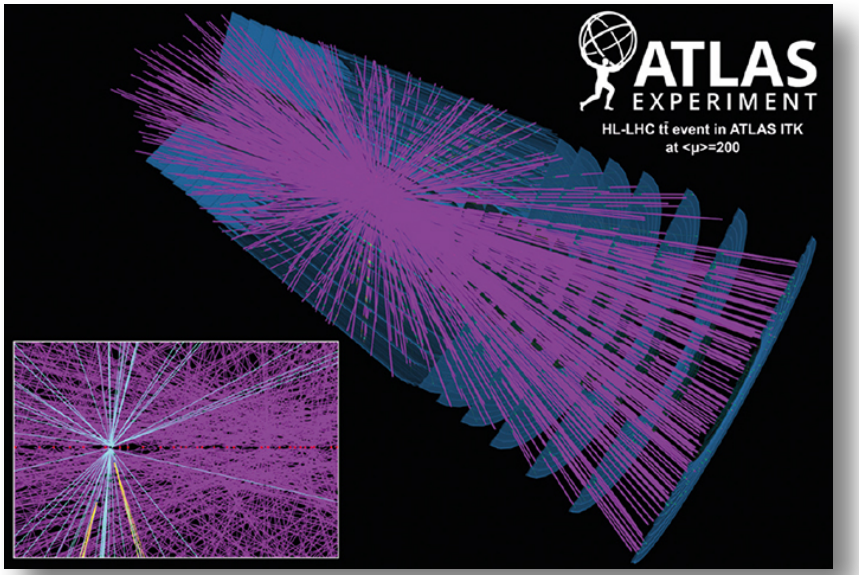
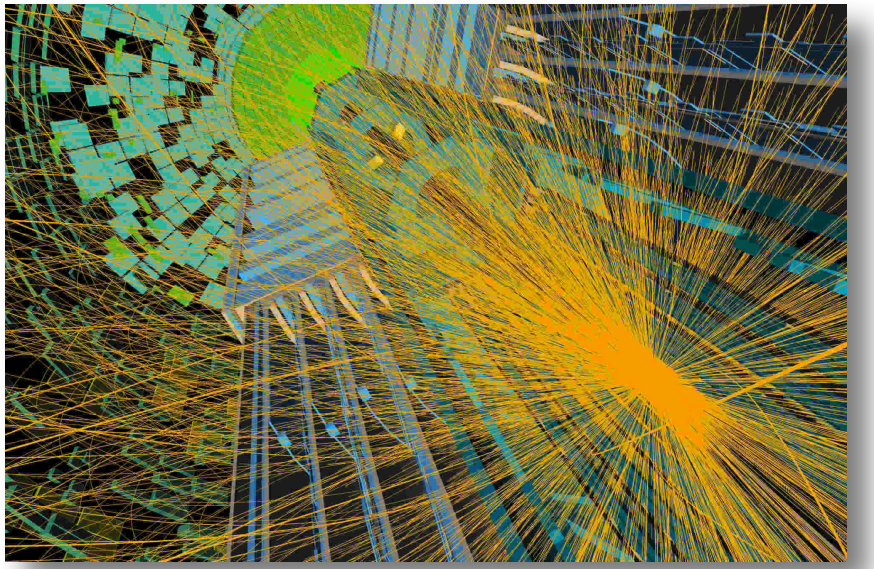




The Phase-2 ATLAS ITk Pixel Upgrade

Mathieu Benoit

On behalf of the ATLAS Collaboration

TIPP, 22-26 May 2017, Bejiing, China

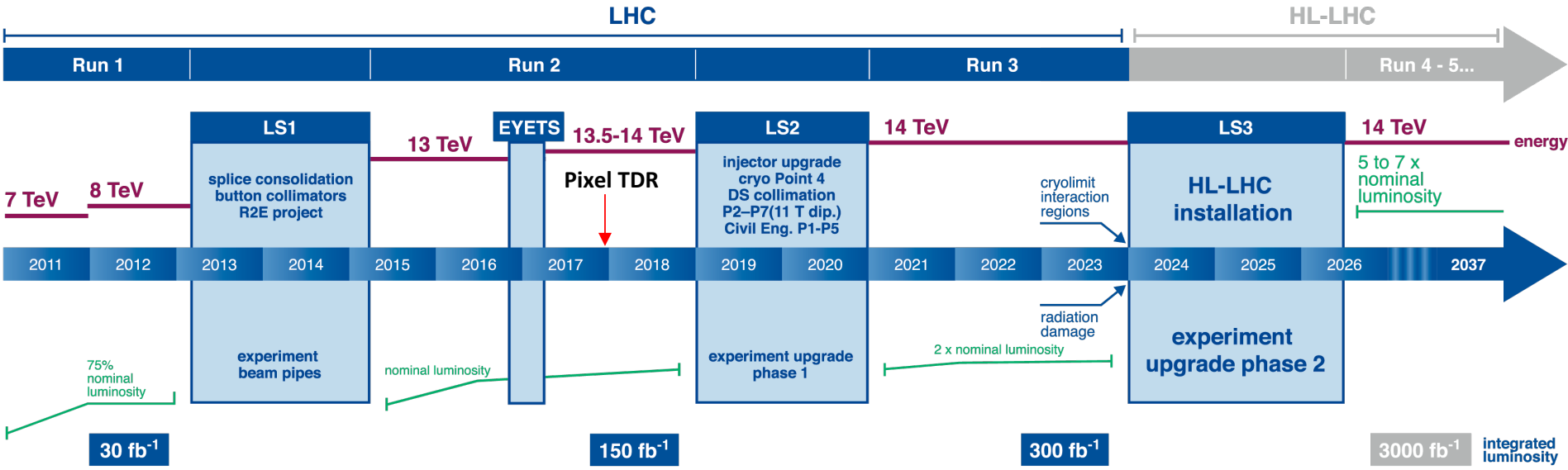
UNIVERSITÉ DE GENÈVE
FACULTÉ DES SCIENCES

Outline

- Schedule of the HL-LHC
- The current Inner Detector and the ATLAS ITk Pixel upgrade
- R&D On Pixel Mechanics and Services
- The RD53 Collaboration
- R&D on pixel sensors and modules:
  - Bump-Bonding
  - 3D sensors
  - Planar sensors
  - An alternative option : CMOS

Schedule

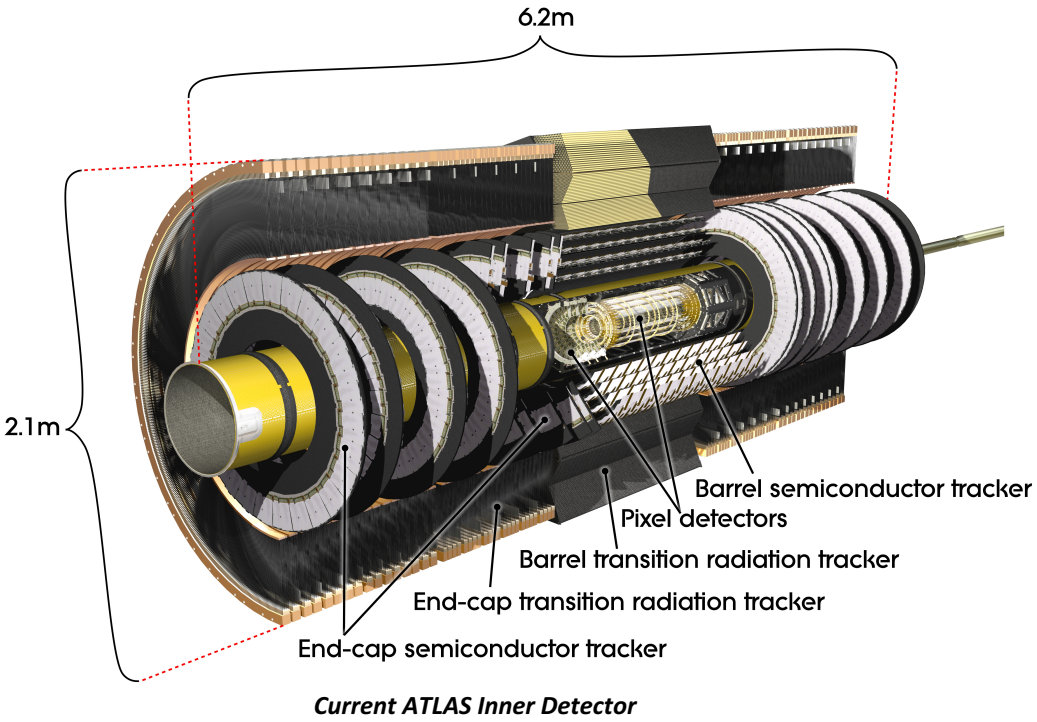
LHC / HL-LHC Plan



The LHC will become the High-Luminosity-LHC (HL-LHC), to produce more than 3000 fb^{-1} of integrated luminosity in 2035.

Higher integrated luminosity → benefits precision measurements and studies of rare processes.

ATLAS Inner detector



Current ATLAS Inner Detector

Same or better performance are expected from the Inner Detector in Phase-II, in order to achieve this goal, several aspects are considered :

- Higher data rate capabilities for the sensor readout and stave services
- Smaller pixel segmentation to reduce misidentification and provide better tracking in dense environment
- Increased radiation hardness of the sensors w.r.t. to current technology
- Increased tolerance to SEU and TID for the readout electronics

HL-LHC scenario implies significant changes that affects the Inner detector w.r.t the current design:

- Peak luminosity: 5-7 x 10^{34} cm^{-2} s^{-1} ~ x 5-7
- Average pile-up: up to <μ> ~200 ~ x 8
- Integrated luminosity: 3000 fb^{-1} ~ x 10
- required radiation hardness: 2x10^{16} n_{eq}/cm^2 x 20

ATLAS ITk will implement an all Silicon tracker :

- **65nm** readout ASIC with **5Gbps maximum data rate** (RD53)
- **Radiation hardened pixel** sensors in 3D and planar technology with **small pixels**
- New mechanics layout to **increase Eta coverage and minimize material budget** and optimize **sensor cooling power**

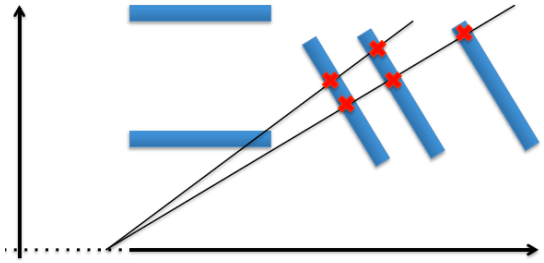
Pixel Mechanics and Services

The layout of the ITk Pixel detector is currently under study by the Layout Task force to identify the final layout to be implemented among the one under study by the community, with different barrel and disk geometry and different Eta coverage.

See : Design of the new ATLAS Inner Tracker for the High Luminosity LHC, Jike Wang

Inclined layout

- Sensors along the barrel stave are inclined in order to be **as perpendicular as possible** to particles coming from the interaction point to reduce material budget
- **Multiple space point per stave** can be measured

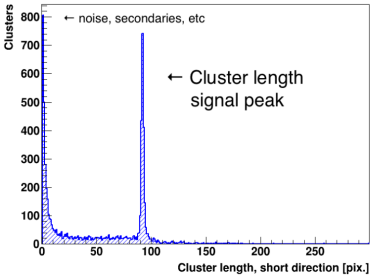


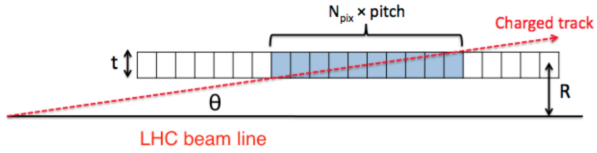
Common

- Pixel volume up to 345 mm radius; then strip to the edge of the solenoid
- 5 Pixel Barrel and 4 (or 3) Rings layers, surface ~14 m^2
- η coverage up to 4.0 (or 3.2) with at least 9 space points
- Pixel innermost detector replaceable.

Extended layout

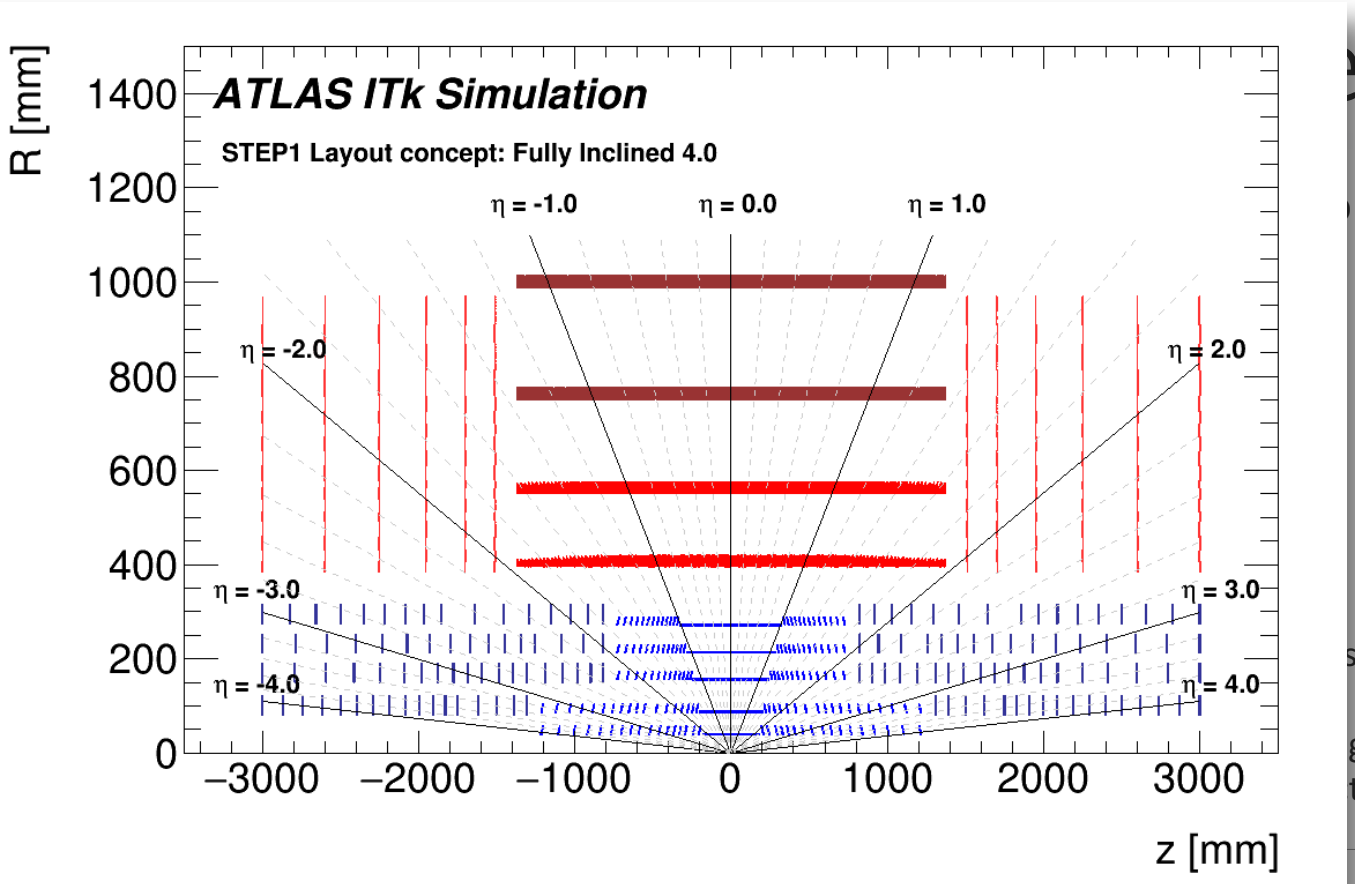
- **Long barrels** covers a large eta region
- **Large clusters at high-eta** can be used to reconstruct tracklets





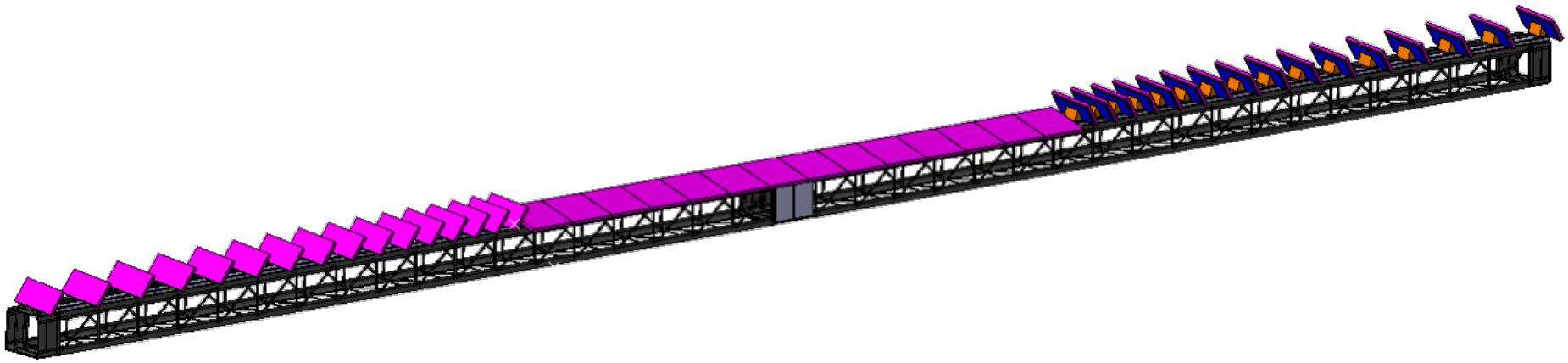
$$N_{pix} = \frac{t}{\tan\theta \times p}$$

The layou
identify t
communi

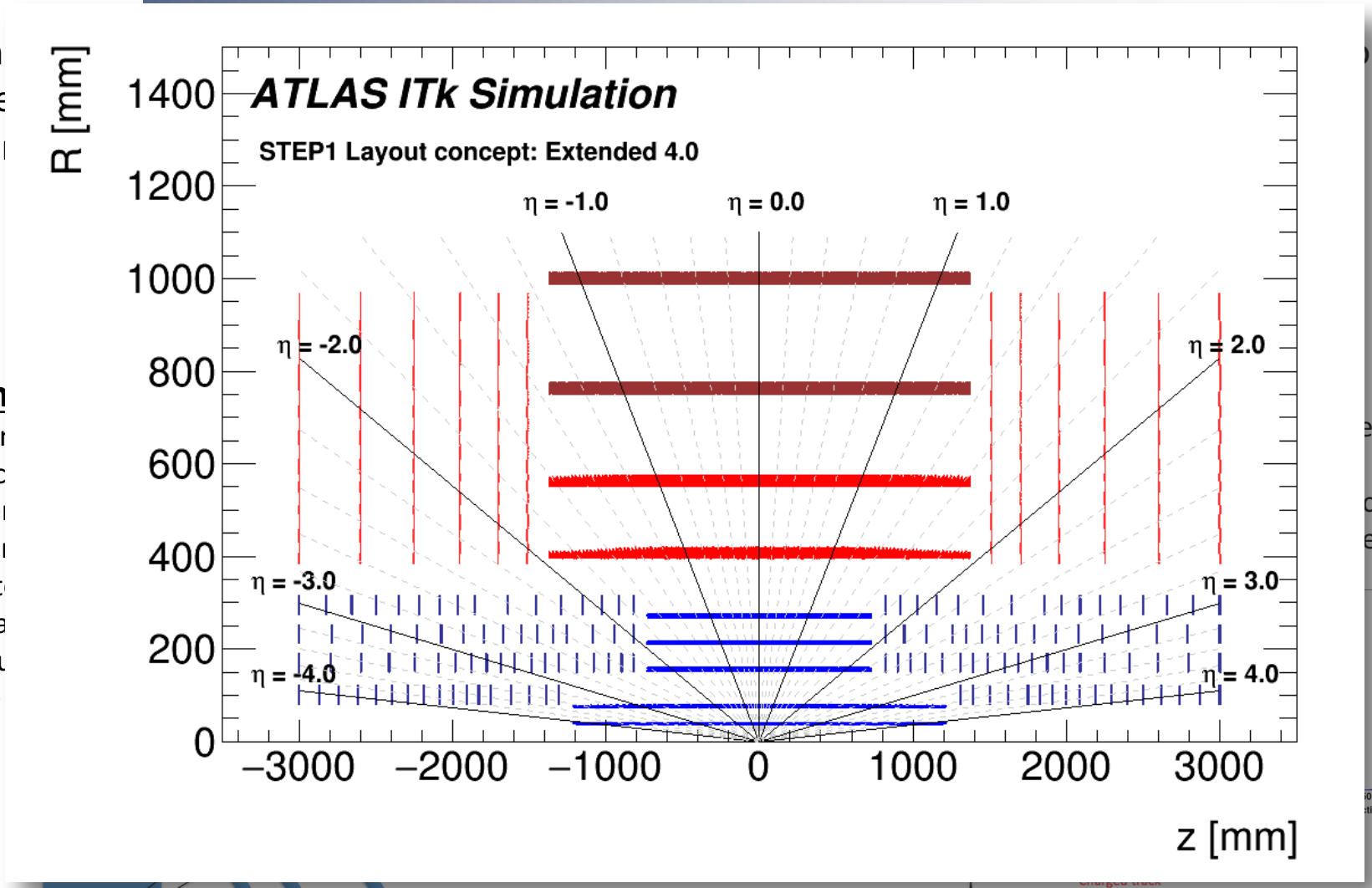


Inclined layo

- Sensors alo
  inclined in c
  perpendicu
  particles co
  interaction



Pixel Mechanics and Services



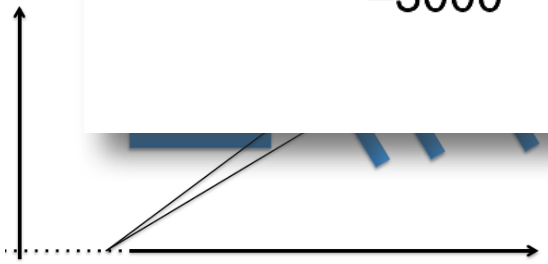
Th
ide
co

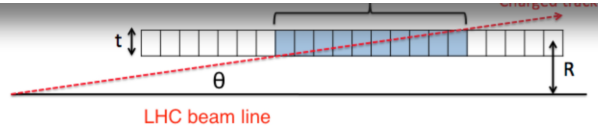
Inclin

- Ser
  inc
  per
  par
  int
  ma
- Mu
  be

e eta

can be
ets





$$N_{pix} = \frac{t}{\tan\theta \times p}$$

Pixel Mechanics and Services

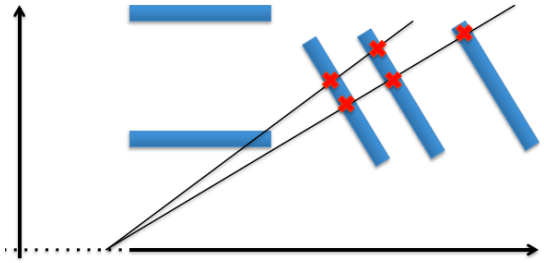
The layout of the ITk Pixel detector is currently under study by the Layout Task force to identify the final layout to be implemented among the one proposed by the community, with different barrel and disk geometry and different Eta coverage.

See :

- **Design of the new ATLAS Inner Tracker for the High Luminosity LHC,** Jike Wang
- **Expected performance of the ATLAS Inner Tracker at the high-luminosity LHC**, *Jason Dhia MANSOUR*

Incline

- Sen… incli… perpendicular as possible to particles coming from the interaction point to reduce material budget
- Multiple space point per stave can be measured

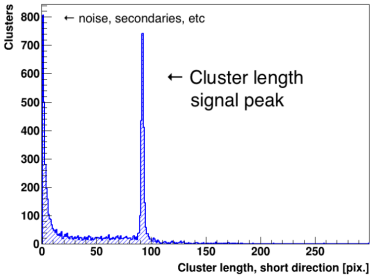


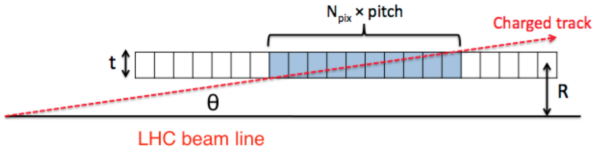
Common

- Pixel volume up to 345 mm radius; then strip to the edge of the solenoid
- 4 Strip Barrel layers + 2x6 EC disks
- 5 Pixel Barrel and 4 (or 3) Rings layers, surface ~14 m^2
- η coverage up to 4.0 (or 3.2) with at least 9 space points
- Pixel innermost detector replaceable.

…ge eta

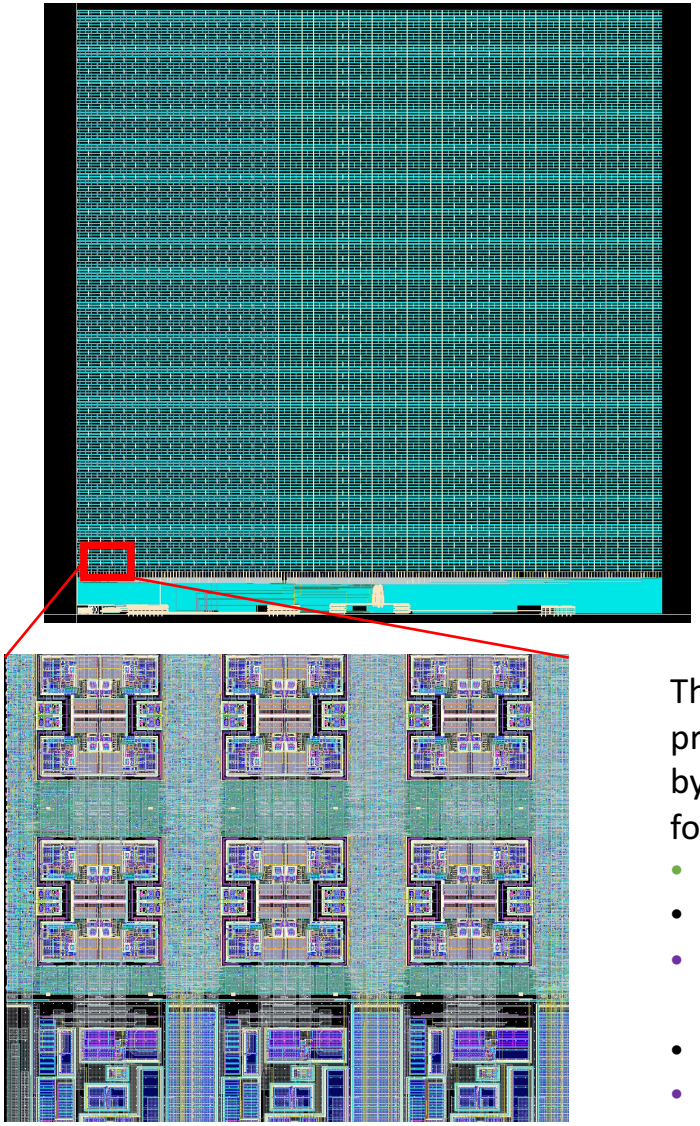
- Large clusters at high-eta can be used to reconstruct tracklets





$$N_{pix} = \frac{t}{\tan\theta \times p}$$

The RD53 Collaboration



Technology	65nm CMOS
Pixel size	**50x50 um²**
Pixels	192x400 = 76800 (50% of production chip)
Detector capacitance	< 100fF (200fF for edge pixels)
Detector leakage	< 10nA (20nA for edge pixels)
Detection threshold	<600e-
In -time threshold	<1200e-
Noise hits	< 10^{-6}
Hit rate	**< 3GHz/cm²** (75 kHz avg. pixel hit rate)
Trigger rate	Max 1MHz
Digital buffer	12.5 us
Hit loss at max hit rate (in-pixel pile-up)	≤1%
Charge resolution	≥ 4 bits ToT (Time over Threshold)
Readout data rate	**1-4 links @ 1.28Gbits/s = max 5.12 Gbits/s**
Radiation tolerance	**500Mrad at -15°C**
SEU affecting whole chip	< 0.05 /hr/chip at 1.5GHz/cm² particle flux
Power consumption at max hit/trigger rate	**< 1W/cm² including SLDO losses**
Pixel analog/digital current	4uA/4uA
Temperature range	-40°C ÷ 40°C

The RD53 collaboration is developping the tools and designs needed to produce the next generation of pixel readout chips needed by ATLAS and CMS at the HL-LHC. The first prototype of a readout ASIC for HL-LHC will be submitted imminently

- **Increased radiation hardness** using 65nm technology
- First time using a fully synthetize digital part in a ”sea of digital”
- **Smallest pitch for hybrid LHC application so far , 50x50um²**, possibility for 25x100um²
- Shunt LDO implemented for compatibility with Serial Powering
- **Highest data rate achievable per ASIC : 5Gbps**

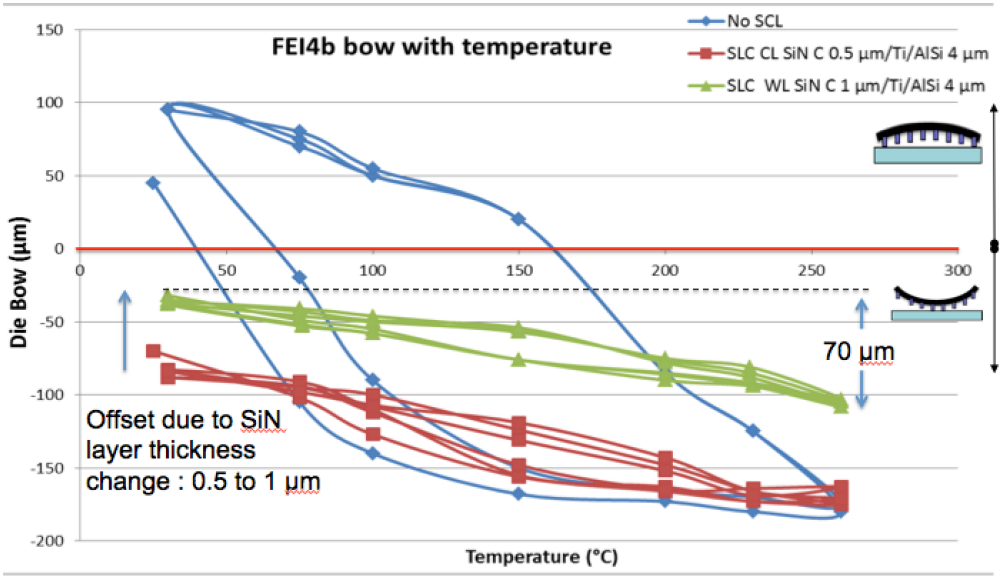
Bump-Bonding

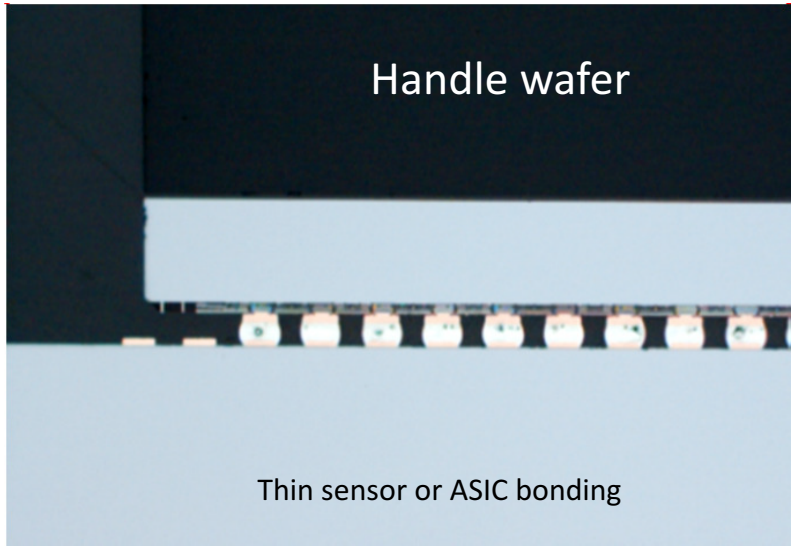
For ITK, the baseline is to rely on ”traditional” bump-bonding, however new challenges emerge :

- 50x50 um^2 pixels, same pitch as before but 5 times higher density
- Larger ASIC wafer size (12”)
- Larger sensor size (~ 4x4 cm)
- Thinner ASIC and Sensors (<150 um)

Work is ongoing to qualify bump-bonding for Itk pixel detector :

- Dummy wafers with **Daisy chain to test** the process at high-density, yield
- **Stress-compensating layers** or **handling wafers** to cope with thin assembly bow
- Evaluation of Bump-deposition vendors on **12”wafers**
- Evaluation of **UBM deposition by sensor vendors**
- Evaluation of **in-house flip-chip** of modules for cost-saving
- Evaluation of **alternate bonding methods** (Indium, wafer to wafer bonding)



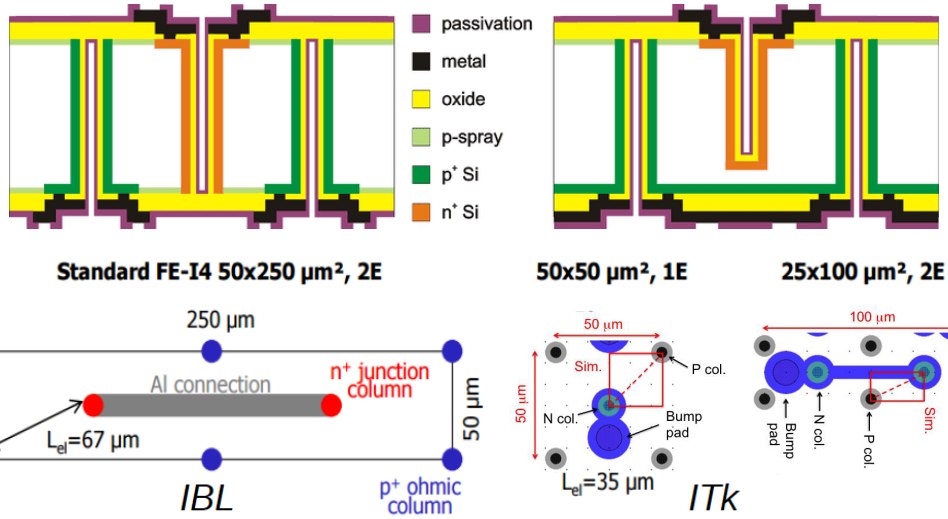


Pixel detectors : 3D Sensors

For the HL-LHC ITk Pixel detector upgrade , the **3D sensor technology**, originally developed and tested in the ATLAS IBL are the prime candidates for the inner layer where extreme radiation hardness is required to survive the dose foreseen.

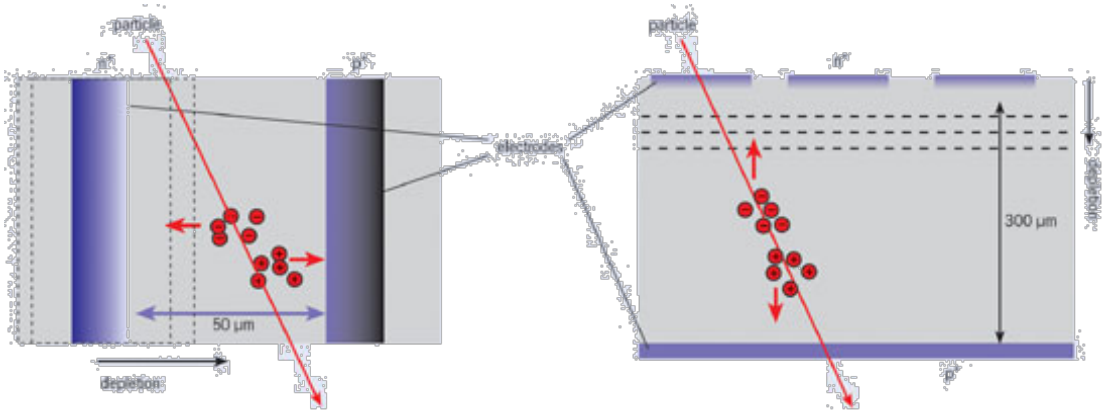
The main challenges for this technology are the following :

- **Smaller pixel needed** (50x50 or 25x100 um^2)
  - Column themselves are not efficient
- **Thinner sensors considered** (<150um)
  - Lower signal
  - Lower occupancy



Recent results with 3D sensors, AUW

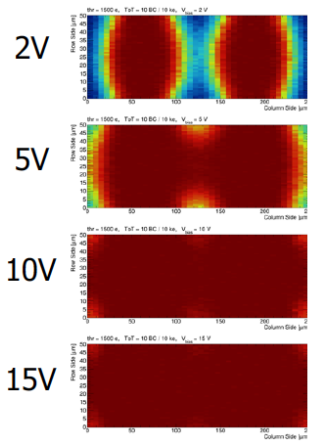
[Beam test measurements of irradiated 3D pixel sensors with 50x50 µm² pixel size](), D.Vasquez, Trento 2017

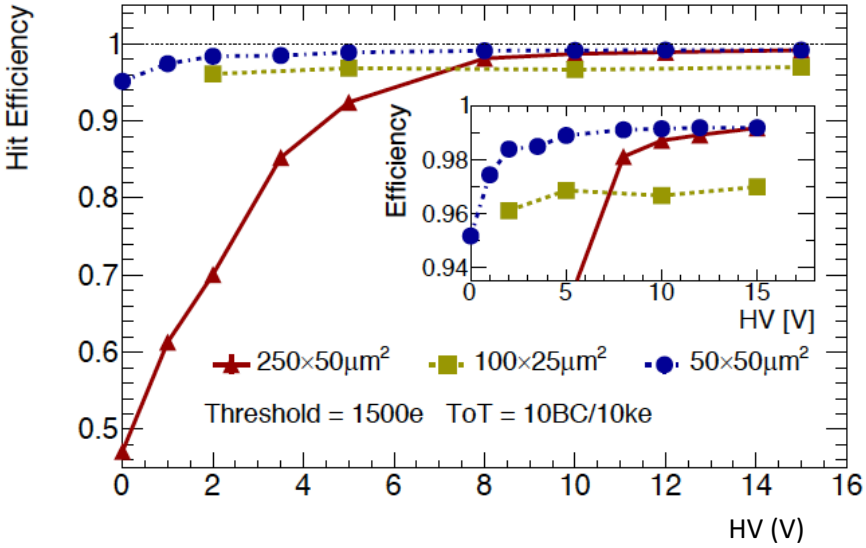


Pixel detectors : 3D Sensors

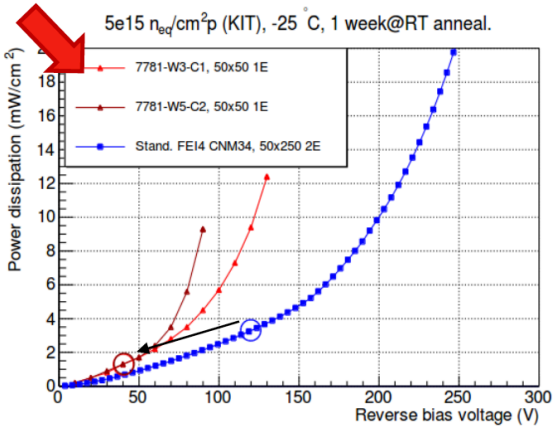
Small pitch sensors were investigated in test beam before and after irradiation up to 1.4e16 n_{eq}/cm^2, showing excellent detection efficiency . Power dissipation has been investigated for the new prototypes

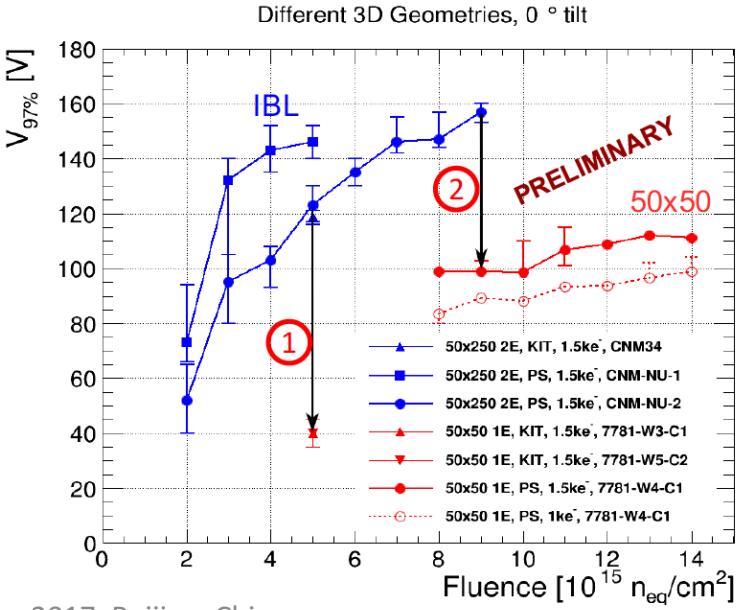
In both case they perform similarly or better than the IBL generation equivalent





Power dissipation 1.5 mW/cm² at 5e15 n_{eq}/cm^2 (vs 3.5 mW/cm² for IBL generation)



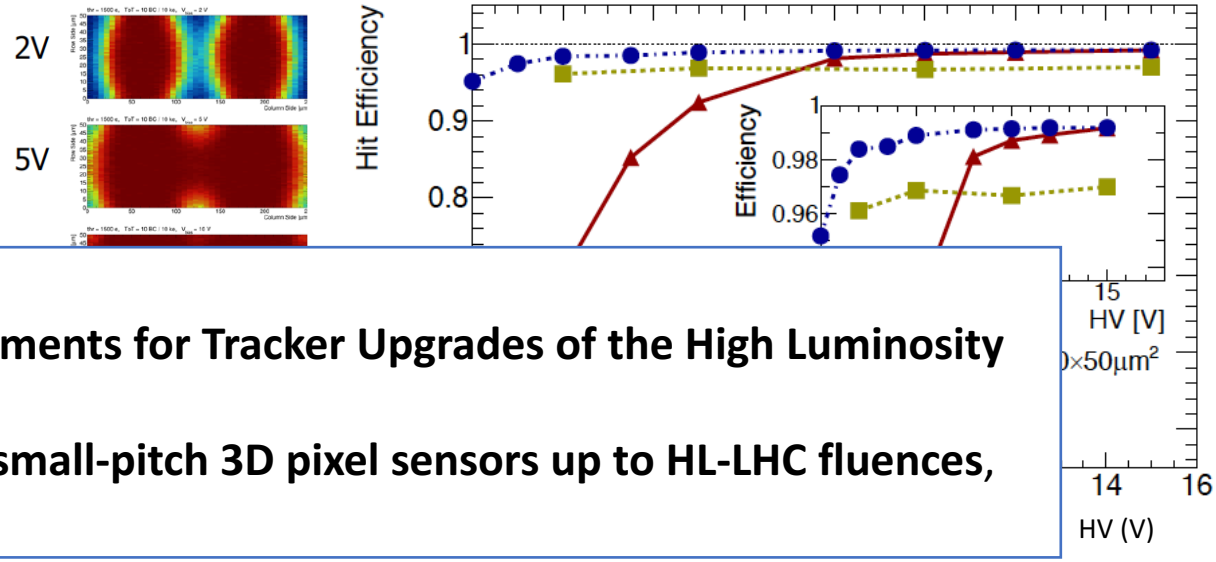


Beam test measurements of irradiated 3D pixel sensors with 50x50 μm² pixel size, D.Vasquez, Trento 2017

Pixel detectors : 3D Sensors

Small pitch sensors were investigated in test beam before and after irradiation up to 1.4e15 n_{eq}/cm^2, showing excellent detection efficiency . Power dissipa
for the

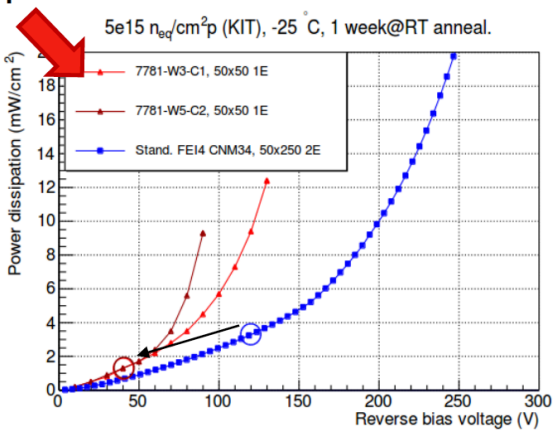
In bot
or bet
equiva

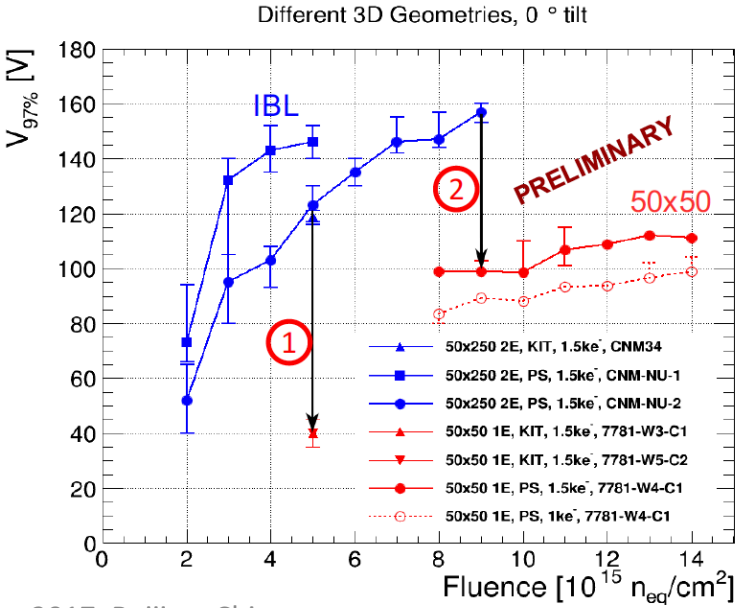


See :

- **Pixel Detector Developments for Tracker Upgrades of the High Luminosity LHC**, *Marco MESCHINI*
- **Radiation hardness of small-pitch 3D pixel sensors up to HL-LHC fluences**, *Joern LANGE*

Power dissipation 1.5 mW/cm² at 5e15 n_{eq}/cm^2 (vs 3.5 mW/cm² for IBL generation)





Beam test measurements of irradiated 3D pixel sensors with 50x50 μm² pixel size, D.Vasquez, Trento 2017

Pixel detectors : Planar sensors

For the HL-LHC ITk Pixel detector upgrade , the **Planar sensor technology**, used in the outer layers of ATLAS Inner Detector and IBL are the prime candidates for the inner and outer layers.

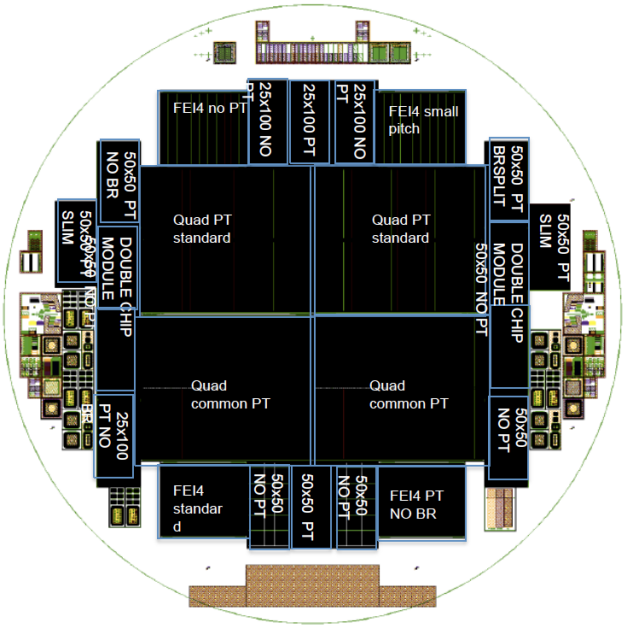
The main challenges for this technology are the following :

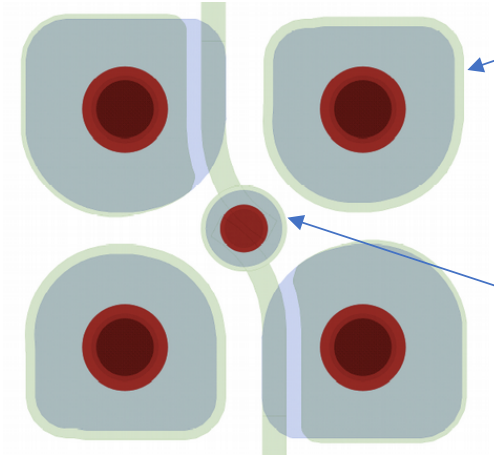
- **Low-Cost** for the outer layer where a large amount of modules are needed
- **Large area** as Quad Assemblies are foreseen to be used in Itk

➢ **Yield improvement needed**

- **Smaller pixel needed** (50x50 or 25x100 um^2)
  - Punch-Through structure, needed for improved yield is creating inefficiencies
  - Bias line steal signal after irradiation
- **Thinner sensors considered** (100-150um)
  - Lower signal
  - Lower occupancy

➢ **New improved design**

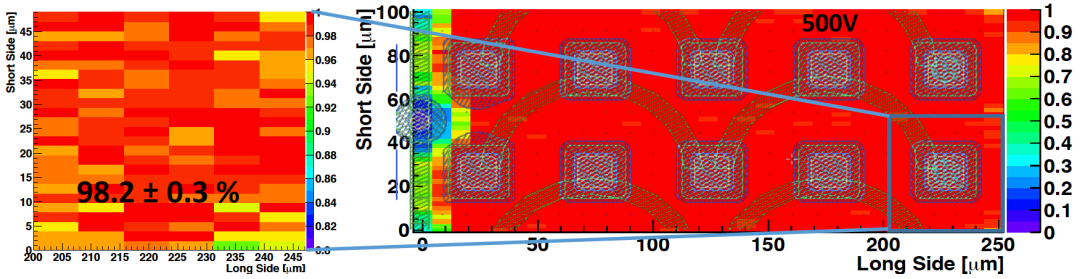




Pixel and Punch-Through structure design for 50x50 µm² pixels

Pixel detectors : Planar sensors

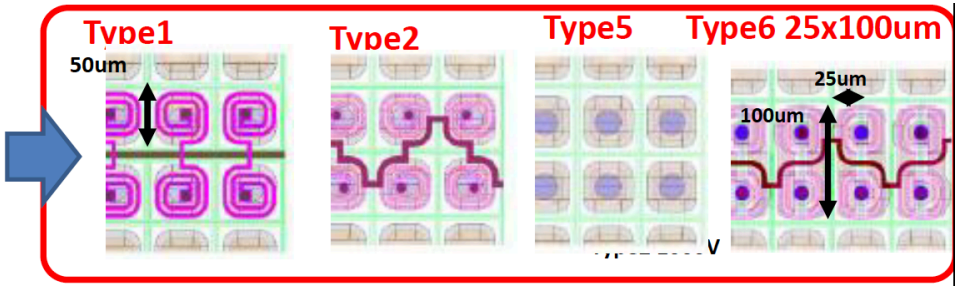
CiS-4 n-in-p production



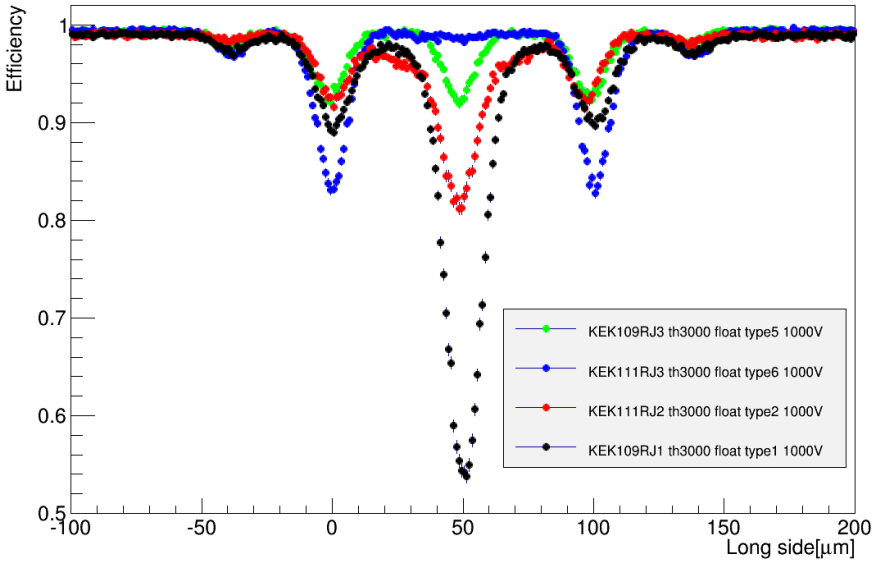
150µm thick sensor, irradiated to 3x10^{15} n_{eq}/cm^2

FEI4 (250x50 um^2 pixels) was the only available ASIC for testing smaller pitch device, several structure were adapted to the FEI4 to allow small pitch studies and extrapolate to the performance expected with the RD53 ASIC

Thin planar pixel sensor productions at MPP for the ATLAS ITk, A Macchiolo, Trento 2017



When assembling large area sensors, yield is an important parameter. The biasing structure on the sensors is important to identify good sensors before the bump-bonding This structure can lead to efficiency loss after irradiation and careful optimization of these structure is ongoing to minimize this

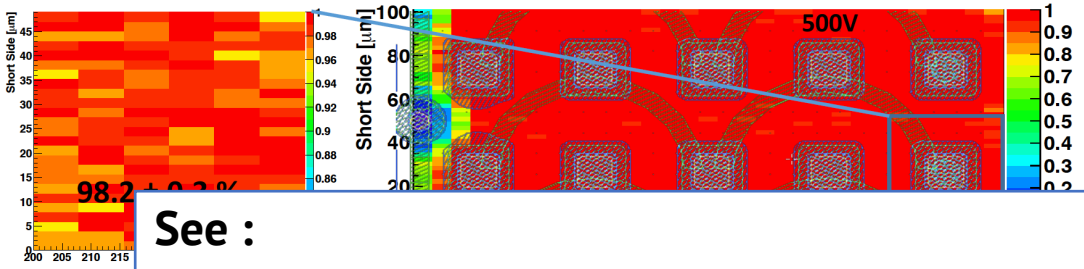


Proton Irrad 3x1E15 1MeV n_{eq}/cm^2

Latest results from development of n^+-in-p planar pixel sensors and LGAD devices by KEK/HPK, Y. Unno, Trento 2017

Pixel detectors : Planar sensors

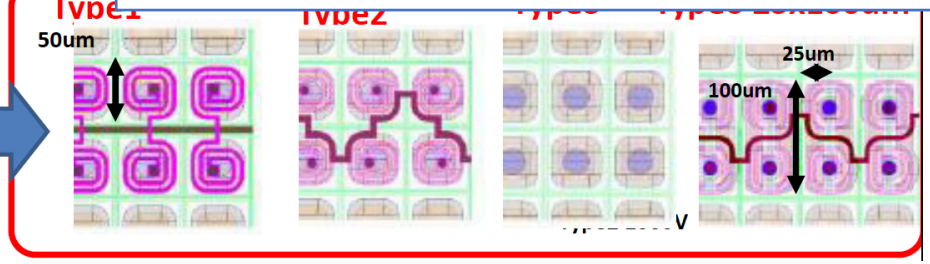
CiS-4 n-in-p production



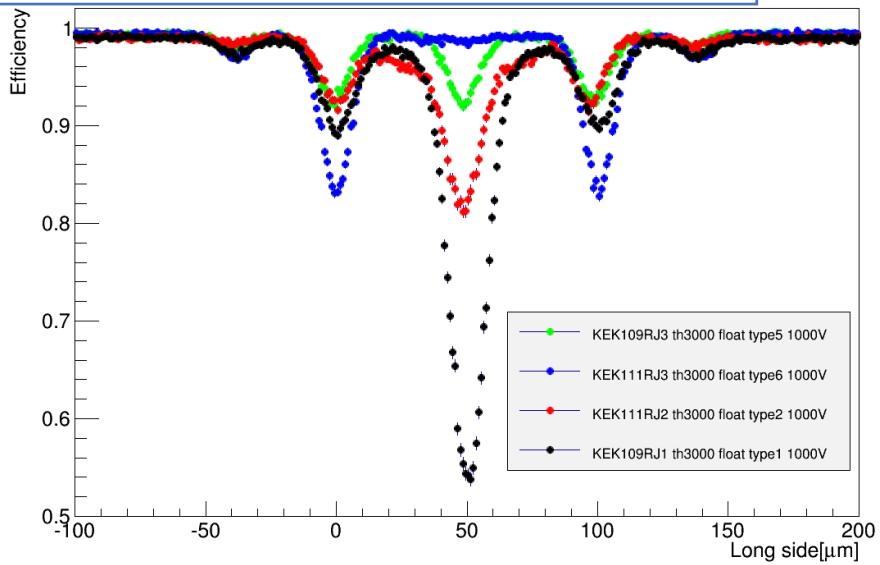
FEI4 (250x50 um^2 pixels) was the only available ASIC for testing smaller pitch device, several structure were adapted to the FEI4 to allow small pitch studies and extrapolate to the performance expected with the RD53 ASIC

See :

- **Pixel Detector Developments for Tracker Upgrades of the High Luminosity LHC**, *Marco MESCHINI*



When assembling large area sensors, yield is an important parameter. The biasing structure on the sensors is important to identify good sensors before the bump-bonding This structure can lead to efficiency loss after irradiation and careful optimization of these structure is ongoing to minimize this



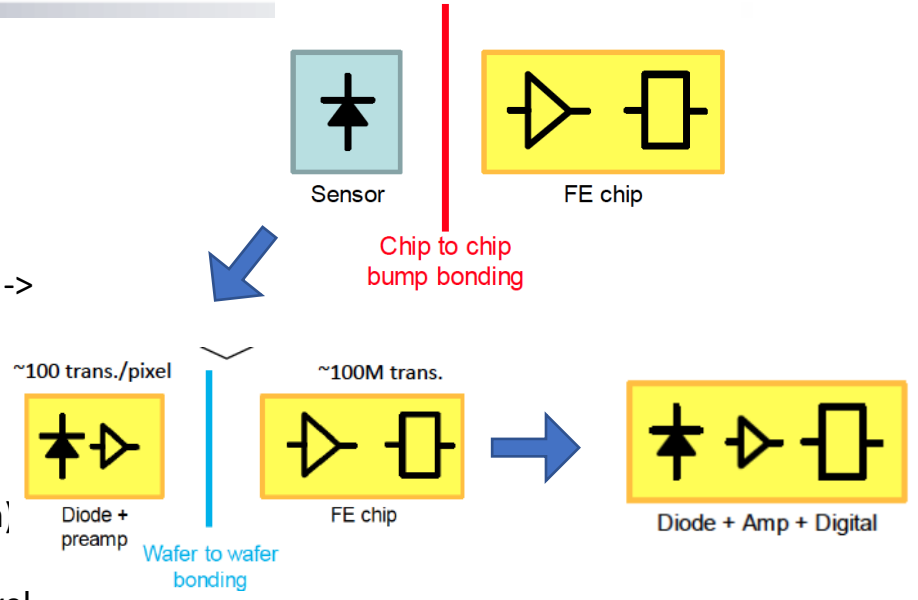
Proton Irrad 3x1E15 1MeV n_{eq}/cm^2

Latest results from development of n^+-in-p planar pixel sensors and LGAD devices by KEK/HPK, Y. Unno, Trento 2017

Pixel detectors : CMOS Sensors

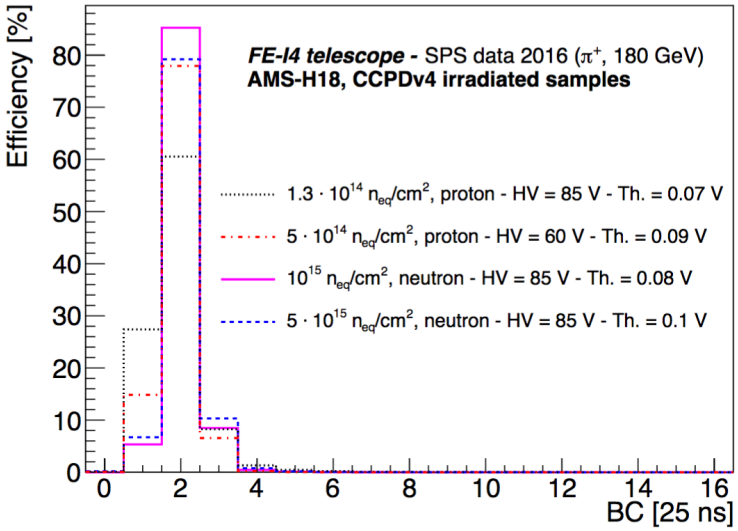
Planar and 3D technologies relies on **Passive High-Resistivity sensors**

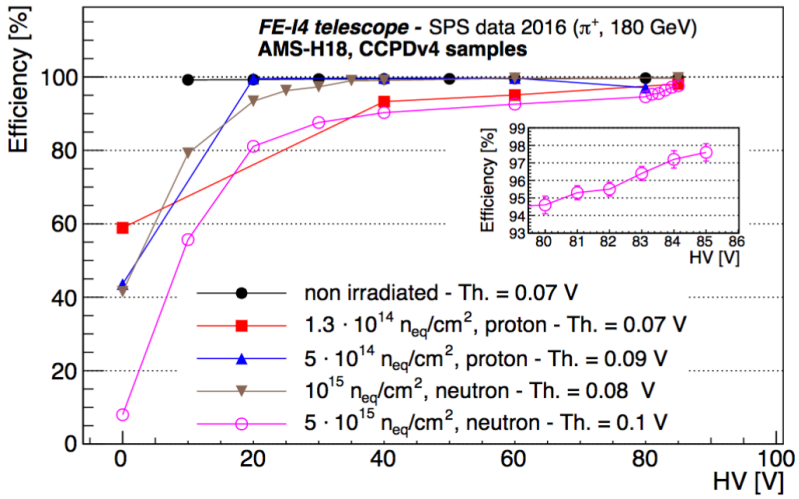
- **Specialty foundries** -> small production capabilities (6” wafers)
- **high-cost** per unit
- **Small signal** -> requires micro-soldering for DC coupling -> large cost



CMOS Technology present many advantages

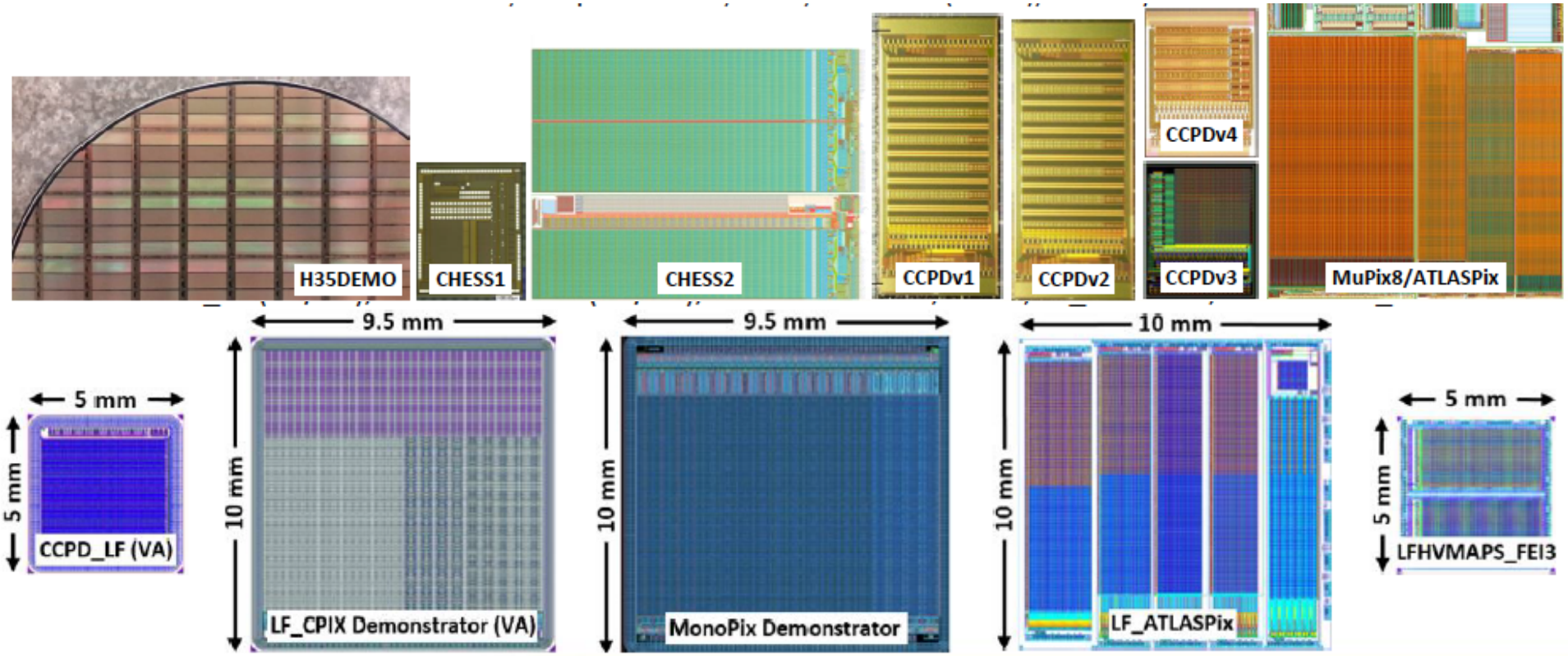
- **Large scale, low-cost** production possible
- **In-Pixel amplification** and logic possible (Well insulation)
- Capacitive coupling to readout CMOS ASIC
- Eventually , possibility to integrate **full electronics in-pixel**

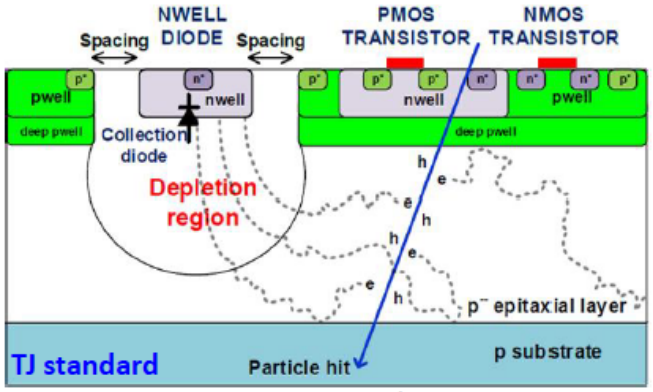




arXiv:1611.02669, M. Benoit et al.

Pixel detectors : CMOS Sensors





D. Kim et al., JINST 11 C02042, 2016

- **CMOS pixel development for the ATLAS experiment at the HL-LHC**, Branislav Ristic
- **Capacitively Coupled Pixel Detectors: From design simulations to test beam**, Mateus Vicente

Perspectives and Conclusion

ATLAS Itk Pixel project propose an ambitious upgrade of the current ATLAS Inner Detector and is moving towards the TDR at the end of 2017

- Peak luminosity: 5-7 x 10^{34} cm^{-2} s^{-1} ~ x 5-7
- Average pile-up: up to <μ> ~200 ~ x 8
- Integrated luminosity: more than 3000 fb^{-1} ~ x 10
- Requested radiation hardness: 2x10^{16} n_{eq}/cm^2 x 20

All system aspects are being addressed to cope with the new conditions and deliver an excellent Pixel detector for the Phase II of HL-LHC

- Mechanics and services are being optimized to offer better η coverage, lower material budget and more space points per track
- A new Readout ASIC is being developped to cope with the increased data rate, smaller pixel pitch and higher radiation dose
- Multiple sensor technologies are being studied to cope with the conditions at the different radii of the ITk Pixel detector
- Cost reduction strategies are being investigated for interconnect, sensor technologies and assembly process to cope with the large scale production needed for this project

Thank you for your attention !

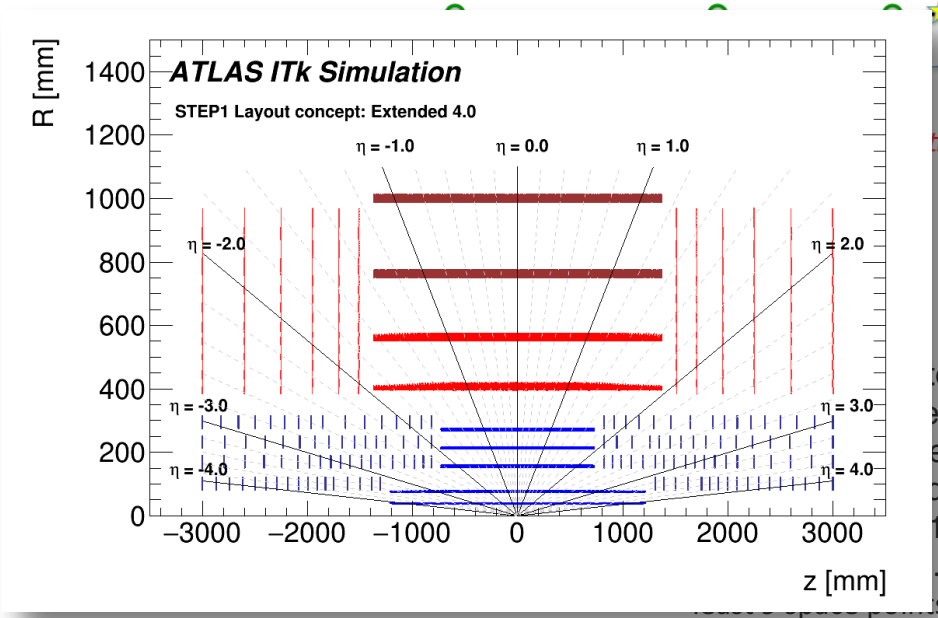
感谢您的关注

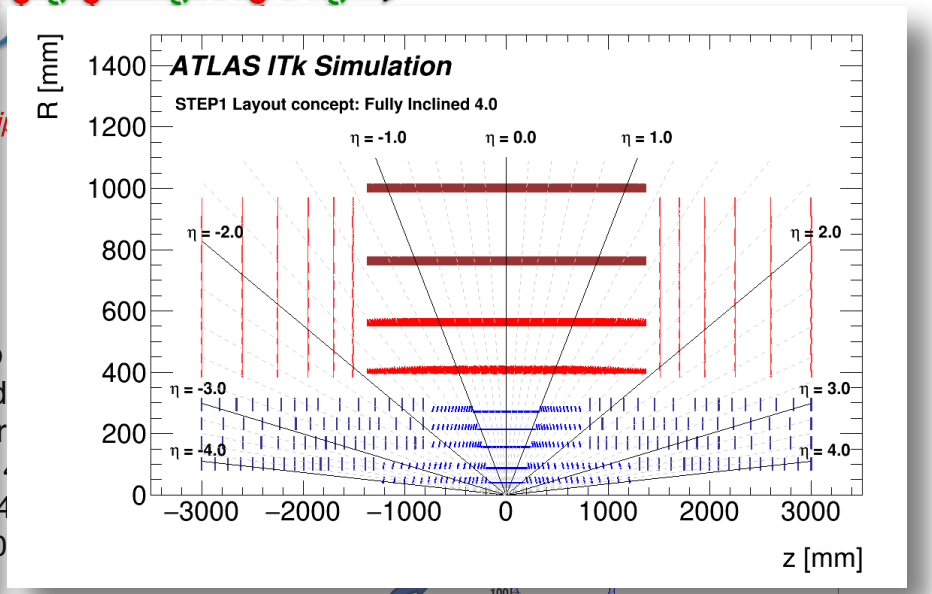
backup

Pixel Mechanics and Services

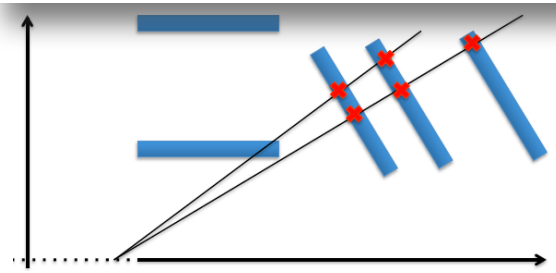
The layout of the ITk Pixel detector is currently under study by the Layout Task force to identify the final layout to be implemented among the one proposed by the community, with different barrel and disk geometry and different Eta coverage.

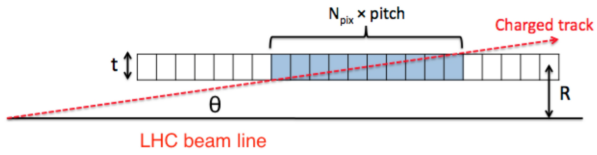
2012 LoI | Q4 2015 Step1.0 | Q2 2016 Step1.5 | Q4 2016 Step1.6 | Q1 2017 Step2.0 | Step3.0





- Pixel innermost detector replaceable.





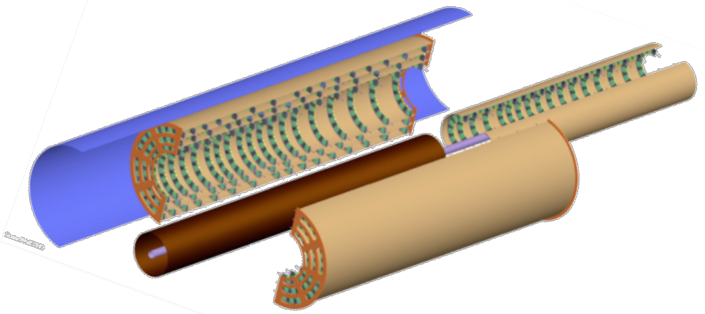
$$N_{pix} = \frac{t}{\tan\theta \times p}$$

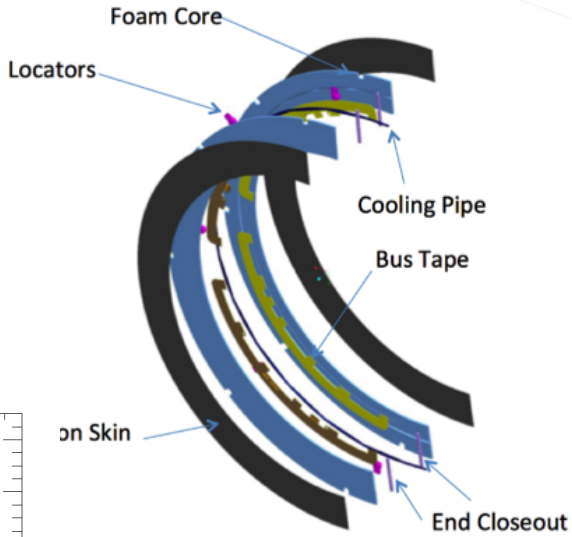
Pixel Mechanics and Services

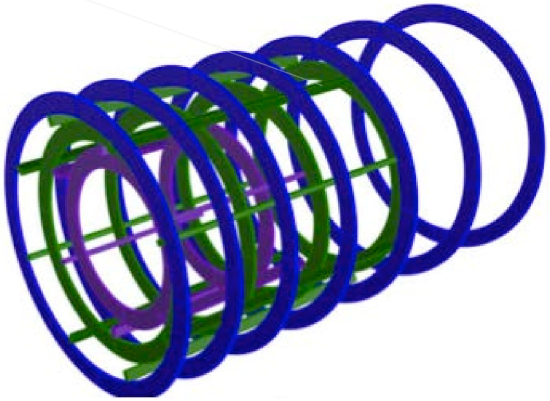
Forward Region

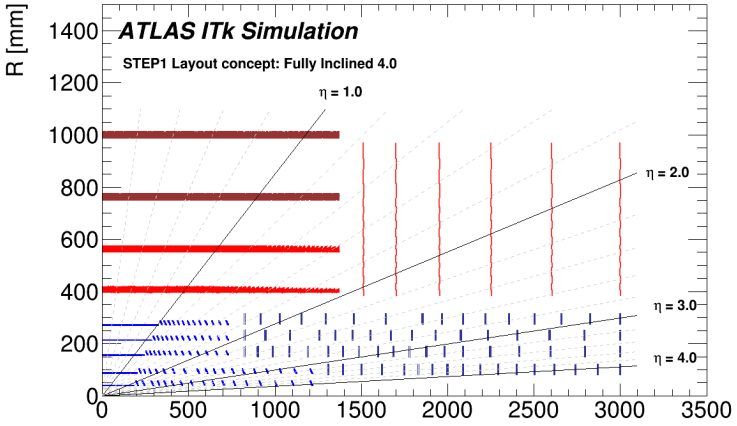
The forward region will be consist of four layers of ring located a different radii and z

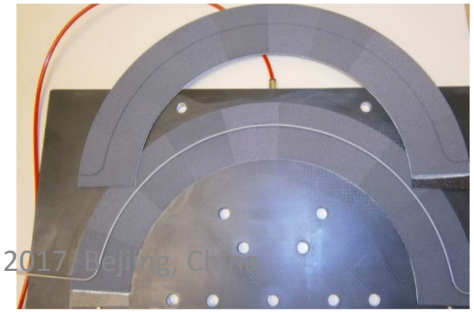
- Compared to disk, ring offer more flexibility for maintaining hermeticity
- Each ring consists of a carbon core containing cooling and electrical services.
- Rings are built out of two half-rings, for ease of construction
- Modules are mounted on both sides of each ring to allow overlap

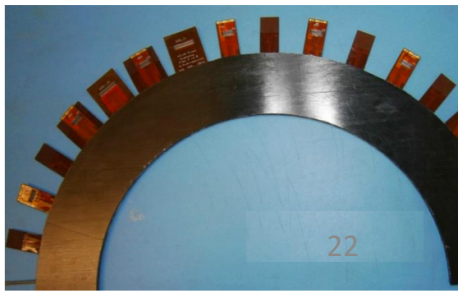






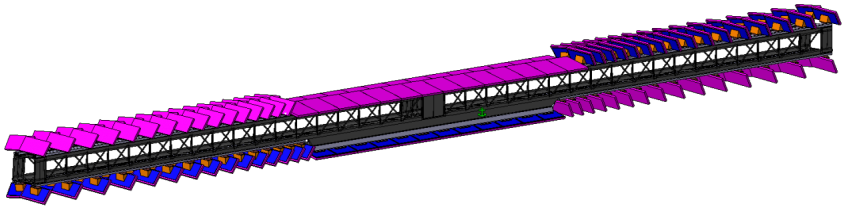




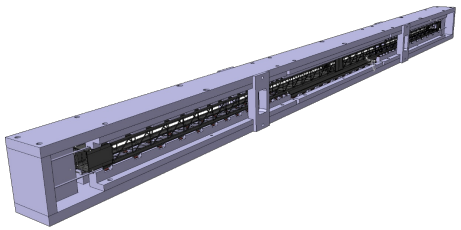


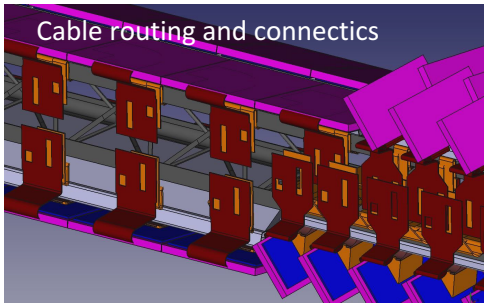
Pixel Mechanics and Services

- **Demonstrator program** : Evaluation and validation of a complete SLIM Longeron
  - mechanical integration, DCS + serial powering, multi-module readout, electrical and thermal performance, system-test
- SLIM Layer 2+3 longeron (1.6 m)
  - 4 cooling lines:
    - One cooling line equipped with electrical modules
    - The rest with thermo-mechanical dummy modules (with heaters)
      - Dedicated stave-flexes for either electrical or dummy modules
- Serial powering scheme, stave-flex running inside longeron
- PSPP chips and DCS controller emulator (FPGA) at both ends
- Multiple readout systems
- CO_2 Cooling

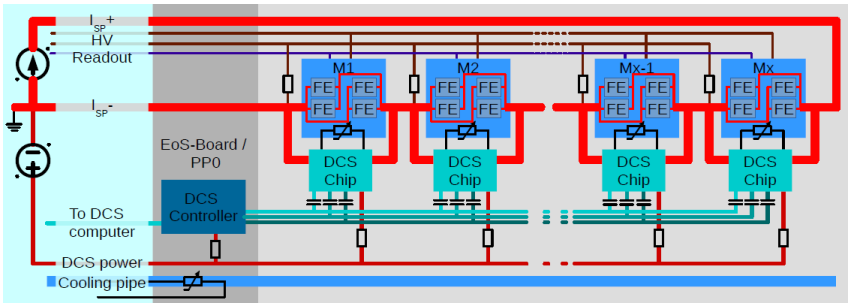


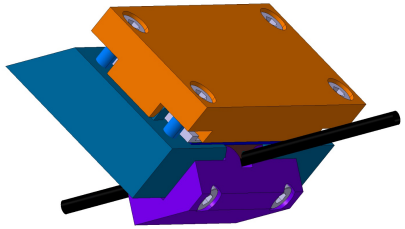
Assembly jig design





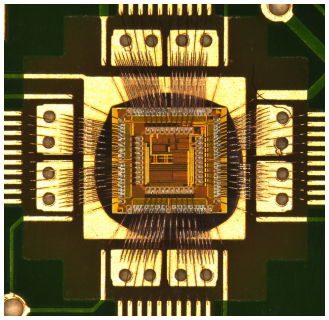
Serial powering scheme





Cell integration

Data transmission scheme



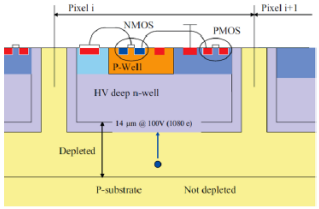
DCS Chip testing for serial powering

Pixel detectors : CMOS Sensors

ams 0.35 µm/180 nm

Key features:

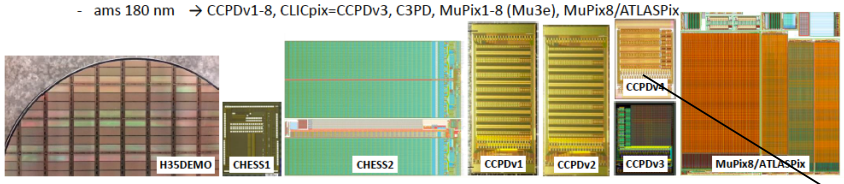
- **Technology node** 0.35 µm/180 nm
- **Wells** No possibility of isolating n-wells from the collecting deep n-well. No CMOS electronics in the sensor area. Can induce cross-talk.
- **Metal layers** 4/6
- **HR** 20 (standard value) – 1k Ω·cm (since 2015/6)
- **HV** -150 V < HV < 0 V
- **Depletion region** 140 µm thick
- **Backside biasing** Not possible
- **Stitching** Not possible



I. Peric, NIMA 650 pp. 158-162, 2011

Prototypes:

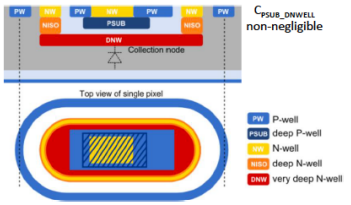
- ams 0.35 µm → Initial R&D developments, H35CCPDv1-2, H35DEMO, HVStrip, CHESS1-2 (strips)
- ams 180 nm → CCPDv1-8, CLICpix=CCPDv3, C3PD, MuPix1-8 (Mu3e), MuPix8/ATLASPix



LFoundry 150 nm

Key features:

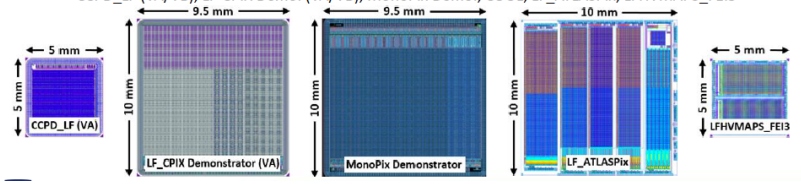
- **Technology node** 150 nm
- **Wells** Deep p-well (PSUB) to isolate n-wells from deep n-well (collecting electrode). Full CMOS electronics are possible in the sensor area.
- **Metal layers** 6
- **HR** 10 Ω·cm – ~4k Ω·cm
- **HV** -120 V < HV < 0 V
- **Depletion region** ~170 µm thick @ -110 V
- **Backside biasing** Possible
- **Stitching** Possible



P. Rymaszewski, JINST 11 C02045, 2016

Prototypes:

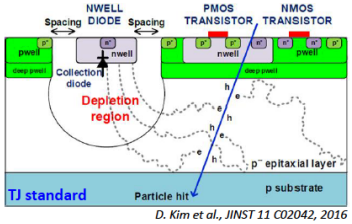
- CCPD_LF (VA/VB), LF-CPIX Demo. (VA/VB), MonoPix Demo., COOL, LF_ATLASPix, LFHVMAPS_FEI3



TowerJazz 180 nm

Key features:

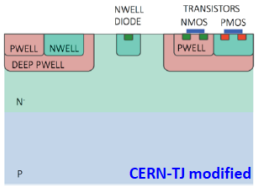
- **Technology node** 180 nm
- **Wells** Deep p-well to isolate n-wells from p-epi layer. Full CMOS electronics are possible in the sensor area.
- **Metal layers** 6
- **Gate oxide** 3 nm (good for radiation tolerance)
- **HR** 1k – 8k Ω·cm
- **HV** -6 V < HV < 0 V
- **Epi-layer** 18 – 40 µm thick
- **Backside biasing** Possible
- Small n-well diode → low sensor capacitance (~5 fF) → higher gain, better SNR, faster signal and potentially lower power consumption



D. Kim et al., JINST 11 C02042, 2016

CERN-TJ modified process:

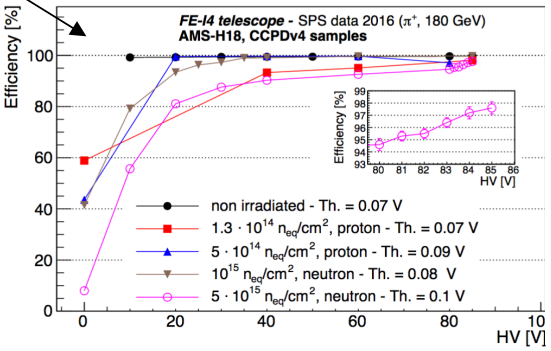
- Normally, small electrodes produce weak fields under deep p-wells and signal collection after irradiation becomes difficult on edges (efficiency drop towards pixel edges)
- CERN-TJ → Add planar n-type layer to significantly improve lateral depletion and charge collection after irradiation. Implemented in Investigator test chip.

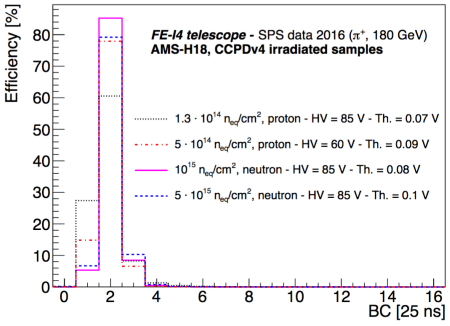


H. Pernegger, Trento Workshop, 2017

Prototypes:

- ALPIDE (ALICE upgrade chip), MISTRAL, ASTRAL, CHERWELL, Explorer, Investigator, MALTA, MonoPix





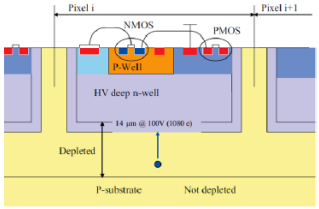
Fluence [n_{eq}/cm^2]	Average Hit Efficiency
$1.3 \cdot 10^{14}$	98.1%
$5 \cdot 10^{14}$	99.7%
$1 \cdot 10^{15}$	99.7%
$5 \cdot 10^{15}$	97.6%

Pixel detectors : CMOS Sensors

ams 0.35 µm/180 nm

Key features:

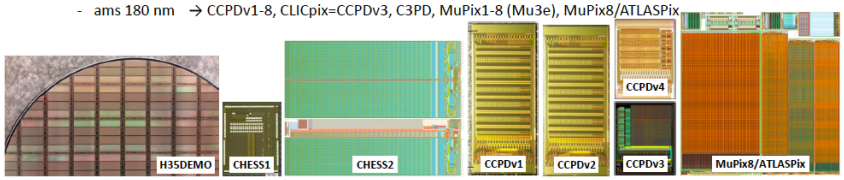
- **Technology node** 0.35 µm/180 nm
- **Wells** No possibility of isolating n-wells from the collecting deep n-well. No CMOS electronics in the sensor area. Can induce cross-talk.
- **Metal layers** 4/6
- **HR** 20 (standard value) – 1k Ω·cm (since 2015/6)
- **HV** -150 V < HV < 0 V
- **Depletion region** 140 µm thick
- **Backside biasing** Not possible
- **Stitching** Not possible



I. Peric, NIMA 650 pp. 158-162, 2011

Prototypes:

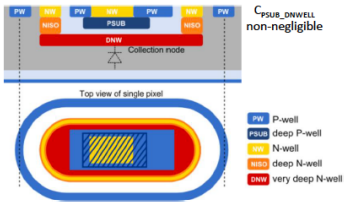
- ams 0.35 µm → Initial R&D developments, H35CCPDv1-2, H35DEMO, HVStrip, CHESS1-2 (strips)
- ams 180 nm → CCPDv1-8, CLICpix=CCPDv3, C3PD, MuPix1-8 (Mu3e), MuPix8/ATLASPix



LFoundry 150 nm

Key features:

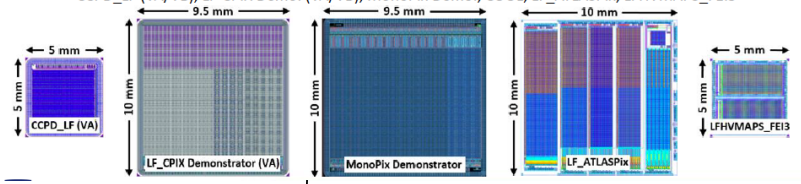
- **Technology node** 150 nm
- **Wells** Deep p-well (PSUB) to isolate n-wells from deep n-well (collecting electrode). Full CMOS electronics are possible in the sensor area.
- **Metal layers** 6
- **HR** 10 Ω·cm – ~4k Ω·cm
- **HV** -120 V < HV < 0 V
- **Depletion region** ~170 µm thick @ -110 V
- **Backside biasing** Possible
- **Stitching** Possible



P. Rymaszewski, JINST 11 C02045, 2016

Prototypes:

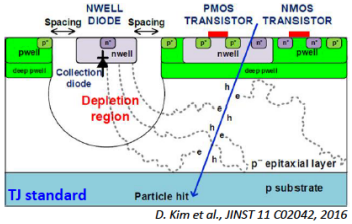
- CCPD_LF (VA/VB), LF-CPIX Demo. (VA/VB), MonoPix Demo., COOL, LF_ATLASPix, LFHVMAPS_FEI3



TowerJazz 180 nm

Key features:

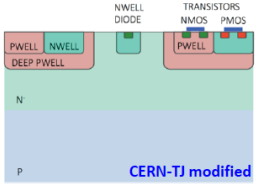
- **Technology node** 180 nm
- **Wells** Deep p-well to isolate n-wells from p-epi layer. Full CMOS electronics are possible in the sensor area.
- **Metal layers** 6
- **Gate oxide** 3 nm (good for radiation tolerance)
- **HR** 1k – 8k Ω·cm
- **HV** -6 V < HV < 0 V
- **Epi-layer** 18 – 40 µm thick
- **Backside biasing** Possible
- Small n-well diode → low sensor capacitance (~5 fF) → higher gain, better SNR, faster signal and potentially lower power consumption



D. Kim et al., JINST 11 C02042, 2016

CERN-TJ modified process:

- Normally, small electrodes produce weak fields under deep p-wells and signal collection after irradiation becomes difficult on edges (efficiency drop towards pixel edges)
- CERN-TJ → Add planar n-type layer to significantly improve lateral depletion and charge collection after irradiation. Implemented in Investigator test chip.

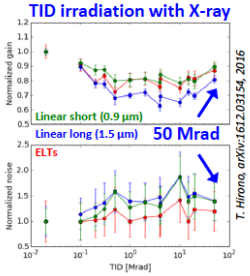


H. Pernegger, Trento Workshop, 2017

Prototypes:

- ALPIDE (ALICE upgrade chip), MISTRAL, ASTRAL, CHERWELL, Explorer, Investigator, MALTA, MonoPix

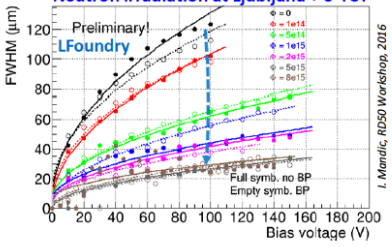
TID irradiation with X-ray



T. Hirono, arXiv:1612.03154, 2016

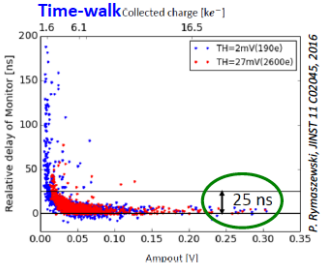
Chips functional after irradiation, but with 20-30% less gain

Neutron irradiation at Ljubljana + e-TCT



I. Mandic, RD50 Workshop, 2016

Time-walk Collected charge [ke⁻]



P. Rymaszewski, JINST 11 C02045, 2016

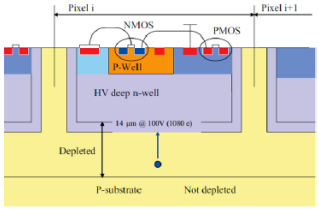
High threshold (2600 e⁻) → 79% hits in-time
Low threshold (190 e⁻) → 91 % hits in-time

Pixel detectors : CMOS Sensors

ams 0.35 µm/180 nm

Key features:

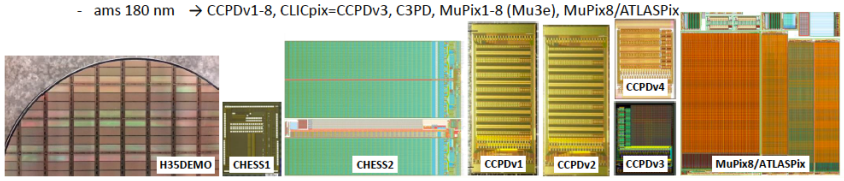
- **Technology node** 0.35 µm/180 nm
- **Wells** No possibility of isolating n-wells from the collecting deep n-well. No CMOS electronics in the sensor area. Can induce cross-talk.
- **Metal layers** 4/6
- **HR** 20 (standard value) – 1k Ω·cm (since 2015/6)
- **HV** -150 V < HV < 0 V
- **Depletion region** 140 µm thick
- **Backside biasing** Not possible
- **Stitching** Not possible



I. Peric, NIMA 650 pp. 158-162, 2011

Prototypes:

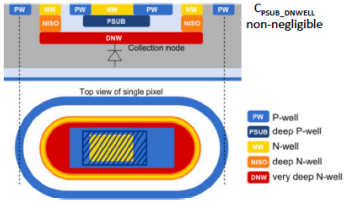
- ams 0.35 µm → Initial R&D developments, H35CCPDv1-2, H35DEMO, HVStrip, CHESS1-2 (strips)
- ams 180 nm → CCPDv1-8, CLICpix=CCPDv3, C3PD, MuPix1-8 (Mu3e), MuPix8/ATLASPix



LFoundry 150 nm

Key features:

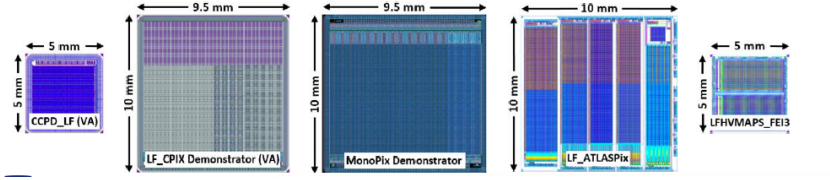
- **Technology node** 150 nm
- **Wells** Deep p-well (PSUB) to isolate n-wells from deep n-well (collecting electrode). Full CMOS electronics are possible in the sensor area.
- **Metal layers** 6
- **HR** 10 Ω·cm – ~4k Ω·cm
- **HV** -120 V < HV < 0 V
- **Depletion region** ~170 µm thick @ -110 V
- **Backside biasing** Possible
- **Stitching** Possible



P. Rymaszewski, JINST 11 C02045, 2016

Prototypes:

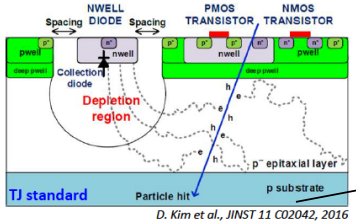
- CCPD_LF (VA/VB), LF-CPIX Demo. (VA/VB), MonoPix Demo., COOL, LF_ATLASPix, LFHVMAPS_FEI3



TowerJazz 180 nm

Key features:

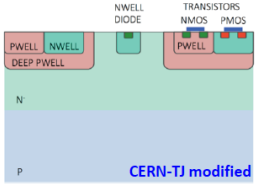
- **Technology node** 180 nm
- **Wells** Deep p-well to isolate n-wells from p-epi layer. Full CMOS electronics are possible in the sensor area.
- **Metal layers** 6
- **Gate oxide** 3 nm (good for radiation tolerance)
- **HR** 1k – 8k Ω·cm
- **HV** -6 V < HV < 0 V
- **Epi-layer** 18 – 40 µm thick
- **Backside biasing** Possible
- Small n-well diode → low sensor capacitance (~5 fF) → higher gain, better SNR, faster signal and potentially lower power consumption



D. Kim et al., JINST 11 C02042, 2016

CERN-TJ modified process:

- Normally, small electrodes produce weak fields under deep p-wells and signal collection after irradiation becomes difficult on edges (efficiency drop towards pixel edges)
- CERN-TJ → Add planar n-type layer to significantly improve lateral depletion and charge collection after irradiation. Implemented in Investigator test chip.



H. Pernegger, Trento Workshop, 2017

Prototypes:

- ALPIDE (ALICE upgrade chip), MISTRAL, ASTRAL, CHERWELL, Explorer, Investigator, MALTA, MonoPix