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A high-resolution clock phase-shifter in a 65 nm CMOS technology

The design of a high-resolution phase-shifter which is part of the LpGBT, a low power upgrade of the gigabit transceiver (GBTX) for the LHC upgrade program, is presented. The phase-shifter circuit aims at producing a programmable phase rotation (up to 360°) with a time resolution of 48.8 ps for several input clock frequencies: 40, 80, 160, 320, 640 or 1280 MHz. The circuit is implemented as two functional blocks: a coarse phase-shifter, with a fully digital implementation, and fine phase-shifter, based on a Delay-Locked Loop (DLL). The course phase-shifter implements a full 360° phase rotation with a resolution of 781.25 ps while the fine phase-phase shifter further interpolates within the 781.25 ps interval down to 48.8 ps. The leading edge of the reference clock is delayed by 781.25 ps to serve as a reference to the DLL. The leading edge of the reference clock also propagates in a 16-stage Voltage Controlled Delay Line (VCDL) within DLL and is used as the second input of the phase comparator. When the DLL is locked, the VCDL outputs 16 clock signals with equally spaced phases. By selecting one of the VCDL outputs the 48.8 ps resolution is achieved. The post-layout simulations show that the peak-to-peak values of INL and DNL are 0.1 and 0.06 LSB (48.8 ps) respectively at 1.28 GHz in the nominal corner while at 40 MHz the values are 0.06 and 0.05 LSB respectively. The phase-shifter has been designed as a radiation-tolerant circuit by means of enclosed layout transistors (ELT) in a 65 nm CMOS technology to achieve high resolution and reduced power dissipation. The typical power dissipation of the fine phase-shifter at the lowest and the highest frequencies are 1.1 mW and 9.1 mW respectively at 1.2 V supply voltage.

Primary authors: Mr YANG, Dongxu (USTC); Mr KULIS, Szymon (CERN)

Co-authors: Mr GONG, Datao (SMU); Mr WANG, Jian (USTC); Mr YE, Jingbo (SMU); Mr MOREIRA, Paulo (CERN)

Presenter: Mr YANG, Dongxu (USTC)

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