Upgrade of the ATLAS Tile Calorimeter for the High Luminosity LHC

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on Behalf of the ATLAS Tile Calorimeter System

Outline

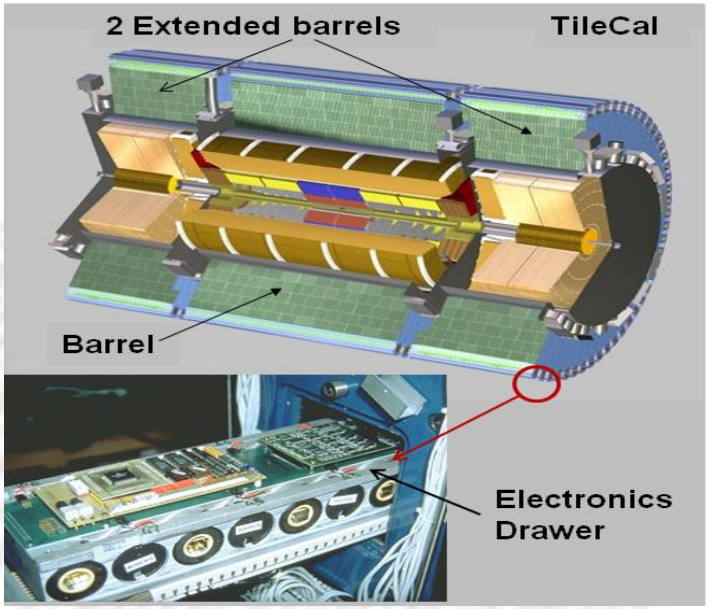
- Overview of TileCal on- and off-detector readout electronics at LHC
- Requirements of TileCal readout electronics for the HL-LHC
- Status of upgrade TileCal on-detector electronics
- Performance and radiation tolerance tests
- Back-end readout electronics
- Summary

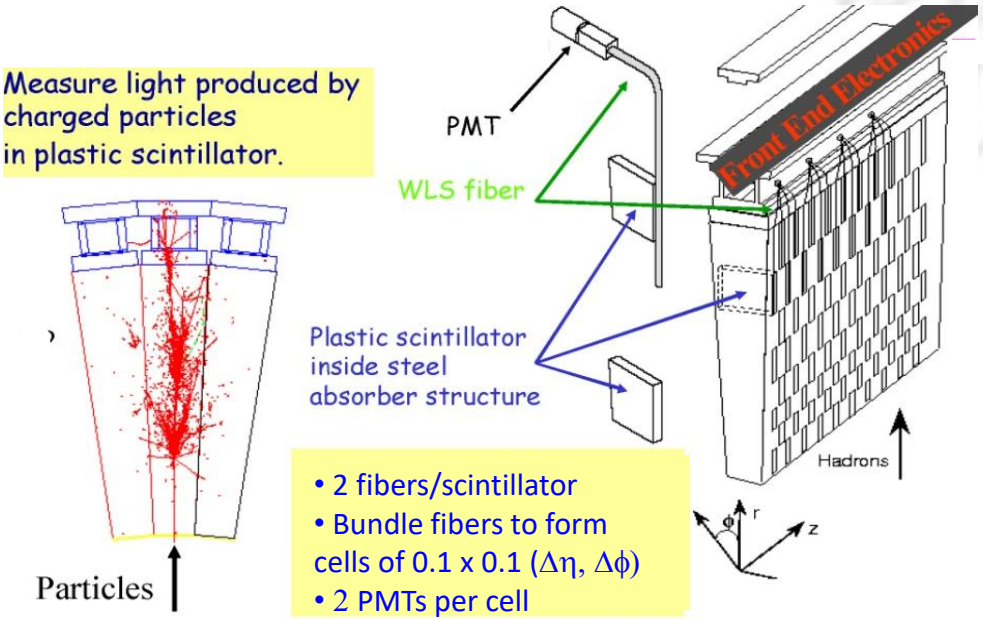
Overview of Tile Calorimeter Readout System at LHC

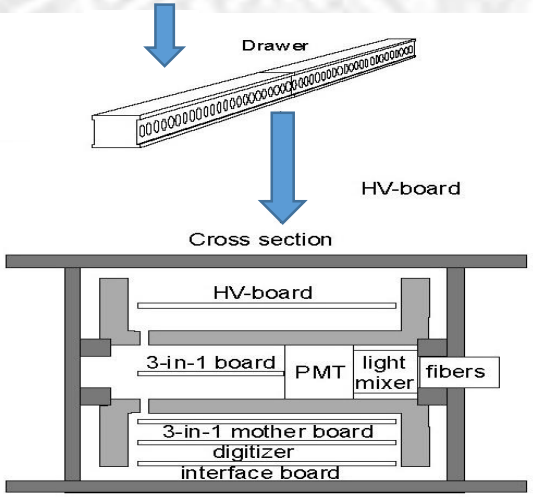
- TileCal measures light produced by charged particles in plastic scintillators.

  → one long barrel in 2 segments and 2 extended barrel segments with 256 detector modules

- Readout ~10000 PMTs with 16-bit readout dynamic range (30 MeV to 2 Tev)
- Analog trigger & Cesium, CIS, Laser calibrations



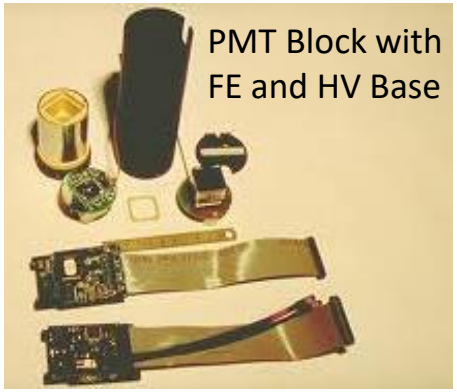


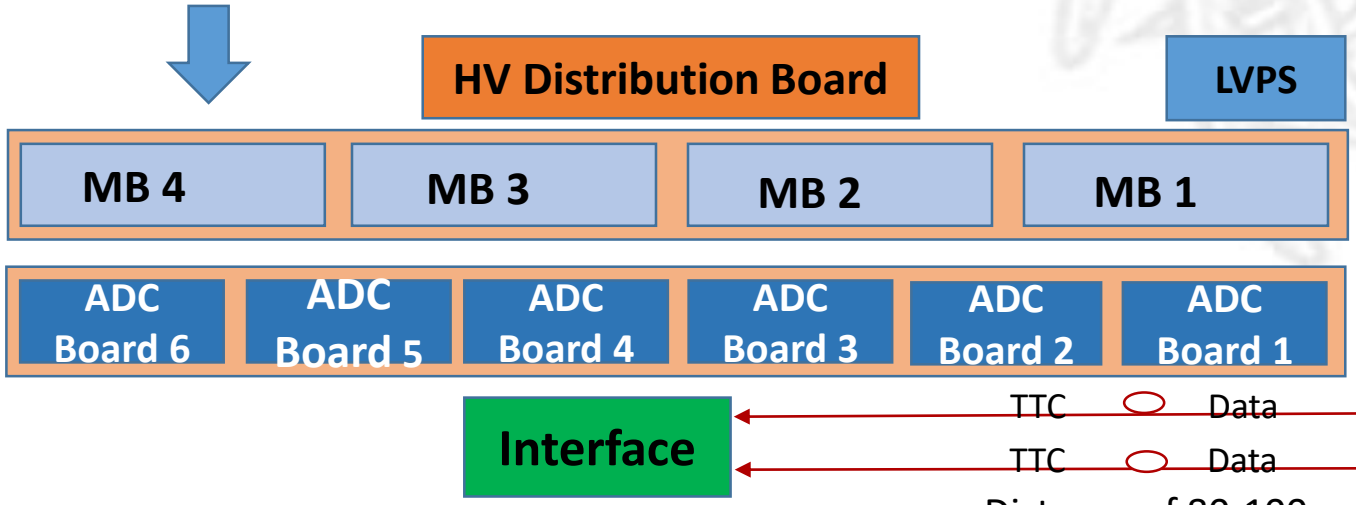


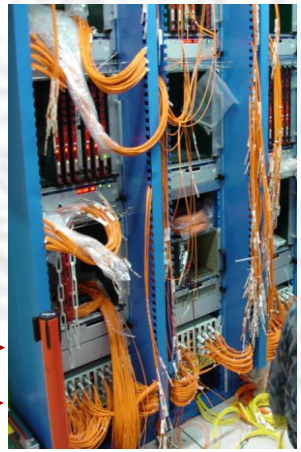
TileCal Drawer Electronics at LHC

256 electronics drawers, each contains 10 types of electronic boards:

1. Up to 45 PMT blocks
2. 4 different Mother boards
3. 1 TTCrx Mezzanine card
4. 6 Digitizing boards with data management
5. Up to 10 Summation card for analog trigger
6. 1 Interface card with 2 pairs of optical links for TTC and data
   → rate of 640Mbps each (one pair is redundant)
7. 1 HV distribution board and 1 LVPS module







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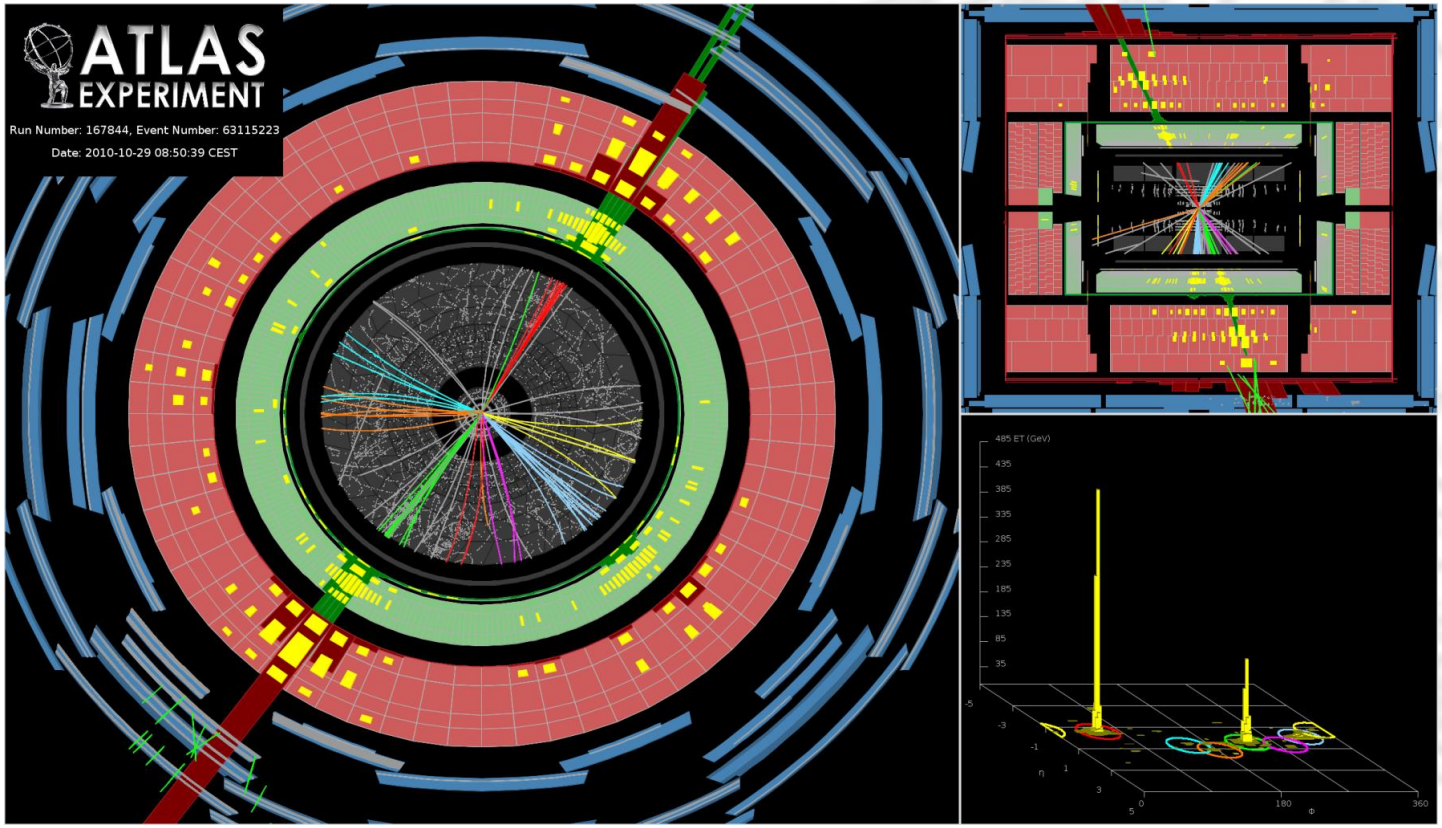
First Demonstrated Hadron Event by TileCal at LHC

Event display of Run 167607, Event 63115223. Showing a central high-pT jet of 1.5 TeV with an invariant mass of 2.8 TeV, collected during 2010.

→ The jets have (pT, y) of (1.5 TeV, -0.58) and (1.0 TeV, 0.44) respectively. The missing ET in the event is 310 GeV. (ATLAS-CONF-2011-047, CERN, March 2011)



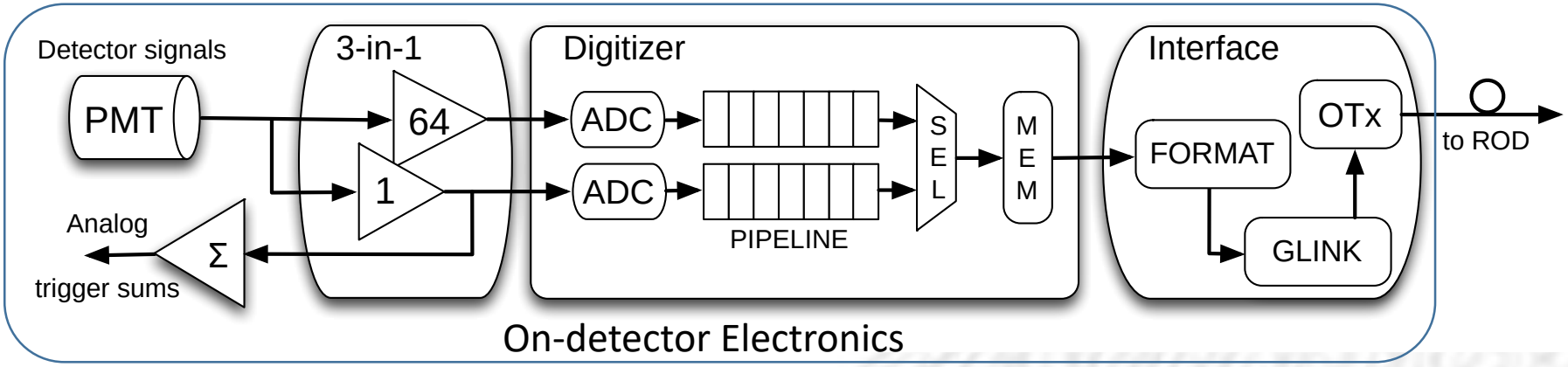
TileCal Upgrade Requirements for HL-LHC

- Increase LHC luminosity to ~ 5-7.5 x 10^{34} $cm^{-2}s^{-1}$ at Phase 2
- With higher luminosity the system will have to cope with considerably more complicated events, making the task of the Level-1 trigger more complex, requiring more data from the FE and more time for processing, collecting and sending all raw data to the counting room in digital trigger (40 MHz)
- Flexible configuration of trigger towers with improved resolution
- Most front-end and back-end electronics need to cope with higher data rates and provide higher reliability and robustness
- Require higher radiation tolerance for the on-detector electronics
- Avoid single point failures
- Better muon identification
- The current electronics system was built 20 years ago, considerable effects of radiation damage and components obsolete

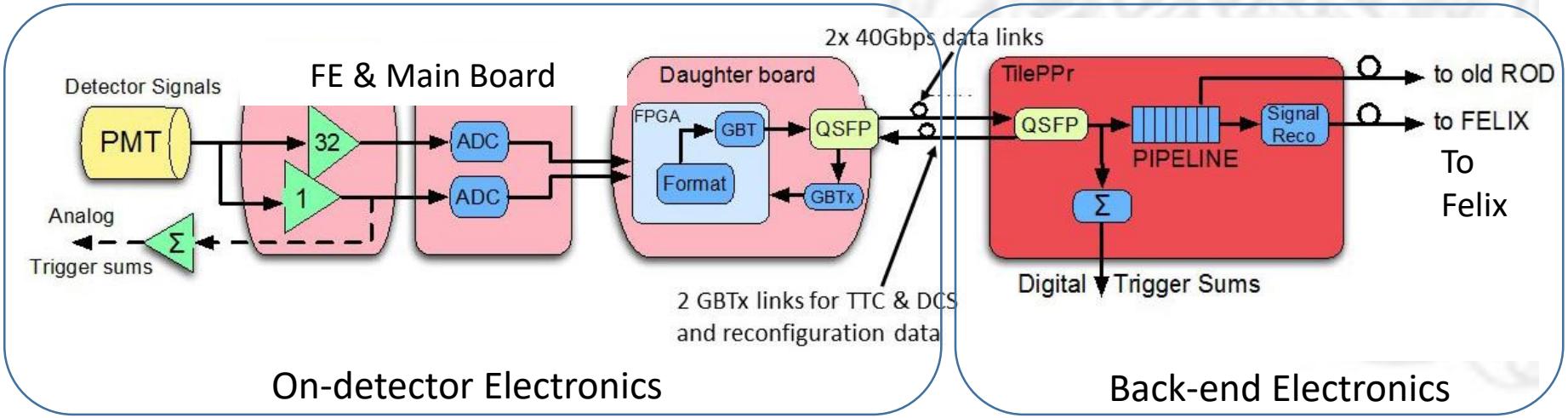
All TileCal electronics must be replaced to satisfy new requirements

TileCal System Structures at LHC and HL-LHC

TileCal Electronics System Diagram at LHC



TileCal Electronics System Diagram at HL-LHC

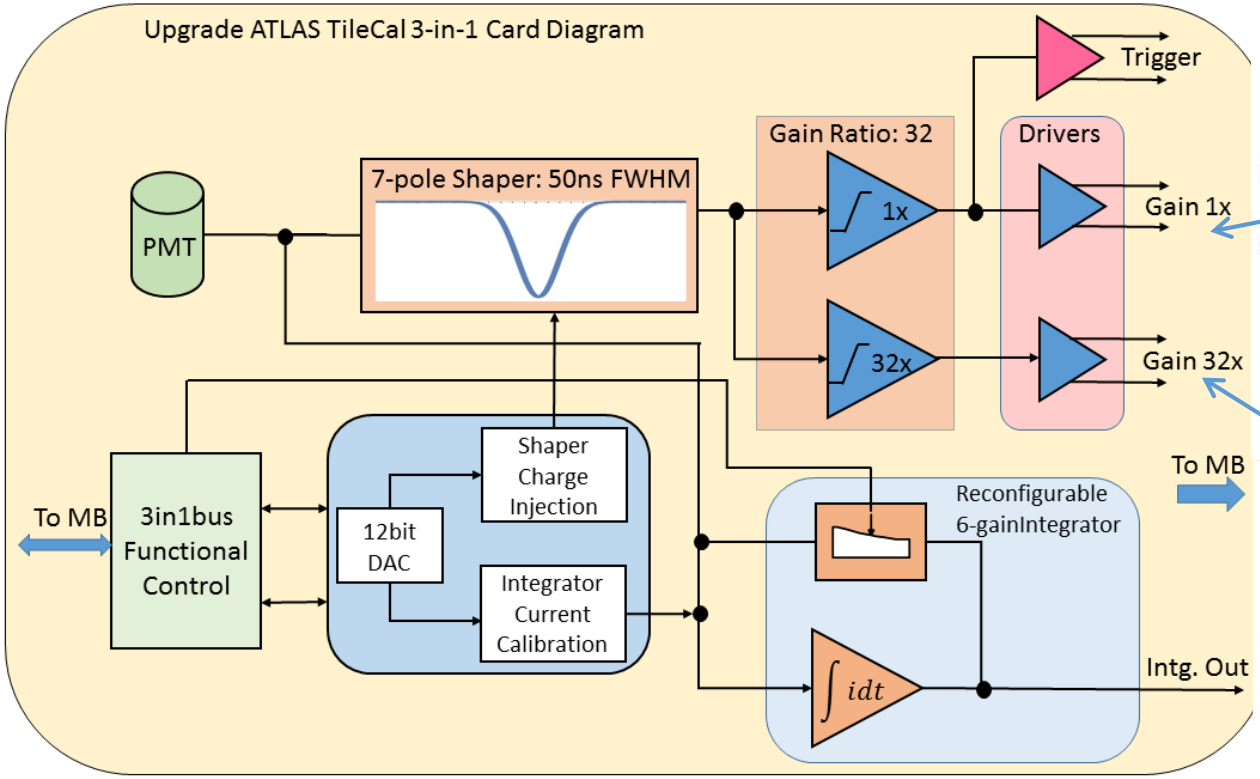


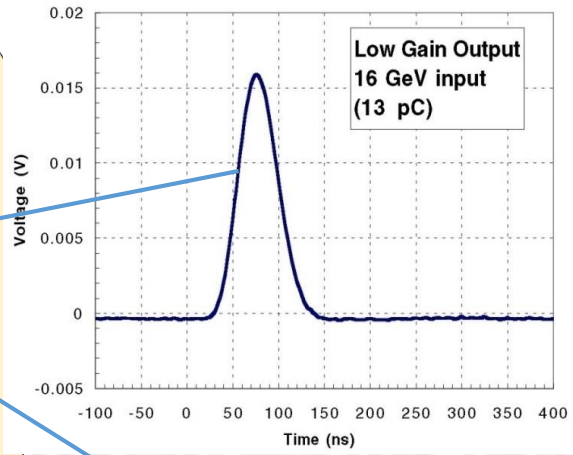
3 Optional Front-end Electronics Developed

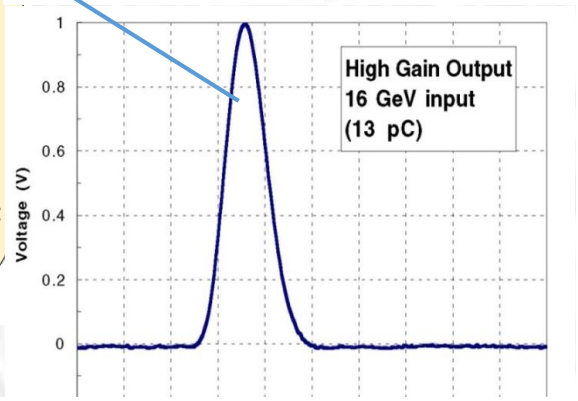
- 3-in-1 front-end electronics at UChicago, USA … (shaped pulse + slow integrator)
- QIE based FE at ANL, USA … (gated integrator and ADC)
- FATALIC based FE at Clermont, France … (current conveyer and ADC)

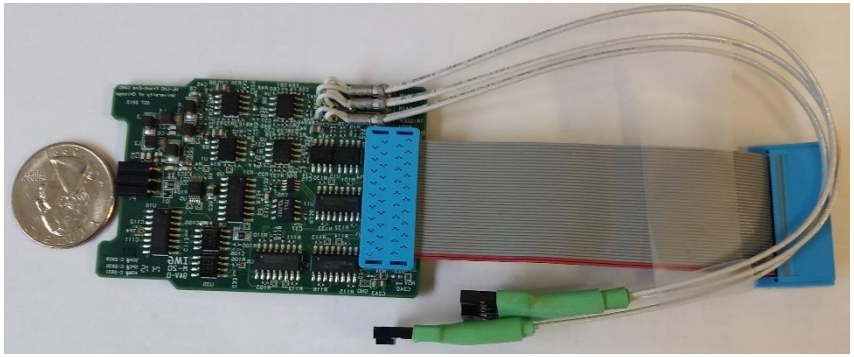
Parameter	3-in-1	QIE	FATALIC
Range	2 (32:1)	4 (16/23: 4/23: 2/23: 1/23)	3 (64:8:1)
Shaping time	25 ns	N/A	25 ns
Analog bandwidth	12.5 MHz	1 GHz	7 MHz
Shaped pulse width	50 ns FWHM	Raw Pulse	45 ns FWHM
Readout dynamic range	17 (or 18)	18	18
ADC	2 x 12b (ext.)	4 x 7b (built-in)	3 x 12b (built-in)
Readout latency	6 x 25 ns	4 x 25 ns	8 x 25 ns
Slow Integ. dyn. range	0-10 uA	0-5 uA	0.3 nA – 1.25 uA
Cost	1703 kCHF	1637 kCHF	1742 kCHF

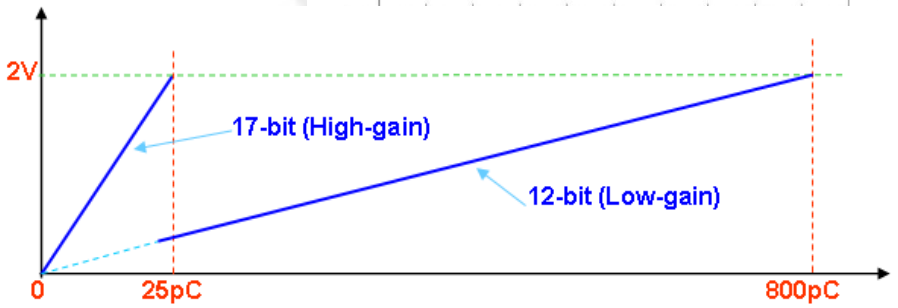
Option-1: 3-in-1 Card Front-end Electronics











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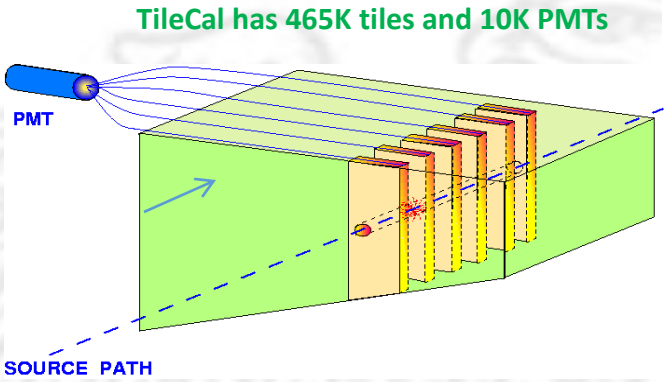
3-in-1 Card: Slow Integrator

Functionality of the Integrator

- Performs Cs calibration for inter-calibration of TileCal cells and normalization of PMT gains
- Measures luminosity during data runs



Requirements of the Integrator at HL-LHC

- Minimum measurable input current
  → ~ 2nA (~40 counts)
- Maximum measurable input current
  → ~10 uA (4095 counts)
- 12-bit resolution
- Good linearity (overall dynamic range <1%)
- 10-20 ms time constant for good sensitivity and proper suppressing ripples

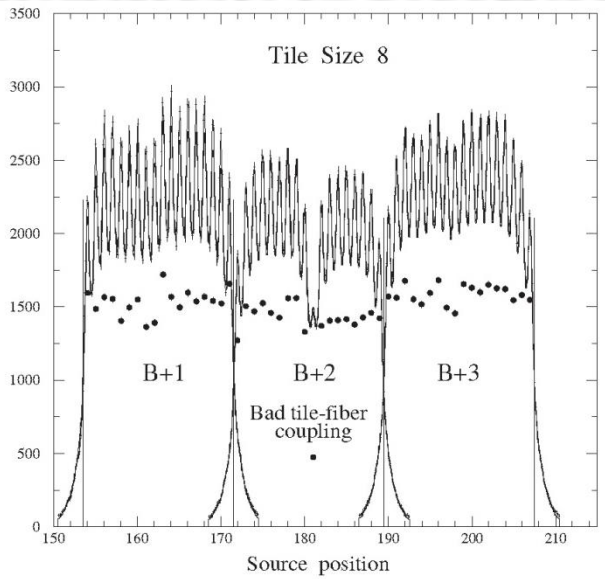


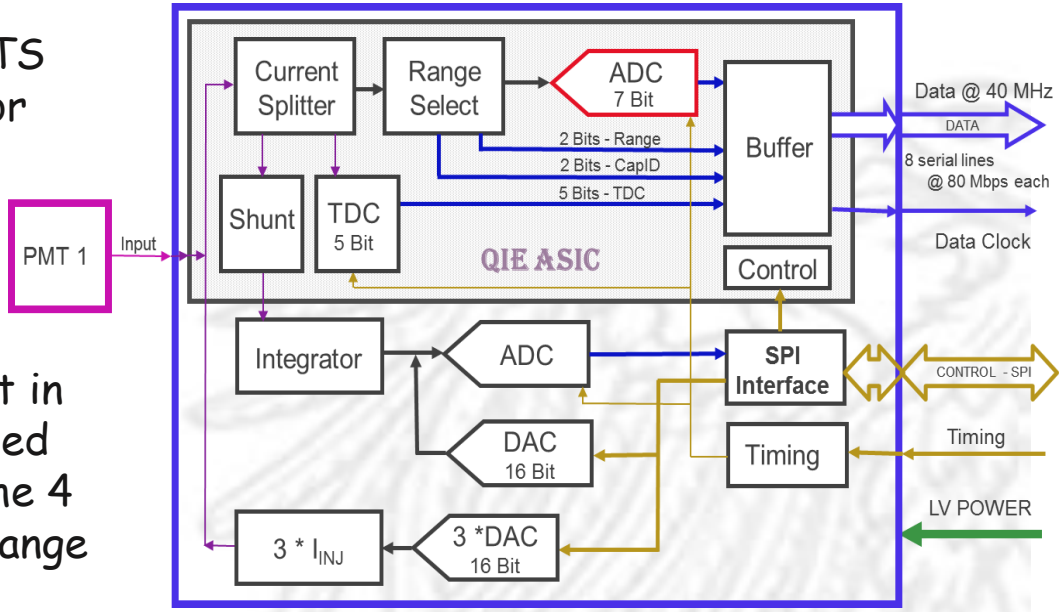
FIGURE 5. The PMT current as a function of the source position for three adjacent cells.

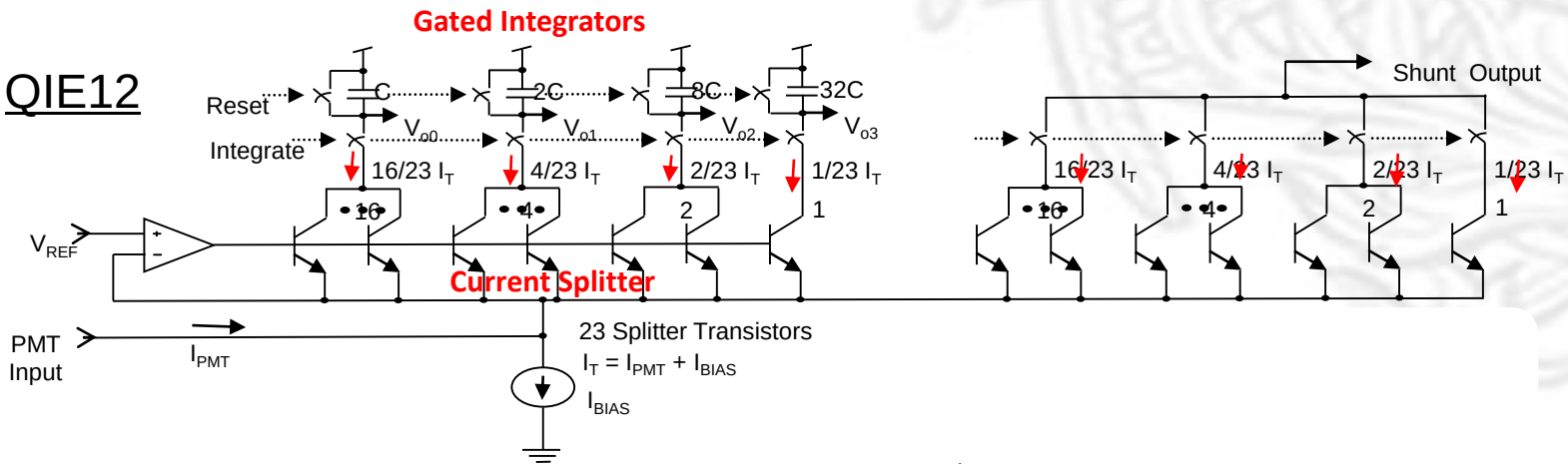
Option-2: QIE ASIC based Front-end Electronics

- The core is QIE 12 ASIC, some of COTS devices in advanced technology used for slow control and calibration purpose

  → **LVDS/LVCMOS buffers, DACs, SAR ADCs, OPAMPS, and Mux**

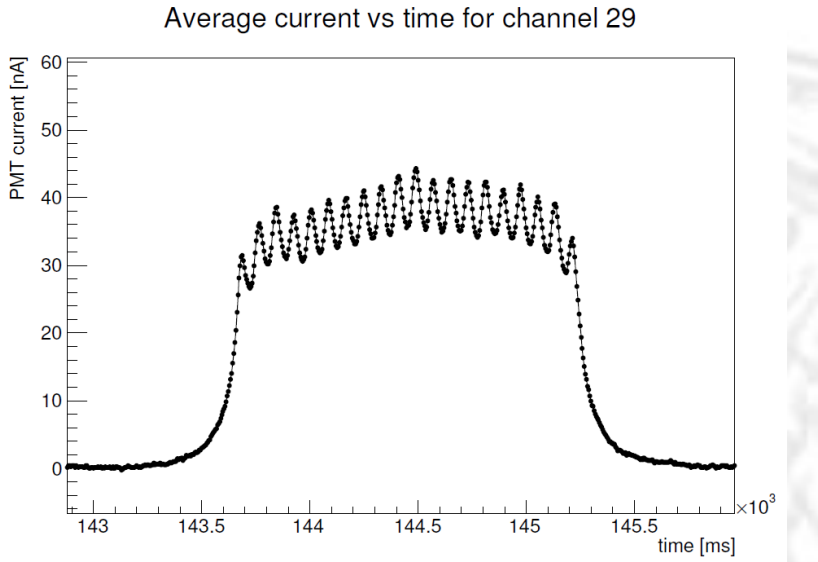
- The QIE splits the PMT output current in 4 ranges, each has a corresponding gated integrator and 7-bit ADC. Combining the 4 ranges, QIE presents 17-bit dynamic range with non-linear transfer function

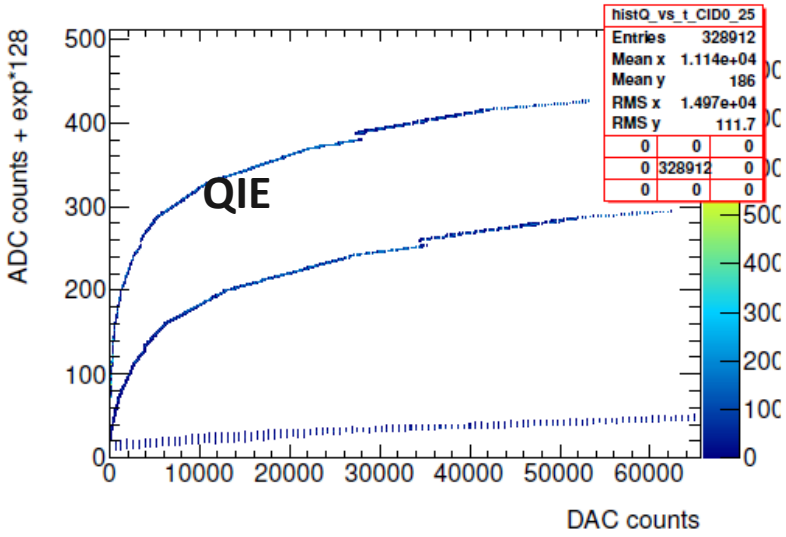


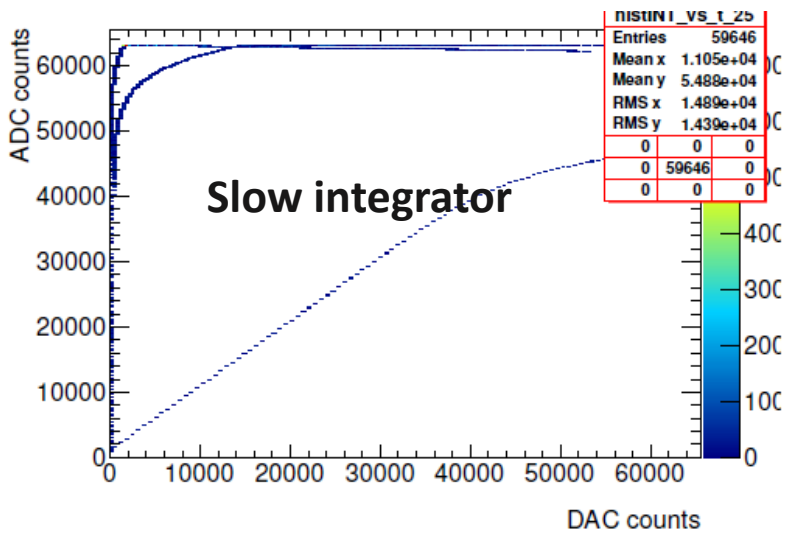


QIE Calibrations with Cesium Scan & Current Injection

- A injected current is measured simultaneously with QIE digital sum and the current integrator
- Cross-calibration between the fast and slow readouts
- The integrator ADC has nA resolution
- Cs scans to obtain the nominal PMT gain



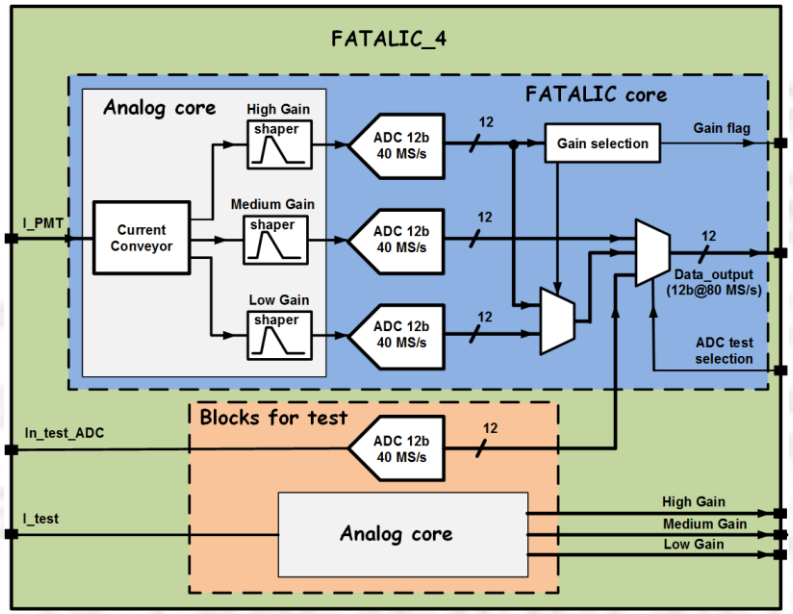


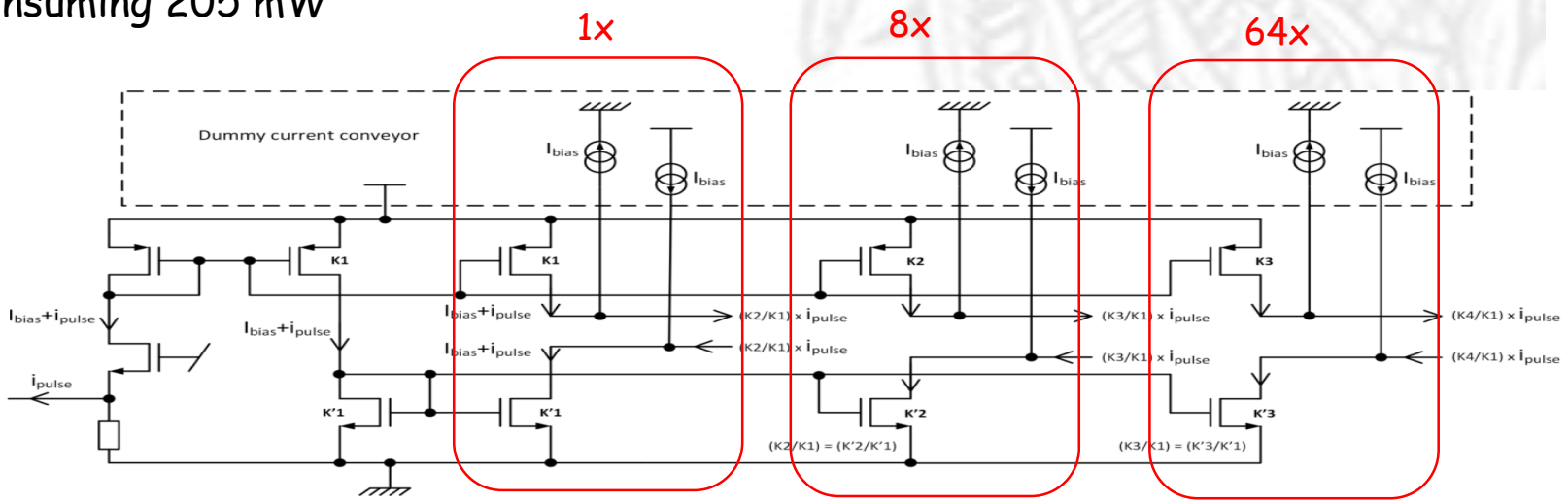


Option-3: FATALIC ASIC based Front-end Electronics

The FATALIC ASIC design has a current conveyer with outputs with a gains ratio of 64:8:1, each followed by an RC shaper to handle the PMT signals

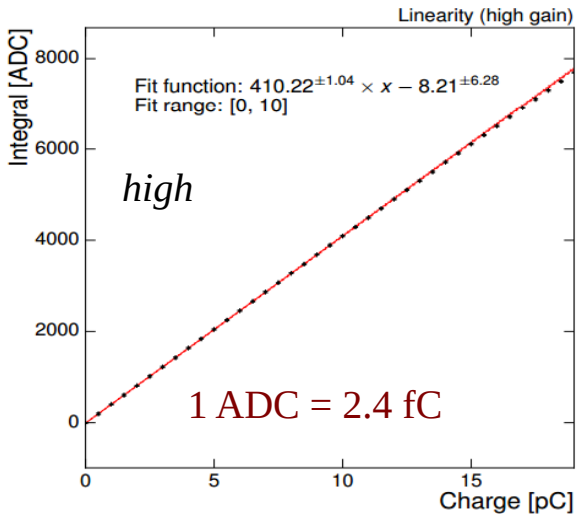
- Three 12-bit ADCs in parallel to digitize the outputs from current conveyer
- Combined dynamic range is 17-bits
- Auto-selection data readout with medium gain + (Low or High gain)
- ASIC built in 130 nm CMOS technology operates in 1.6V, consuming 205 mW

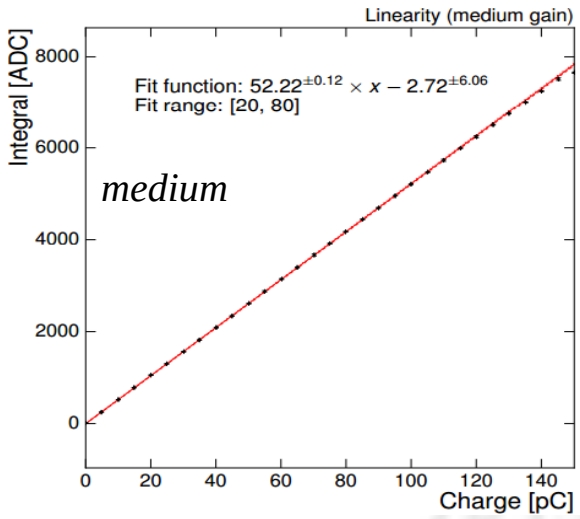


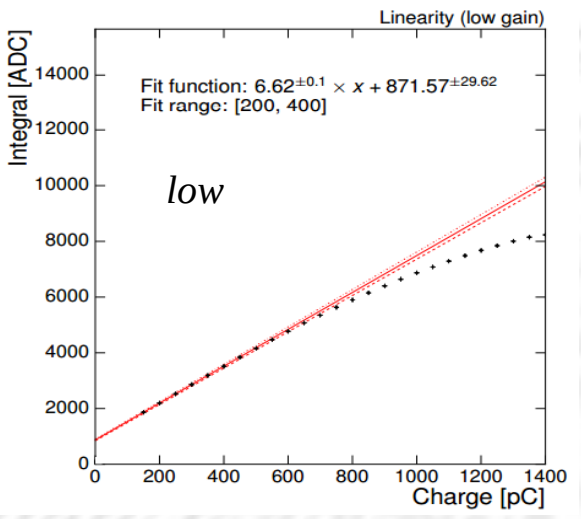


Electronics/Test Beam Performance of FATALIC FE Card

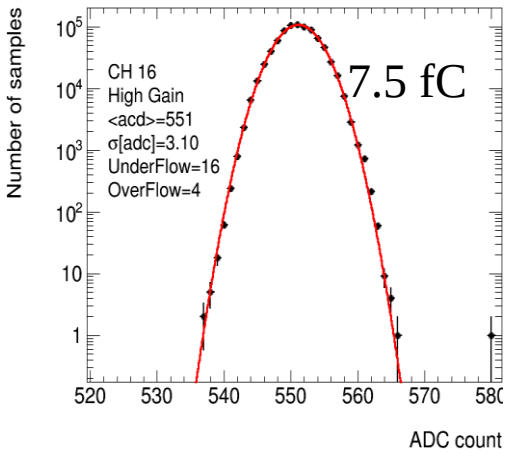
Charge injection linearity (lab)



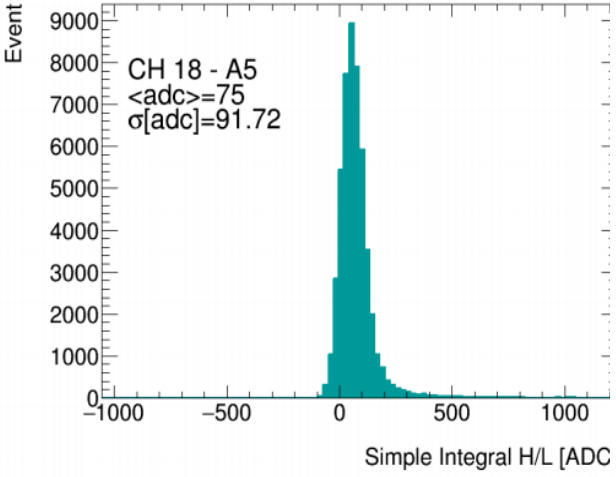




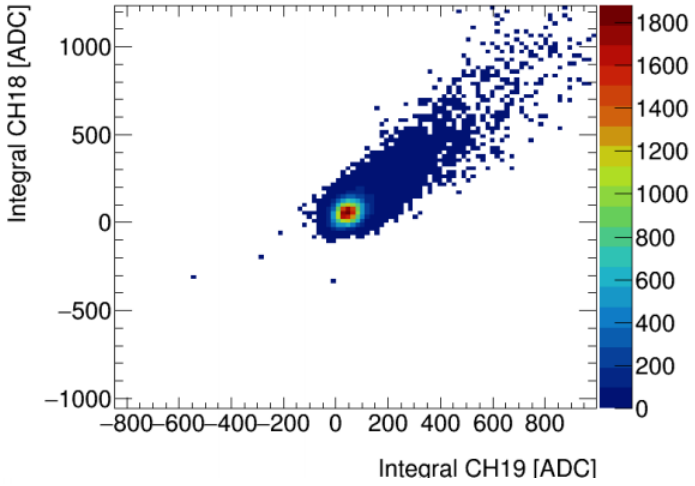
Noise (test beam)



Muon (test beam)

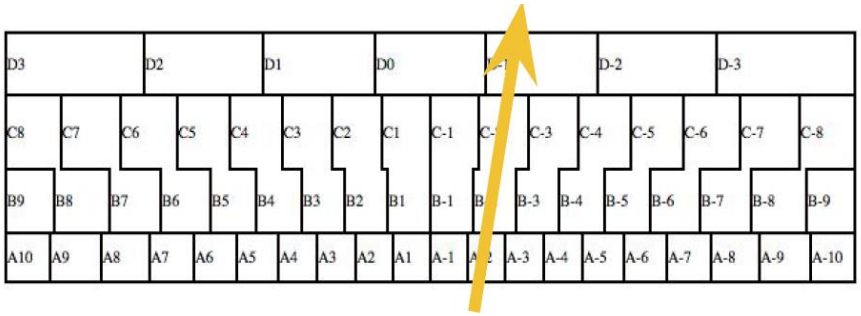


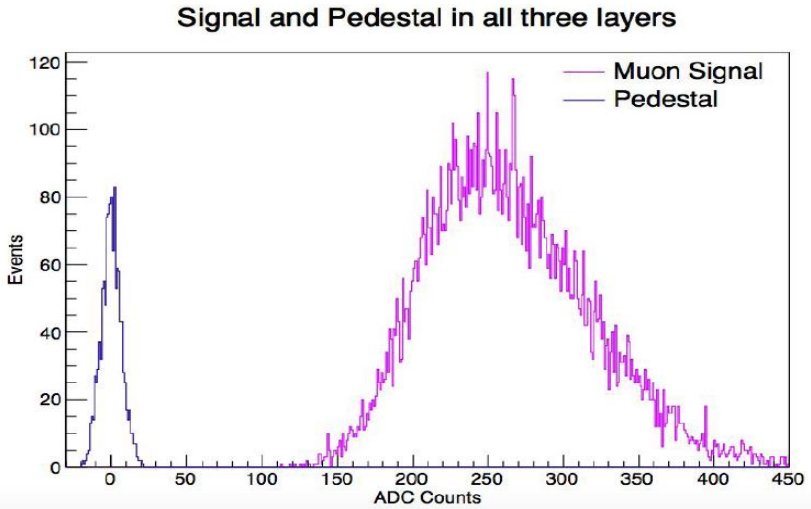
Muon (test beam)



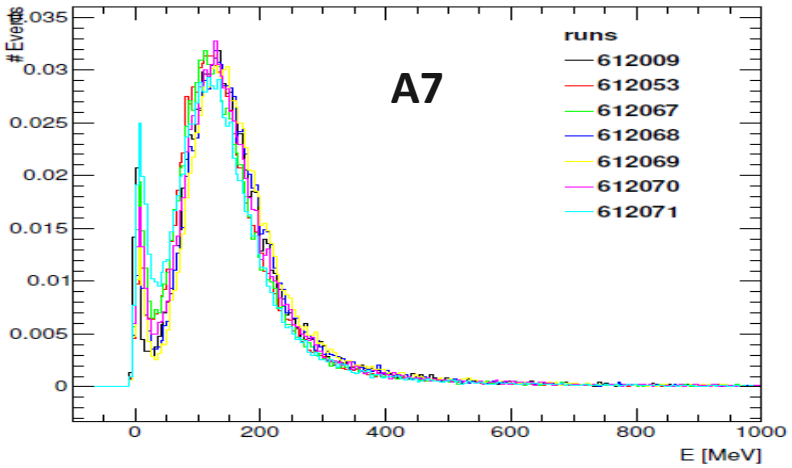
3-in-1 and QIE Test Beam Results

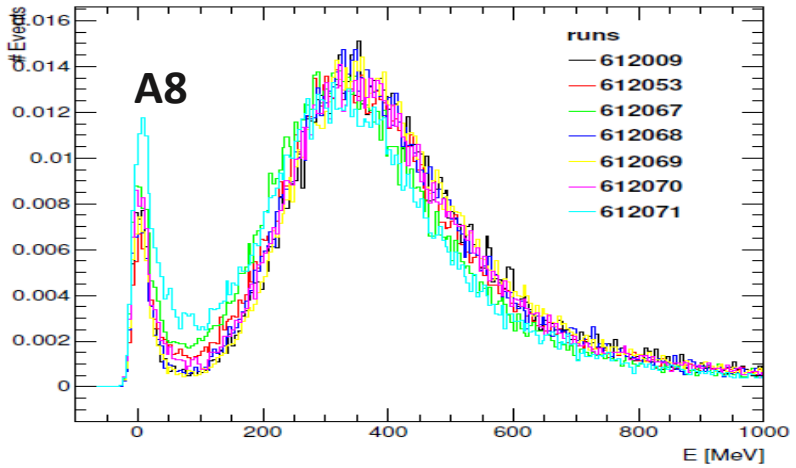
(a) Results from 3-in-1 card





(b) Results from QIE FE Card





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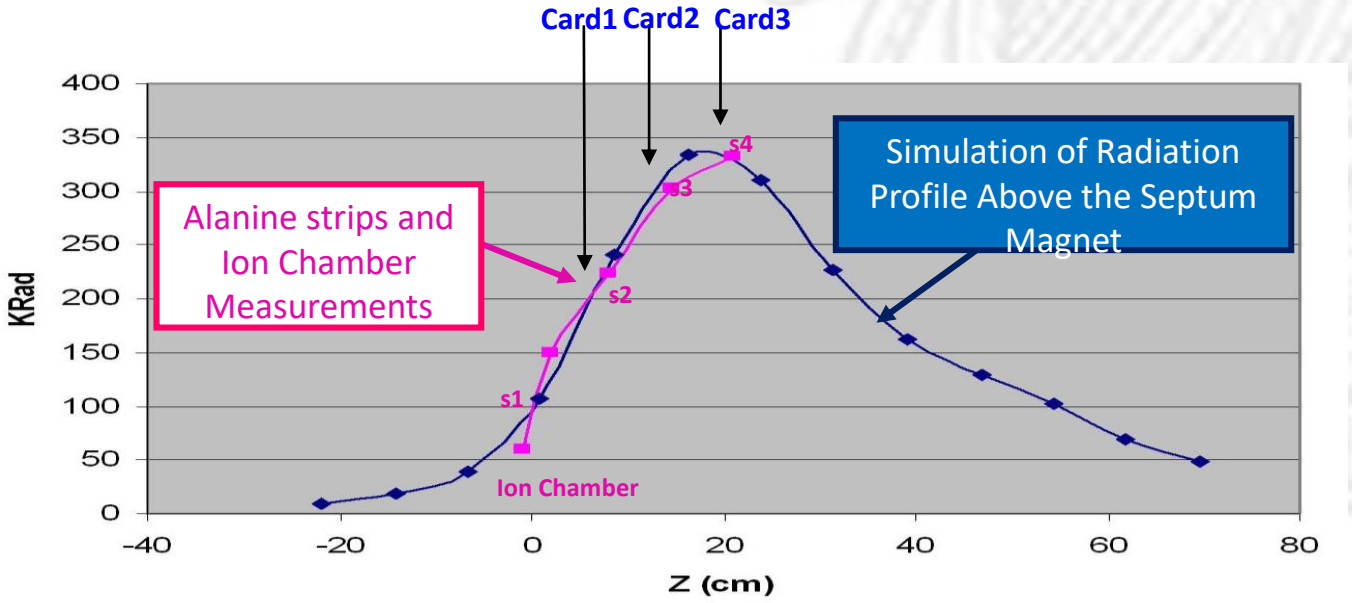
Radiation Tolerance of 3-in-1 Card

- Radiation tolerance specs for FE electronics
  - TID: 1 krad → 30 krad (safety factor of 30)
  - NIEL: 1.03e12 → 8e12 n/cm^2 (safety factor of ~8)
  - SEE: 2.46e11 → 2e12 p/cm^2 (safety factor of ~8)

- Analog switch TS5A2360 died at 60-90 krad (card 1, 2, 3)
- All other components survived even to 330 krad



Radiation Tolerance of the QIE system

- Radiation tolerance of the QIE system is well above the requirements
- TID
  - Exposed to > 45 krad (250 krad for QIE ASIC itself)
  - Requires 30 krad for FE (including the safety factor of 30)
- NIEL
  - Exposed to > 1e13 n/cm^2
  - Requires 8e12 n/cm^2 for FE , including the safety factor ~8
- SEE
  - Exposed to 1e12 p/cm^2
  - Requires 2e12 p/cm^2 for FE, including the safety factor ~8
  - No single-event failures and latch-ups or any critical failures found

- The rare SEEs are intermittent and recoverable by comparing energy and time measurements in different channels.

  → No need to reset power or re-program after an SEU

- The -5V switching regulator on the Main boards needs to be investigated further

Main Board & Daughter Board

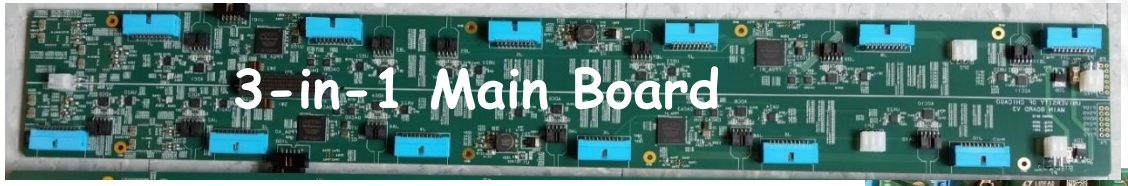
2 types of Main boards have been built: 3-in-1 and FATALIC/QIE

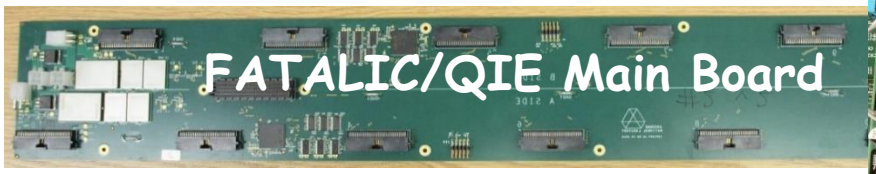
Main Board for 3-in-1 cards

- 24-ch of ADCs to support 12 3-in-1 cards with serial data rate of 560 Mbps each
- Distribute the slow control commands to the FE cards
- Manage charge injection calibration and remote system configurations

Daughter Board is designed to support two types of Main Boards

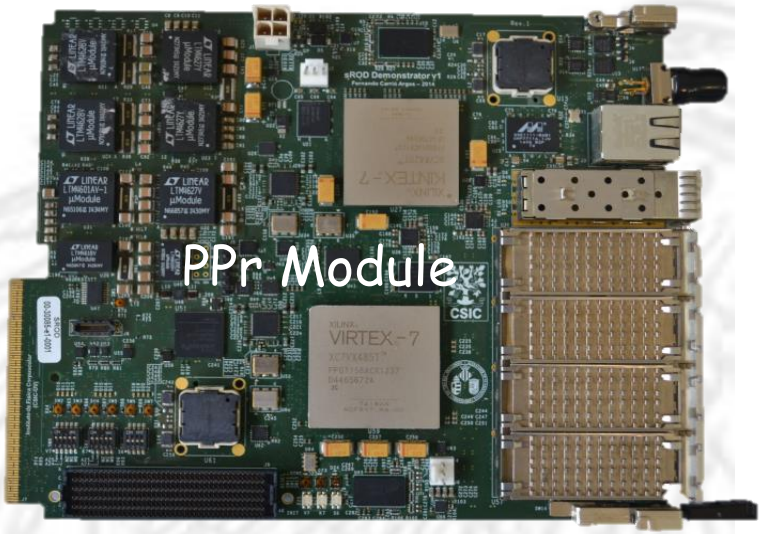
- Receives GBT TTC signal and slow control commands from the back-end PPr module and distributes to the Main Board and HV Board
- Collects/concentrates the ADC data from the Main Board and transmit data over optical links to the back-end PPr module (80 Gbps/per board in redundancy, but only 40 Gbps reach PPr)

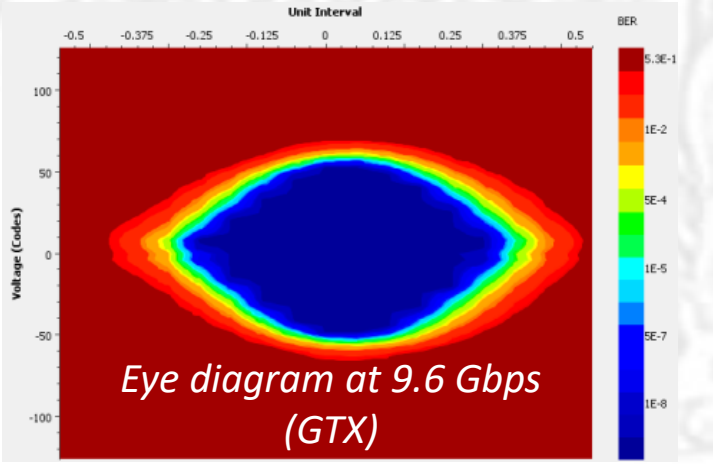




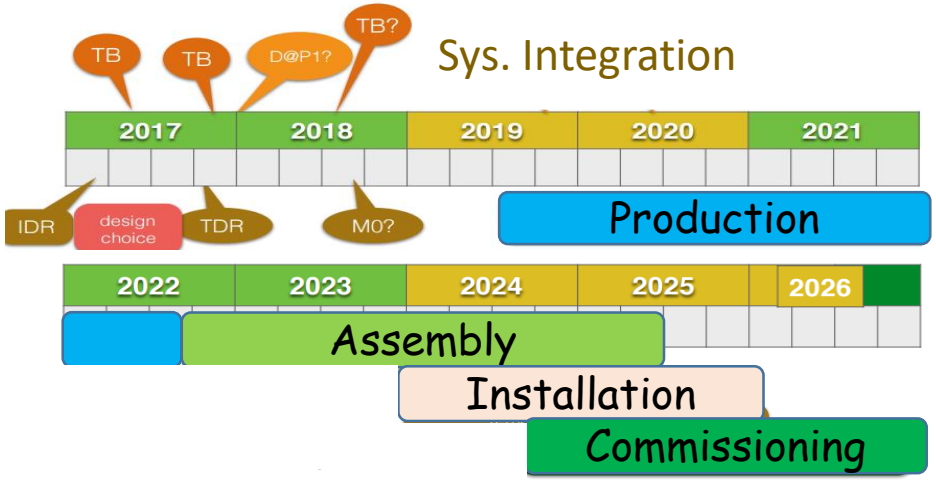
TileCal Back-end Electronics PPr Module

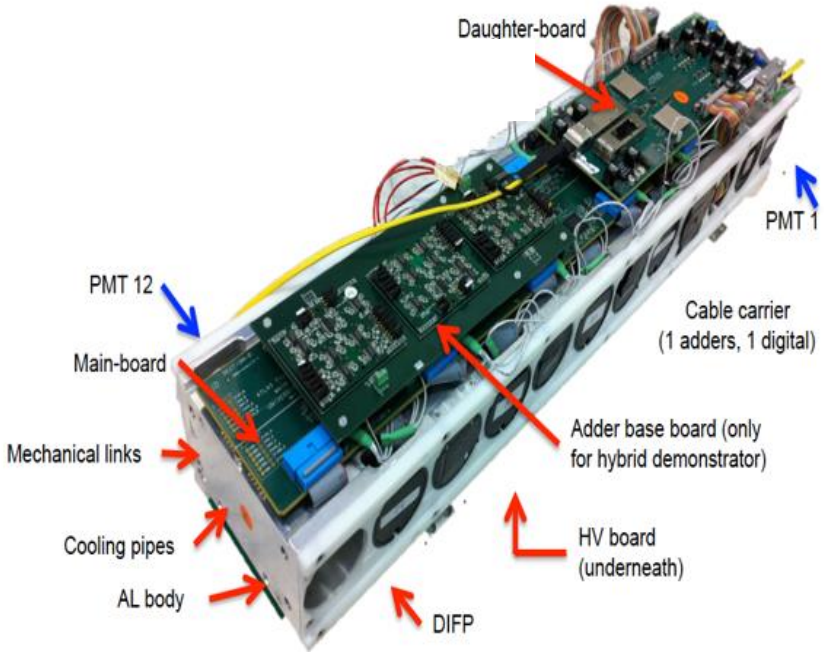
- Final design of PPr module for Phase 2, one per detector module
- Virtex 7 + 4 QSFPs (Data readout)
  - TTC/DCS distribution to FE
  - Interface to FELIX
  - Energy and time reconstruction algorithms
- Kintex 7 + Avago MiniPOD TX (Trigger)
  - Send trigger data to L0/L1Calo
  - Pre-trigger algorithms
- DDR3 memories, FMC, GbE ports, PCIe
- BERT 5×10^{-17}, error-free with 16 links at 9.6 Gbps in PRBS31 for 115 hours

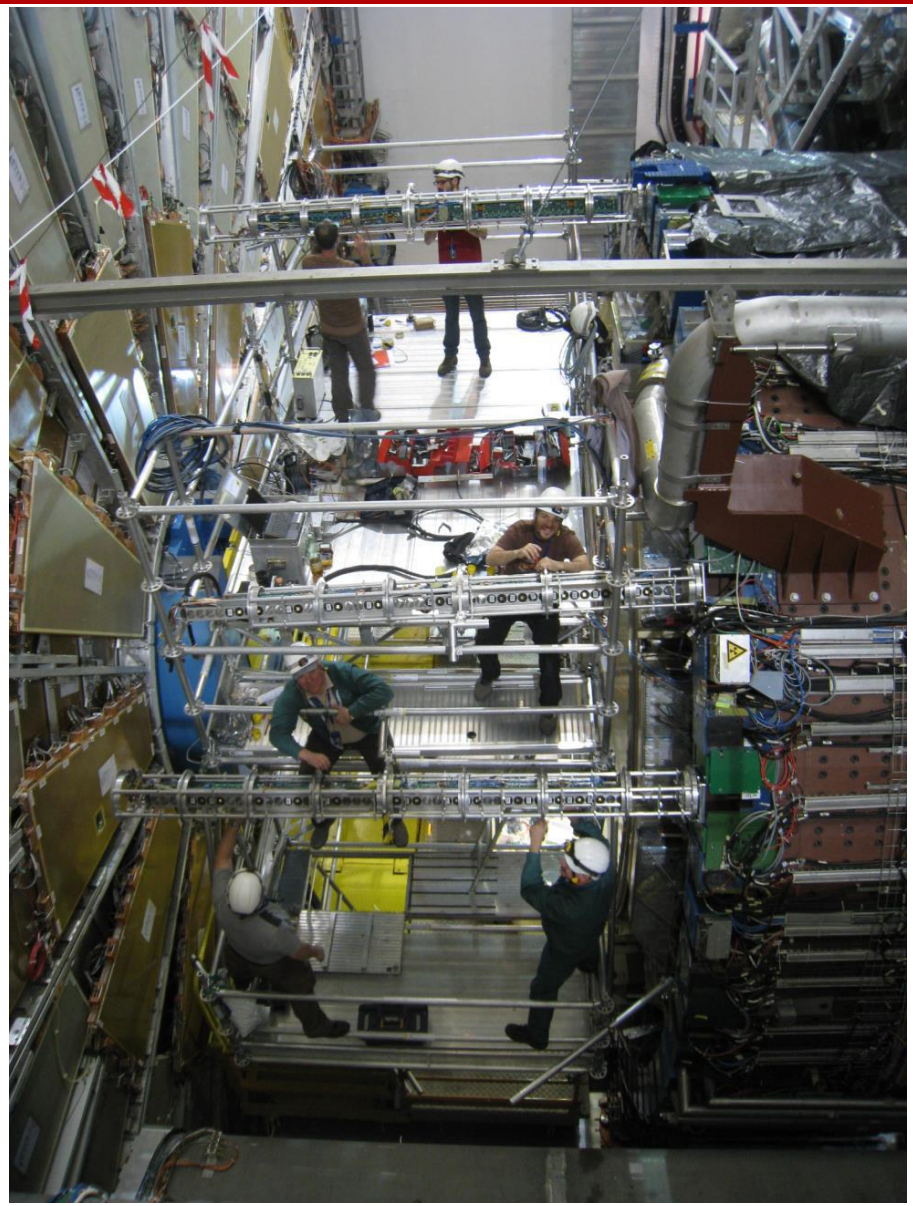




Milestones Towards Commissioning







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Summary

- A Demonstrator with 3-in-1 system aimed at early installation (end of 2017) in ATLAS has been fully tested and compared with the current TileCal readout system at LHC to ensure compatibility
  - electronic noise level more that an order of magnitude below inherent shower fluctuations compared the current TileCal readout system at LHC
  - System energy resolution and linearity has been improved
  - The Cesium calibration and minimal bias current monitoring well meet the requirements
- All 3 FE options appear to meet TileCal readout requirements in terms of electronic performance and test beam results
- FE down select will be based on performance, reliability, cost and support by July 2017
- Daughter Board will use new Xilinx UltraScale+ FPGAs, which will improve radiation tolerance and high speed data transmission reliability
- Some required radiation tests need to be completed, such as SEE, NIEL…
- Finalized the designs to meet the IDR and TDR milestones