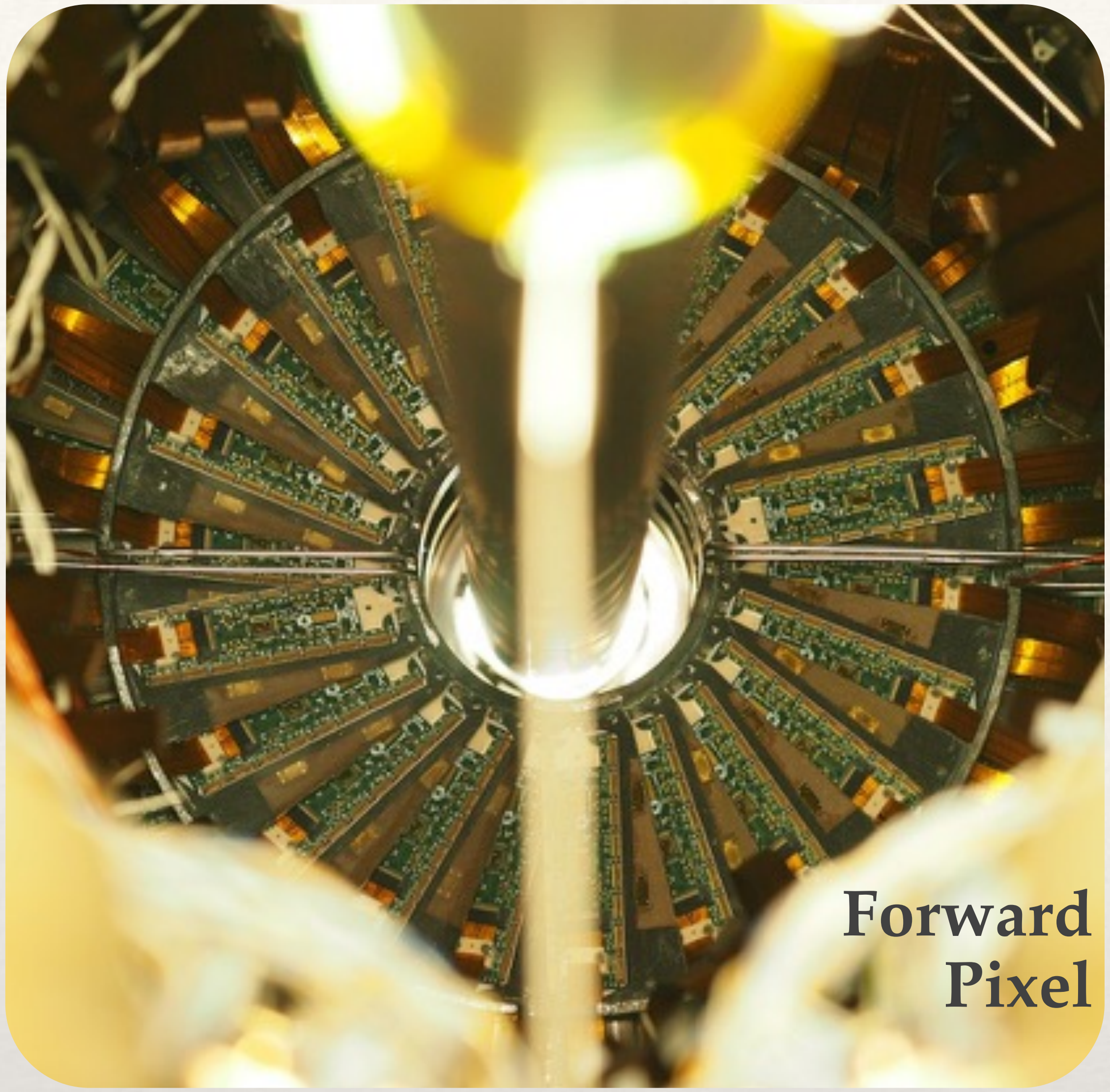
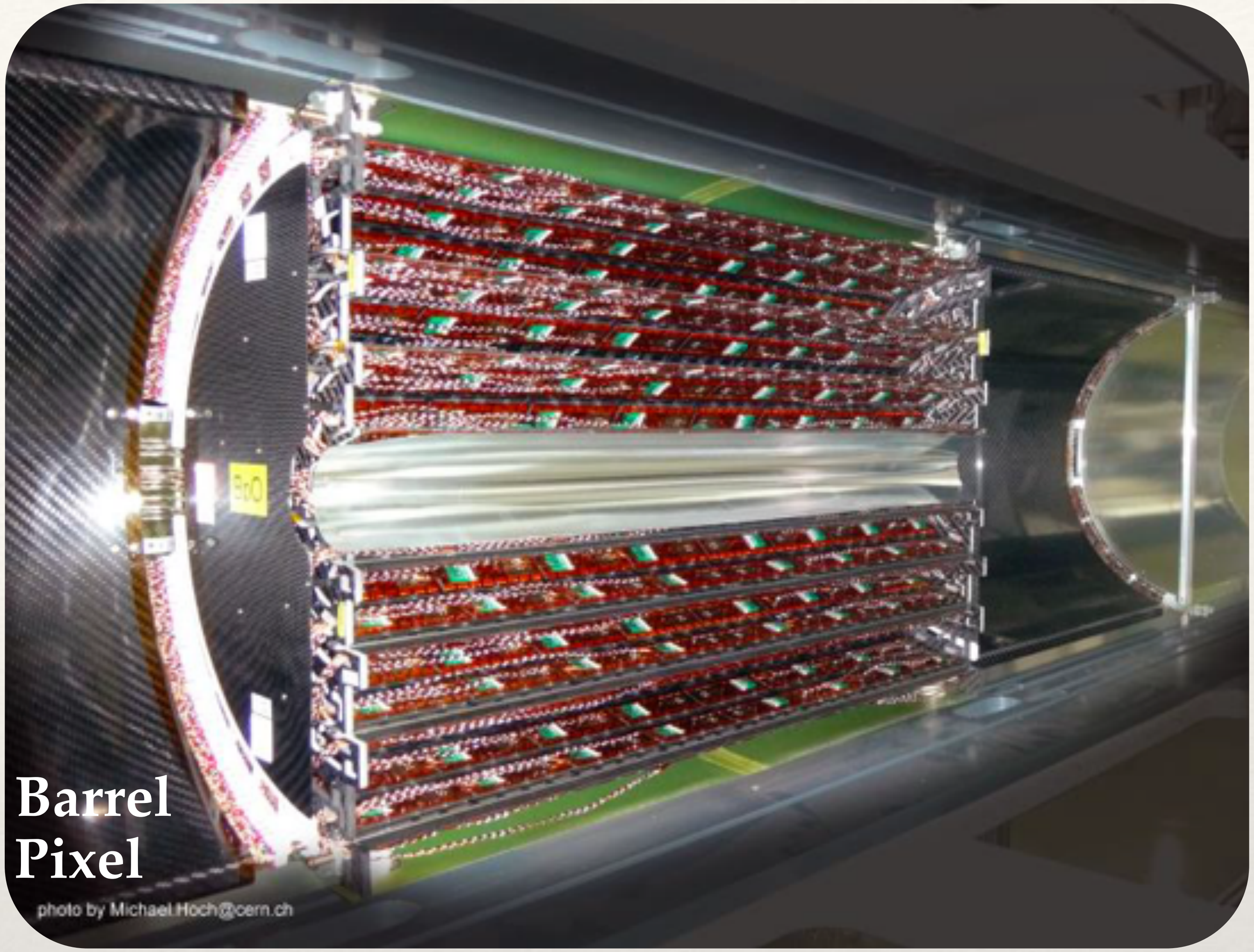




TECHNOLOGY AND INSTRUMENTATION IN PARTICLE PHYSICS 2017, May 22-26, 2017

Construction of the Phase I upgrade of the CMS pixel detector

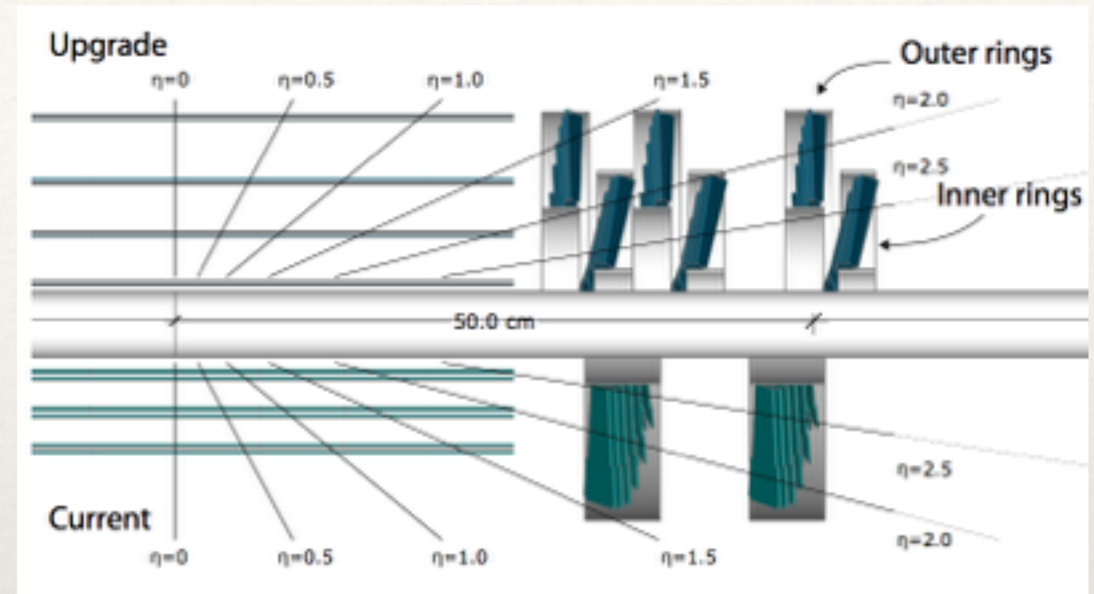
Satoshi Hasegawa
Fermi National Accelerator Laboratory

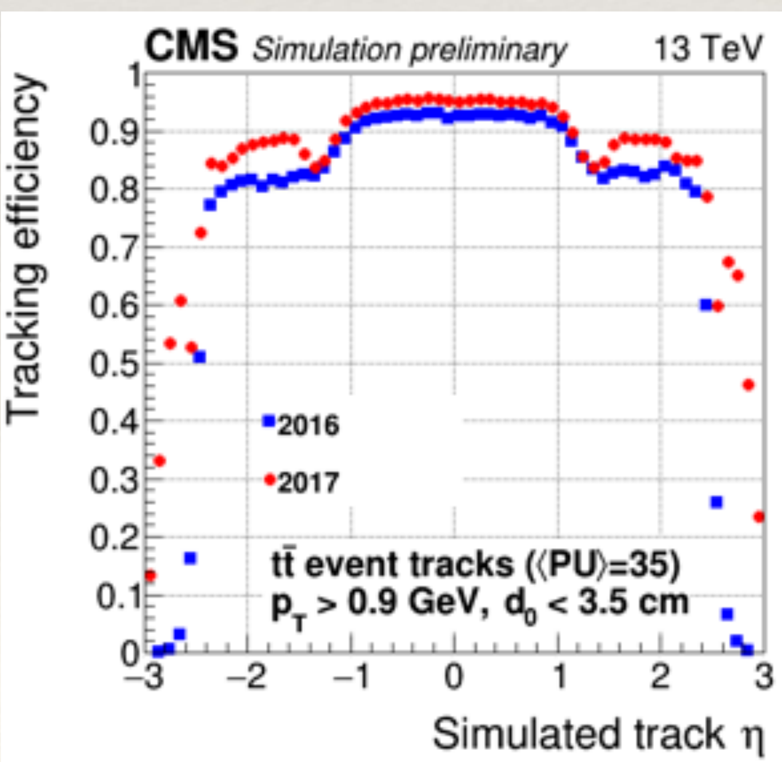
Presented by
Benedikt Vormwald
University of Hamburg

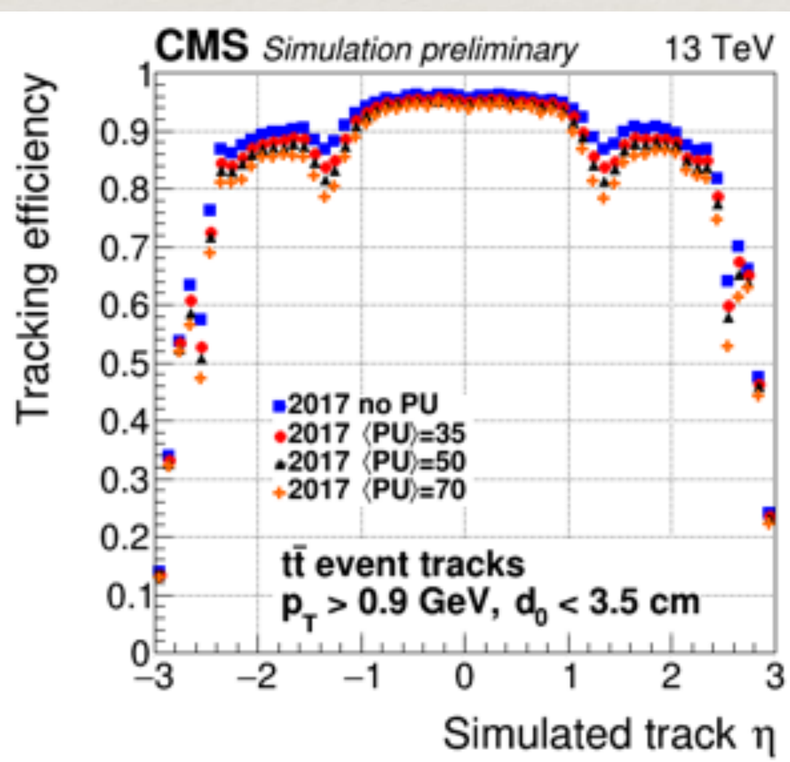
on behalf of the CMS collaboration

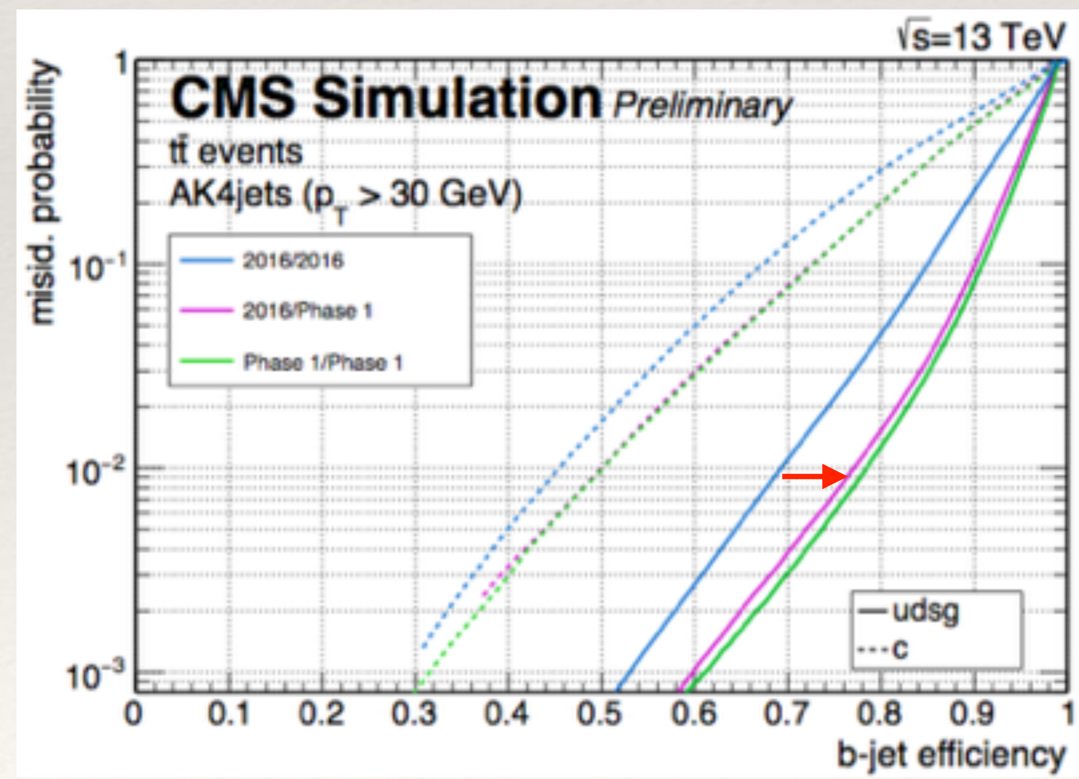
Pixel Phase-1 upgrade project

- Original detector not suited for operation at L~2×10^{34} $cm^{-2}s^{-1}$
    - limited bandwidth readout chip to backend
- Upgrade detector
    - Faster digital readout chip
    - One extra layer for more robust tracking closer to the interaction point
    - Reduced material budget with CO_2 cooling system
    - Use DC-DC converters to avoid replacing power cables
    - Will operate until LS3







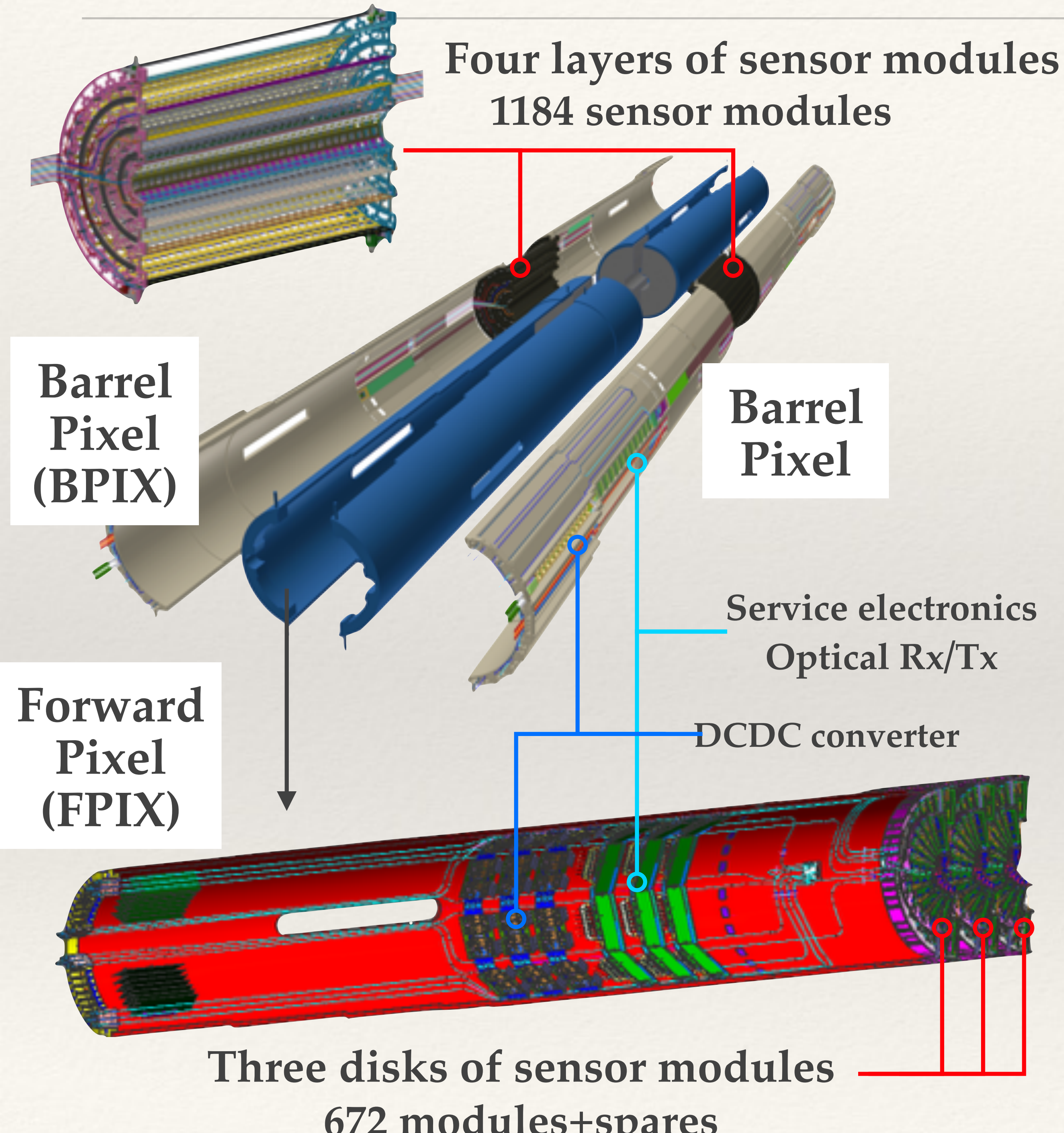


"Construction of the Phase I upgrade of the CMS pixel detector" Satoshi Hasegawa, TIPP2017, May 22-26, 2017. Presented by Benedikt Vormwald.

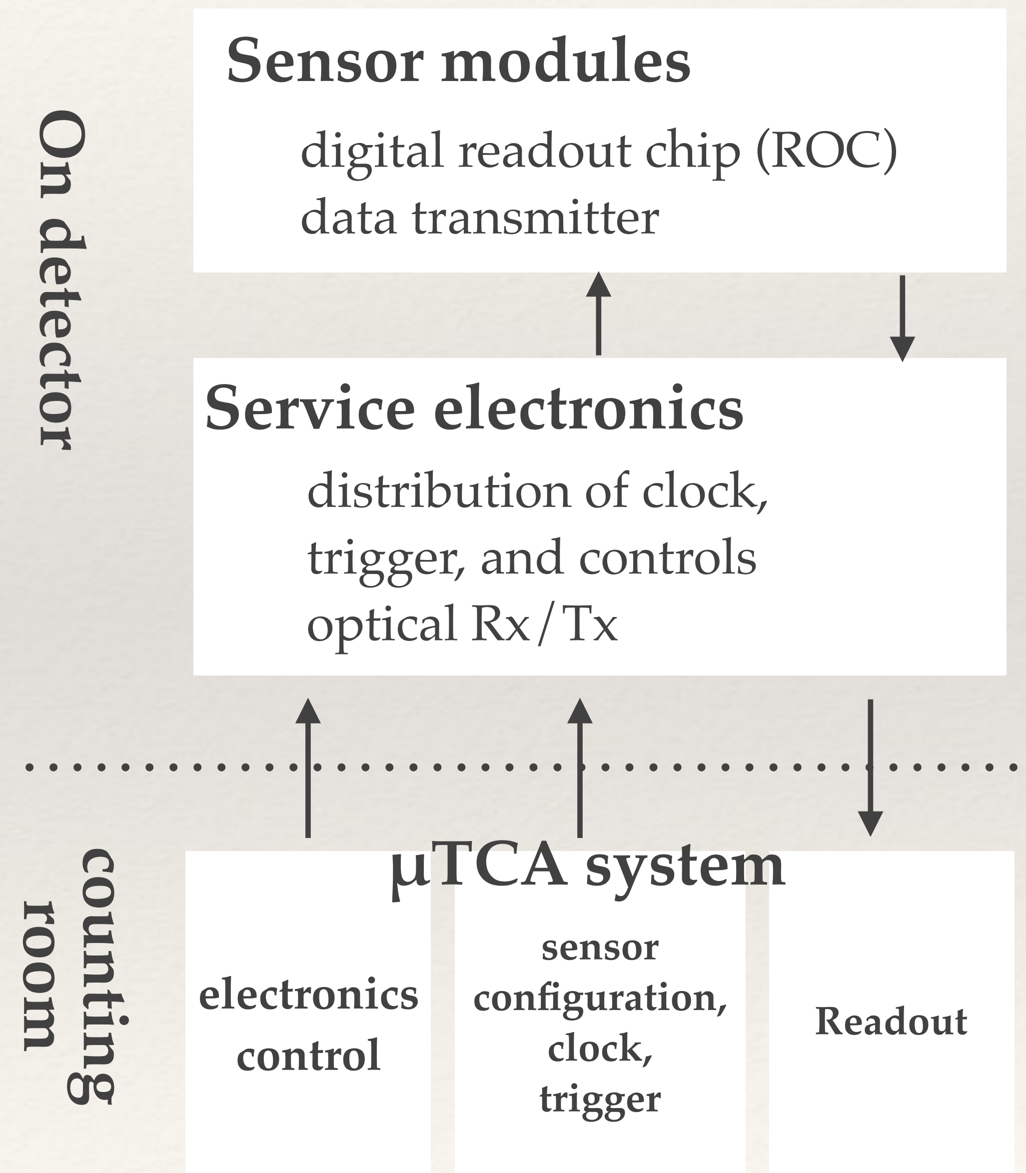
Scope of the presentation

- **The detector has been installed at the beginning of March** and it is now being commissioned.
  - Commissioning details in the next presentation by Benedikt Vormwald.
- In this presentation, review the design and technology choices :
  - Upgrade in the readout system
    - Sensor modules with newly developed digital readout ASIC and transmitter
    - Backend control and readout system based on μTCA framework
  - No increase in material budget despite additional tracking layer
    - lightweight carbon fiber supports
    - two phase CO_2 cooling system
    - DC-DC converters

Detector and services



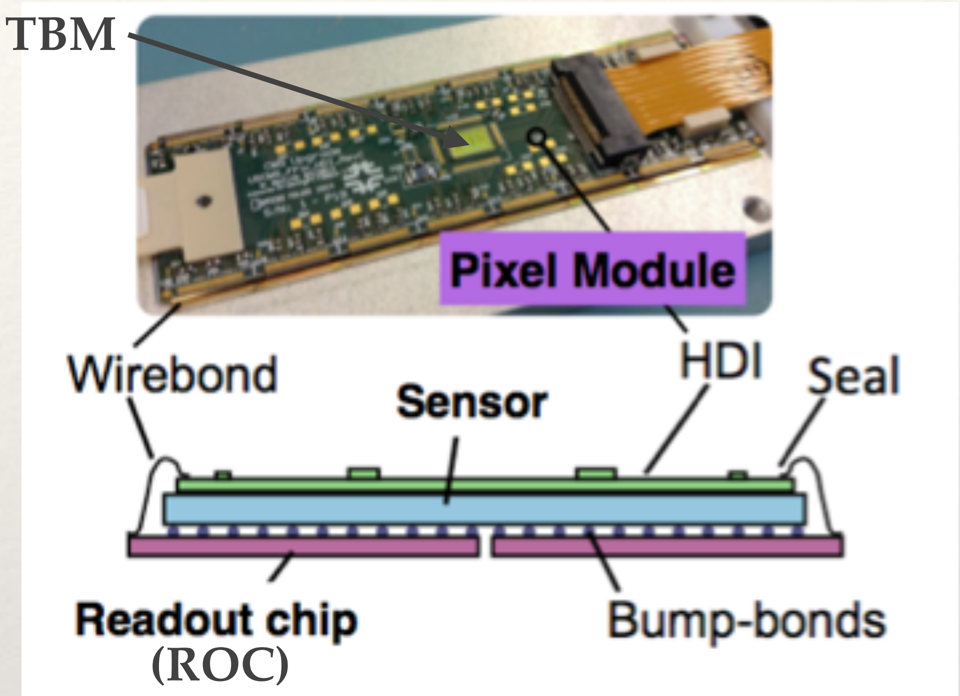
ROC: analog (40 MHz) --> digital (320Mbps)
Backend: VME --> µTCA
Controls largely unchanged



 "Construction of the Phase I upgrade of the CMS pixel detector" Satoshi Hasegawa, TIPP2017, May 22-26, 2017. Presented by Benedikt Vormwald.

Sensor modules

- Sensor design unchanged relative to original detector
  - Only 1 sensor geometry through entire detector
  - n+ in n sensors, 66560 pixels with 100x150 um^2 size
  - Total active area 16.2 x 64.8 mm^2 covered with 16 readout chips



- New digital readout chips (**ROCs**) used
  - Layer 1 requires dedicated chip to meet data transmission needs.
  - Each ROC transmits data at 160 Mbps

- Data from ROCs merged in single output stream
 in token bit manager ASIC (**TBM**) on each module with 320 Mbps (parallel readout) :
  - 1 single data stream per module in FPIX and BPIX Layer-3/L4 (1 "*TBM8*" chip)
  - 2 data streams per module in BPIX L2 (1 "*TBM9*" chip)
  - 4 data streams per module in BPIX L1 (2 "*TBM10*" chips)

 "Construction of the Phase I upgrade of the CMS pixel detector" Satoshi Hasegawa, TIPP2017, May 22-26, 2017. Presented by Benedikt Vormwald.

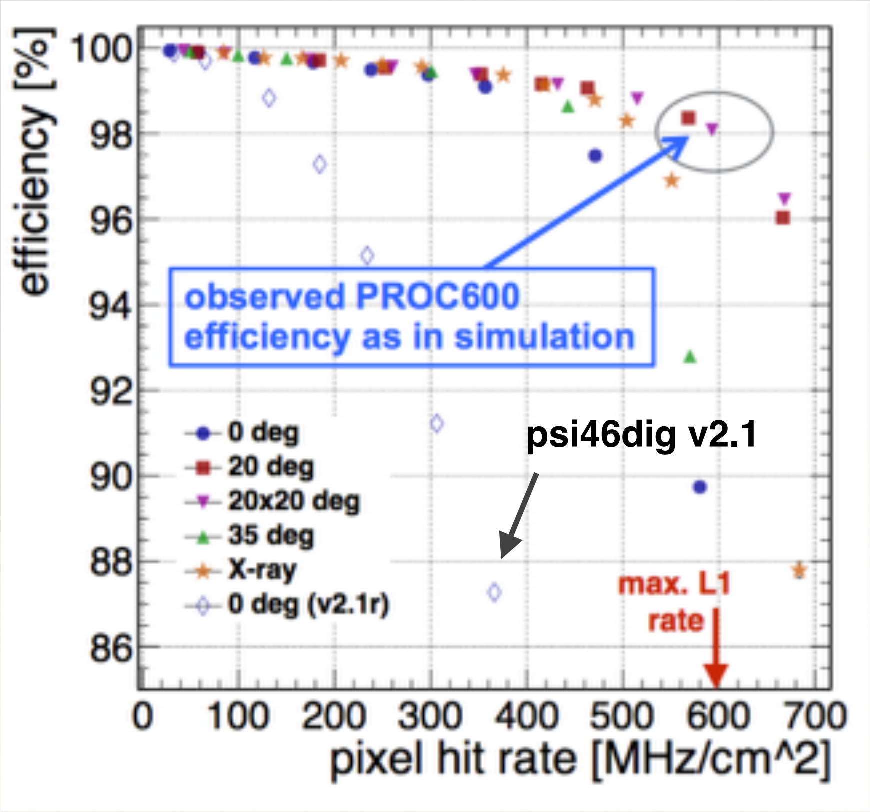
Digital readout chips

BPIX L2-L4 and FPIX use "psi46dig v2.1"

- evolution of ROC of previous detector
- double column drain architecture
- **8bit ADC** on chip, data transmission at **160 Mbps**
- **larger buffers** to reduced inefficiency at high occupancy
- **lower threshold**: from 3500 e- (current detector) **to ~1800 e-**
  - redesigned power distribution to reduce cross talk noise
  - faster comparators to reduce time-walk
- data streams from 2 ROC banks merged inside the TBM

BPIX Layer 1 uses "PROC600"

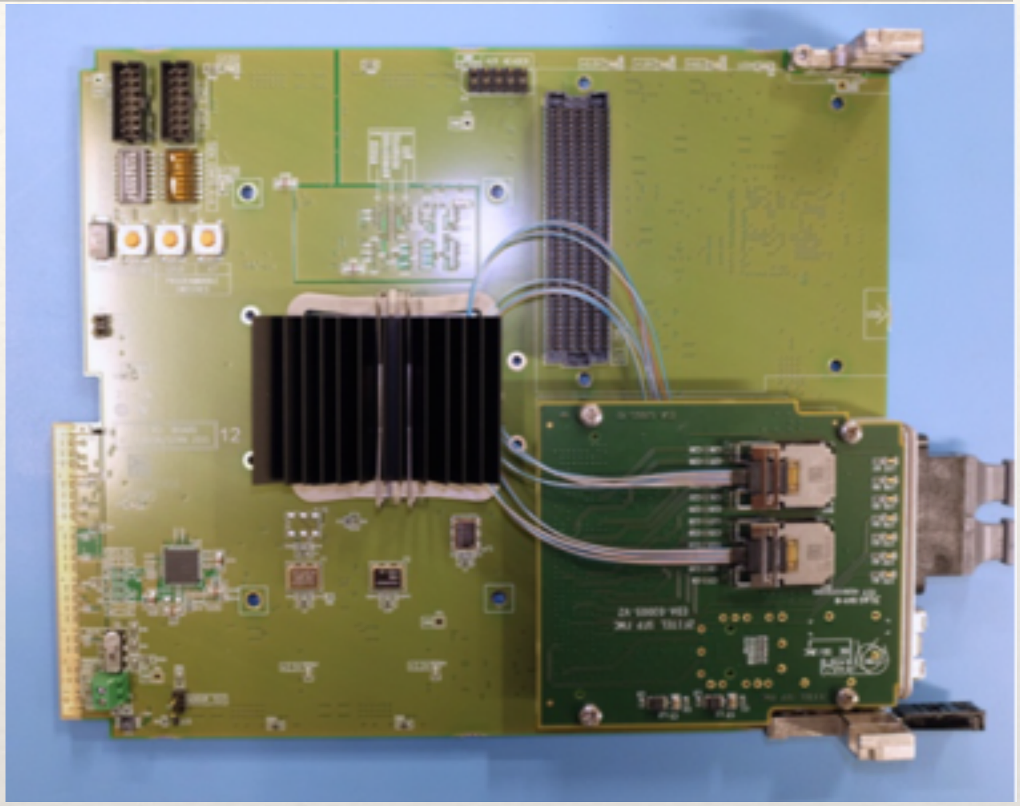
- handles hit rate of 600 MHz/cm^2
  - **improve data throughput** by building 2x2 clusters in the double columns and transmitting cluster information
  - **further increase in buffer sizes** in ROC periphery
- performance not degraded well beyond dose expected for Layer 1 (120 MRad)

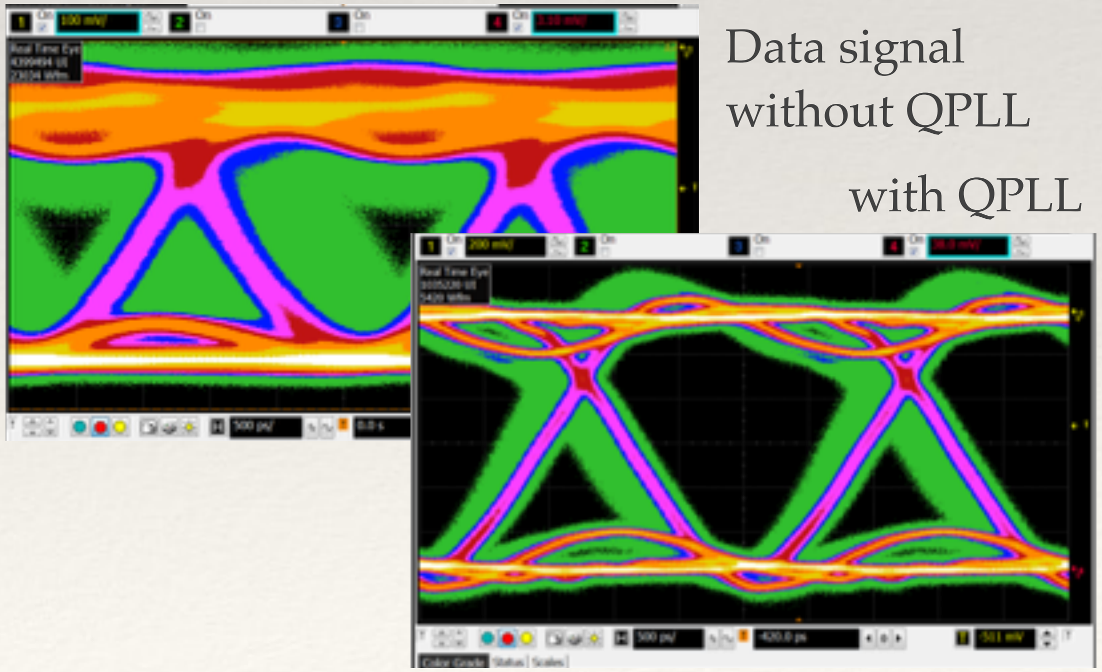


"Construction of the Phase I upgrade of the CMS pixel detector" Satoshi Hasegawa, TIPP2017, May 22-26, 2017. Presented by Benedikt Vormwald.

Readout system

- Micro Telecommunications Computing Architecture (μTCA)-base system replaced VME-base backend.
- FC7 mother board with mezzanine boards with Fitel optical receivers.
    - a μTCA compatible Advanced Mezzanine Card for generic data acquisition/control applications equipped with a Xilinx Kintex 7 FPGA.
- Firmware ready for LHC collisions.
    - current design allows handling data rates expected for 2017 (100 kHz L1 trigger rate, with PU=65)
- Control backend also moved to μTCA boards
- Stability of high bandwidth readout requires reduction of clock jitter, obtained by adding QPLL filter in the services electronics inside the supply tube / service cylinders.





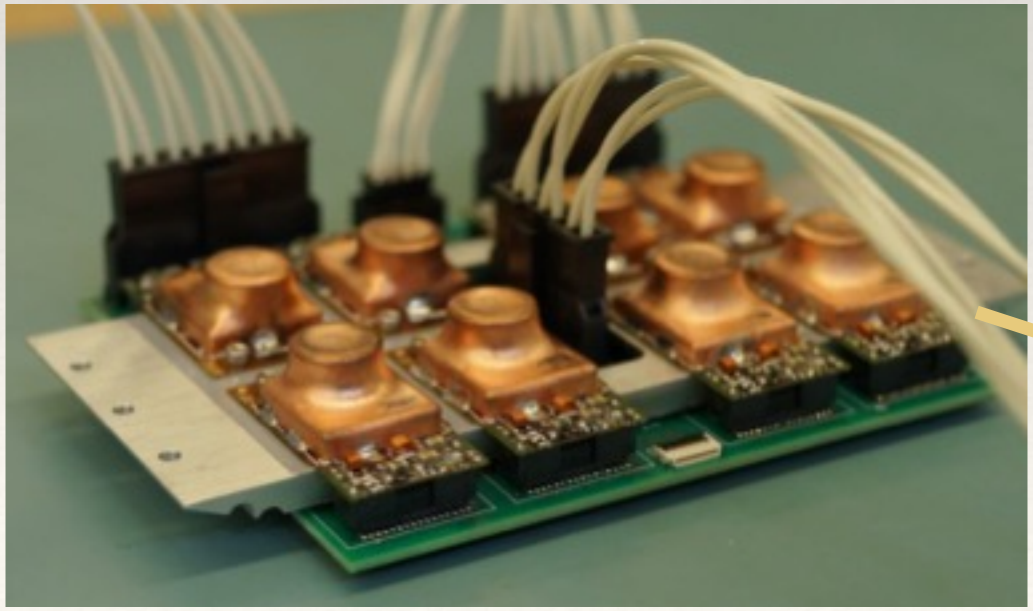
Data signal without QPLL

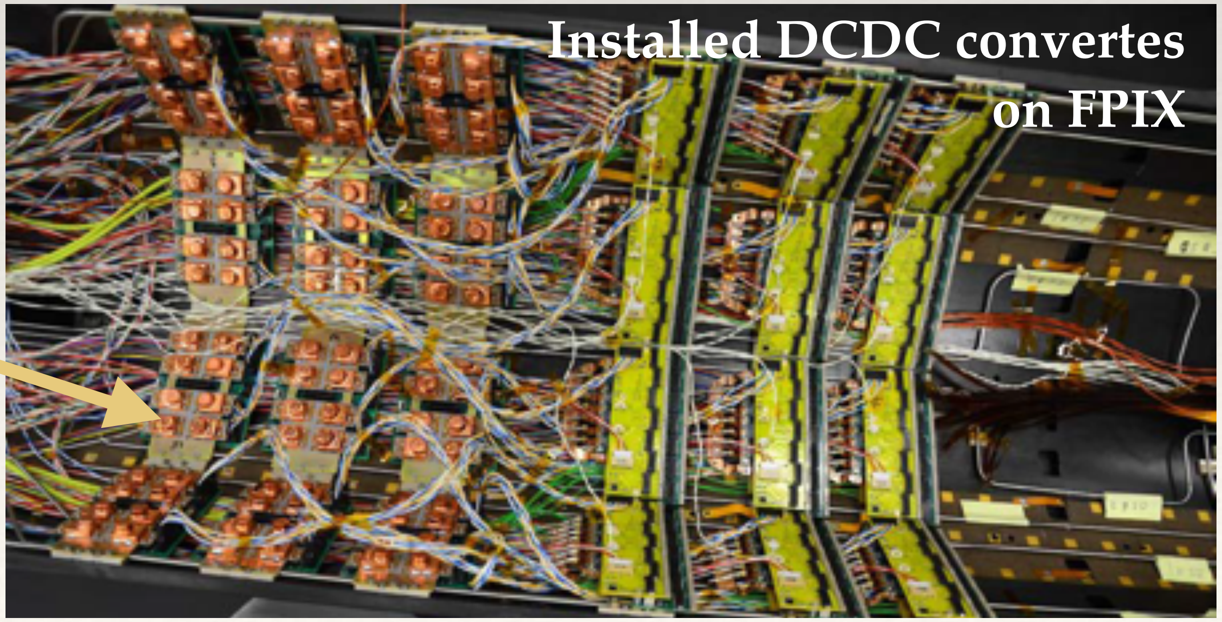
with QPLL

"Construction of the Phase I upgrade of the CMS pixel detector" Satoshi Hasegawa, TIPP2017, May 22-26, 2017. Presented by Benedikt Vormwald.

DCDC converters

- The upgrade detector has factor 1.9 more channels, and it requires more power than the previous.
- To avoid replacing power supply cables and large voltage drops:
  - Adopt powering scheme with DC-DC converters
  - Power supplies deliver 10 V to the detector
  - DC-DC converters inside the support structure convert
  - Voltages to 2.5-3.6V (depending on application)
  - Radiation hard DC-DC converters used (CERN FEAST2 chip)
  - No impact on sensors / readout noise

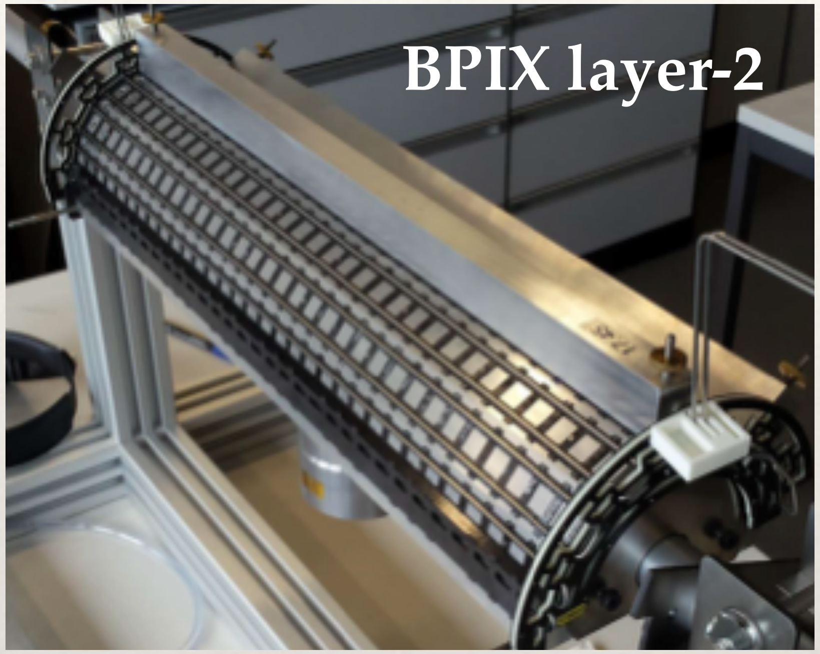


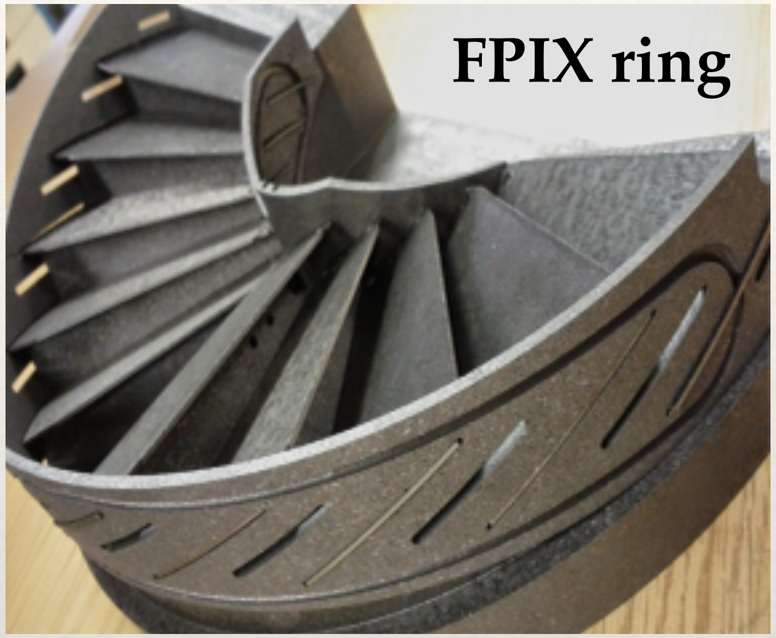


"Construction of the Phase I upgrade of the CMS pixel detector" Satoshi Hasegawa, TIPP2017, May 22-26, 2017. Presented by Benedikt Vormwald.

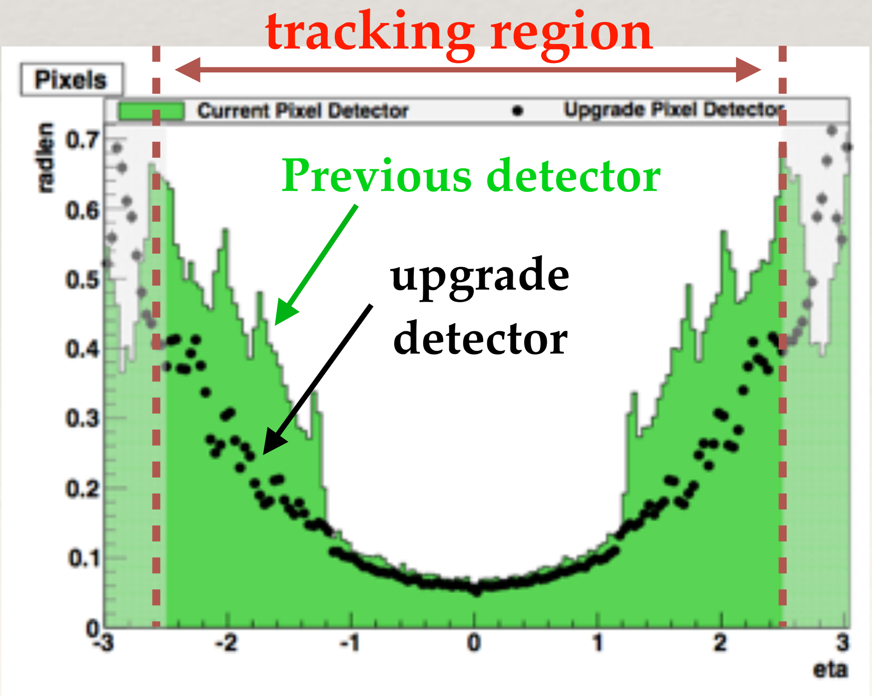
Mechanics

- Detector supports built with carbon fibers / foam and graphite.





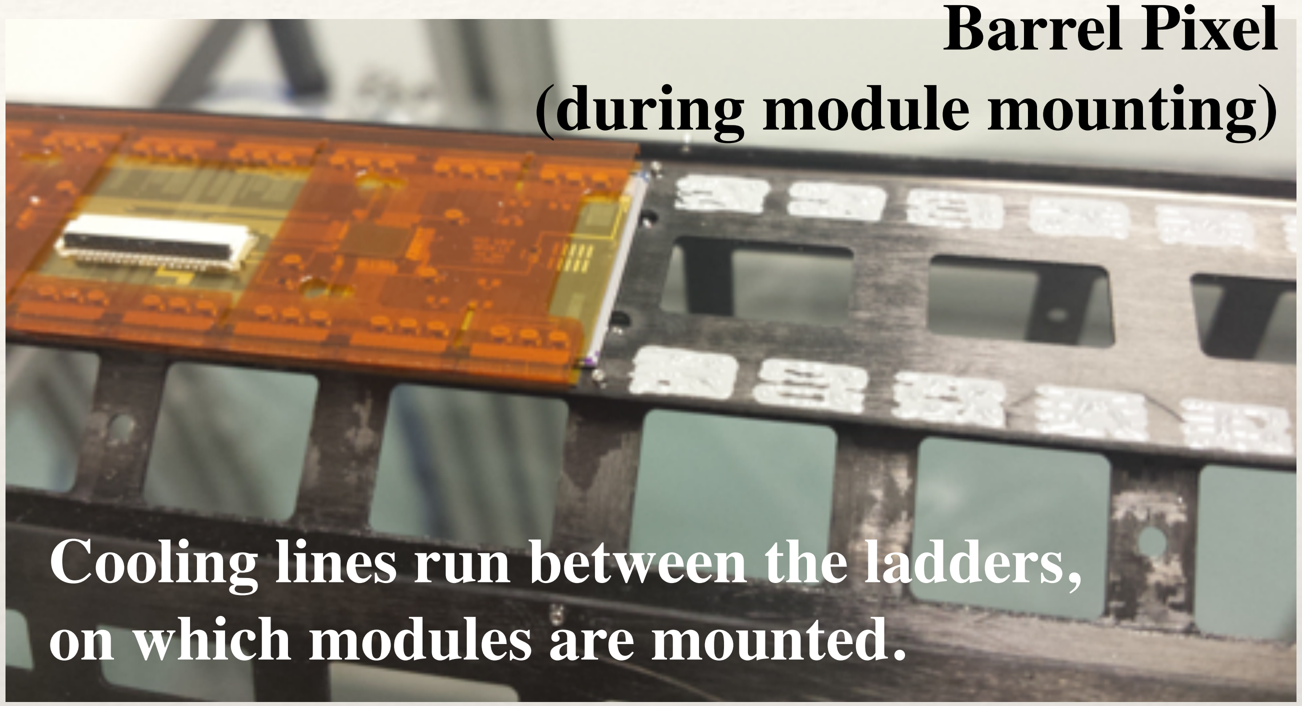
- Thanks to CO_2 cooling and DC-DC converters, no increase in material budget despite additional tracking layer
- Material moved to higher rapidities

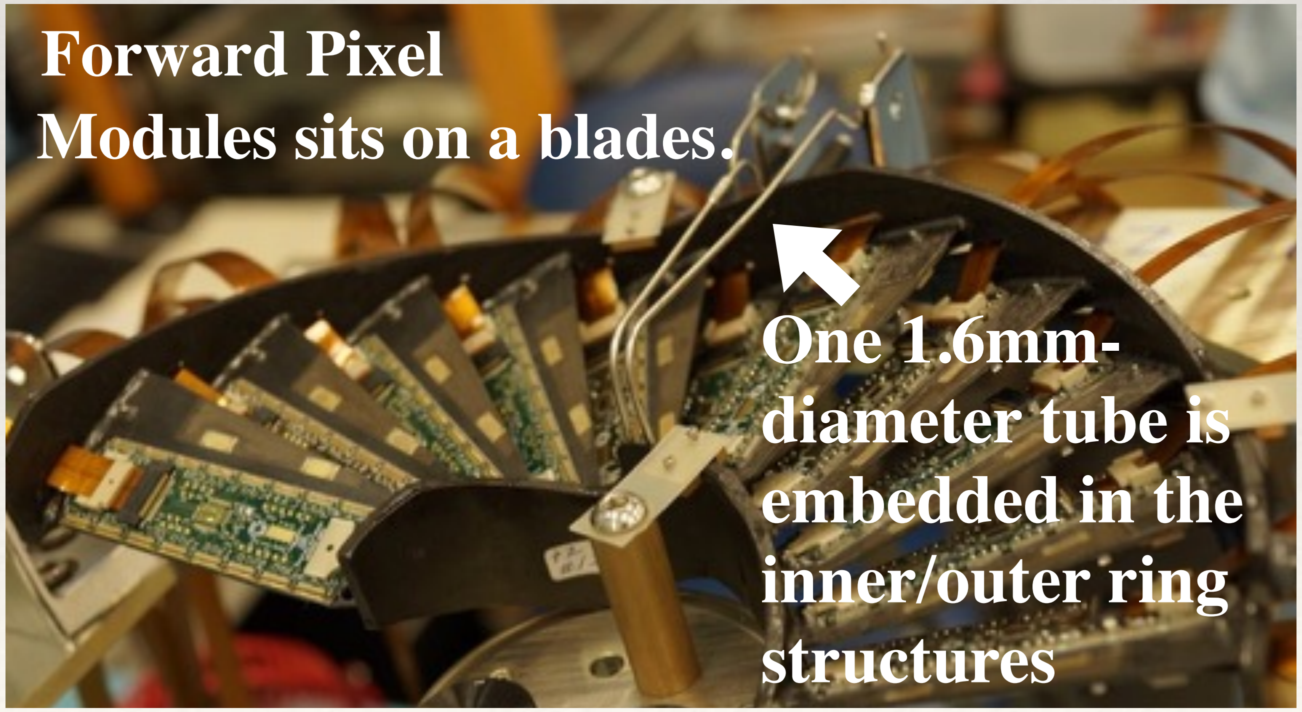


"Construction of the Phase I upgrade of the CMS pixel detector" Satoshi Hasegawa, TIPP2017, May 22-26, 2017. Presented by Benedikt Vormwald.

CO2 cooling system

- Two-phase CO_2 cooling system replaced single phase C_6F_{14}.
- Modules are mounted on carbon fibre plates, which are thermally connected to the cooling pipes.
- Less flow required by exploiting the latent heat, which can enable the radius of pipes smaller (diameter of 1.6-3.0mm, wall thickness of ~0.1-0.2mm).
- Cooling lines and connections pressure tested at 150 bar, leak tests at 100 bar, operating pressure at -20C is 20-30 bar.



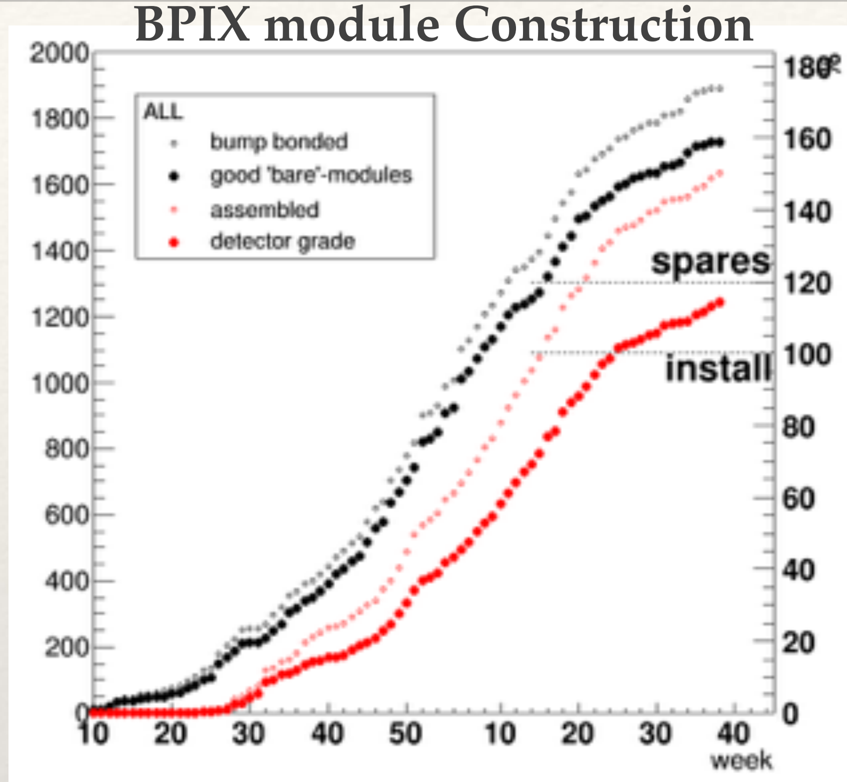


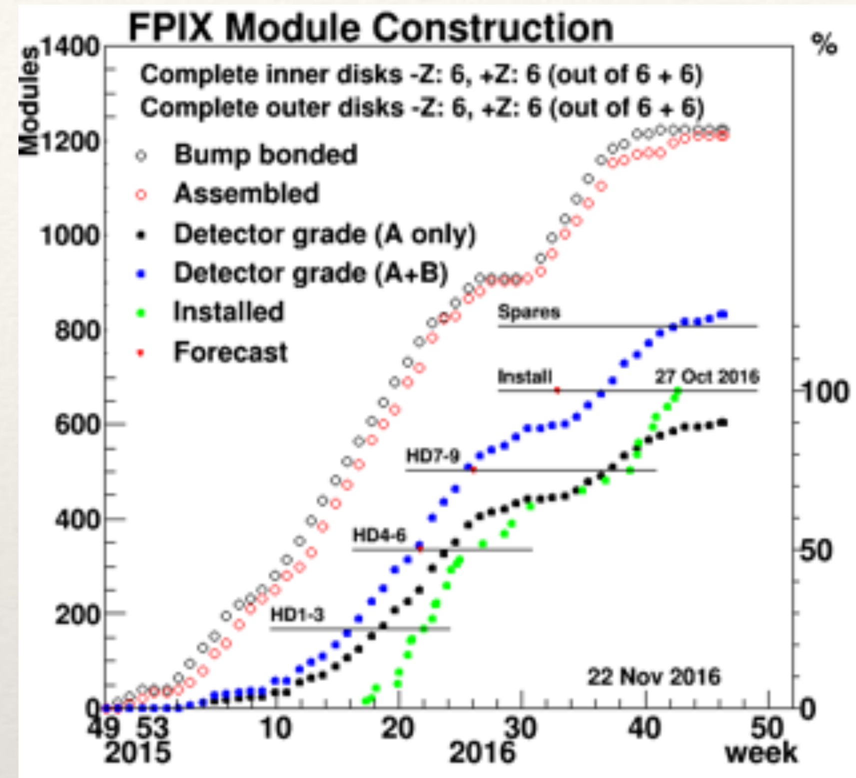
 "Construction of the Phase I upgrade of the CMS pixel detector" Satoshi Hasegawa, TIPP2017, May 22-26, 2017. Presented by Benedikt Vormwald.

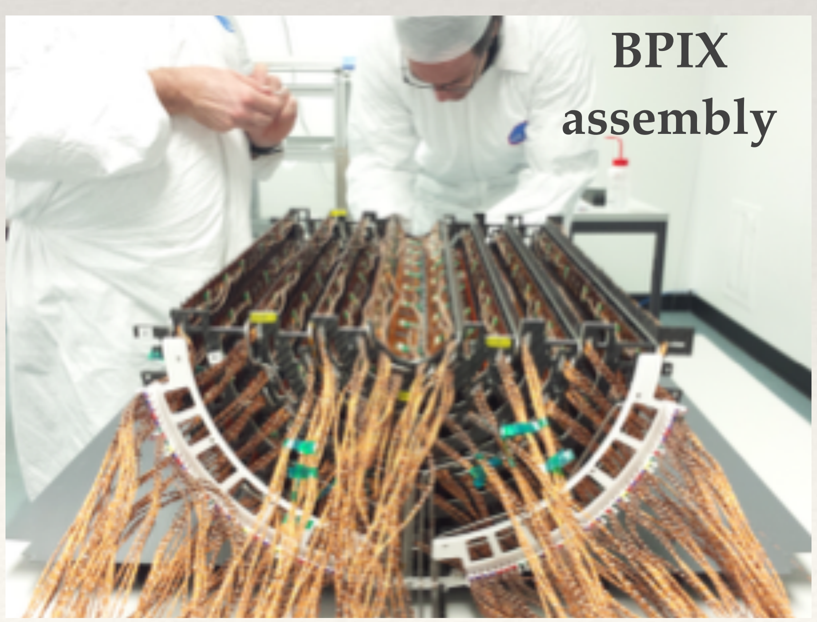
Detector construction

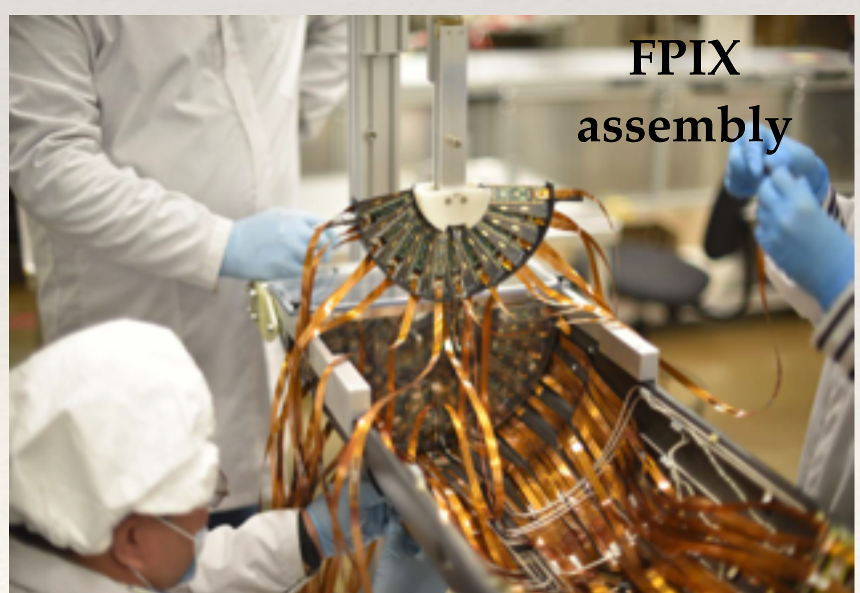
- Various module production chains
- Single set of qualification criteria.
- Results of module calibrations from test stands used as starting point for commissioning after installation
- Module production done in ~1 year

BPIX module Construction









- Detector assemblies (integration of modules, mechanics and electronics) in Switzerland (PSI+Zurich) for BPIX, in the US (Fermilab) for FPIX
- After transport to CERN full test of detectors on the surface prior to installation (see next talk)

Summary

- Upgraded pixel detector was installed to CMS at the beginning of March,
  - detector designed to remove bottleneck in readout and to provide improved performance.
- Readout system has been changed from 40MHz analogue-encoded to 320Mbps digital-encoded, with larger buffers.
  - Two types of digital readout chips have been developed.
- Detector and backend ready for data taking.
- Better tracking performance expected with additional tracking layer and reduced material in the tracker acceptance.

This is a significant improvement of the CMS detector that will enable future discoveries / high precision measurements.