Progress of PandaX-III Readout Electronics

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- **D** Background
- □ Introduction to PandaX-III TPC Detector
- **D** Design of the readout system
- Recent progress
- □ Summary



Background



 $^{A}_{Z}X \rightarrow ^{A}_{Z+1}Y + e^{-} + \nu_{e}$



 $0\nu\beta\beta$ decay





Scientific significances of searching for $0\nu\beta\beta$

- Whether neutrino is a Majorana particle or a Dirac particle
- Know the mass scale of neutrino
- Lepton number violation

Essential characteristics of 0vββ experiments

• High energy resolution

- Several percents to less than 1%

Large scale and long term operation

~100 kilogram or even scalable to ~1 ton

Ultralow radioactive background

- High radiation purity for detector materials and auxiliary facilities
- Perfect shielding (deeply under ground)
- Tracking (or other?) information may be utilized for background discrimination





Experiments for 0vββ decay searching







PandaX-III experiment

- Hopefully the first 0vββ experiment in China
- To be carried out at Jinpin underground Laboratory
 - Sichuan province, China
- Proposed in 2015
 - SJTU, USTC, PKU…









see 25/5/2017 10:12 - 10:30 AM, Ke HAN, TIPP2017 Oral talk

PandaX-III TPC detector (Phase I)



Signal features of PandaX-III TPC



- Signal amplitude: 10pC in total
 - Gain of Micromegas: 10³
 - Q_{ee} =2.5MeV, ϵ = 30eV/e
- Drift velocity : 1mm/us
- Drift length: ~1m
- Max. tracking length: ~30cm





Design specifications for the readout electronics

Readout Channels:

- ◆ 10496 channels of Micromegas strip signal
- ◆ 82 channels of mesh signal (for trigger)
- Dynamic range of each channel: $\geq 10 \text{pC}$
- Time window: $\geq 40 \mu s$
- ◆ INL: < 2%
- ♦ Noise: < 12fC (in RMS)



Choice of front-end ASIC: AGET chip

Main Features:

- Designed by Saclay, IRFU CEA, France
- 0.35um AMS CMOS technology
- 64 input channels
- Input range: 120fC/240fC/1pC/10pC
- Shaping time: 50ns 1us, configurable
- 512-cell SCA for each channel
- Sampling rate: 1MHz 100MHz, configurable



USTC



Prototype electronics with AGET chip

• To verify the design concept of front-end electronics with AGET chip





Test results of prototype electronics



Architecture of PandaX-III readout system



- □ 42 Front End Card (FEC)
 - ✓ 256 channels/FEC
- □ 2 Mesh Readout Card (MRC)
- □ Backend electronics cards
 - ✓ S-TDCM, M-TCM
 - ✓ DAQ&Trigger&Clock functions

Design of FEC module







Design of MRC module







Design of a prototype DAQ module

- A simplified version to verify the design concept of back-end electronics
- To operate together with FEC and MRC for the test of TPC R&D



- □ 6 fiber interface with FEC
- I Gb ethernet interface with PC



CHENG LI, Design of the FPGA-based Gigabit Serial Link for PandaX-III Experiment, TIPP2017 poster



Mass product









Some results of electronics tests

≻FEC

Noise: 0.7fC +0.01fC/pF (@1pC input range)
INL: ~1%

≻MRC :

□Noise <1.25fC (@10pC input range)

≻DAQ

□BER<10⁻¹³ (48 hrs)





Joint test with Micromegas at USTC



⁵⁵Fe source

Resistive Micromegas



Initial joint test with prototype TPC at SJTU





Gas: Ar + C_4H_{10} (2 bar)



Summary

- Prototype design of PandaX-III readout electronics has been finished.
- A small system of the readout electronics has been setup
 - with 5 FEC +1 MRC +1 DAQ (>1280 channels)
 - Meet the test requirements of PandaX-III TPC R&D and construction process
- Joint test with PandaX-III prototype TPC is ongoing...
 - Preliminary results show that the readout electronics performs well
- Next step: engineering design will be carried out soon



Thank you!

