Analysis and simulation of HV-CMOS assemblies for the CLIC vertex detector

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On behalf of the CLICdp collaboration

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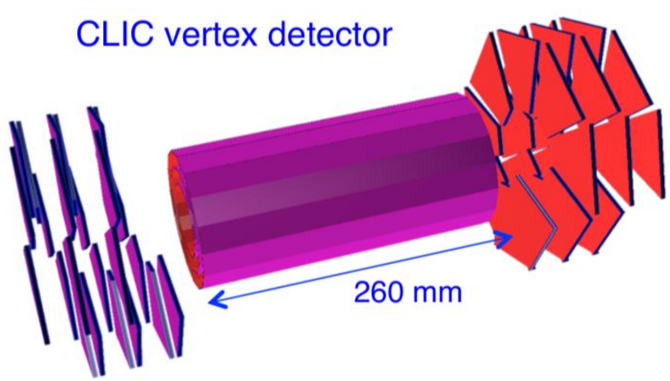
Introduction

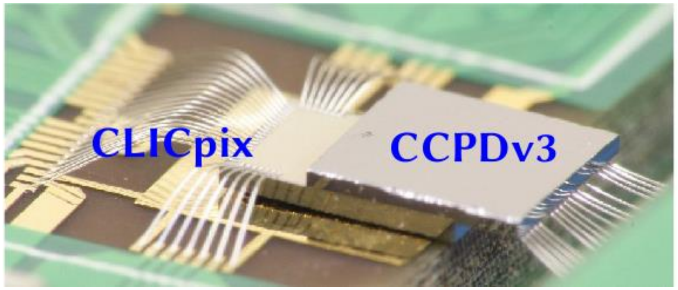
- The Compact Linear Collider (CLIC) is a proposed electron-positron collider operating at energies up to 3TeV
- Precision physics requirements and the experimental environment impose stringent conditions on the vertex detector:
  - 3 μm point resolution
  - Low material budget, ~0.2% X_0 per layer => thin sensors, forced air cooling
  - Low power consumption => power pulse operation
  - ~10 ns time stamping to reduce backgrounds => fast signal generation

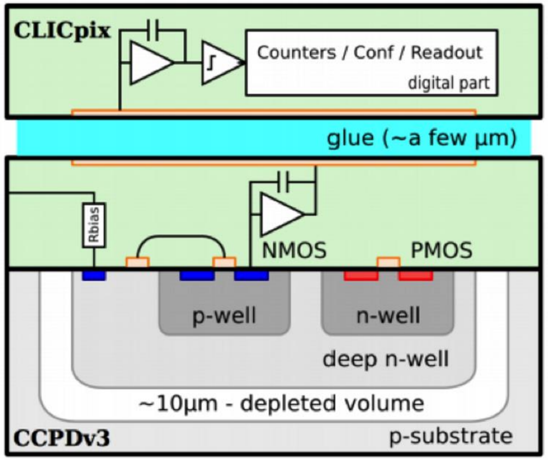
- HV-CMOS sensors capacitively coupled to readout electronics are one of the proposals for the vertex detector technology
  - Prototype assemblies produced to measure performance
  - Simulations carried out to reproduce results
  - Use simulations to help with future sensor design



HV-CMOS for CLIC

- High-voltage CMOS (HV-CMOS) embeds the pixel circuitry inside a deep n-well, which isolates them from the substrate
- Shielding allows a bias voltage to be applied to the substrate => large depletion region
- Deep n-well acts as the charge collection diode
- Dedicated HV-CMOS chip was produced for CLIC - CCPDv3 - for use as a capacitively coupled sensor. Small pitch (25µm), no bump-bonding
- The sensor is coupled to the CLICpix readout ASIC (64x64 pixels), contains a 4-bit time over threshold (ToT) and time of arrival (ToA) counter
- Testbeams with prototype assemblies carried out at the CERN SPS with 120 GeV/c pions

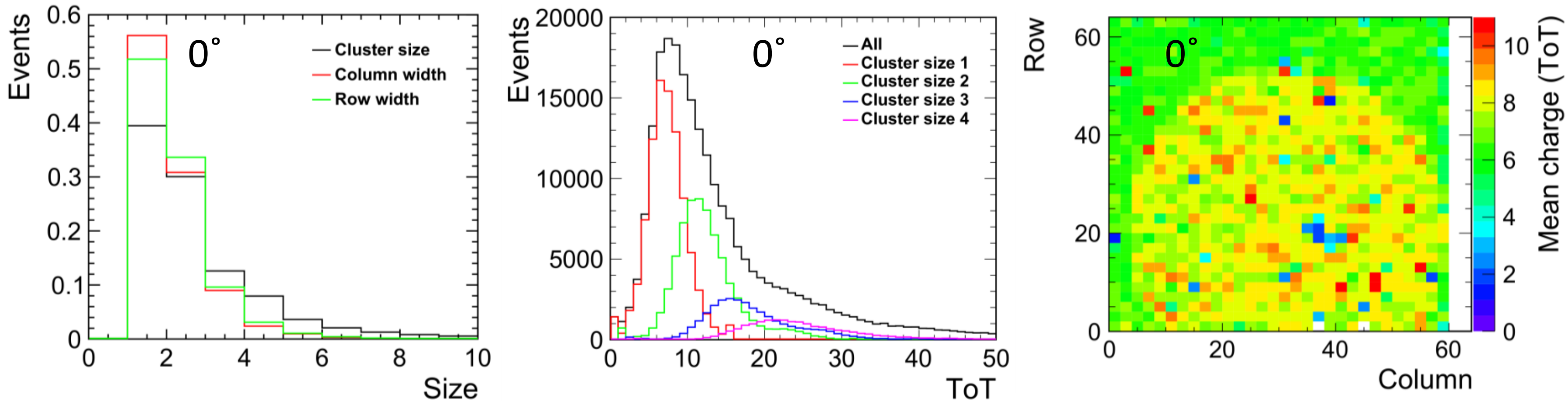




Performance measurements: testbeam

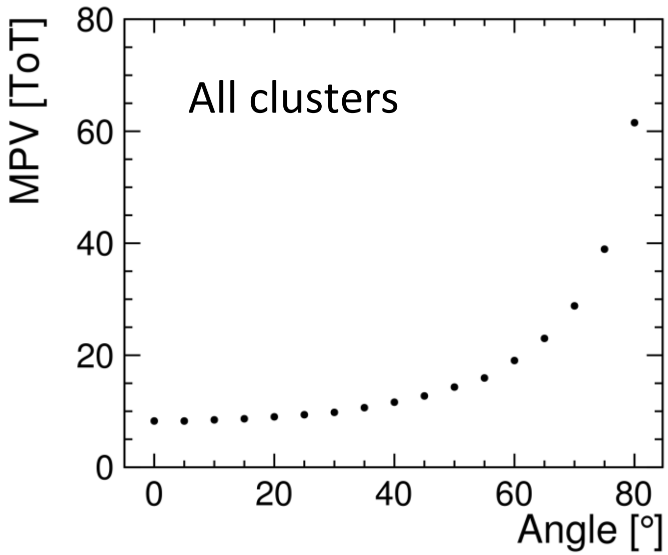
Charge collection & signal propagation

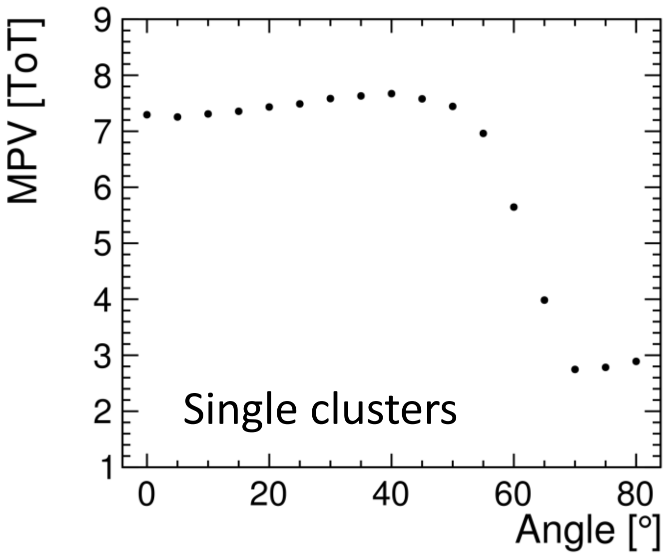
- At perpendicular incidence there is limited charge sharing hence there are mainly 1-2 hit clusters (active depth ≈26μm, slide 10)
- Mean ToT over the chip shows non-planarity, with a circle of higher ToT => stronger coupling due to a glue spot (seen only in some assemblies)
- Efficiency of 99.7% measured
- Angular studies are needed to determine the performance expected in the geometry of the CLIC vertex detector



Charge collection at inclined angles

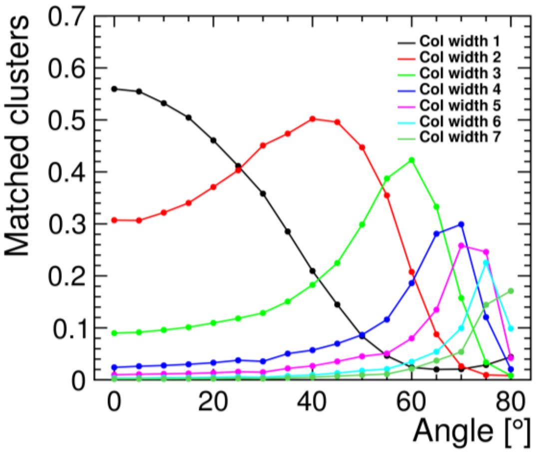
- As expected the most probable value for the cluster ToT increases with angle
- For single pixel clusters there is a sharp drop at 50˚, as the track passes geometrically through multiple pixels
- This drop results from a combination of low charge deposited and/or several neighbours being under threshold

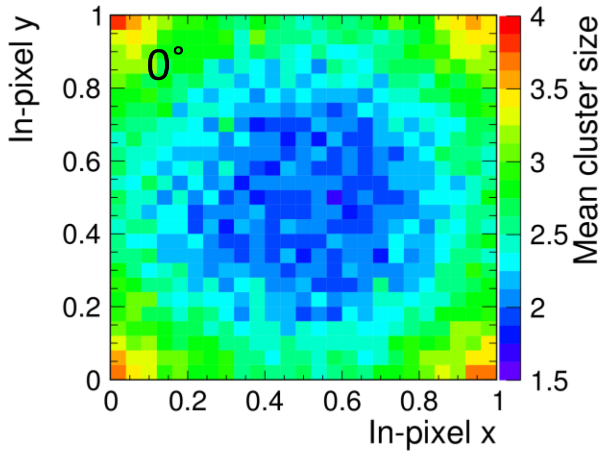


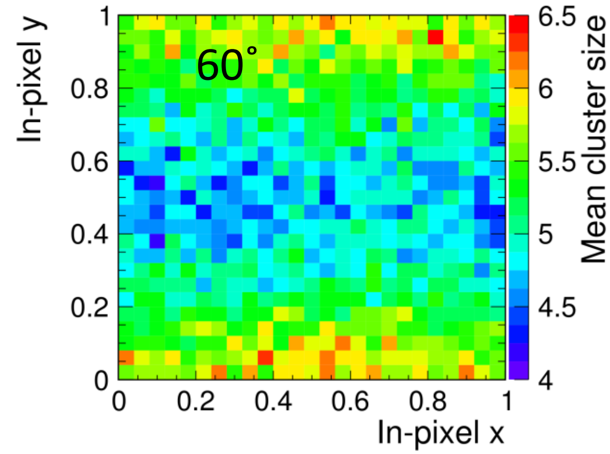


Cluster formation

- At angles up to 60˚, dominated by clusters with column width < 4
- At 80˚the dominant width becomes 7
- The in-pixel mean cluster size at 0˚ shows mainly 1-hit clusters in the centre and larger clusters at the edges, as expected
- At 60˚ there is a strip through the centre of size 4 along the inclined axis, at the top and bottom there are cluster sizes 5-6 due to sharing with neighbours in the row direction

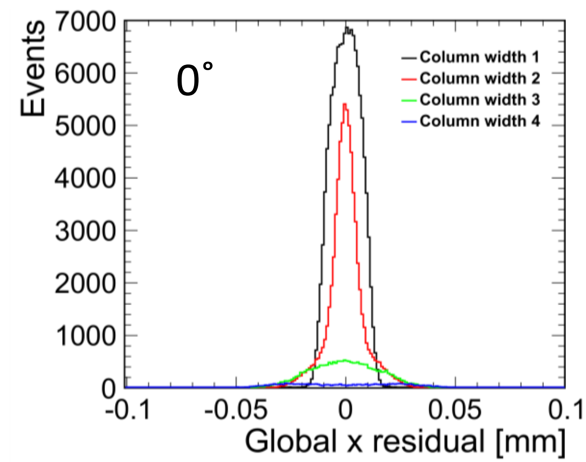


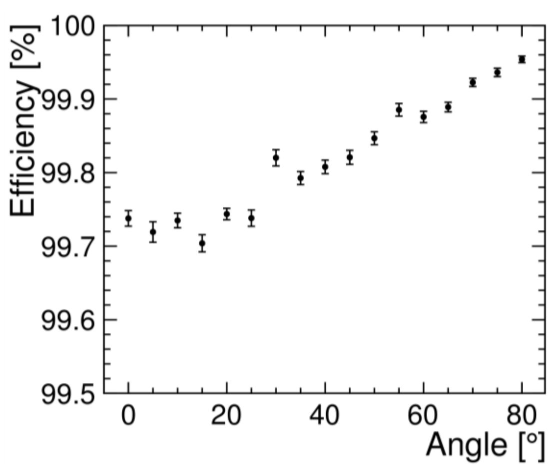


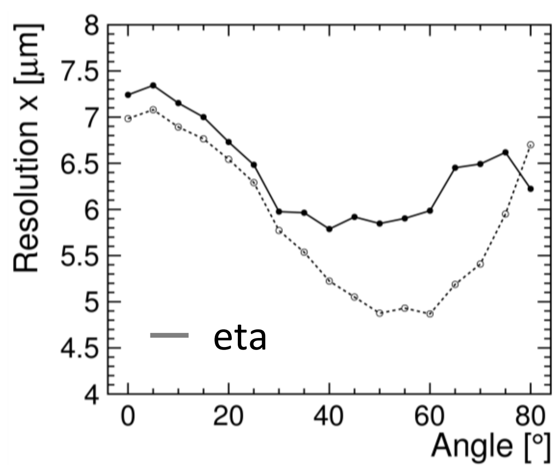


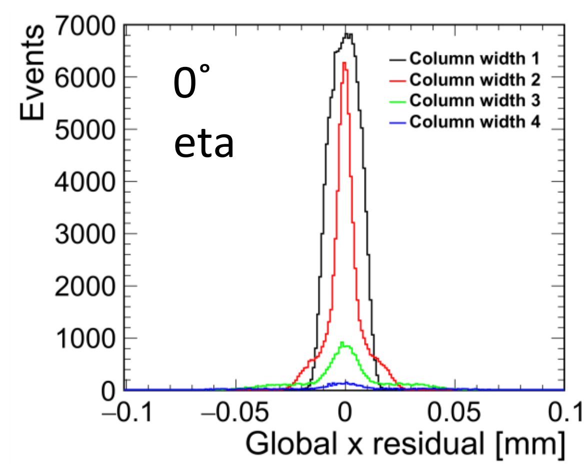
Tracking performance

- Vertex detector needs good efficiency (>99%) and spatial resolution (3µm)
- Very high efficiency over whole angle range
- Resolution not at target, improve this with eta correction (correct for the effects of non-linear charge sharing), still not at target
- Although the residuals are limited by cross-coupled hits, we suffer more from limited charge diffusion (small cluster size)



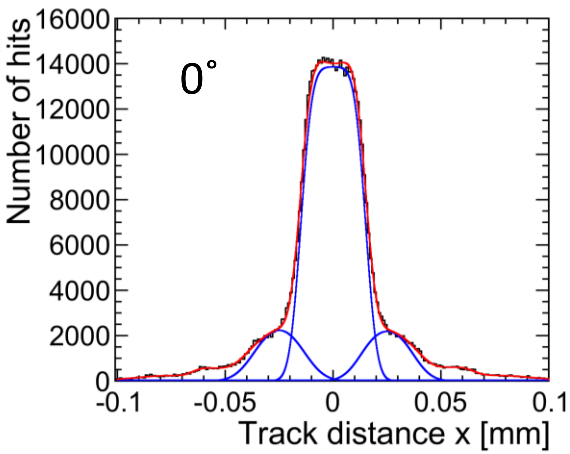


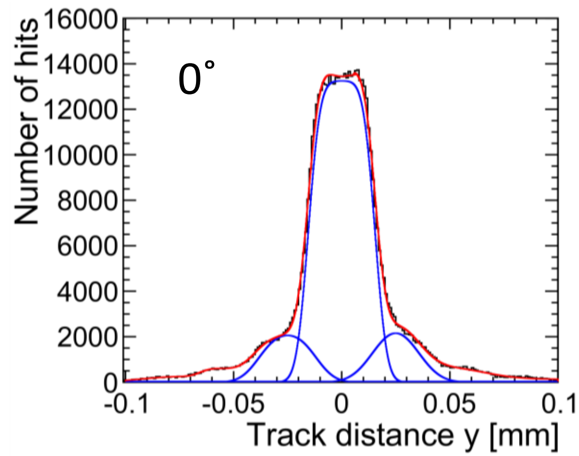


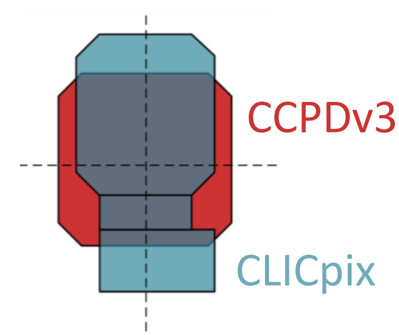


Cross-coupling

- Signal is transferred over pixel-to-pixel capacitance, but capacitance to neighbours could be non-zero
- Signal on one HV-CMOS pixel could be transferred to multiple pixels on the readout side (cross-coupling)
- Scan beam along the matrix to see when a pixel responds, produces a central peak from “real” charge collection and additional peaks from cross-coupling
- Symmetric in both column and row direction at 0˚, in accordance with the metal pads being aligned by centre of gravity

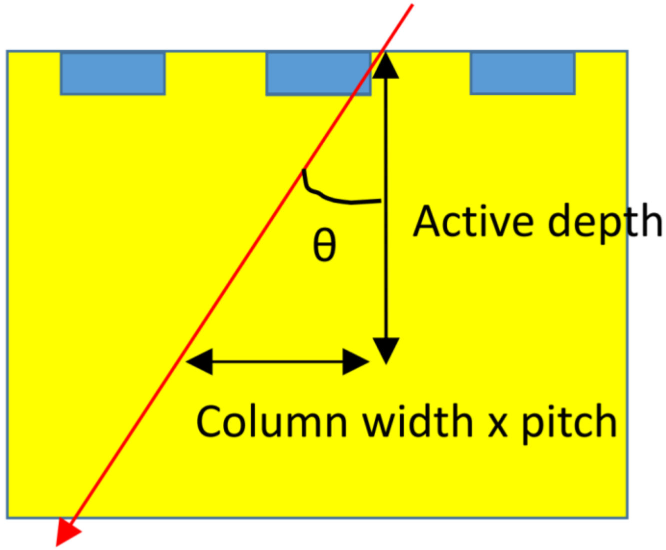


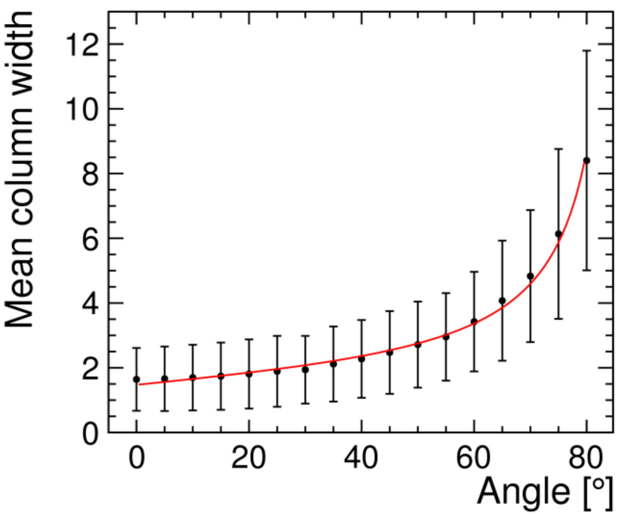




Active depth

- The exact depletion depth for the samples is not known, there are contributions from drift and diffusion: try to gauge the active depth
- This is how deep into the sensor charge contributes to the signal, a rough estimate is given by a geometric approximation
- Fit: column width$= \tan(\theta + \Delta\theta)\frac{d}{p} + c$, where d=active depth p=pitch, $\Delta\theta$=angular offset and c=intercept
- Active depth of ≈26μm, estimate of the depletion depth is 10-15μm => have contribution from diffusion

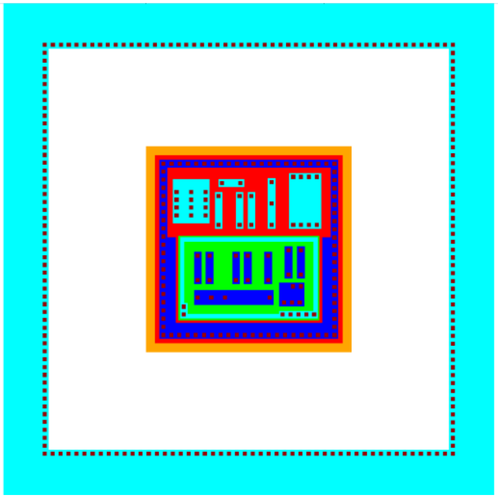


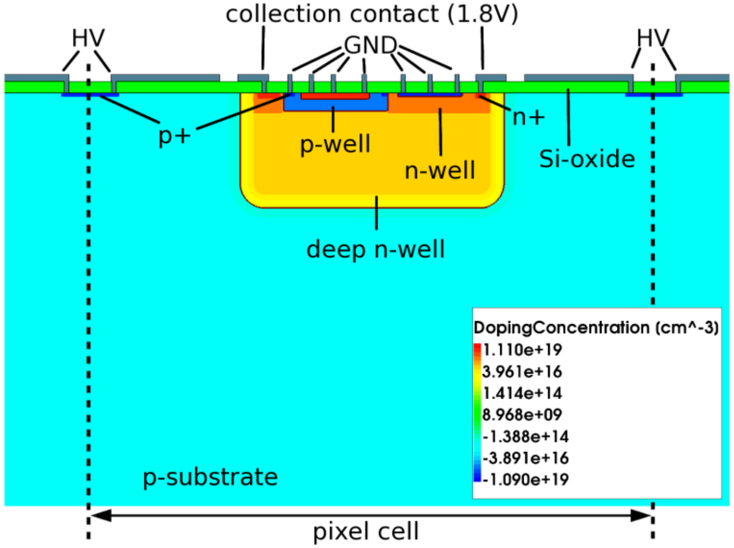


Interpreting the results: simulations

TCAD simulations

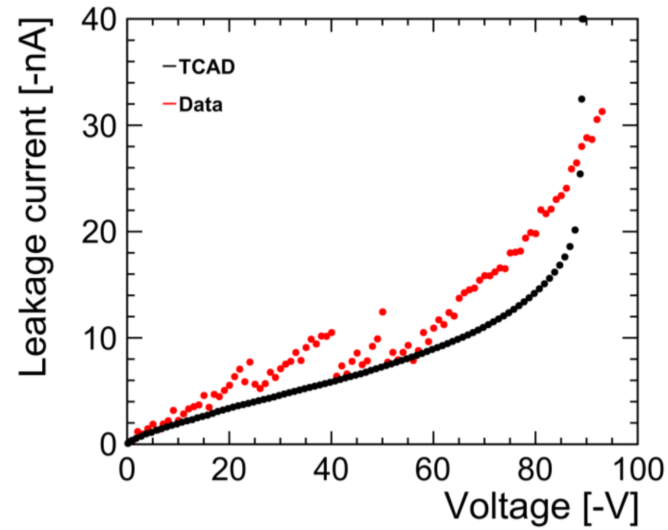
- TCAD is a finite element simulator used for semiconductor fabrication and for studying the behaviour of complex structures
- The simulations can help to understand features of the sensor:
  - Current-voltage characteristics and breakdown
  - Depletion region
  - Signal collection
- Using the design file (gds) of the chip can produce structures in TCAD
- Extraction of the relevant implant layout is used to create a mask for the simulations

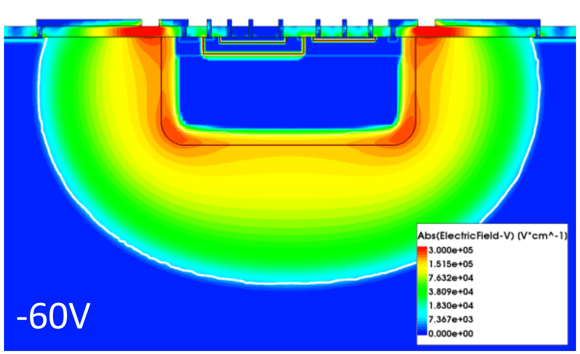


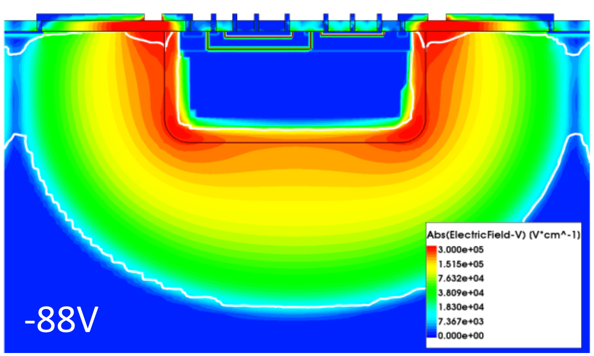


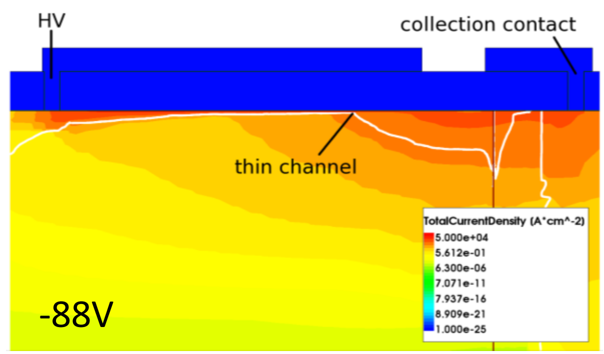
Electric field and leakage current

- Both leakage current and breakdown are reproduced well in simulations
- Breakdown: data -93V, TCAD -88V
- Large electric field near the deep n-well
- Depletion region extends from deep n-well, gives fast charge collection across pixel
- At high enough bias a thin channel forms which shorts the HV and deep n-well



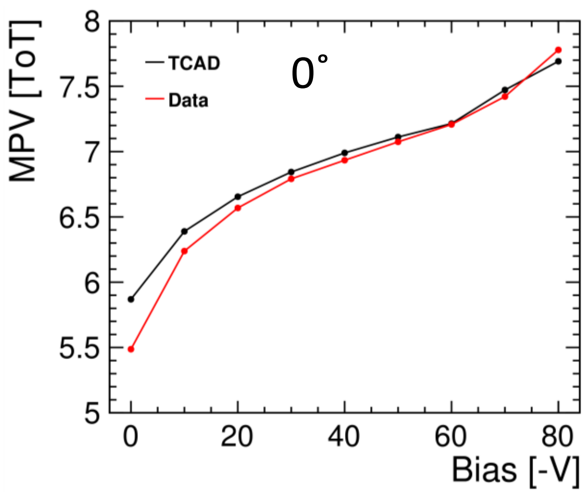


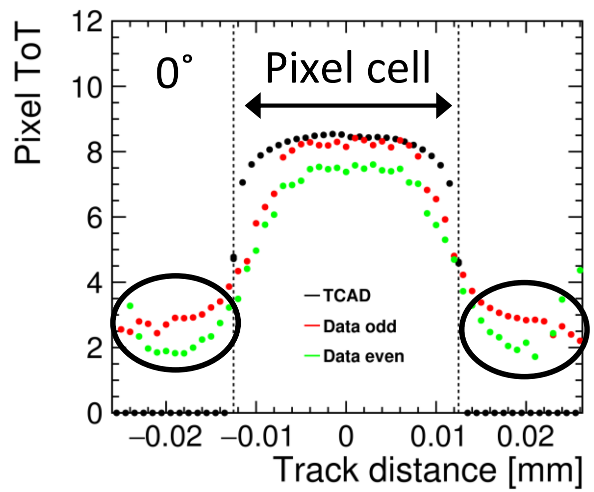


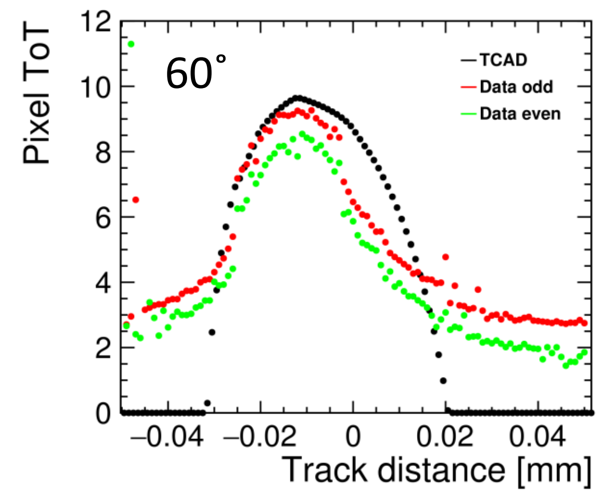


Charge collection simulations

- Calibrations with a radioactive source are used to convert the TCAD output to ToT
- Bias scan at 0° matches with data, the increase in gradient at -70V and -80V due to avalanche multiplication
- Pixel ToT response is split into two for data due to a known bug: charge injection for certain columns (not in the simulation)
- TCAD matches well at 0° but the width is too large at 60° possibly due to neighbours in the row direction being under threshold or limitations of 2D simulation
- ToT values of ≈3 at the sides due to cross-coupling, not put into simulation

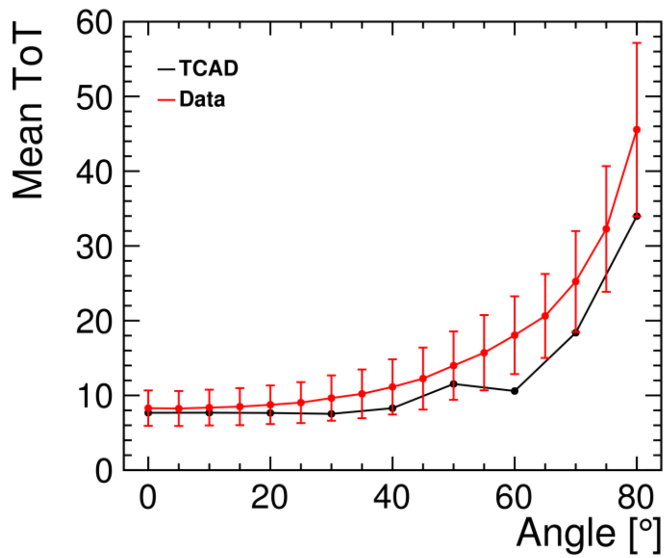


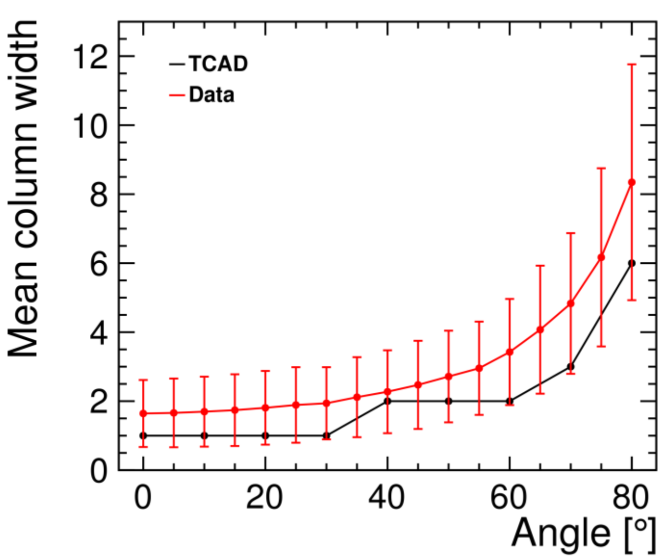




Charge collection simulations

- Mean collected charge and cluster width in the direction of rotation as a function of angle match well with data
- All TCAD charge collection results are similar to data but some effects produce deviations:
  - No Landau deposition of charge considered in simulation
  - Variations in calibration

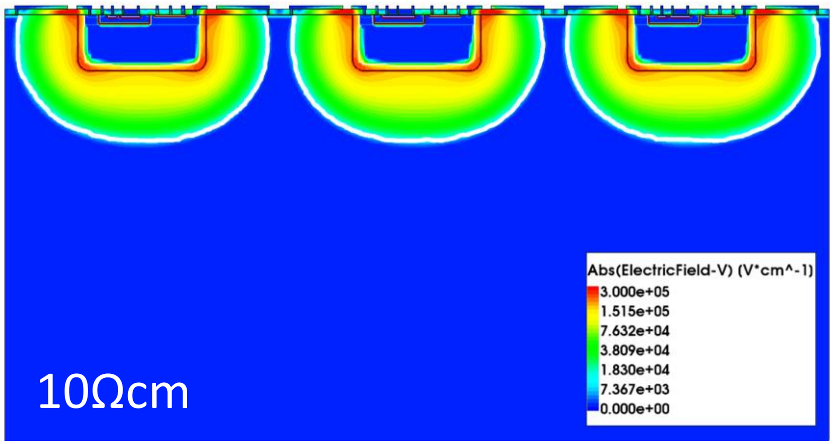


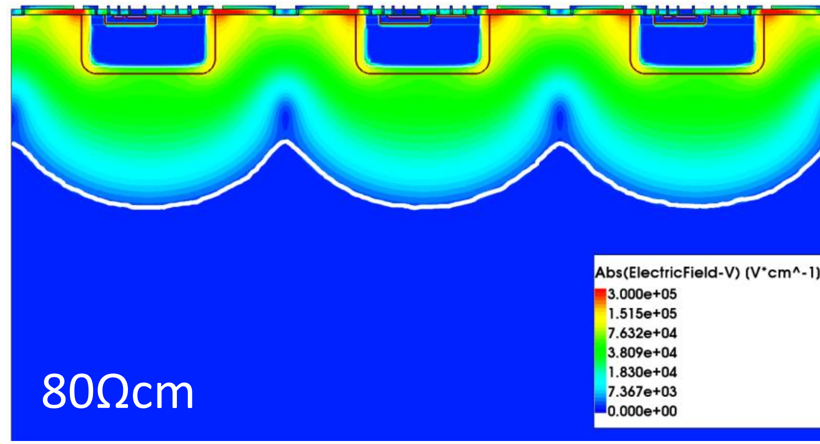


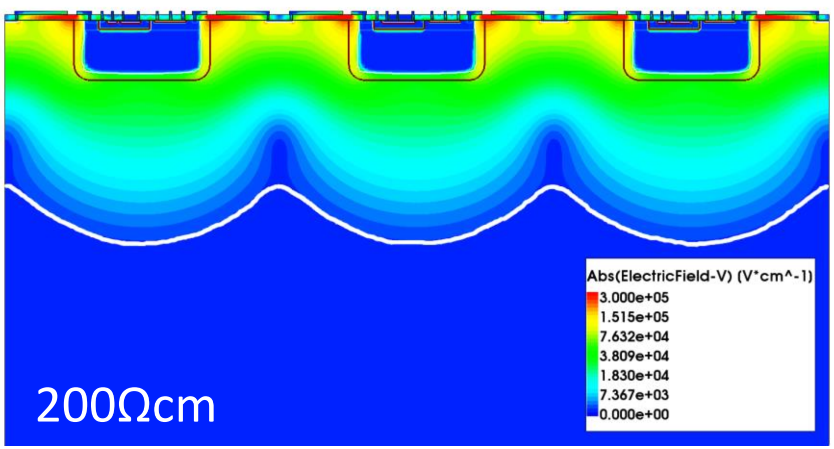
Prospects for improved performance

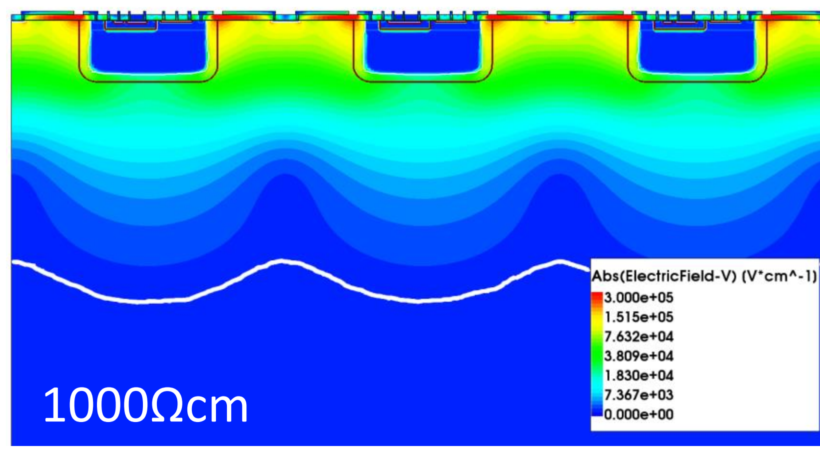
Substrate resistivity

- Increase in electric field depth and depletion depth with resistivity
- Field strength underneath deep n-well decreases



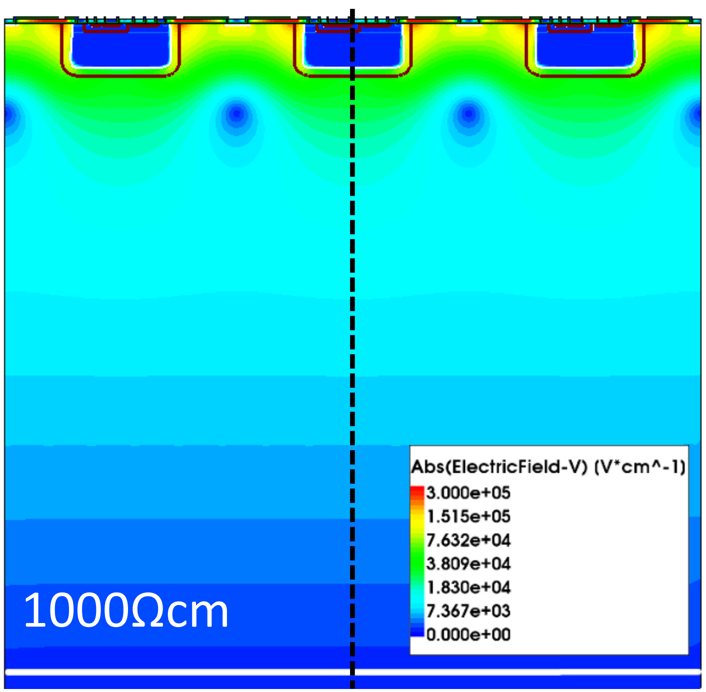


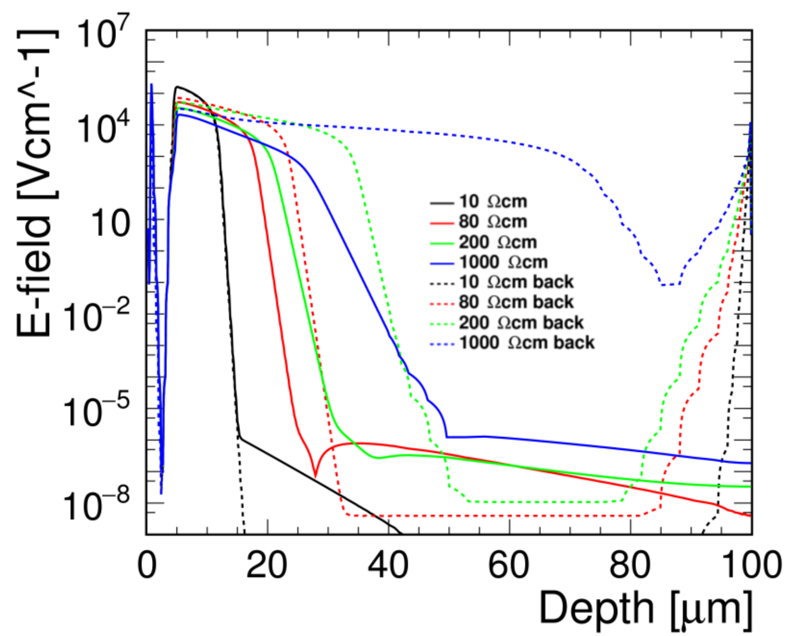




Back-side biasing

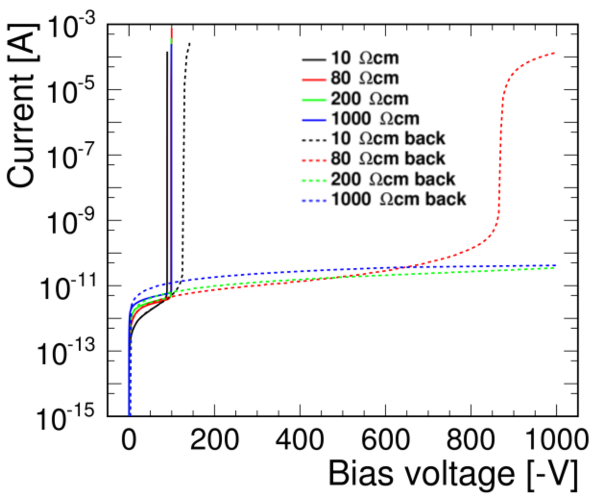
- Biasing from the back by adding a p+ implant along the backside
- See a larger increase in E-field depth and depletion depth
- Compare to topside biasing:
  - No difference at 10Ωcm
  - Difference in depletion depth at 1k Ωcm is ~40 μm

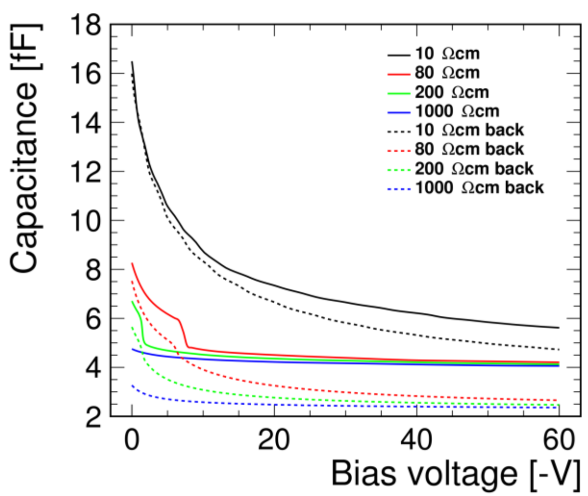


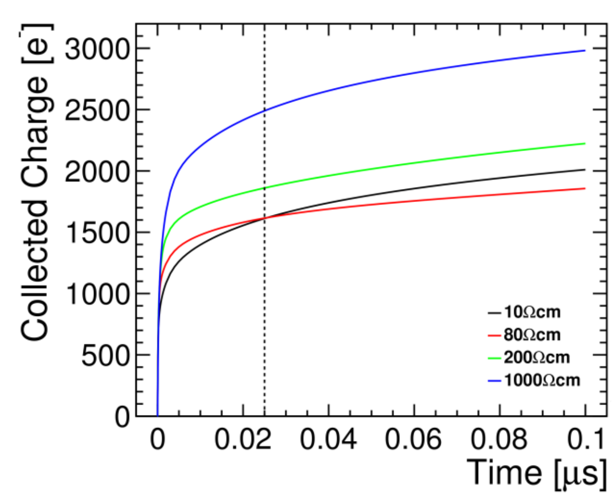


Voltage characteristics and charge collection

- Higher resistivities also produce:
  - Larger breakdown voltages
  - Smaller deep n-well to bulk capacitance, less noise
  - Larger and faster charge collection, improved timing performance
- Again 1k Ωcm produces the largest improvement
- Improvements in IV and CV from higher resistivity are magnified when biasing from the back







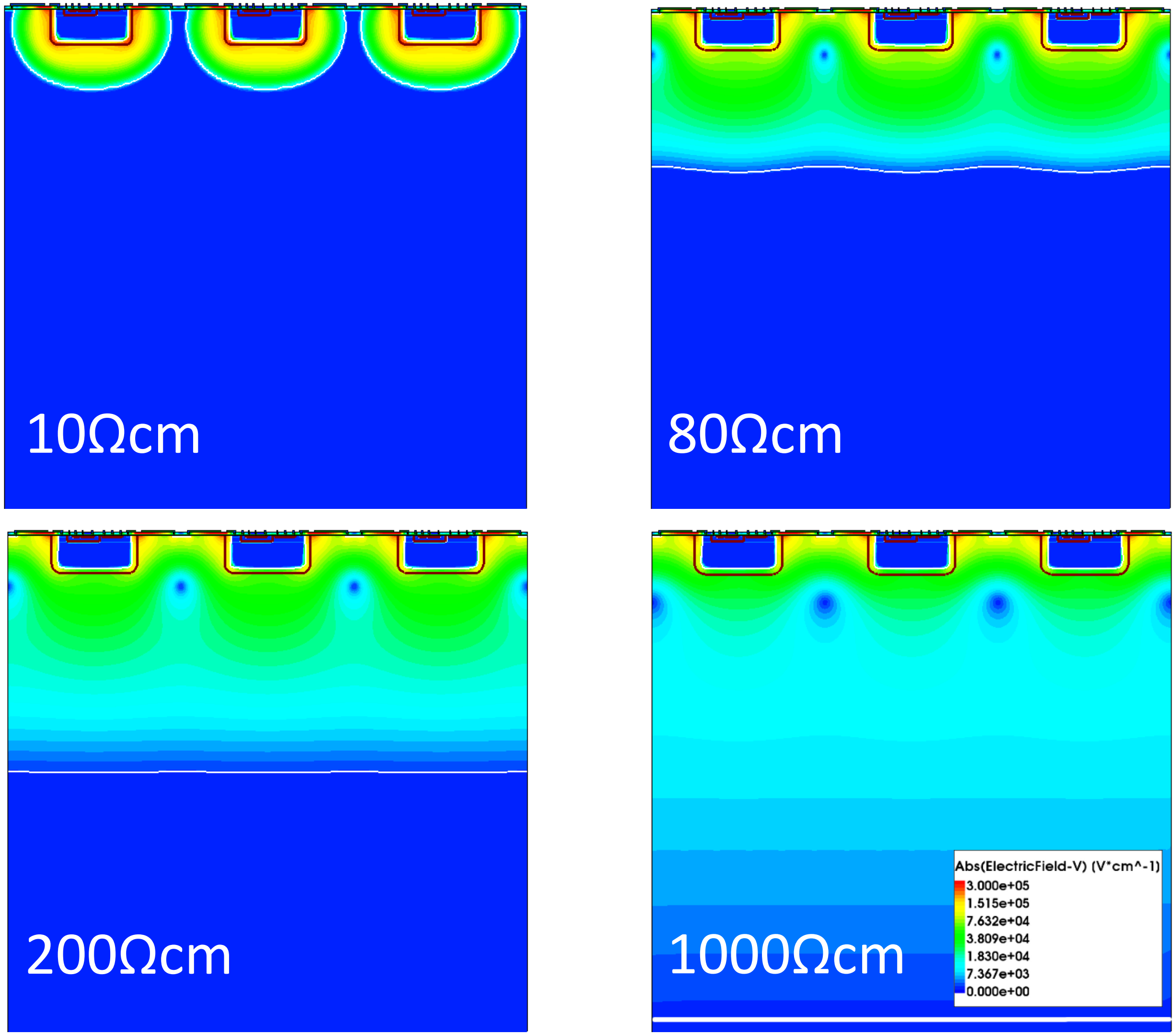
Summary

- Measurements of HV-CMOS assemblies for the CLIC vertex detector have shown excellent tracking efficiency and the resolution is as expected across the full detector acceptance
- TCAD simulations have been used to estimate sensor properties and compare well to measurements
- Using a higher resistivity should lead to larger breakdown voltages, smaller capacitance and faster charge collection, with even greater improvements for backside biasing

Backup

Electric field and depletion depth

- Biasing from the back



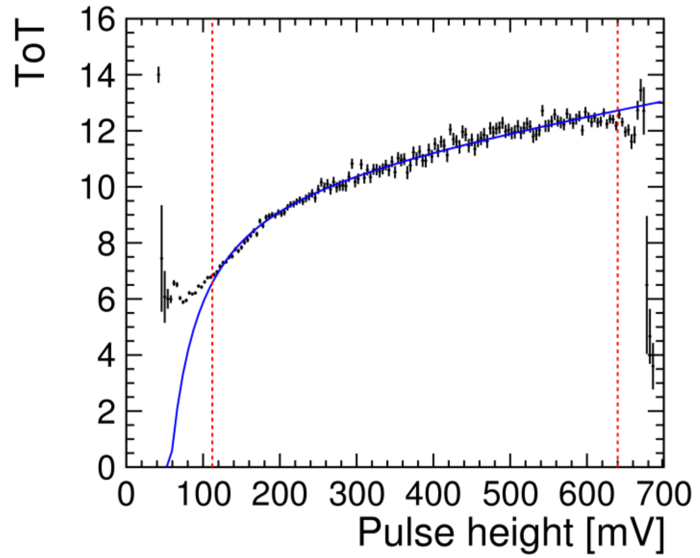
Calibration

- TCAD outputs a current which is integrated w.r.t time to get a charge
- The CCPDv3 two stage amplifier is then simulated
- For the first stage the charge gain depends on the feedback capacitance, C_{fb}, which is estimated to be 1.5 fF, from simulations
- The charge is converted to a voltage using:

$$\Delta V = \frac{\Delta Q}{C_{fb}}$$

- For the second stage CADENCE simulations gave a peak-to-peak gain of ~1.15
- The TCAD pulse height is then converted to ToT using the calibration curve which is fitted with the surrogate function:

$$y = [0]x + [1] - \frac{[2]}{x-[3]}$$



Charge collection TCAD

- First simulation did not match the data, left plot
- Introduced the avalanche model and matches the data better, right plot