Design of High Performance Compute Node for Belle II Pixel Detector Data Acquisition System

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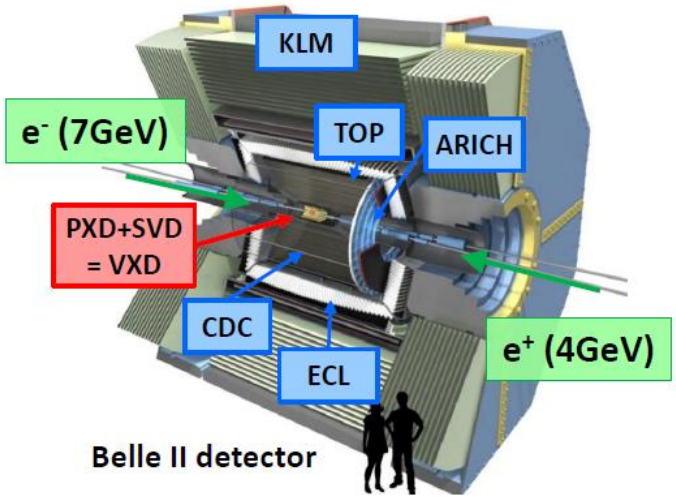
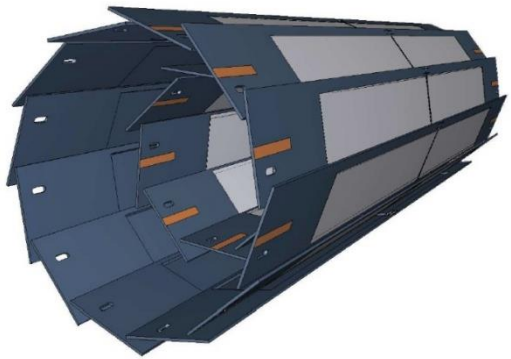
Outline

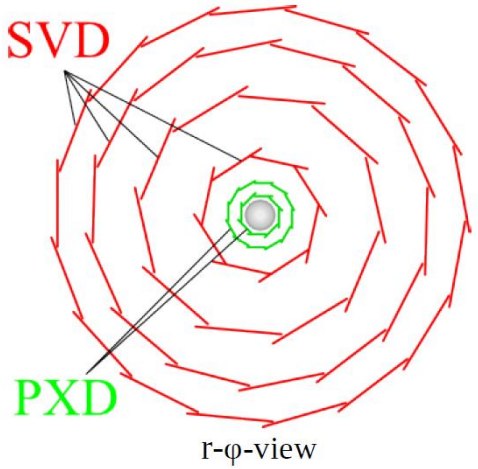
- Belle II Pixel Detector(PXD) and DAQ requirement
- Design of Compute Node
- Status of Belle II PXD-DAQ
- Summary

Belle II Pixel Detector

- PXD detector is a new detector in the upgrade of Belle II. It is consisted of DEPFET sensors, ASIC readout, cooling and structure frame.
- It has two layers. 8 ladders (16 half ladder) in inner layer and 12 ladders (24 half ladder) in outer layer.
- 4 layers SVD outside PXD.
- Huge data output
  - 240Gb/s
  - >sum of Belle II other detectors 24Gbps

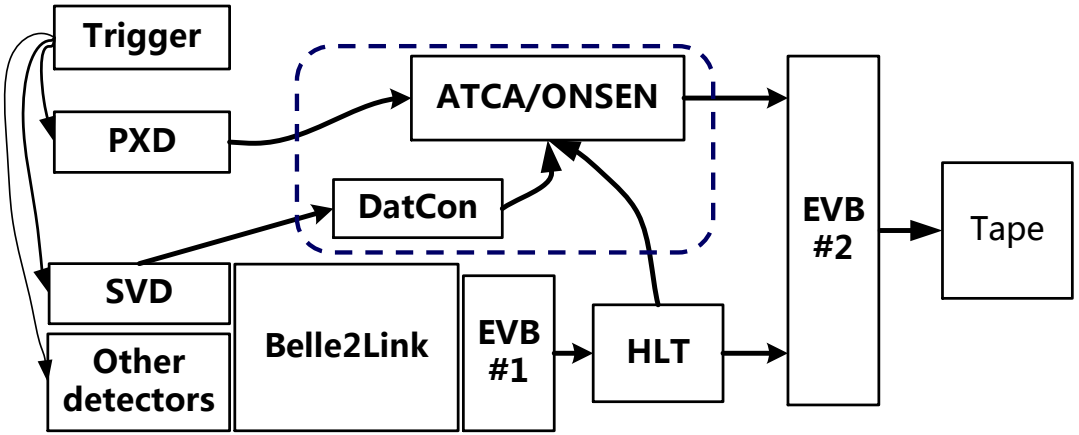


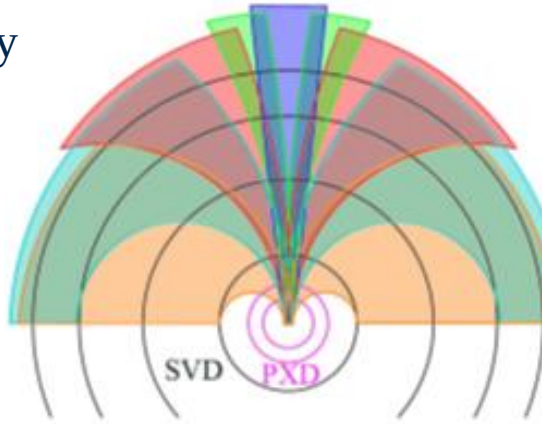


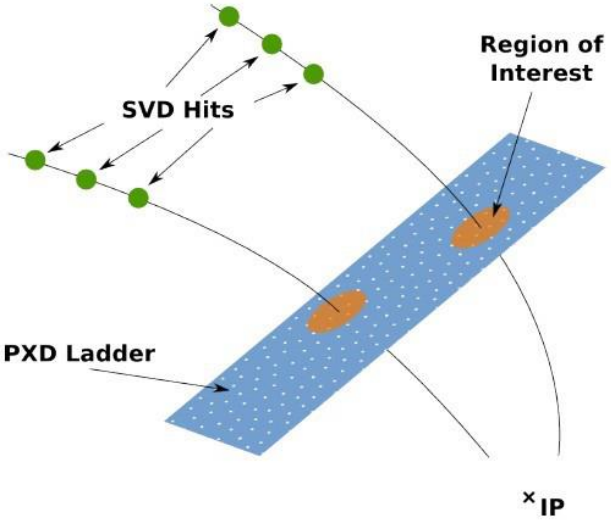


Principle of reduction

- **Reduction 1/30**
- **PXD reduction**
  - Based on HLT result
    - 1/3 reduction
  - Help with SVD data
    - 1/10
  - Tracking back
  - ROI searching
  - Data extraction
- **Difficulties**
  - Computing capability
  - Algorithms
  - 5s data buffer
- Data sharing between Processing node







Belle II PXD data rate

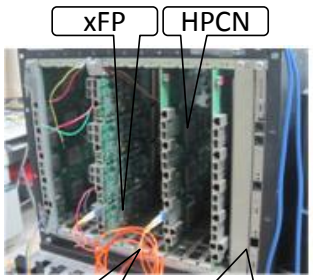
average occupancy	1%	
maximum occupancy	3%	(A. Moll: inner ≈ 1%, outer ≈ 0.5%)
average cluster size	2	(A. Moll: ≈ 2.281)
pixel per half ladder	$0.192 \cdot 10^6$ pixel	250 · 768 Pixel
number of half ladder	40	
pixel full PXD	$7.68 \cdot 10^6$ pixel	$40 \cdot 0.192 \cdot 10^6$ Pixel
average fired pixel rate (half ladder)	$43.6 \cdot 10^6$ Hz	$0.192 \cdot 10^6$ pixel · 22.7 kHz · 1%
maximum fired pixel rate (half ladder)	$131 \cdot 10^6$ Hz	$0.192 \cdot 10^6$ pixel · 22.7 kHz · 3%
average fired pixel rate (PXD)	$1.74 \cdot 10^9$ Hz	$40 \cdot 43.6 \cdot 10^6$ Hz
maximum fired pixel rate (PXD)	$5.23 \cdot 10^9$ Hz	$40 \cdot 131 \cdot 10^6$ Hz
average data rate (half ladder)	174 MB/s	4 byte · $43.6 \cdot 10^6$ Hz
maximum data rate (half ladder)	523 MB/s	4 byte · $131 \cdot 10^6$ Hz
average data rate (PXD)	6.97 GB/s	4 byte · $1.74 \cdot 10^9$ Hz
maximum data rate (PXD)	20.9 GB/s	4 byte · $5.23 \cdot 10^9$ Hz
reduction rate by HLT	3	
reduction rate by ROI selection	10	
average output rate (half ladder)	5.81 MB/s	$\frac{1}{3} \cdot \frac{1}{10} \cdot 174$ MB/s
maximum output rate (half ladder)	17.4 MB/s	$\frac{1}{3} \cdot \frac{1}{10} \cdot 523$ MB/s
average output rate (PXD)	232 MB/s	$\frac{1}{3} \cdot \frac{1}{10} \cdot 6.97$ GB/s
maximum output rate (PXD)	697 MB/s	$\frac{1}{3} \cdot \frac{1}{10} \cdot 20.9$ GB/s

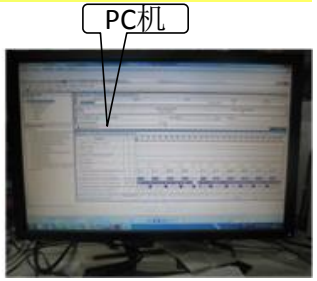
Design of PXD-DAQ

- High Performance FPGA is used for data computing,
- RocketIOs are used for high speed data transmission between data processing node,
- DDR is used for mass data buffering,
- ATCA/xTCA architecture is used for PXD DAQ,
- Intelligent platform management control system is used for system stable.

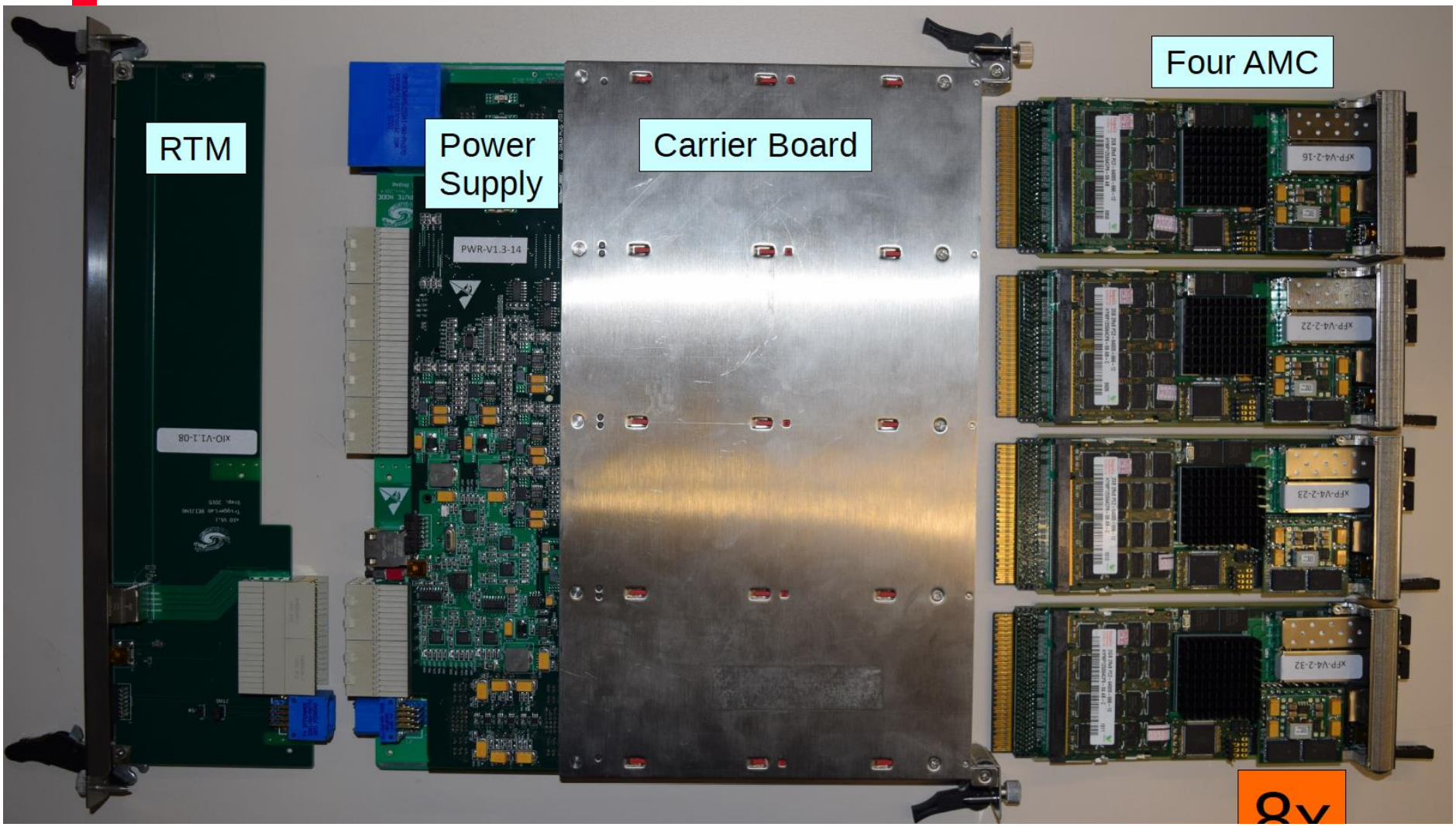
Key parts of PXD-DAQ

- ONSEN/PXD-DAQ
  - Firmware(Giessen Uni)
  - Hardware(IHEP Beijing)
    - 1 ATCA Shelf
    - 2 shelf managers
    - 1 Power Supply
    - 9 Compute Node(CN)
      - 1 ATCA Carrier(PICMG3.8)
      - 1 RTM
      - 1 Power Board
      - 4 xFP/AMC cards
      - 1 IPMC+ 4 MMCs



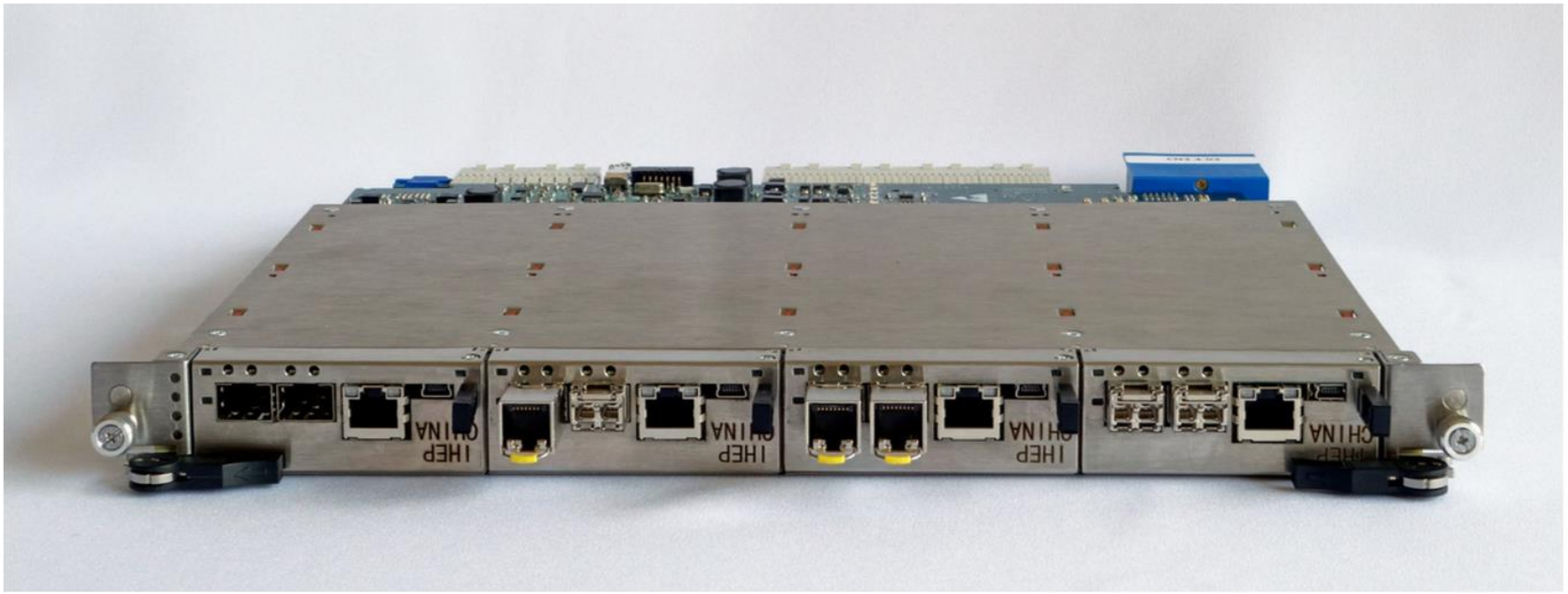


Full Compute Node



Carrier Board

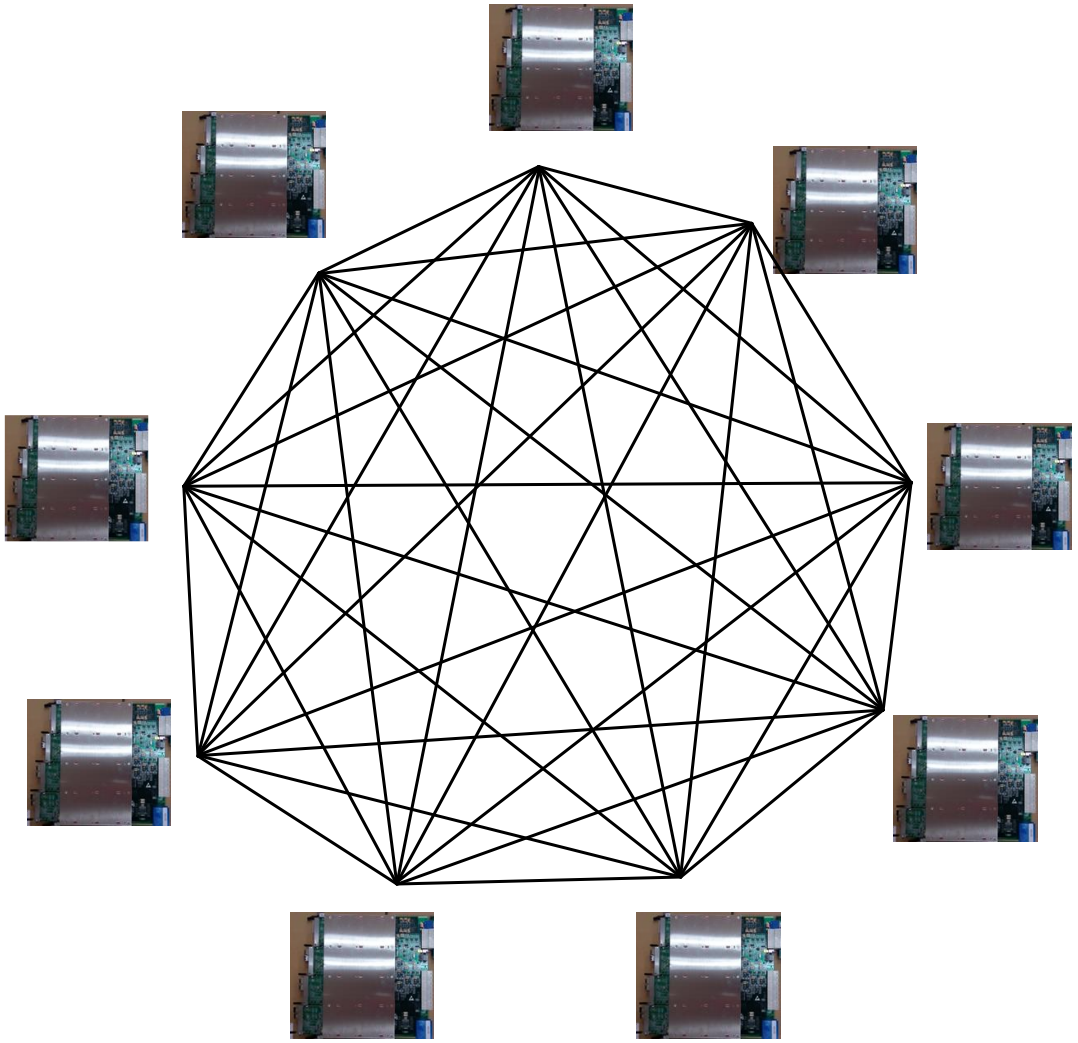
CNCB (Compute Node Carrier Board) v3.3 (May 2015)



- Four full-width **AMC slots**
- Virtex-4 FX60 FPGA as **switch** to ATCA backplane

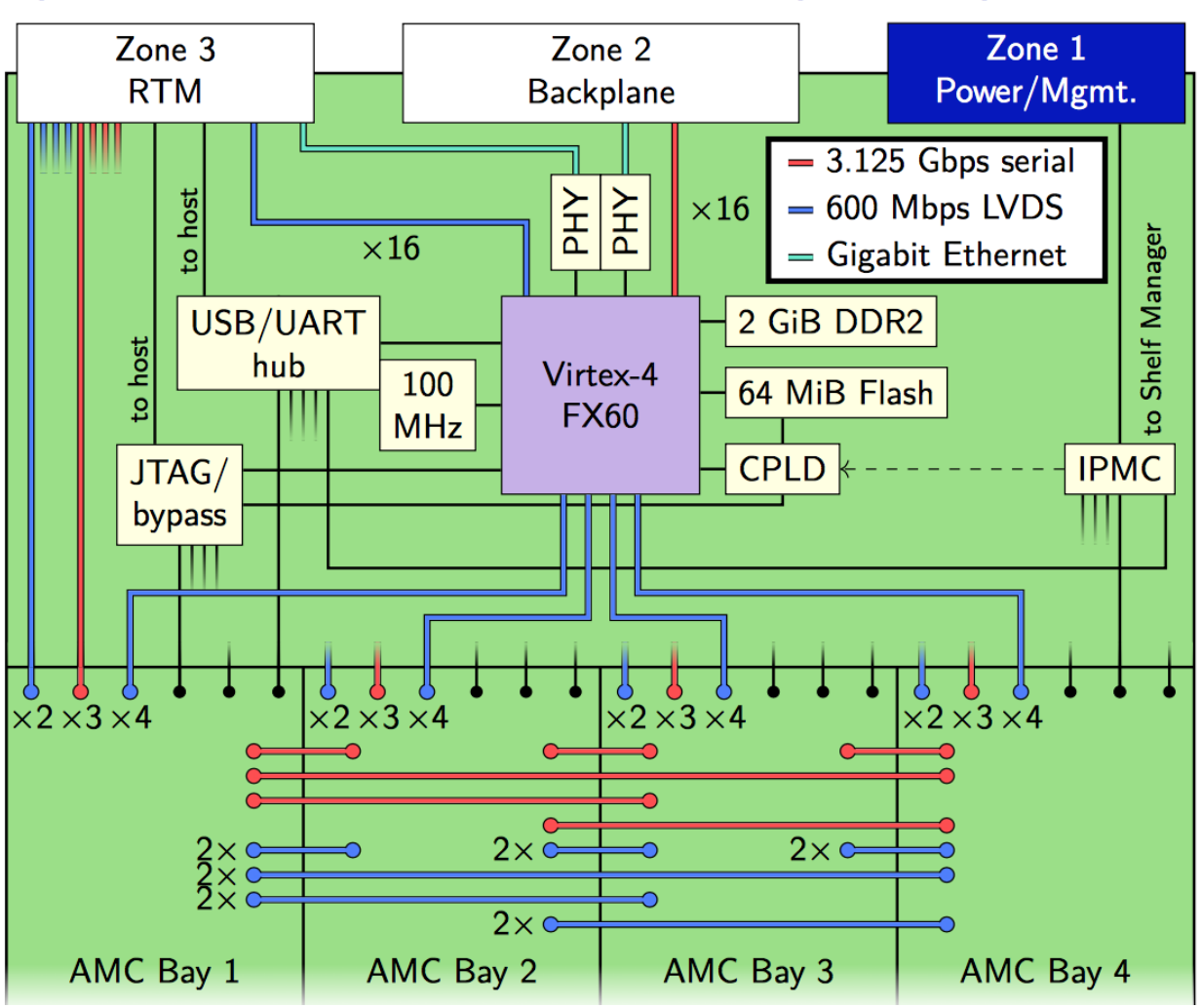
Backplane Full Mesh for CN

- Full mesh backplane for CN data share with each node,
- Point to Point via one MGT channel,
- Line rate up to 3.125Gbps



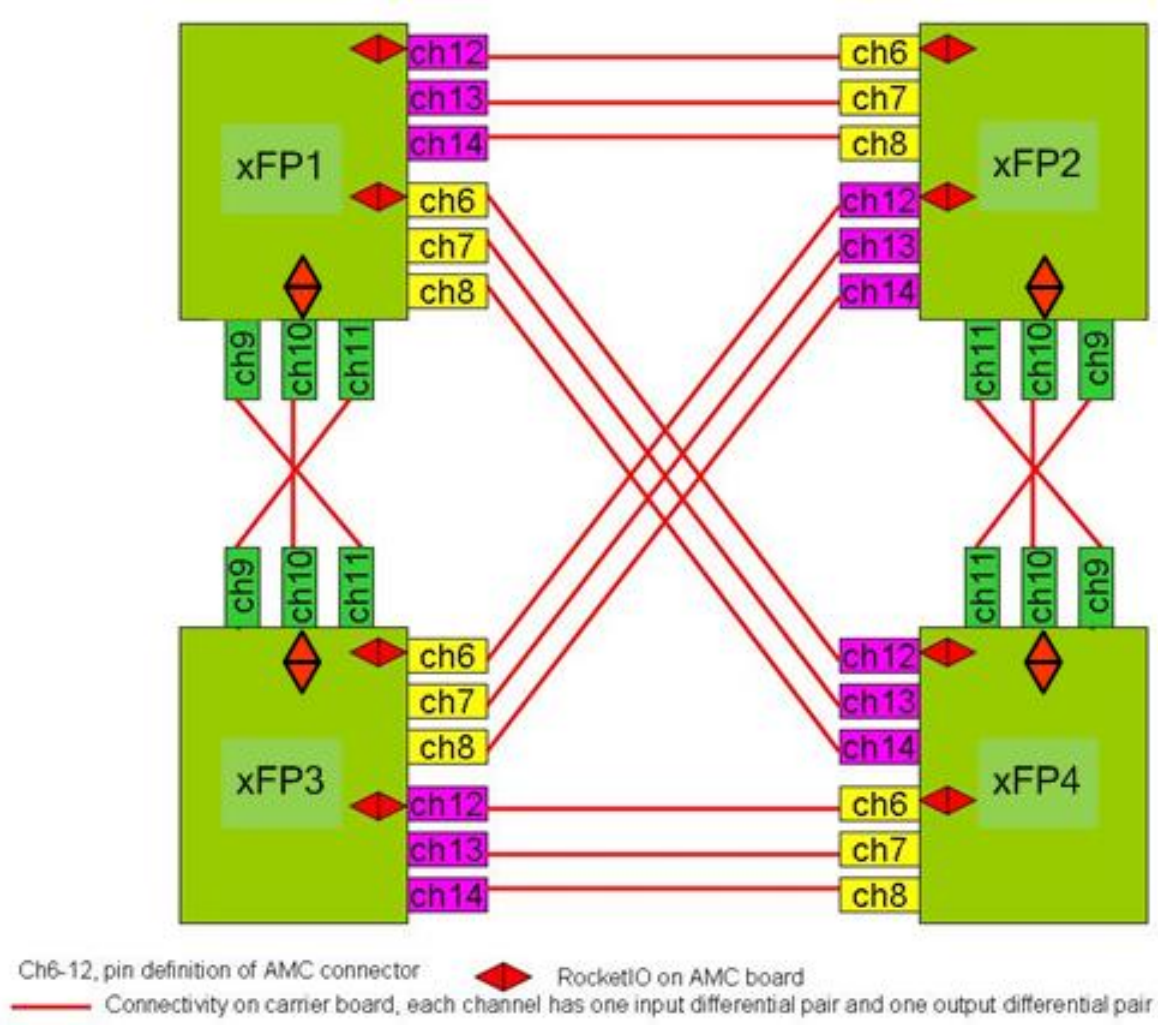
CNCB(CN Carrier Board) V3.3

- Founction
  - Virtex-4 FX60 with PowerPC405,
  - Embeded linux system for slow control,
  - 16 RocketIO channel connect to backplane,
  - 2GB DDR2,
  - 2 Ethernet ports,
  - 64MB Flash,
  - JTAG,UART Hub,
  - IPMC



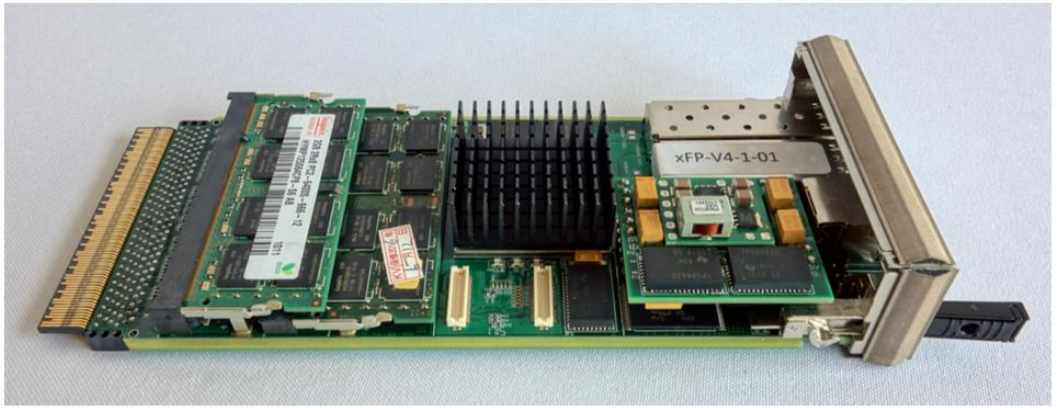
CN Carrier Full mesh for AMC

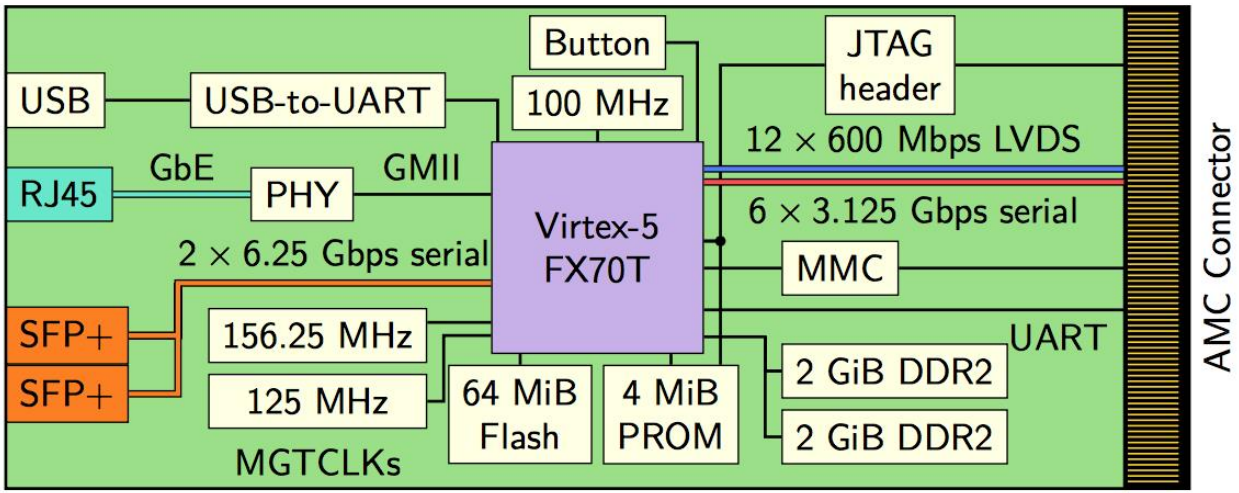
xFP-xTCA based FPGA Processor (AMC card)



xFP(xTCA-based FPGA Processor)

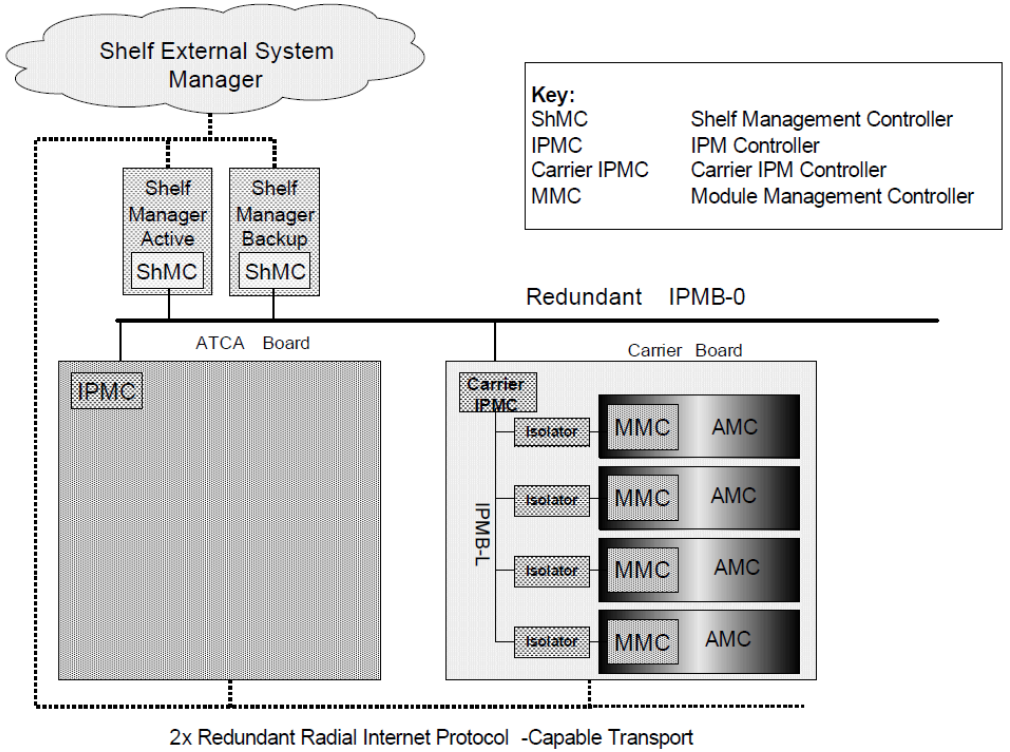
- Founction
  - Virtex-5 FX70T with PowerPC440,
  - Embeded linux system for data management,
  - 2 SFP+ port, 6.25Gbps/ch
  - 4GB DDR2,
  - 1 Ethernet ports,
  - 64MB Flash,
  - PROM for FPGA Program
  - UART port,
  - MMC





Intelligent Platform Management system

- IPM system
  - ShMC,
  - Carrier IPMC,
  - MMC,
  - Power control
  - and Fan control.
- In Belle II DAQ:
  - CN hotswap,
  - Monitoring current, voltage,
  - Power dissipation management,
  - Temperature control.
- Collaborate developed with Bjoern.

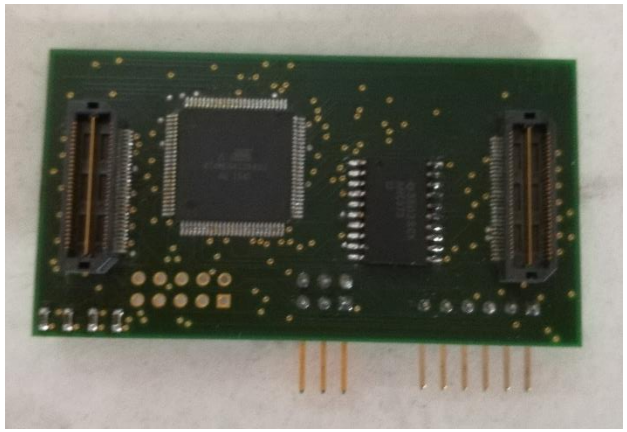


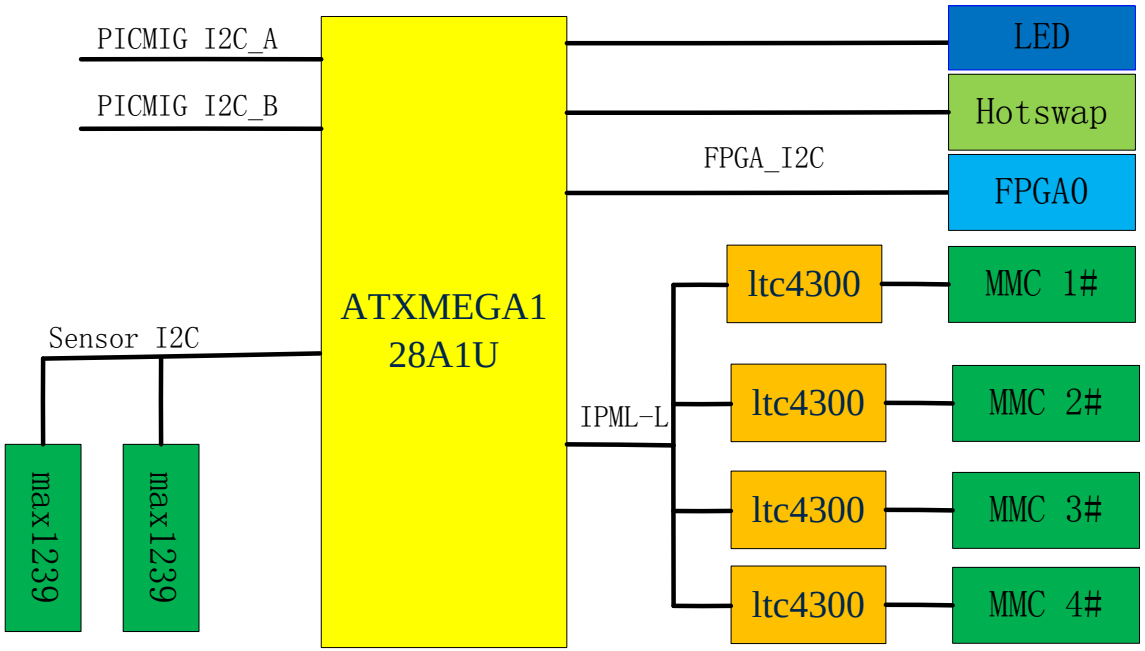
IPMC-Intelligent Platform Management Controller

MMC-Module Management Controller

Intelligent Platform Management system

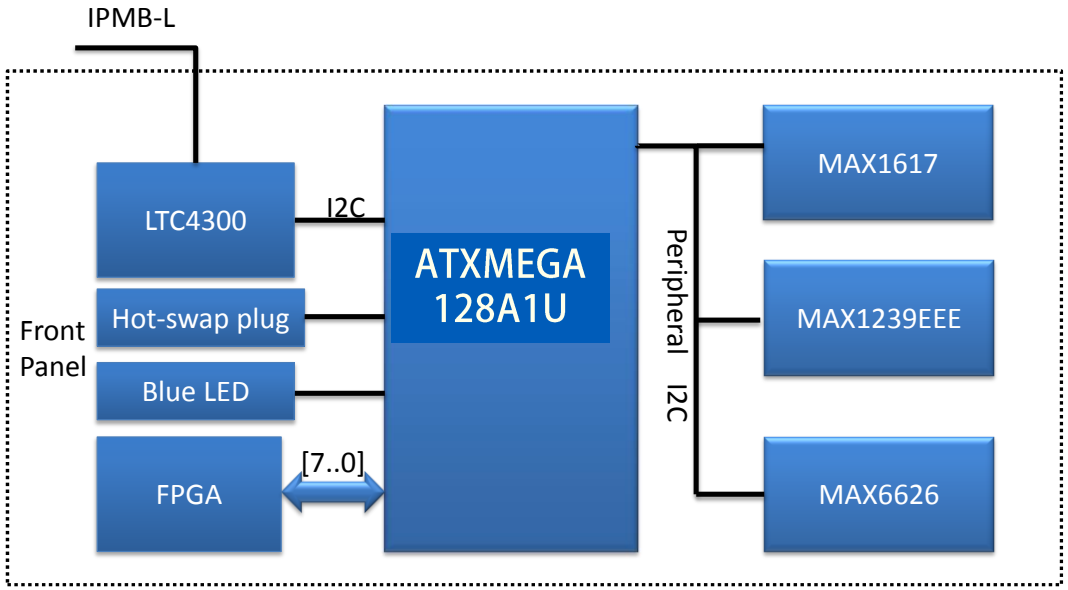
- IPMC
  - Microcontroller: ATXMEGA128A1U,
  - I2C bus for IPMI Local bus and sensor bus,
  - UART for data print out and import,
  - Memory for data recording.

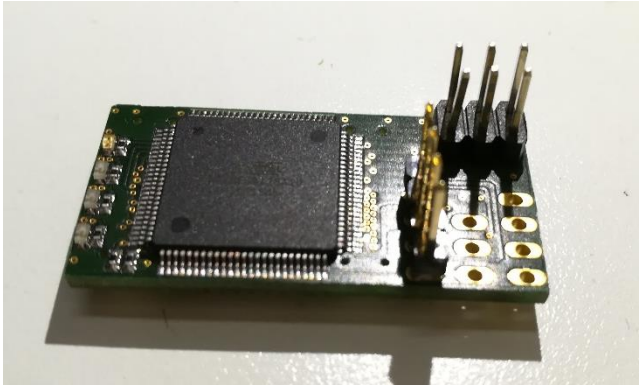




Module Management Controller

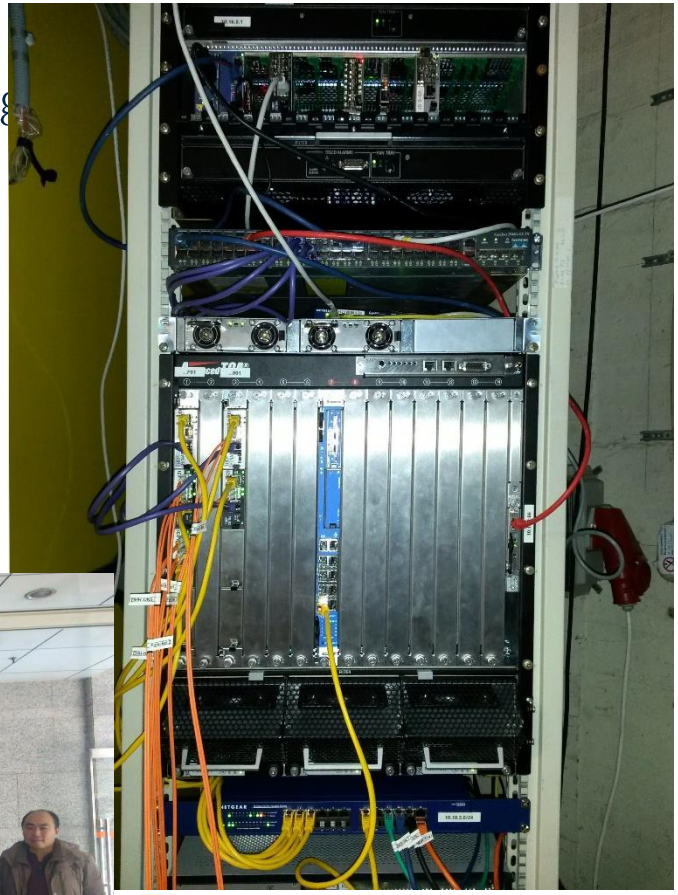
- MMC
  - Microcontroller: ATXMEGA128A1U, same as used on IPMC for uniform firmware development.
  - I2C bus for IPMI Local bus and sensor bus,
  - UART for data print out and import,





Status of Belle II xTCA PXD-DAQ

- Frist Beam test in DESY in 2014
- Second BT in 2016
  - The whole DAQ chain was tested with up to 2kHz, Long time stability tested for 8h.
  - Everything stably watched by run and slow control
- Complished in 2016
  - Mass Production 2015
  - System integration Nov.2016
  - Now whole system is being prepared to delivered to KEK for system install.



summary

- PXD detector is a new detector in the upgrade of Belle II and has huge data output.
- xTCA Based Compute Node has successfully designed, tested and mass produced for Belle II PXD.
- Now whole system is being prepared to delivered to KEK for system install.

Thanks for your attention.