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The LHCb Vertex Locator Upgrade

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The Large Hadron Collider Beauty detector is a flavour physics detector, designed to detect decays of b- and c-hadrons for the study of CP violation and rare decays. At the end of Run-II, many of the LHCb measurements will remain statistically dominated. In order to increase the trigger yield for purely hadronic channels, the hardware trigger will be removed and the detector will operate at 40 MHz. This, in combination with the five-fold increase in luminosity necessitates radical changes to LHCb ' s electronics with entire subdetector replacements required in some cases. The Vertex Locator (VELO) surrounding the interaction region is used to reconstruct the collision points (primary vertices) and decay vertices of long-lived particles (secondary vertices). The upgraded VELO modules will each be equipped with 4 silicon hybrid pixel tiles, each read out with by 3 VeloPix ASICs. The highest occupancy ASICs will have pixel hit rates of 900 Mhit/s and produce an output data rate of over 15 Gbit/s, with a total rate of 1.6 Tbit/s anticipated for the whole detector.

The VELO upgrade modules are composed of the detector assemblies and electronics hybrid circuits mounted onto a cooling substrate. The modules are located in vacuum, separated from the beam vacuum by a thin custom made foil. The foil will be manufactured through a novel milling process and possibly thinned further by chemical etching. The front-end hybrid hosts the VeloPix ASICs and a GBTx ASIC for control and communication. They hybrid is linked to the the the opto-and-power board (OPB) by 60 cm electrical data tapes running at 5 Gb/s. The tapes must be vacuum compatible and radiation hard and are required to have enough flexibility to allow the VELO to retract during LHC beam injection. The OPB is situated immediately outside the VELO vacuum tank and performs the opto-electrical conversion of control signals going to the front-end and of serial data going off-detector. The board is designed around the Versatile Link components developed for high-luminosity LHC applications. From the OPB the detector data are sent through 300 m of optical fibre to LHCb's common readout board (PCIe40). The PCIe40 is an Altera Arria10-based PCI-express control and readout card capable of 100 Gb/s data throughput. The PCIe40 firmware is designed as a series of common components with the option for user-specific data processing. The common components deal with accepting the input data from the detector over the GBT protocol, error-checking, dealing with reset signals, and preparing the data for the computing farm. The VELO-specific code would, for example, perform clustering of hits and time reordering of the events scrambled during the readout.

An additional challenge is the non uniform nature of the radiation damage, which results in requiring a guard ring design with excellent high voltage control. In addition, the n-in-p design requires the guard ring to be on the chip side making the high voltage reach the vicinity of the ground plane (about 30 μm apart). This requires a high voltage tolerant setup for irradiated assemblies which can be achieved using a vacuum chamber. The performance of the prototype sensors has been investigated in a test beam in which a dedicated telescope system was created read out by Timepix3 ASICs. Several different tests of the of the sensor prototypes were performed before and after irradiation. A collection of preliminary results will be presented, as well as a comparison of the performance of the different sensor prototypes.

The design of the complete VELO upgrade system will be presented with the latest results from the R\&D. The LHCb upgrade detector will be the first detector to read out at full LHC rate of 40 MHz. The VELO upgrade will utilise the latest detector technologies to read out at this rate using while maintaining the necessary radiation hard profile and minimising the detector material.

Summary

The Vertex Locator (VELO) surrounding the interaction region is used to reconstruct the collision points (primary vertices) and decay vertices of long-lived particles (secondary vertices). The upgraded VELO modules will each be equipped with 4 silicon hybrid pixel tiles, each read out with by 3 VeloPix ASICs. The highest occupancy ASICs will have pixel hit rates of 900 Mhit/s and produce an output data rate of over 15 Gbit/s, with a total rate of 1.6 Tbit/s anticipated for the whole detector.
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