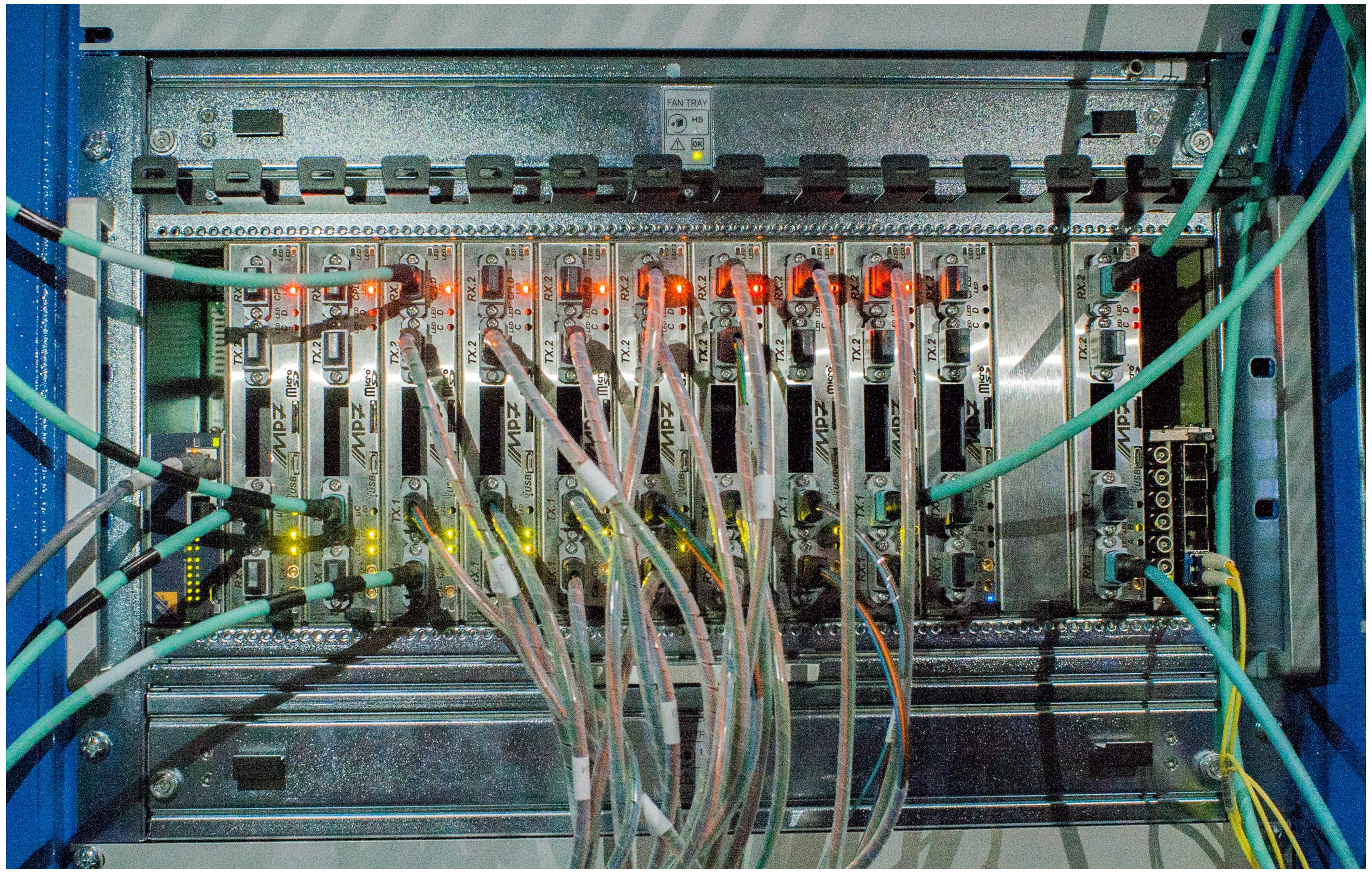
INTERNATIONAL CONFERENCE ON TECHNOLOGY AND INSTRUMENTATION IN PARTICLE PHYSICS

BEIJING, 22-26 MAY 2017



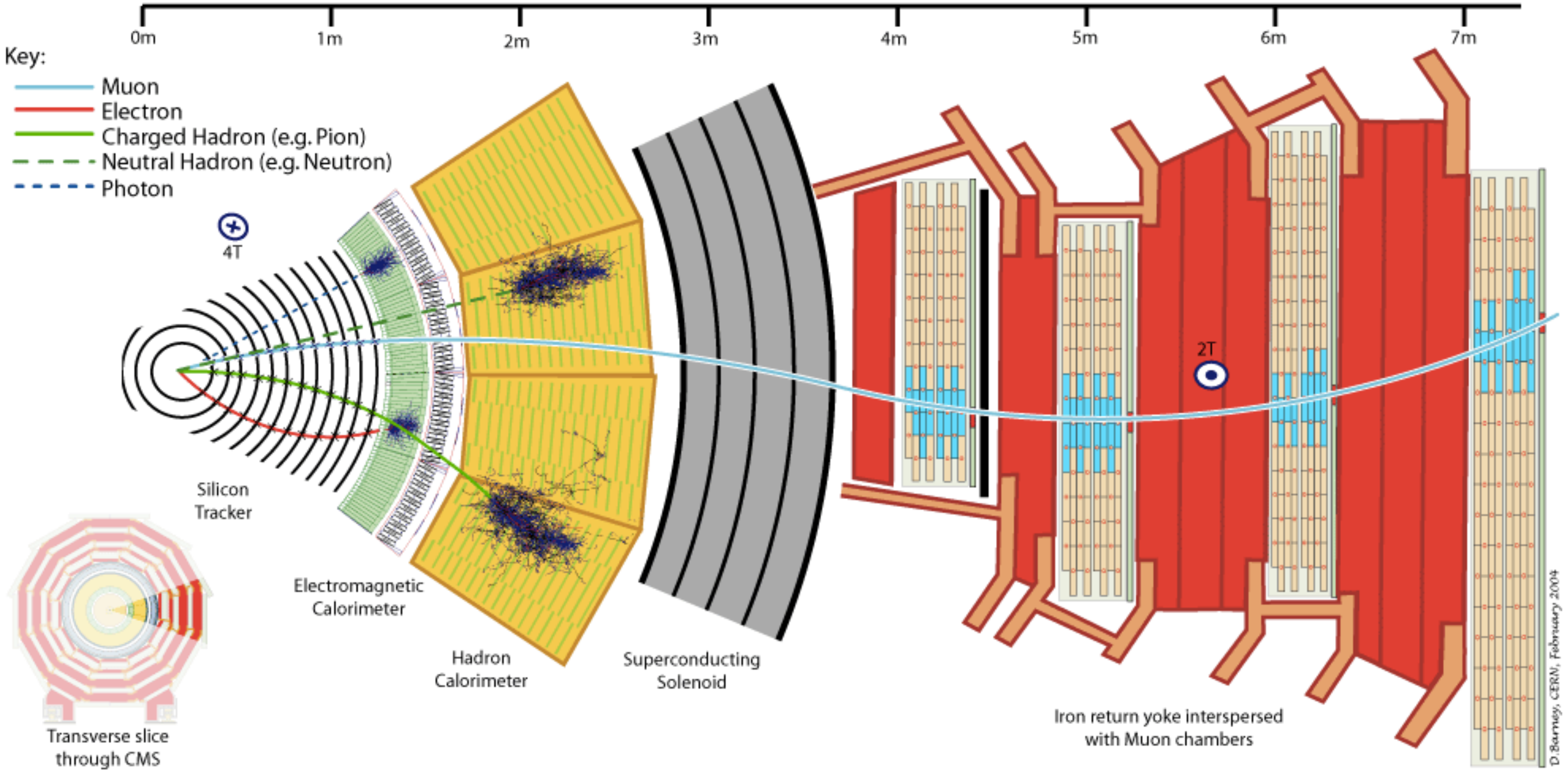
TOM JAMES, IMPERIAL COLLEGE LONDON

TRACK FINDING FOR THE LEVEL-1 TRIGGER OF THE CMS EXPERIMENT

INTRODUCTION TO COMPACT MUON SOLENOID (CMS)

- **Large, all-purpose detector**, designed to investigate a **wide range of physics** (Higgs, Supersymmetry, Dark Matter). 20-40 **simultaneous collisions (pileup)** at 40 MHz

1. **Silicon strip tracker** (~1.2m radius, 200 m^2 area), largest silicon tracker in operation
2. Within **3.8 T** superconducting solenoid. **Transverse momentum (p_T)** measured with curvature in B-field
3. **Level-1 (L1) trigger**, latency O(3-4 μs), rejects uninteresting events, rate reduction O(x400)
4. Data size/rate from tracker **too large** to use in L1-trig



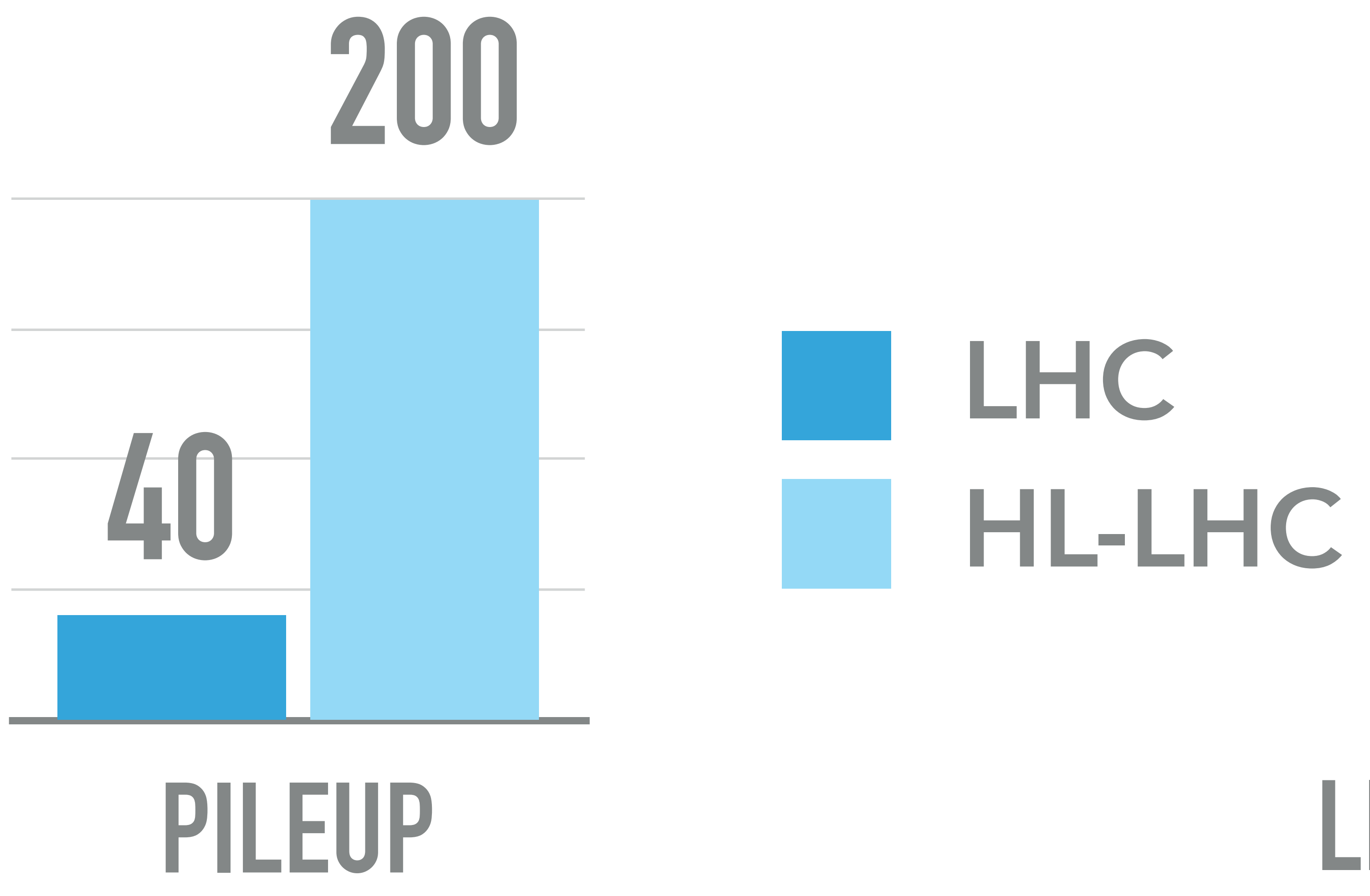
p_T = curvature in transverse direction to beam

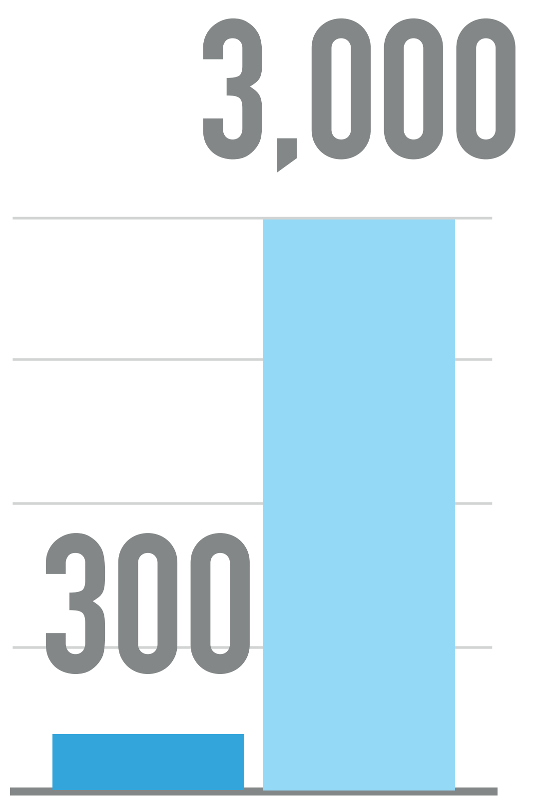
η = angle in longitudinal direction to beam

HIGH LUMINOSITY LHC

precision measurements, **push** search limits, **rare** processes

- By 2026 - **LHC** will be **upgraded** in **luminosity** -> 2-3x improved **statistics by 2035 vs no upgrade**
- **Silicon strip tracker will be replaced** (radiation damage) - Phase II CMS
  - **Challenging high occupancy conditions, ~15,000 tracks per bx,** must **perform ≥ at present**
  - Need completely **new handle** at L1 trigger, to keep rate < 750 kHz, while maintaining sensitivity to interesting physics
  - **New tracker design** will allow **read out of some data at 40 MHz**



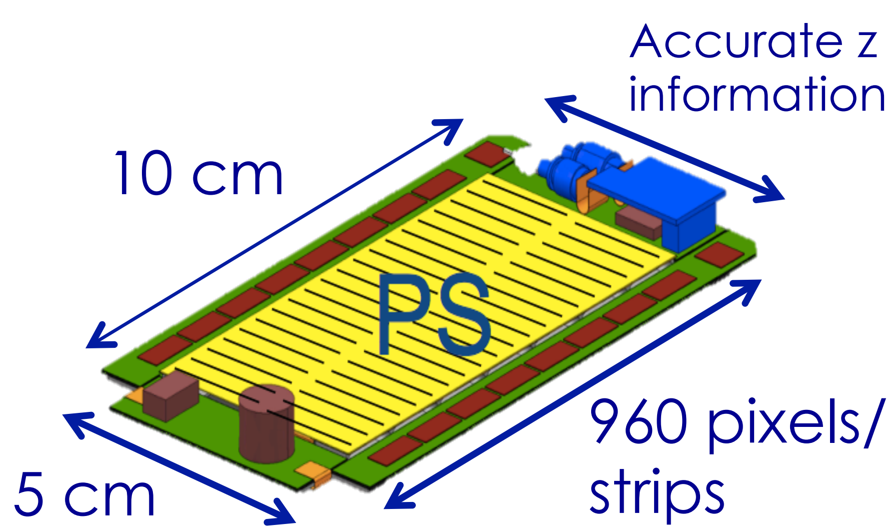


INTRODUCTION

CMS TRACKER UPGRADE

See A. Konig, *The CMS Tracker Phase II Upgrade for the HL-LHC era*

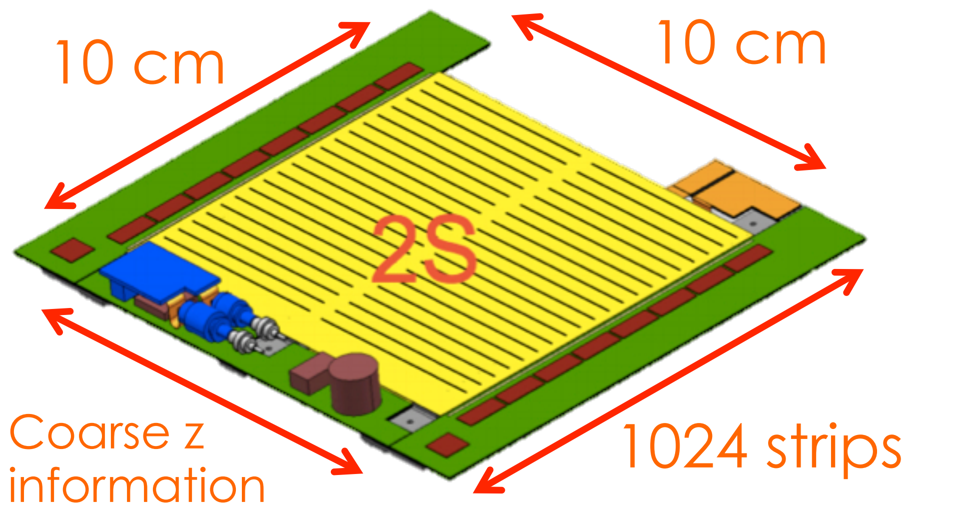
"PS" Pixel + Strip Modules 20 < r < 60 cm



Strip Sensor × 2: 2. 5 cm × 100 μm
+
Pixel Sensor × 32: 1.5 mm × 100 μm

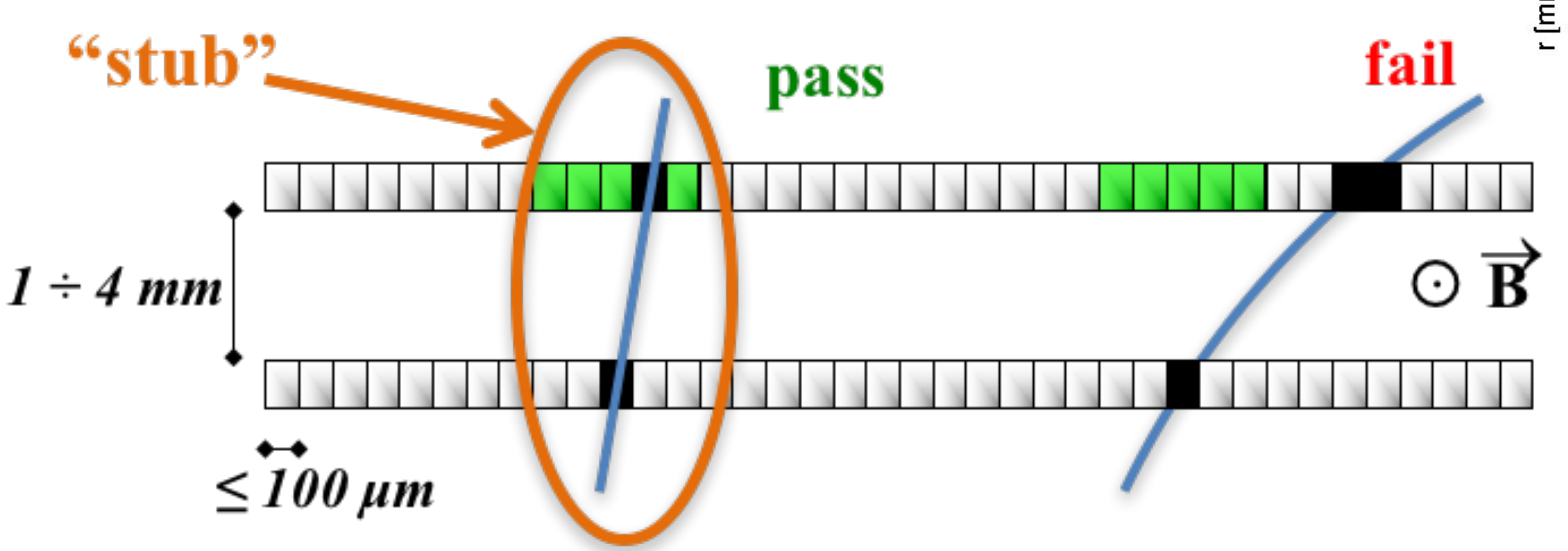
"2S" 2 Strip Modules r > 60 cm

Strip Sensor × 2: 5 cm × 90 μm
+
Strip Sensor × 2: 5 cm × 90 μm

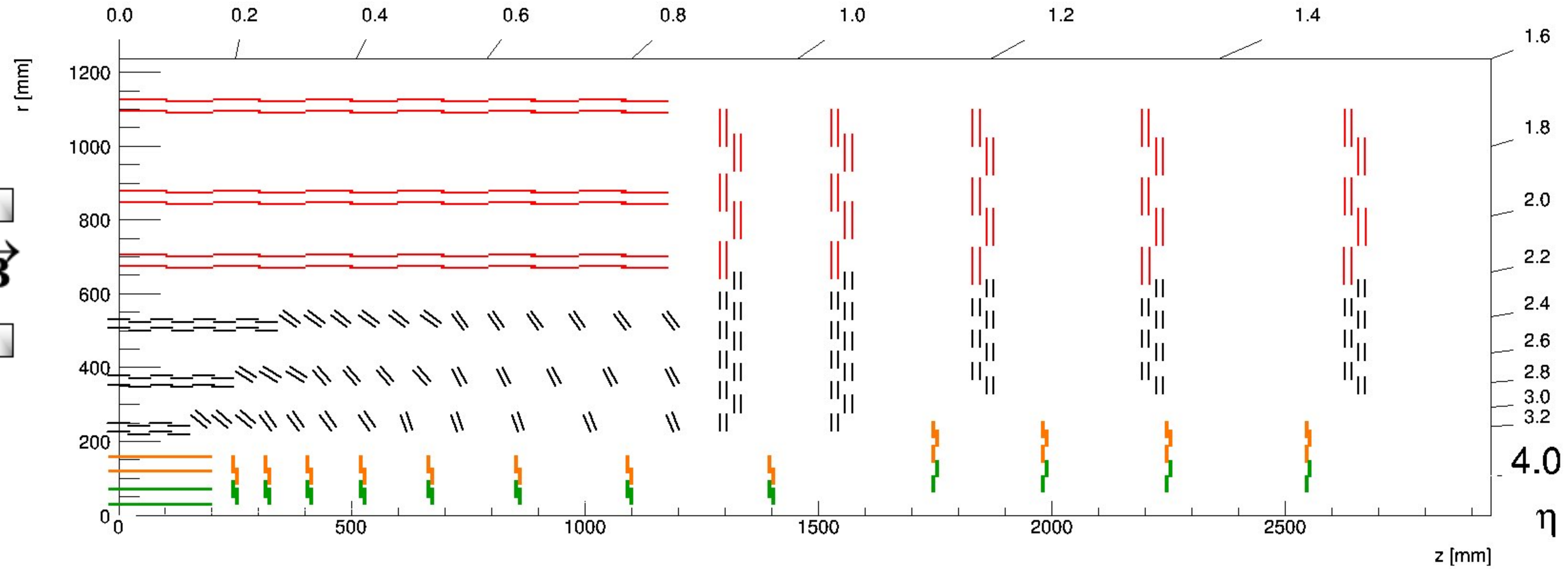


- High p_T tracks signs of interesting physics (decays of high mass particles)
- **Novel tracking modules** utilise two **1.6-4.0 mm spaced silicon sensors**, to **discriminate p_T > 2-3 GeV**
  - Forward these ***stubs*** to **off-detector trigger electronics -** rate reduction O(10)

2S PS



Innovative stacked module ideas originated at Imperial College. Prototype modules under beam-testing

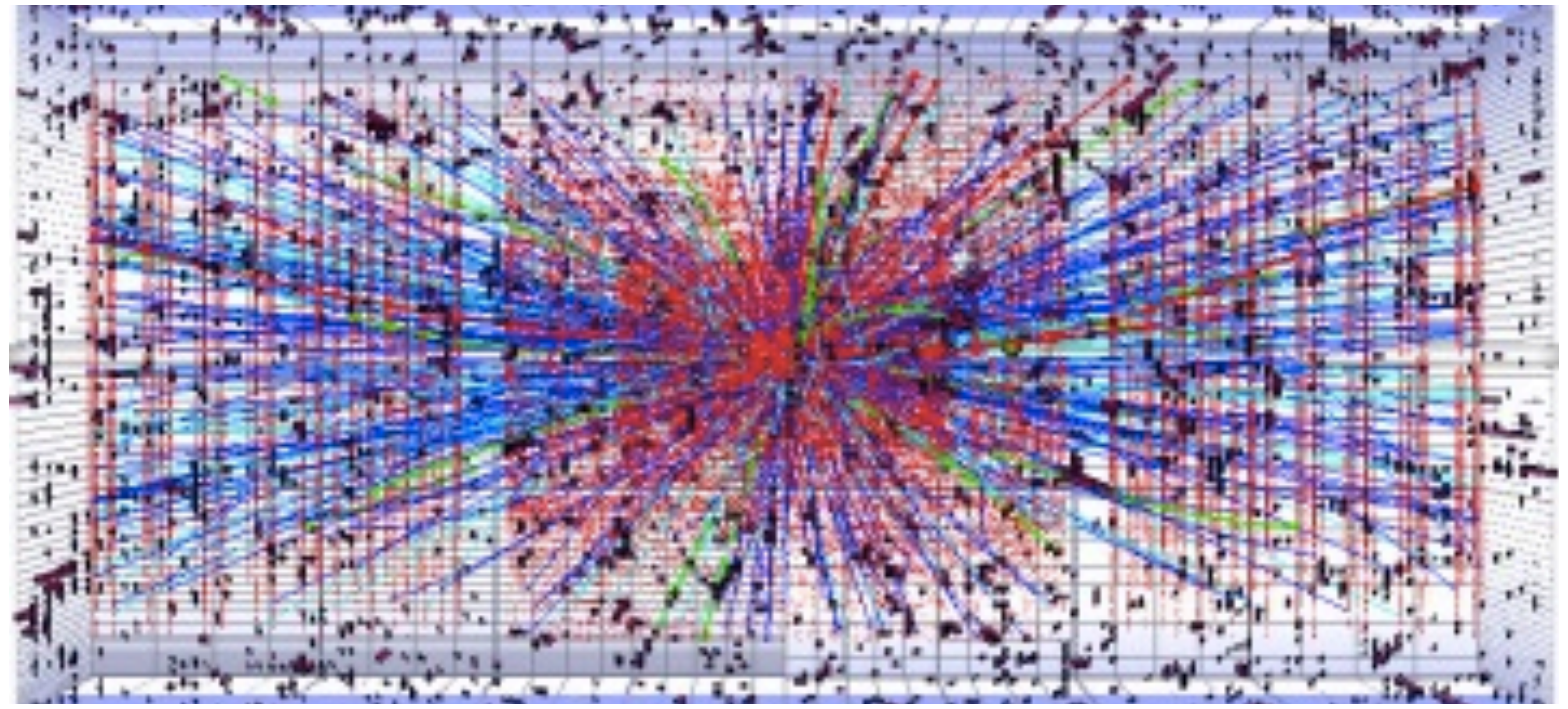


Proposed upgraded tracker geometry

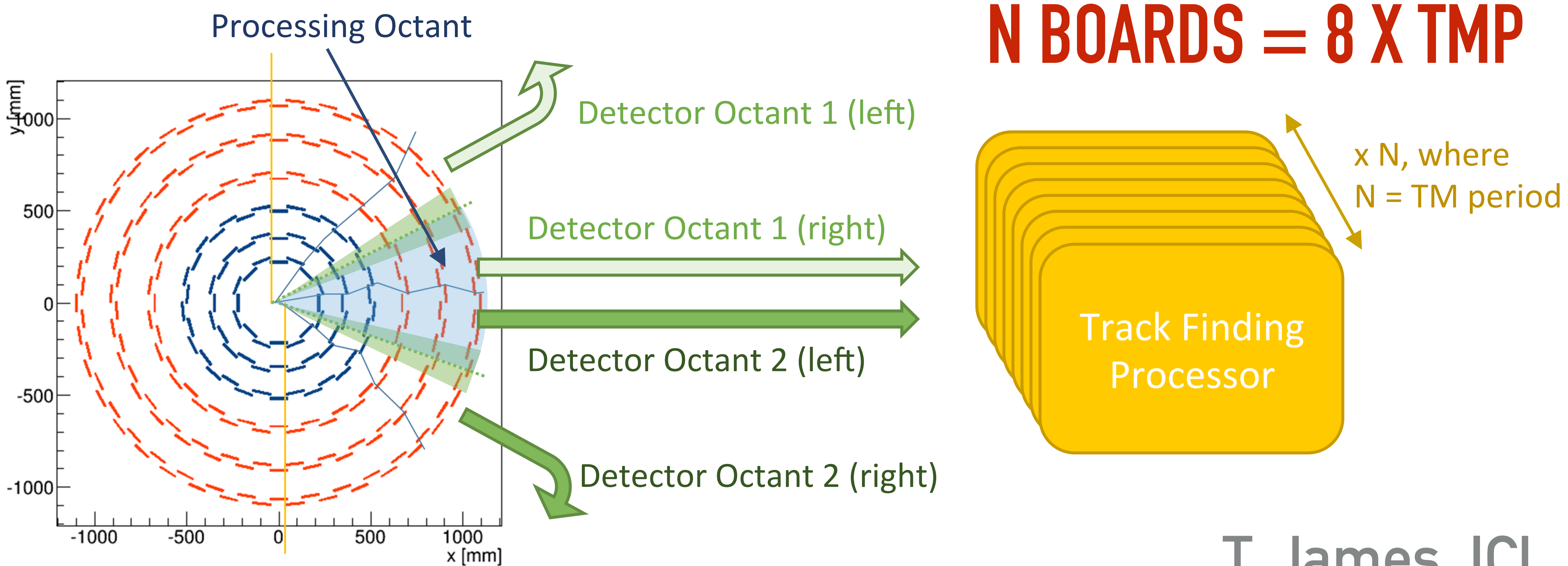
TRACK TRIGGER PROPOSAL

Field-Programmable Gate Array (FPGA) - programmable digital integrated circuit

pileup 140 simulation



- **~4 μs available for track finding (~12.8 μs total L1)**
- **Very high data rates (~20,000 stubs per bx)**
- **Proposal**: A Track Finding Processor (TFP)
    - Data-stream FPGA-based processing board
    - Processes 1/8 of tracker in **φ and 1/(time multiplex period)**
    - **Choice** of physical/time segmentation dictated by data rates out of the detector and into FPGA board
- **Objective**: Build **hardware demonstrator** to prove **feasibility** and **capability** of such an object
    - Each TFP operates **independently**
    - One TFP becomes the ***demonstrator slice***



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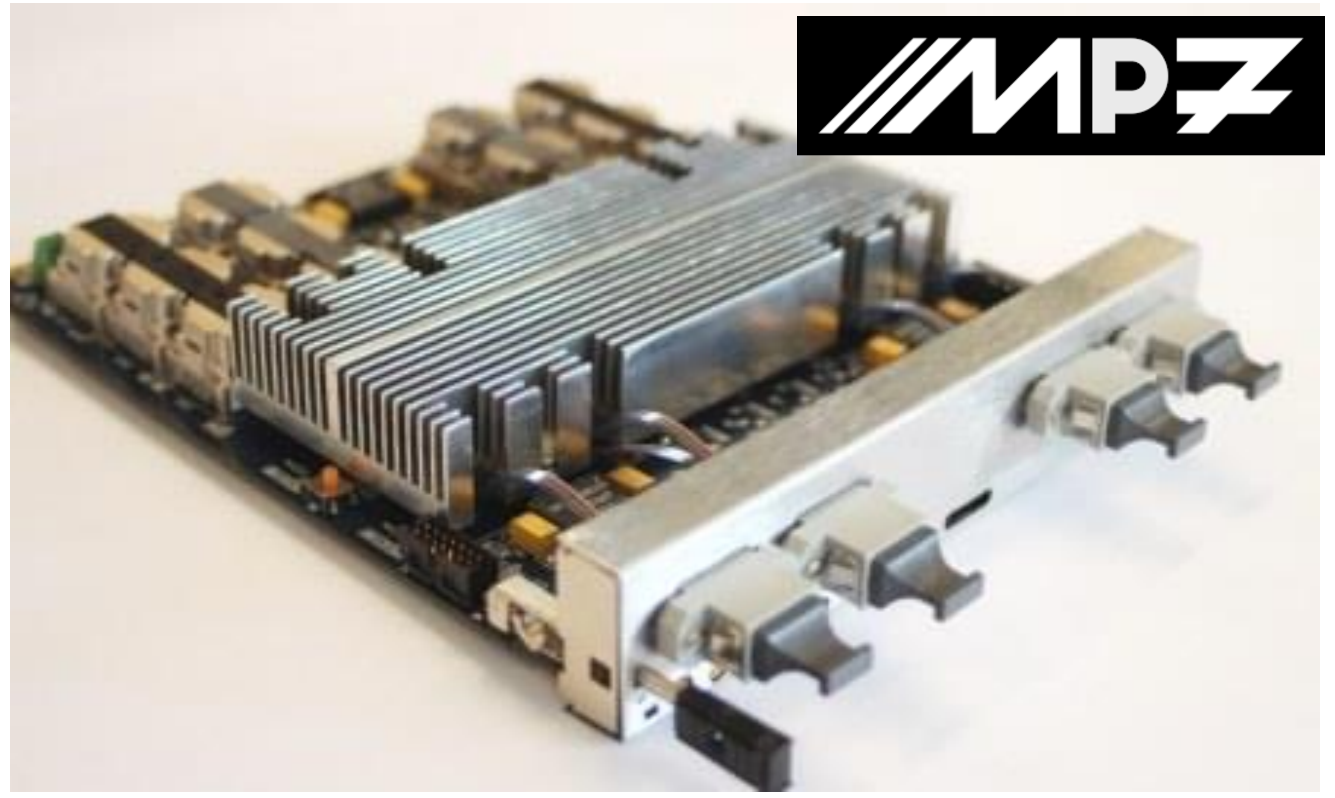
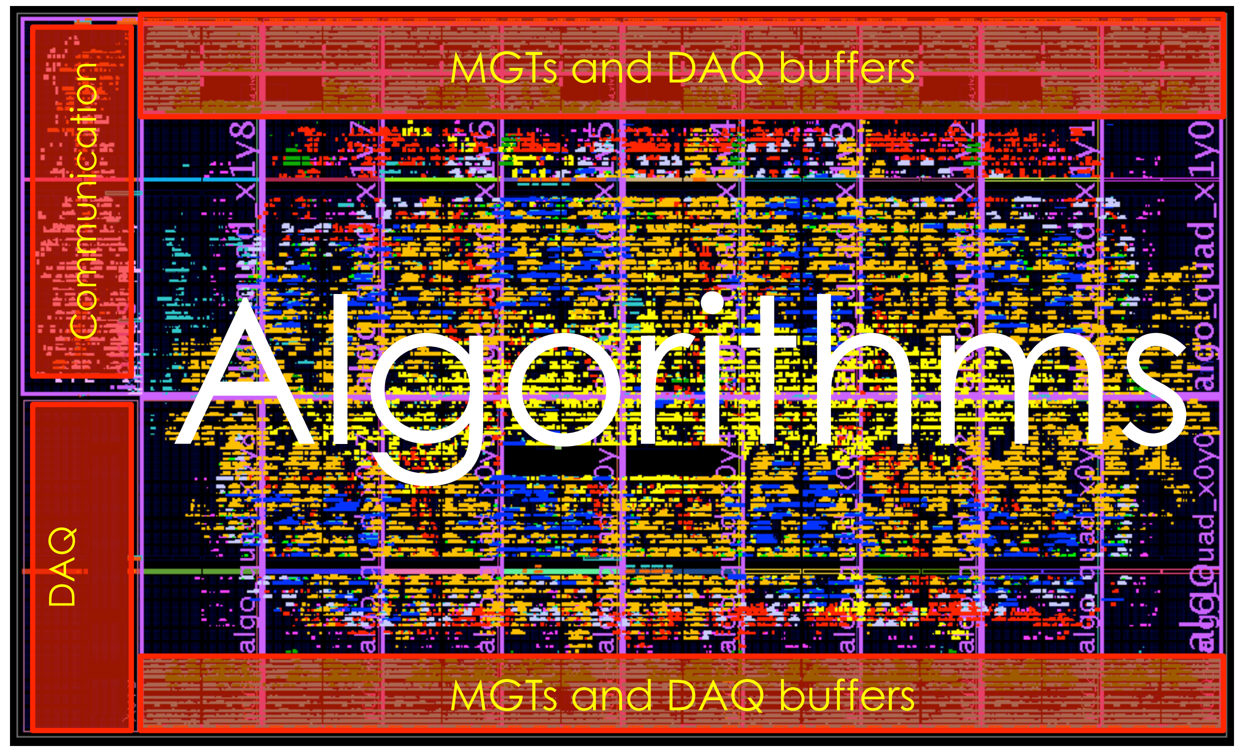
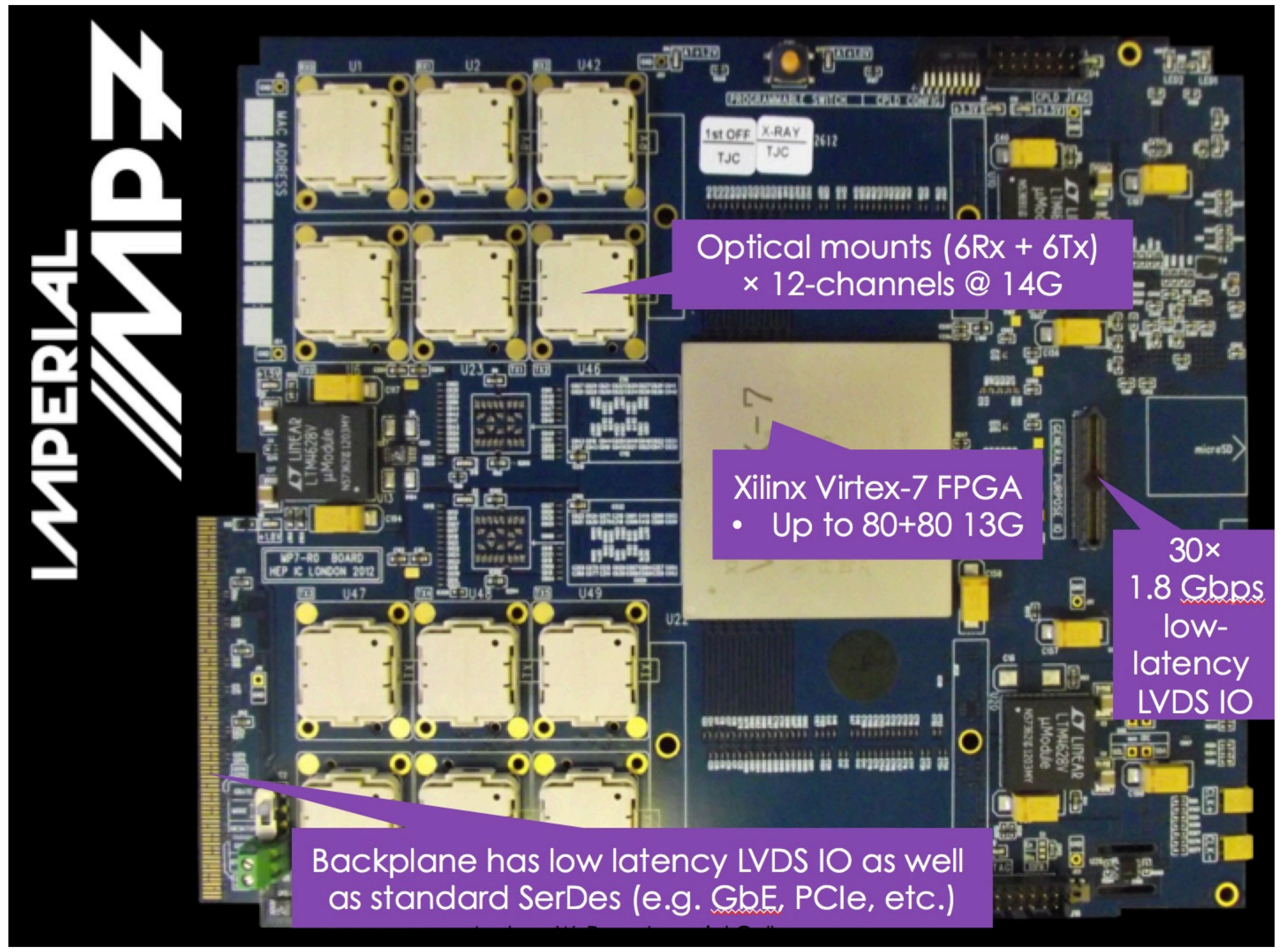
THE IMPERIAL MASTER PROCESSOR 7 (MP7)



- A generic, **high-performance FPGA, high-bandwidth, data-stream processing double-width AMC card**
- Currently used widely in CMS trigger
- **Xilinx Virtex-7 690 FPGA**
- **72 optical transmitters/receivers** running at **10.3 Gbps** 8b/10b
  - Usable optical bandwidth **0.55 Tbps** each way
- **Infrastructure firmware** that provides transceiver buffering, I/O formatting & external communication and configuration kept separate from algorithm space

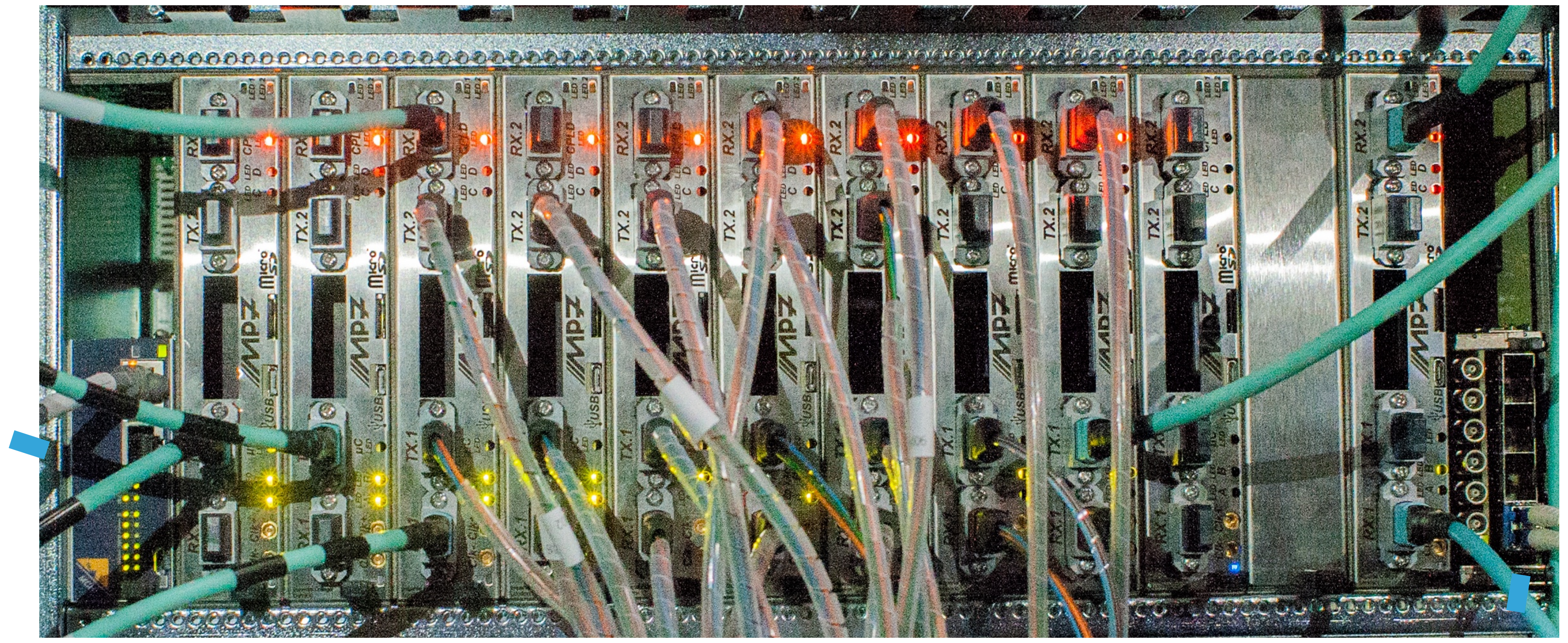
See A. Thea, The CMS Level-1 Calorimeter Trigger Upgrade for LHC Run II





DEMONSTRATOR SYSTEM

11 MP7s in MicroTCA crate



MCH

AMC13

- **CERN rack** provides **turbine, 3-phase power, air deflector, water cooling/heat exchangers**
- **MicroTCA carrier hub** (MCH) for GbE communication via backplane
- **AMC13** for synchronisation, timing & control

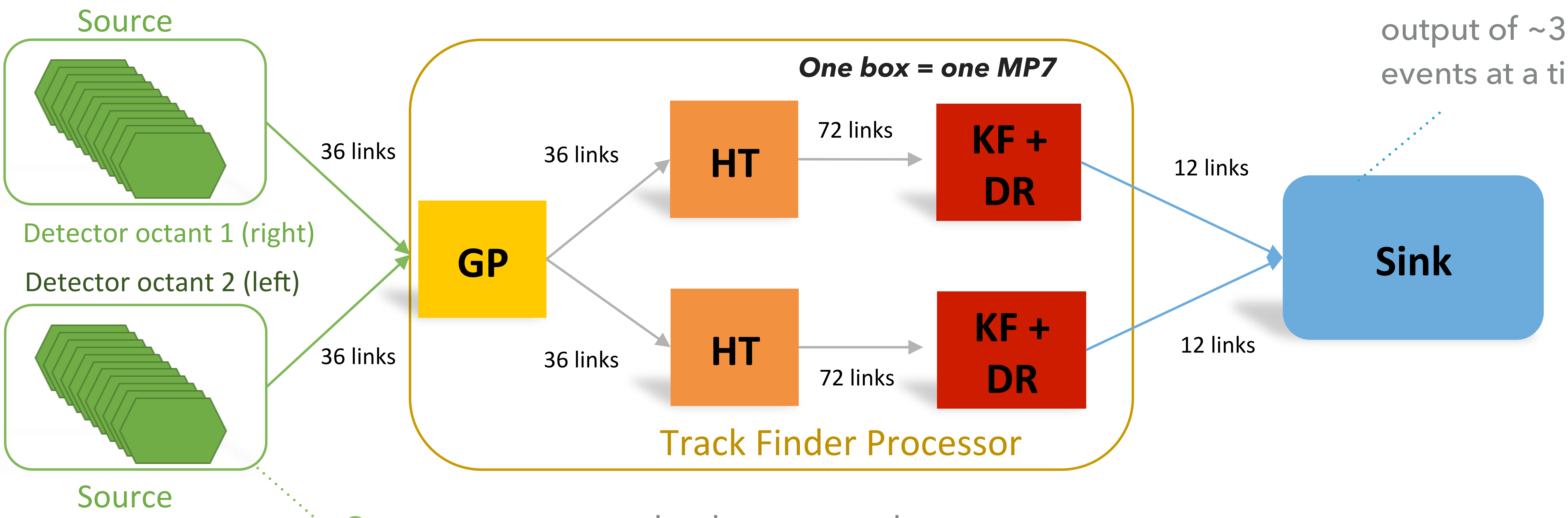
LOCATION: TRACKER INTEGRATION FACILITY, CERN

THE TRACK FINDING PROCESSOR (TFP)

FPGA firmware - generated by a specialised computer language used to describe structure and behaviour of electronic circuits

- TFP **firmware is divided into logical algorithm elements**, where (for demonstration), **each element implemented on a separate MP7 -** can extrapolate to future FPGA resources

Sink - stores the output of ~30 events at a time

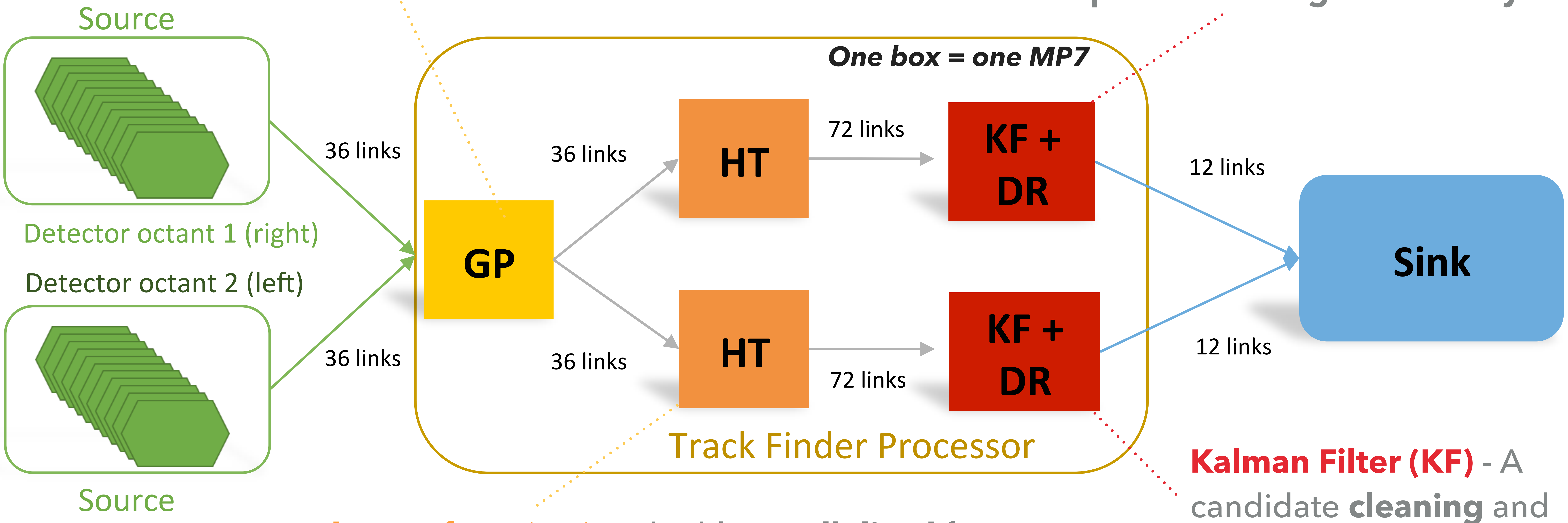


Source - represents the detector readout over one φ octant

THE TRACK FINDING PROCESSOR (TFP)

Geometric Processor (GP) - **pre-processes stub data**, and **divides the octant** into 36 **finer sub-sectors**

Duplicate Removal (DR) - Uses precise fit information to **remove duplicate tracks generated by the HT**



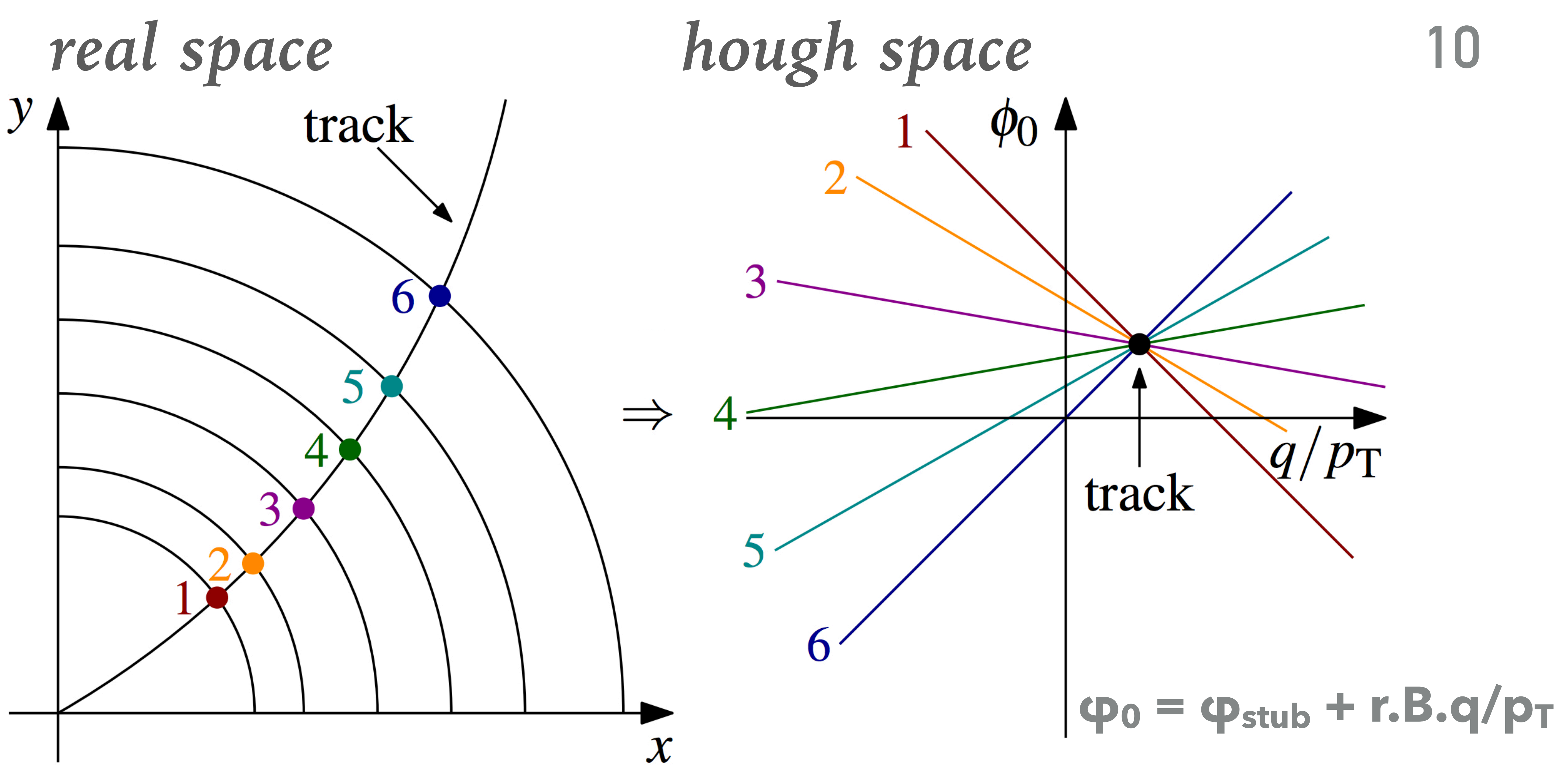
Kalman Filter (KF) - A candidate **cleaning** and **precision fitting** algorithm

Hough Transform (HT) - A highly **parallelised** first stage **track-finder** that identifies **groups of stubs consistent with a track in the r-φ plane**

2D HOUGH TRANSFORM (HT)

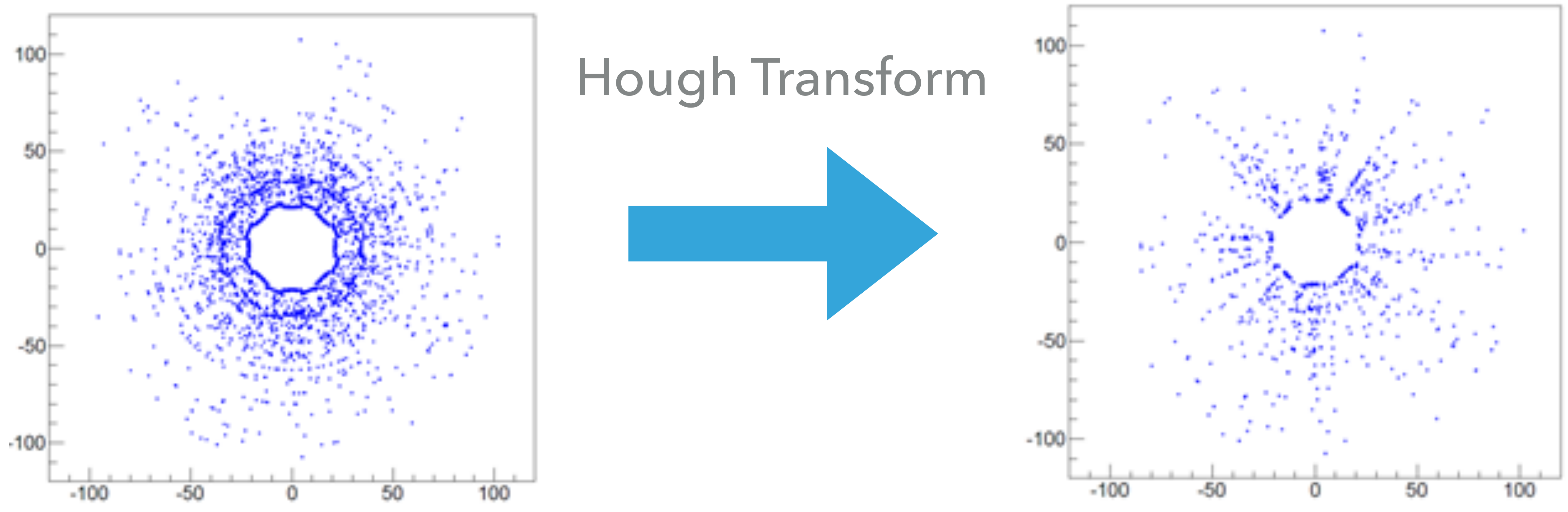
- Widely used **feature extraction technique** to **find imperfect instances of objects** within a space e.g tracks in our tracker hit map
- Search for **primary tracks in the r-φ plane**, using the **parameterisation (q/p_T, φ_0)**
  - **Stub positions correspond to straight lines in Hough Space**
  - **Where 4 or more lines intersect -> track candidate**

q/p_T is the free parameter, but p_T estimate from stacked modules used to constrain allowed q/p_T space



~20,000 stubs in tracker

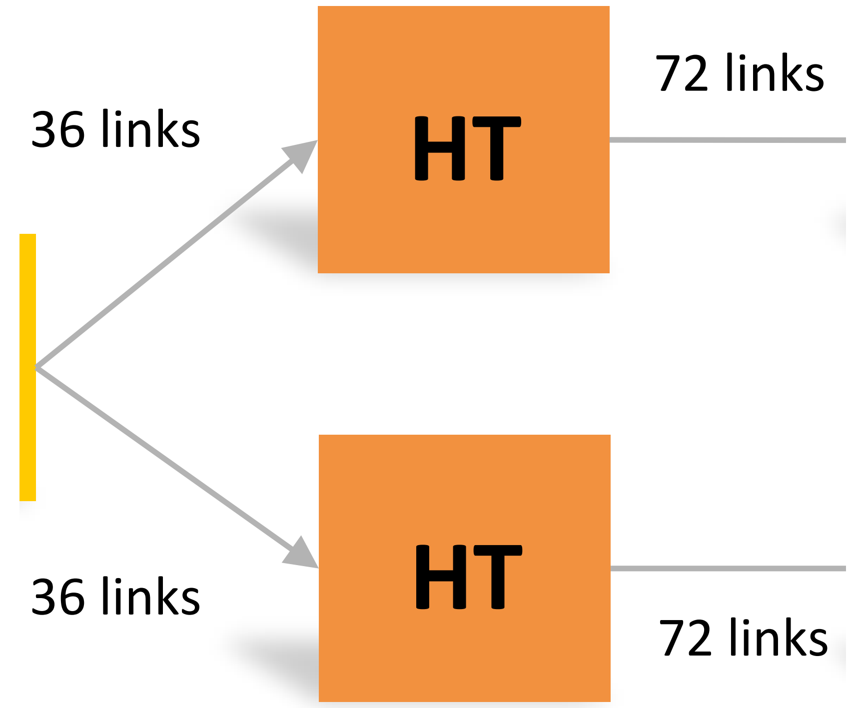
~270 track candidates

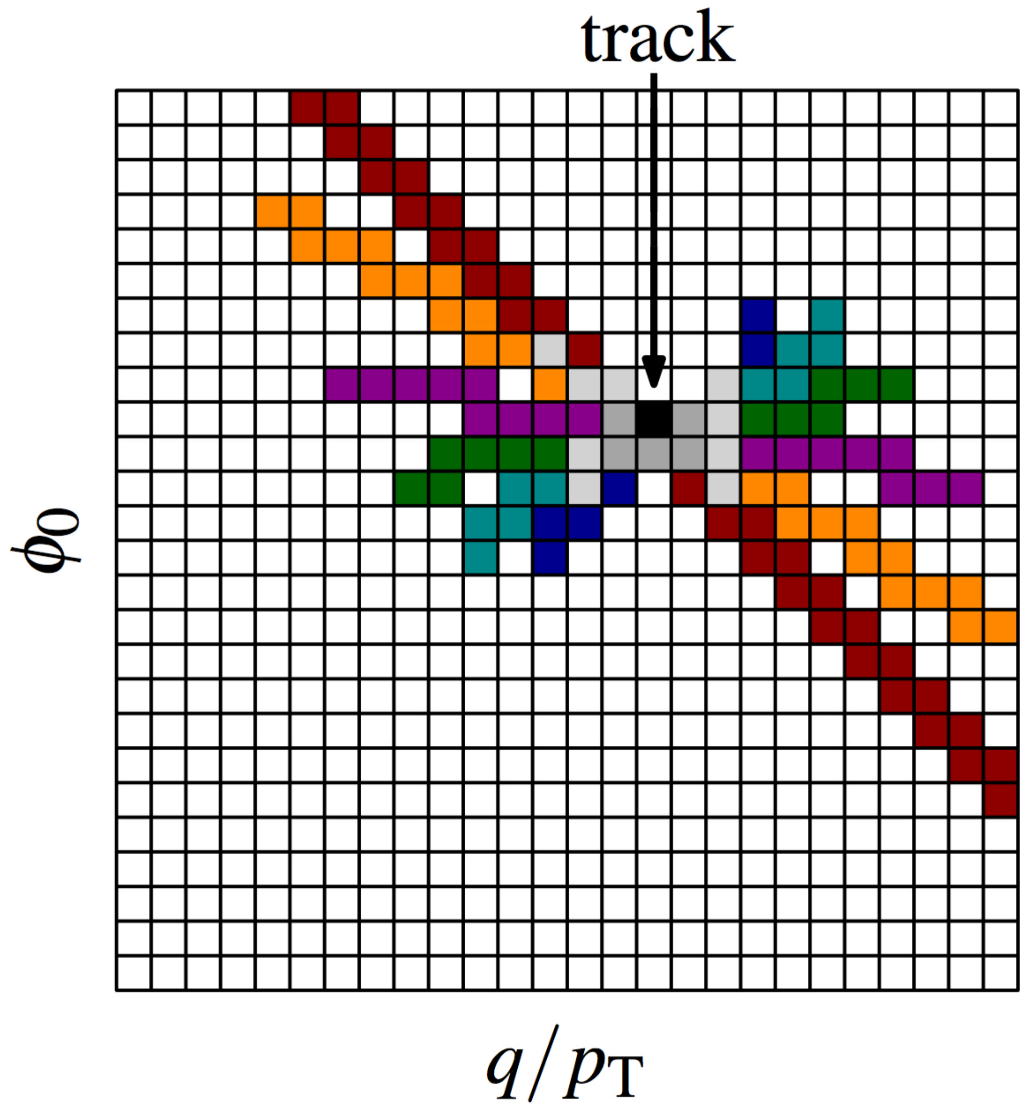


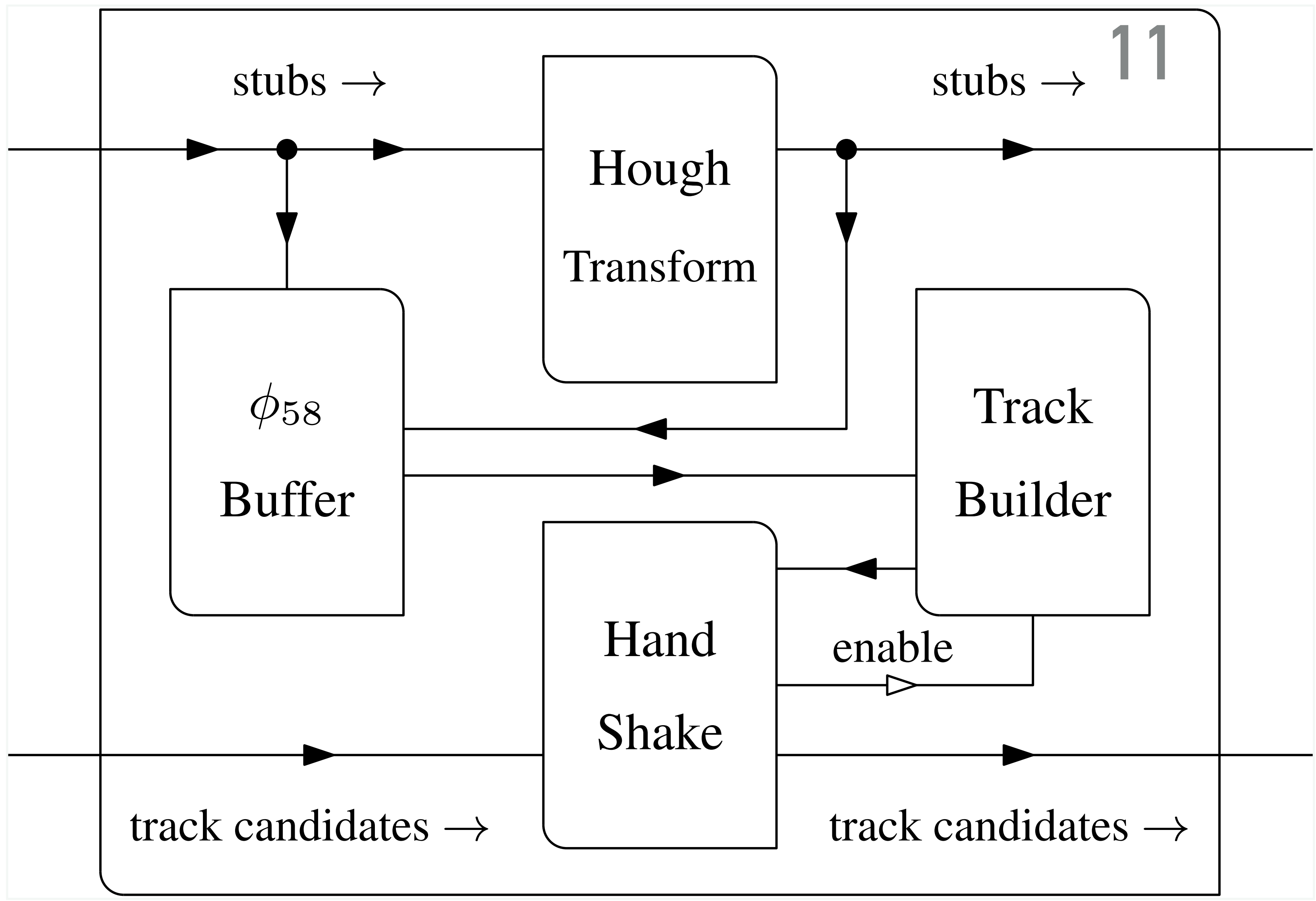
DEMONSTRATOR FIRMWARE

HOUGH TRANSFORM (HT)

- **Each sub-sector implemented as a fully independent, pipelined 32 x 64 array**





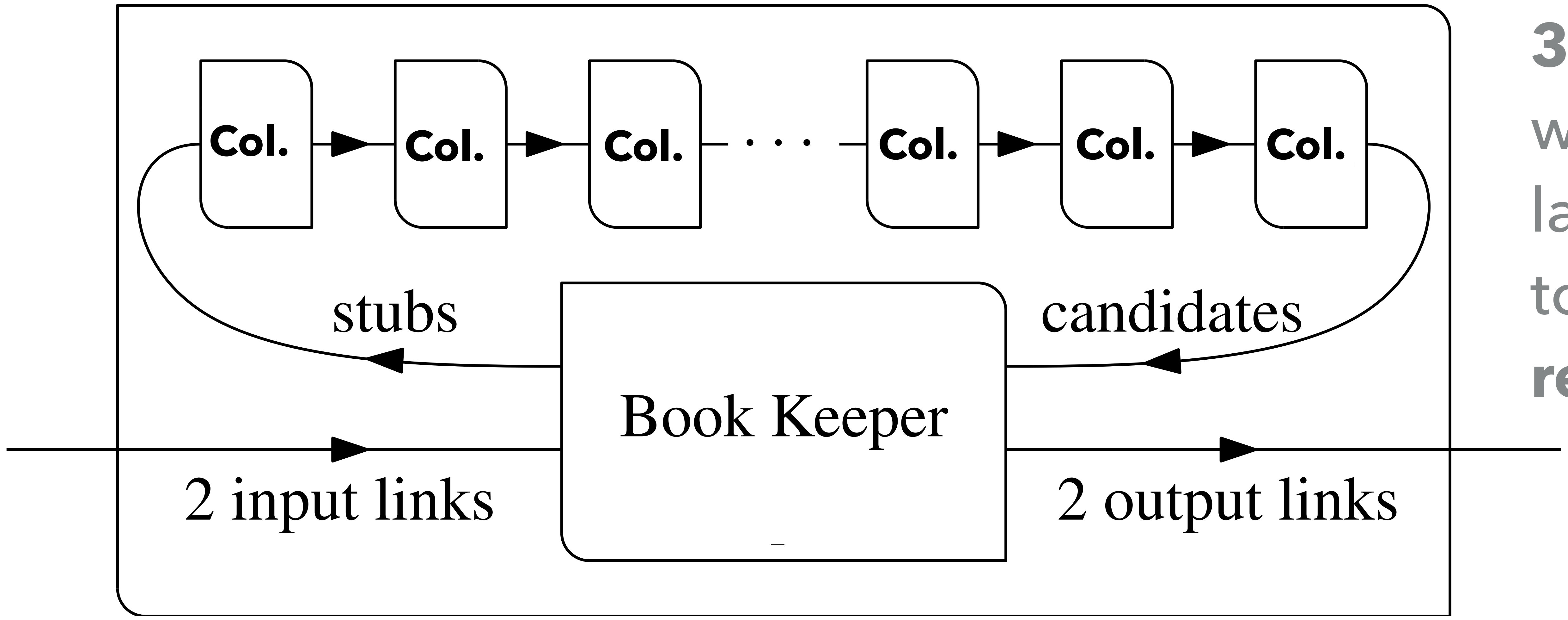


One HT Column, 32 per sub-sector

2) In each **Column (Col.)**, the corresponding φ_0 of the stub for the column is calculated and the appropriate cell(s) are marked

1) Book keeper receives stubs and propagates to each q/p_T column in turn.

p_T estimate from stacked modules used to constrain allowed q/p_T space



One HT sub-sector, 18 per MP7

3) Candidates marked with stubs from > 4 layers propagate back to the **Book Keeper for read-out**

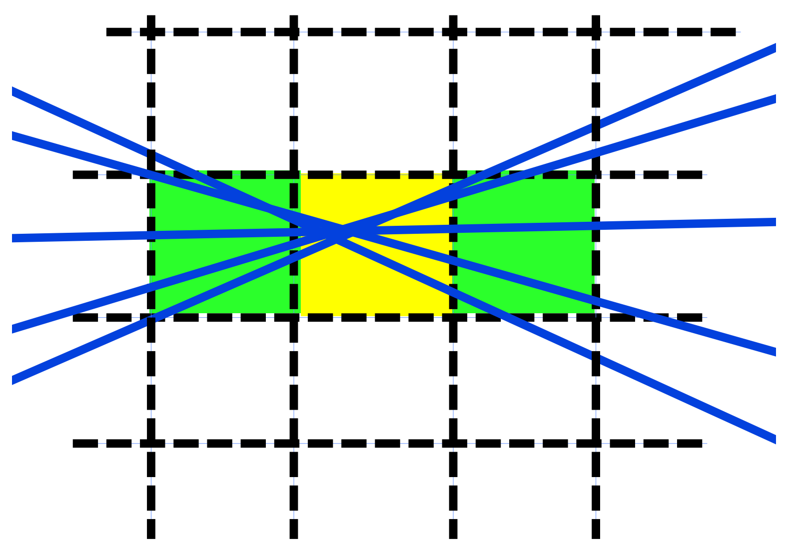
3D KALMAN FILTER (KF)

state = estimated track parameters

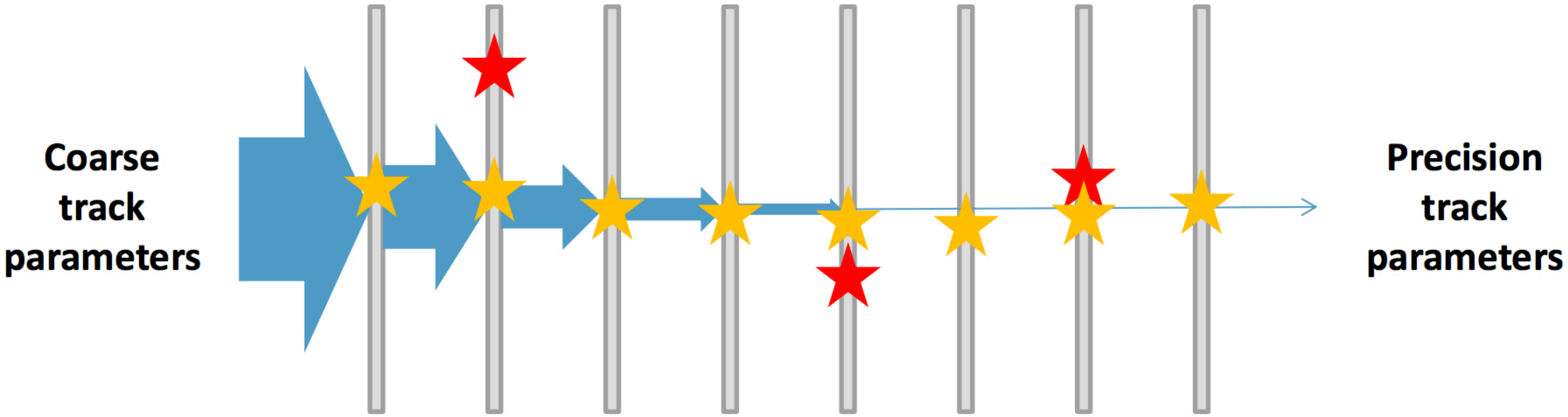
measurements = stubs on track candidate

- Commonly used **iterative algorithm; series of measurements** containing inaccuracies and noise -> estimates of **unknown variables**

1. Initial estimate of track parameters (HT seed) & their uncertainties
2. Stub used to update state (weighted average)
3. χ^2 calculated, used to reject false candidates, incorrect stubs on genuine candidates
4. Repeat until all stubs are added



Simple DR block removes HT candidates with same helix parameters



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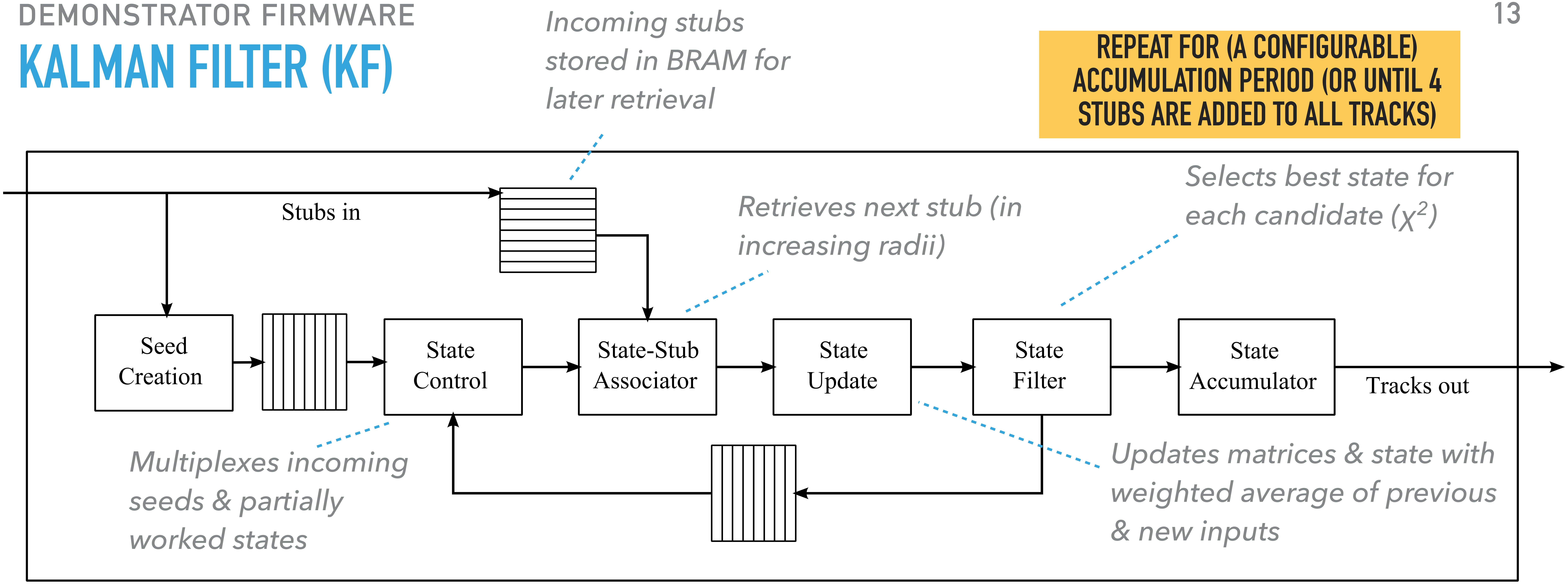
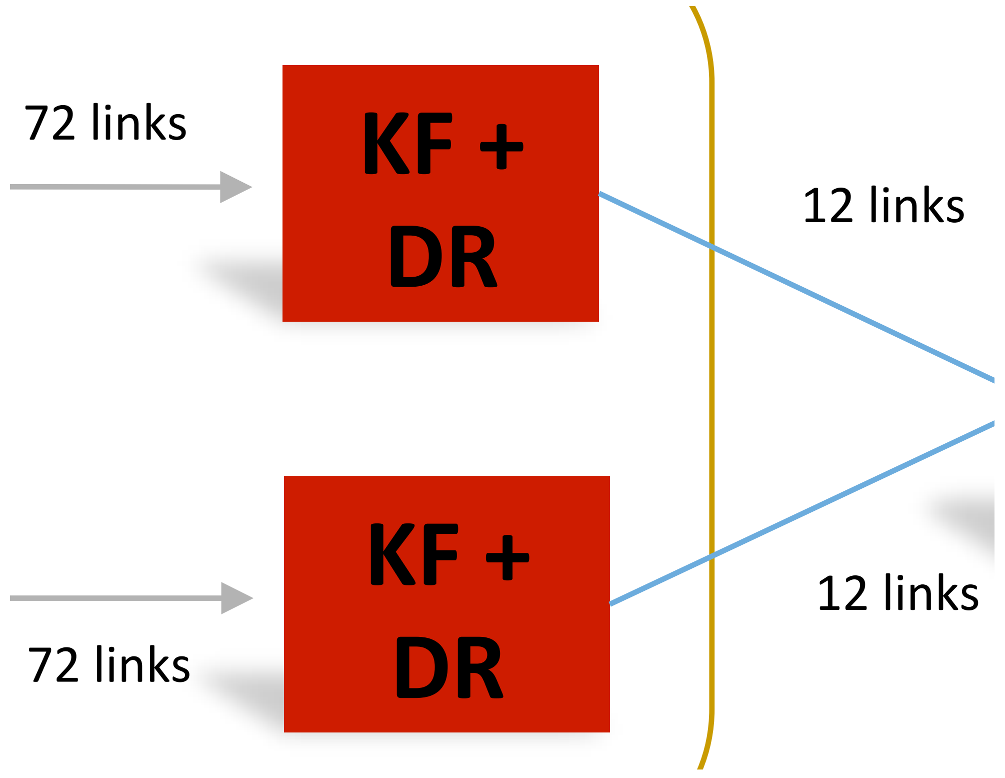
DEMONSTRATOR FIRMWARE

KALMAN FILTER (KF)

REPEAT FOR (A CONFIGURABLE) ACCUMULATION PERIOD (OR UNTIL 4 STUBS ARE ADDED TO ALL TRACKS)



One KF node - 36 per MP7



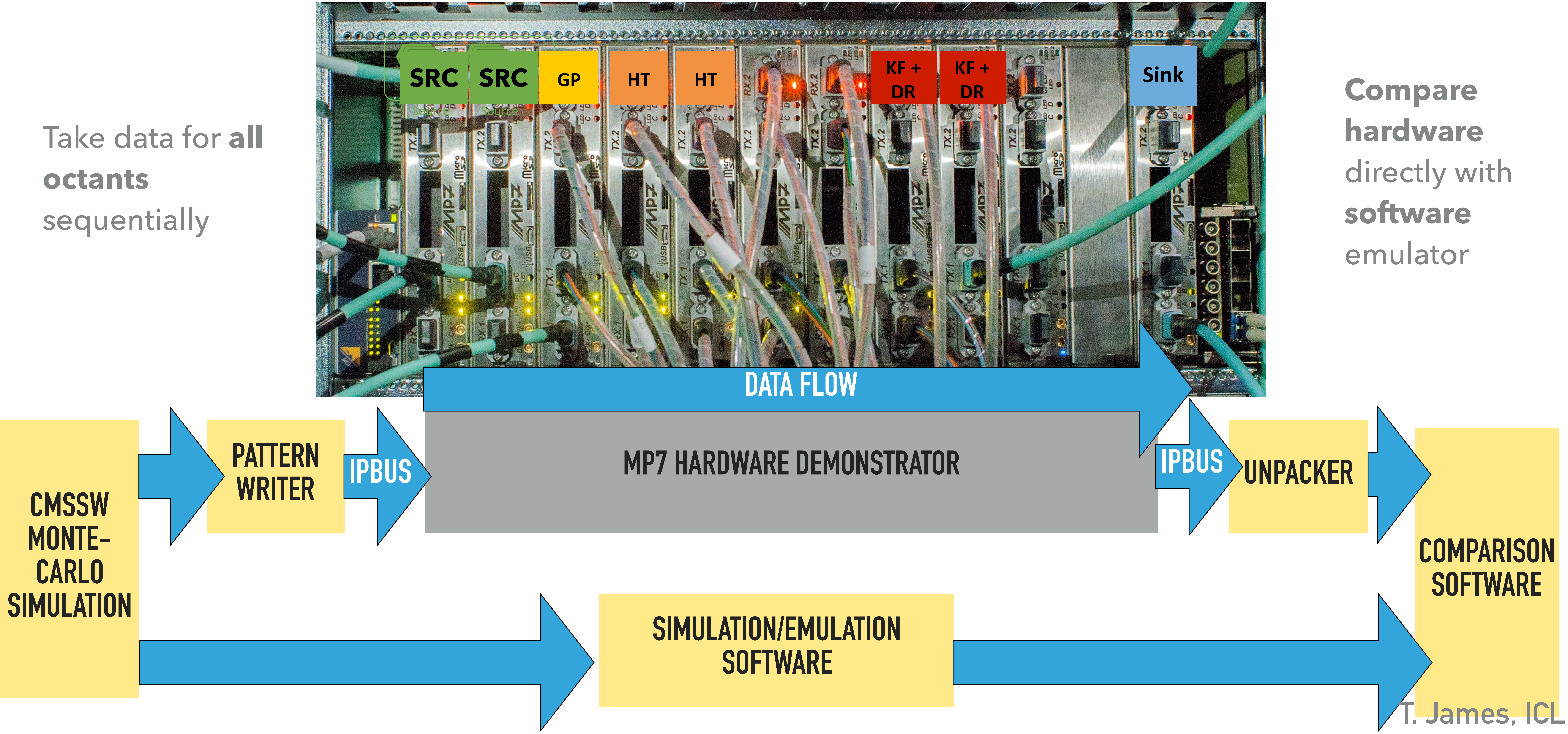
- **Accumulation period** configured to **1550 ns**
- **Processing latency** dominated by **matrix maths** update, **230 ns / iteration**

DEMONSTRATOR DATA TAKING

Objective - Run **Monte-Carlo physics samples** emulating **conditions at HL-LHC** through hardware demonstrator

Take data for **all octants** sequentially

Compare hardware directly with **software** emulator



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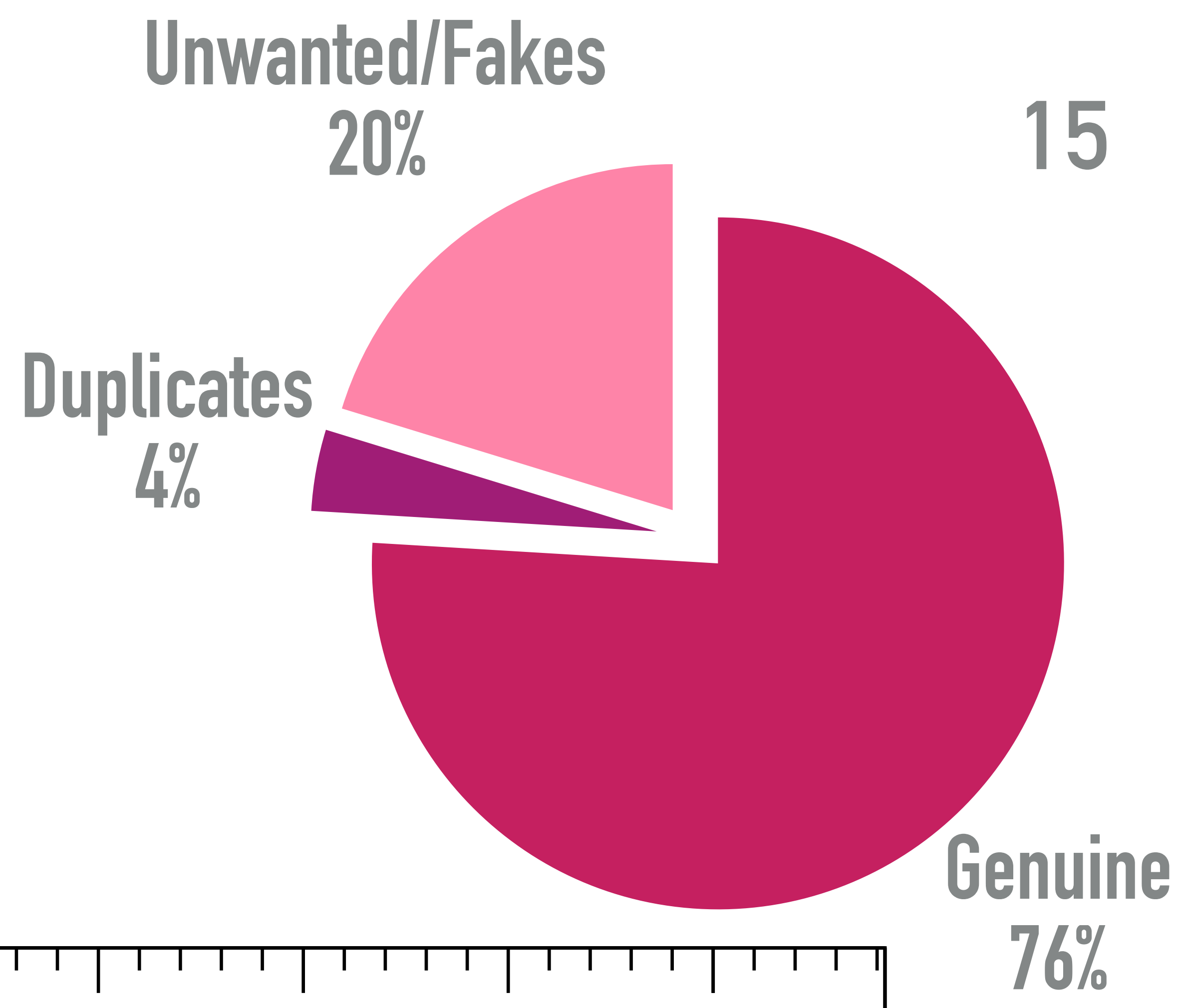
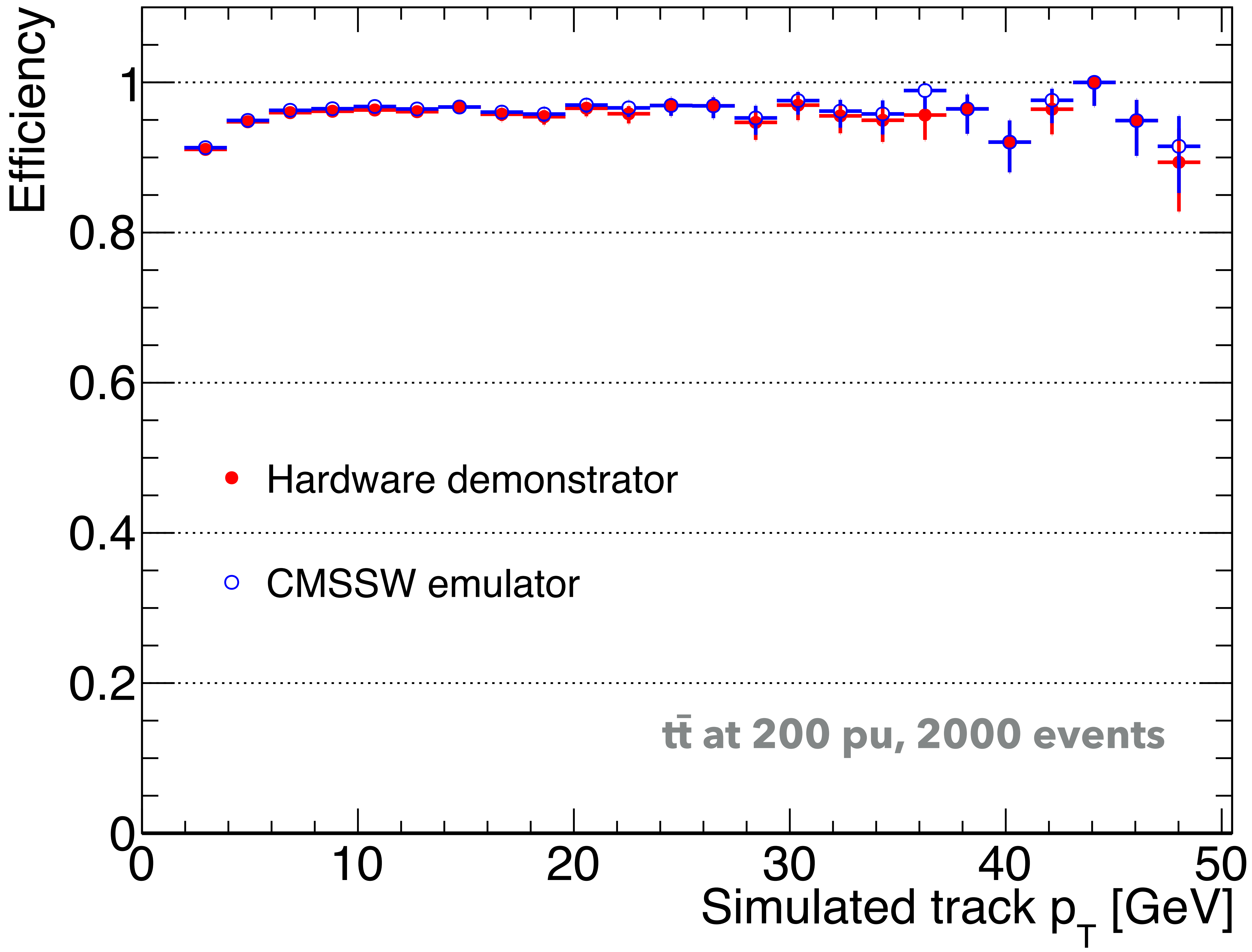
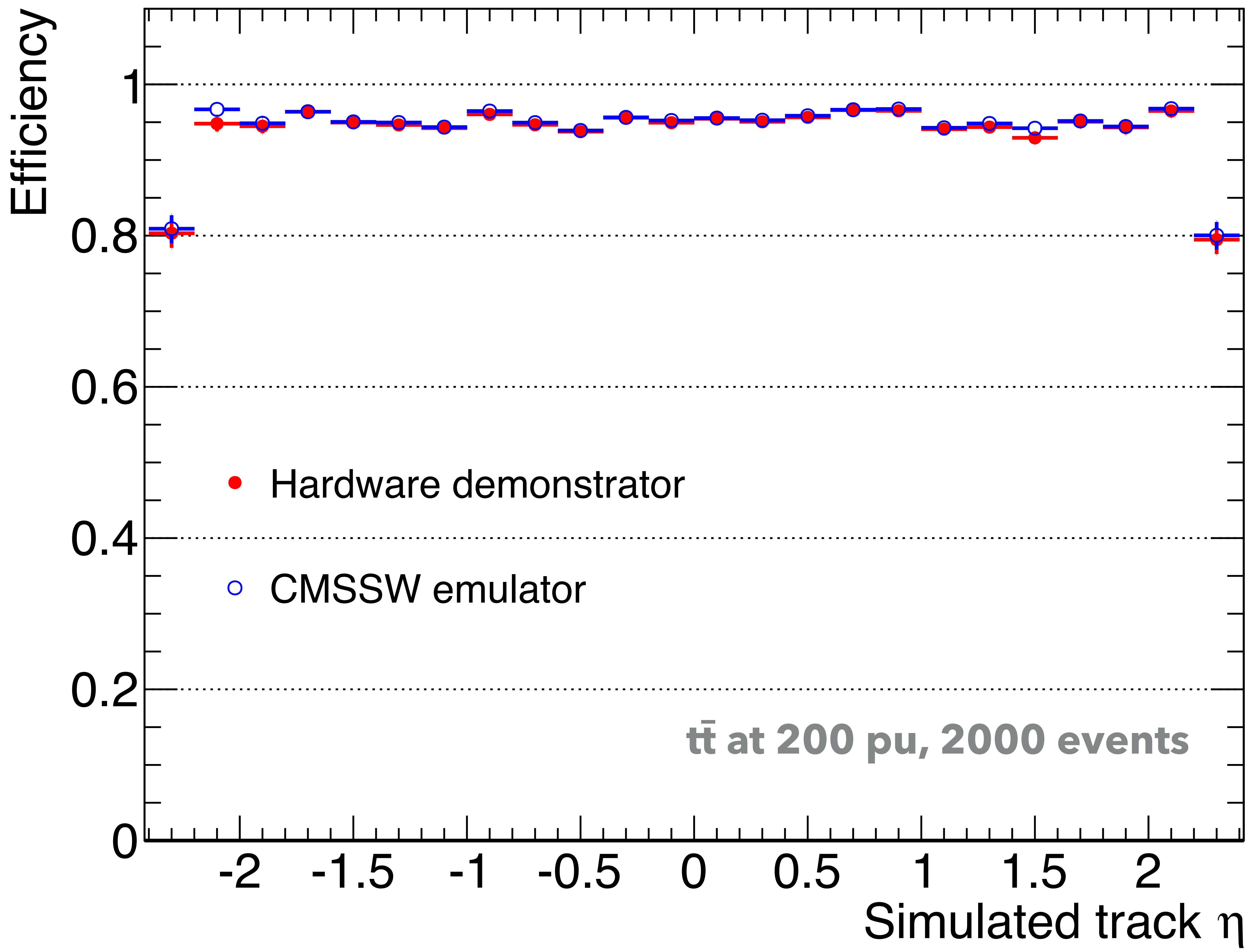
TRACK FINDING PERFORMANCE

~70 tracks per event average ($t\bar{t}$ at 200 PU)



- **95% average track finding efficiency** for inclusive $t\bar{t}$ tracks (> 3 GeV)
- **97%** for muons





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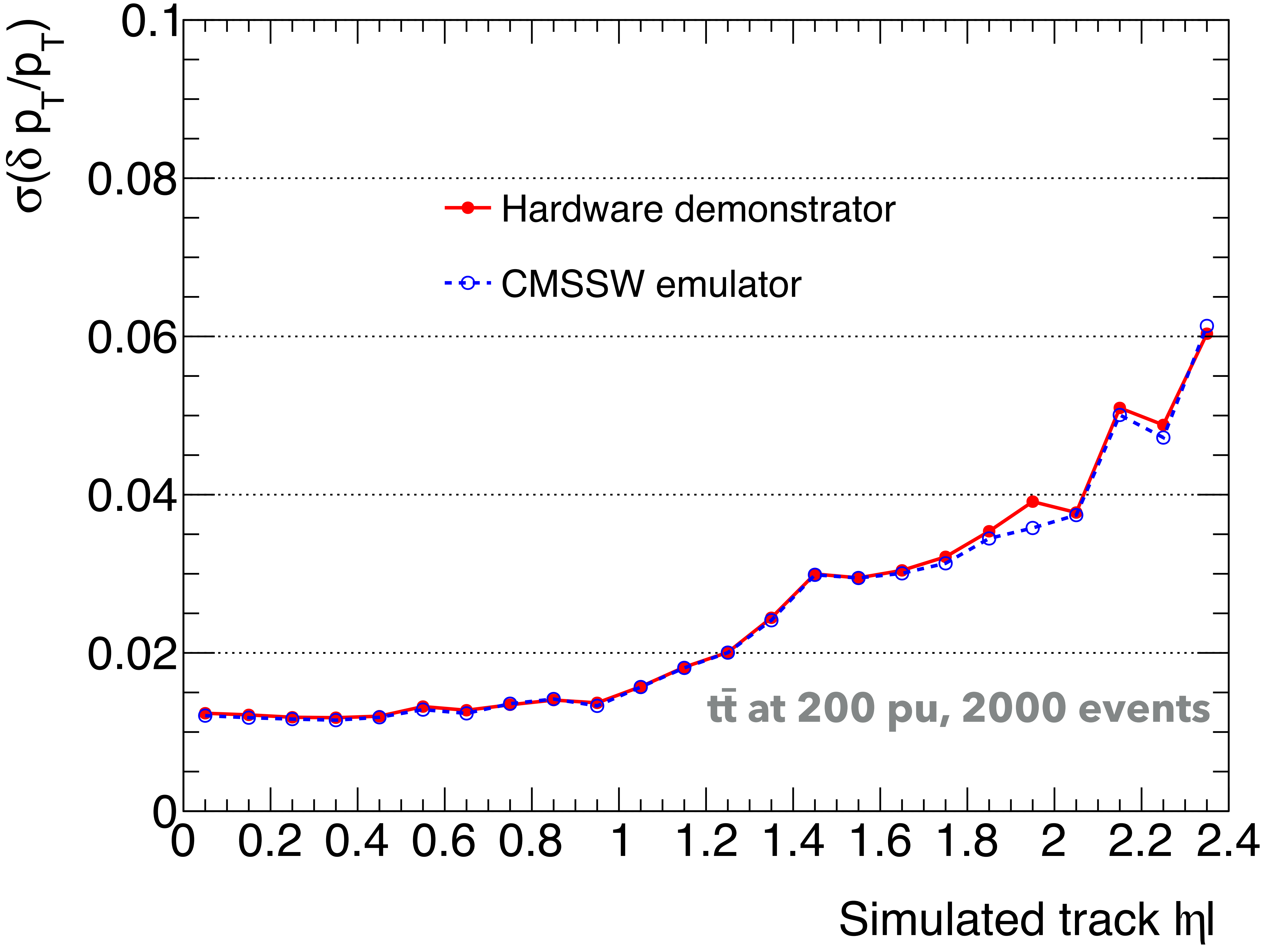
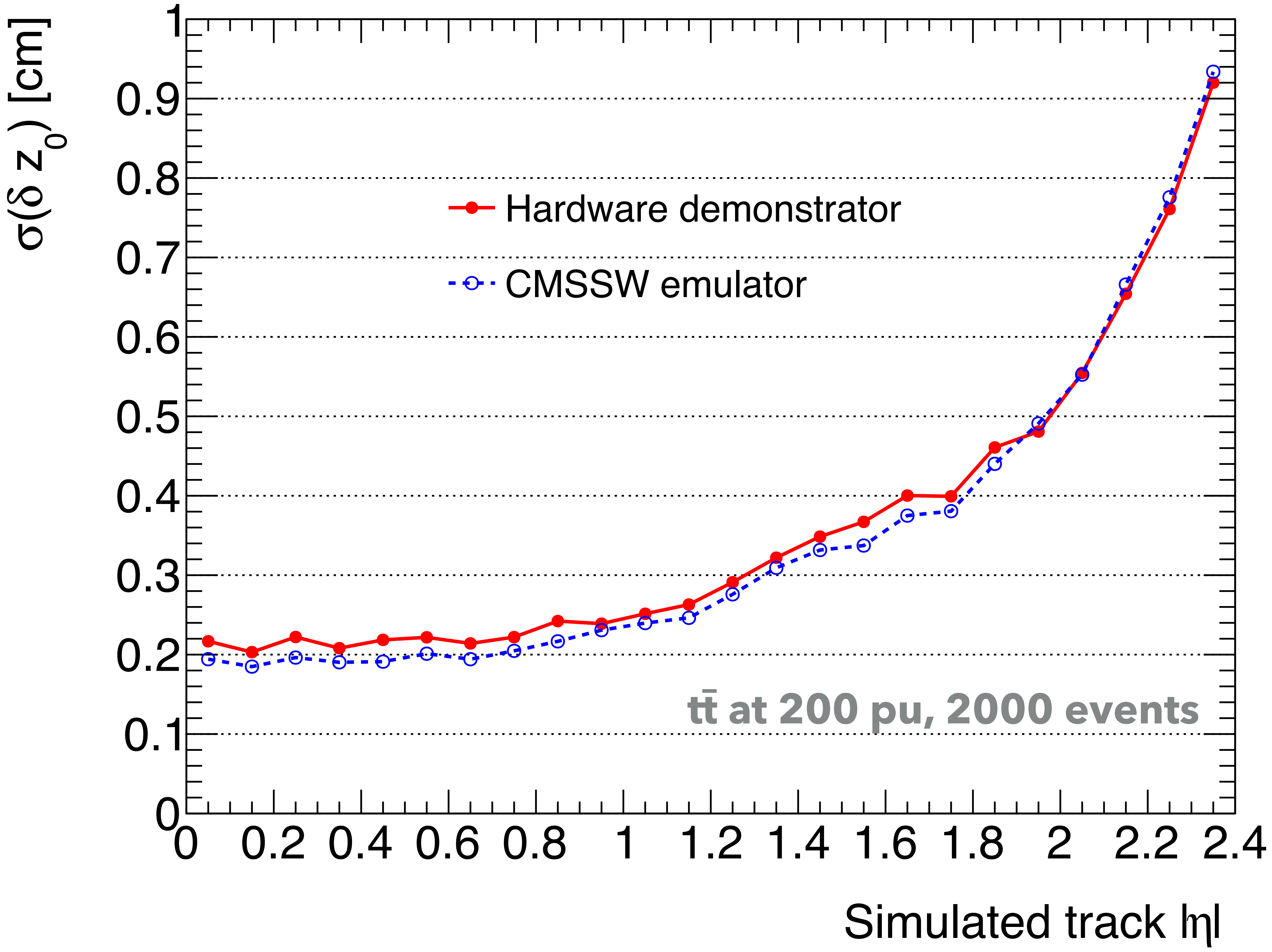
TRACK FINDING PERFORMANCE

p_T resolution -> precision of mass estimate of decaying particle

z_0 resolution -> ability to match tracks to initial decay vertices

- **~1% p_T resolution, 2 mm z_0 resolution in barrel**
  - 1-2 extra bits to encode stub position, **z_0** res -> 1mm in barrel





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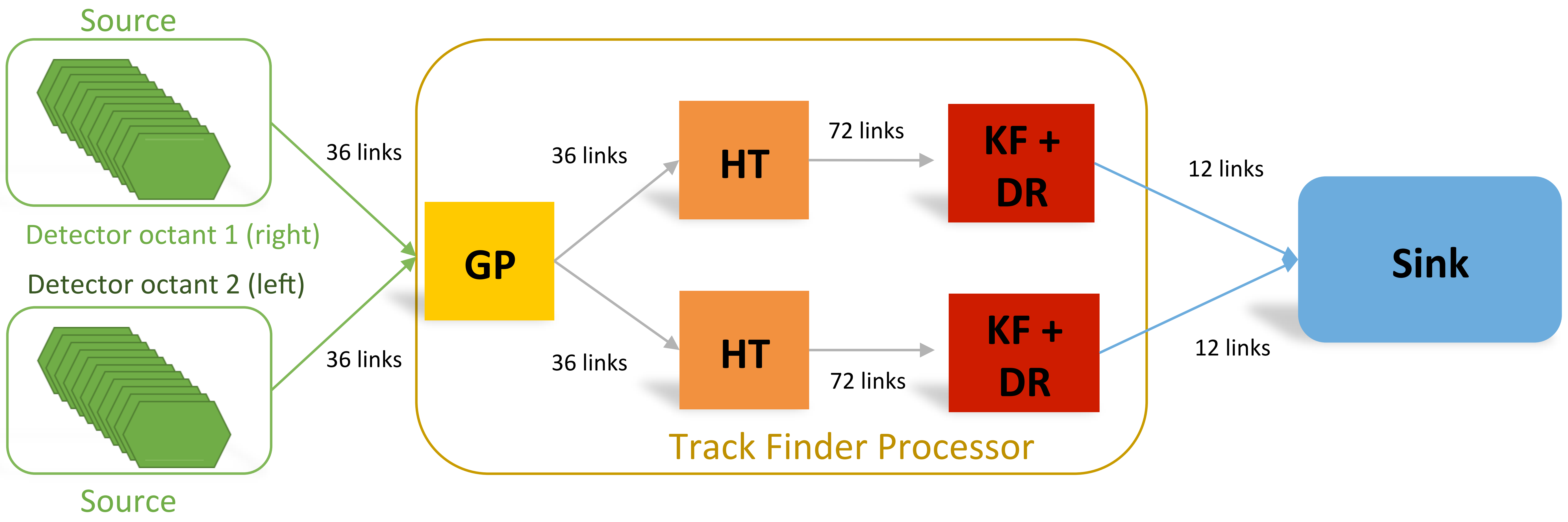
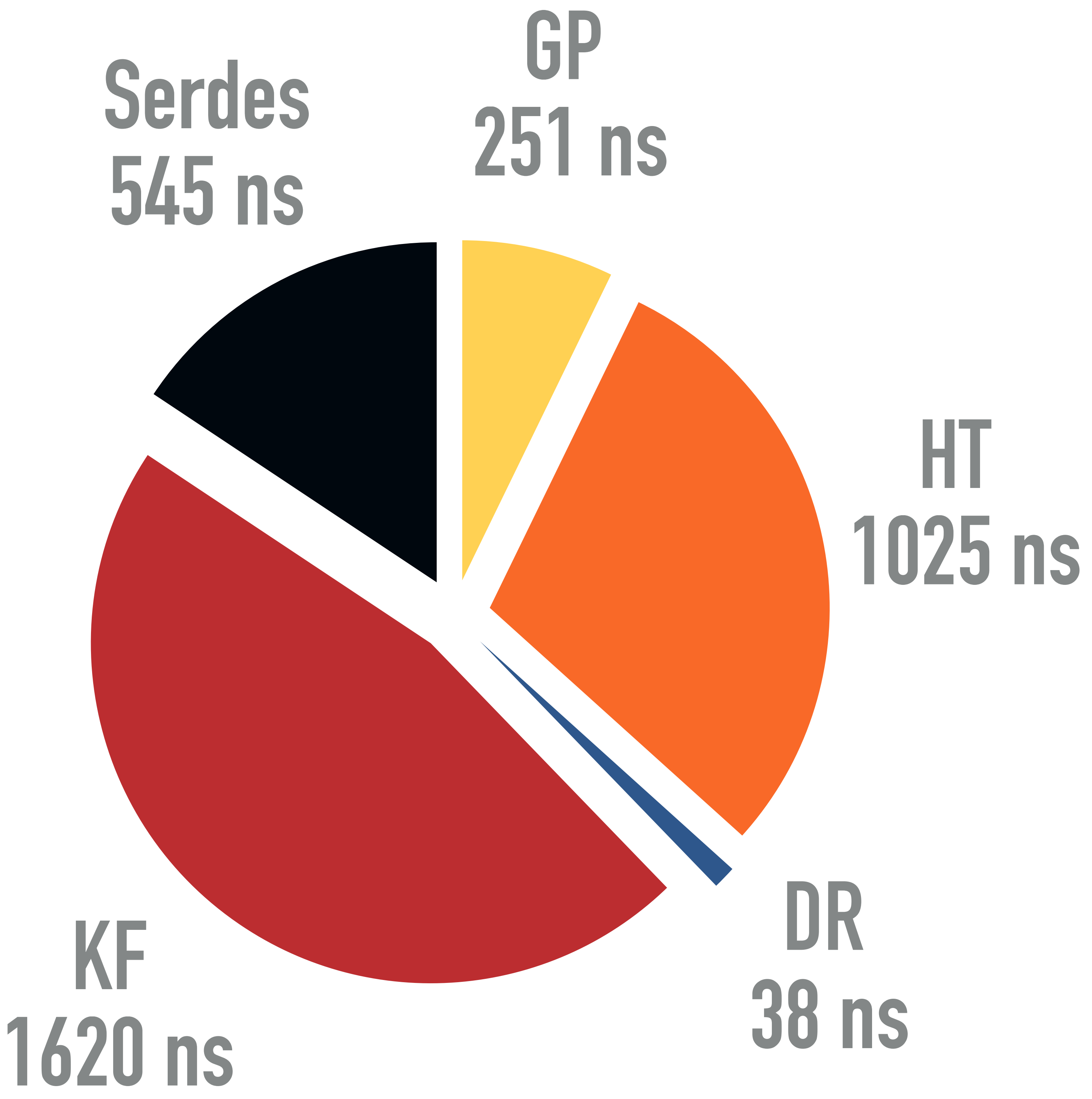
LATENCY MEASUREMENTS

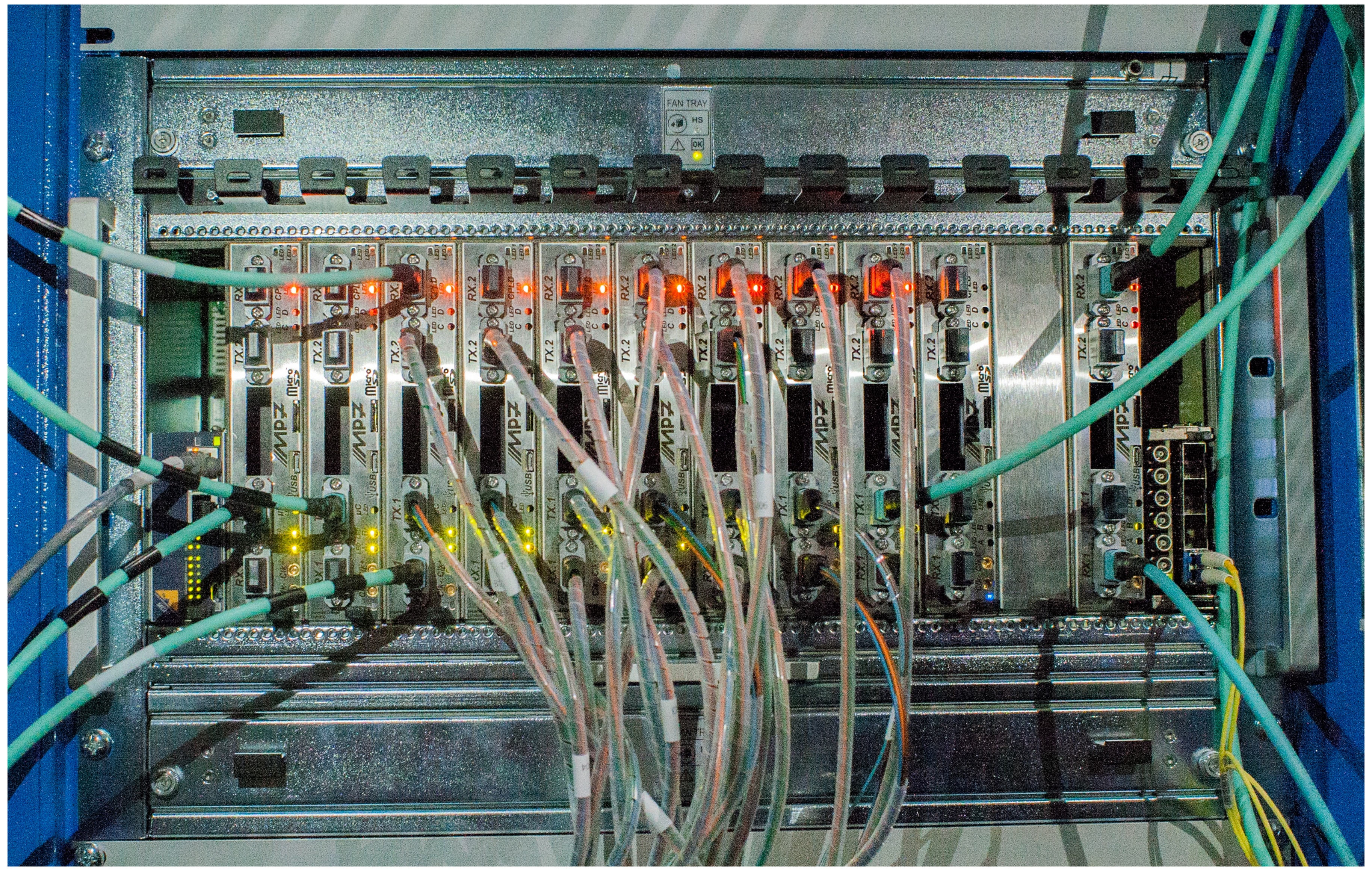


- **Fixed latency -** event independent
- Plenty of margin in design
- Room to increase clock speed, link speed, and to improve utilisation -> **lower latency possible**



SUMMARY

- **Highly flexible** track-finder/pattern recognition algorithm
- **Highly scalable,** time/physical segmentation could be as large/small as required based on data rates



- **Proven** with **currently available hardware**, that a level-1 track-trigger based on **FPGA** processing boards is a **feasible** and **safe** solution
- Plenty of **time to improve and optimise** algorithms for global trigger requirements

Thanks for listening

I look forward to answering your questions

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- An FPGA-Based Track Finder for the L1 Trigger of the CMS Experiment at the High Luminosity LHC Presented at 20th IEEE-NPSS Real Time Conference, Padua, Italy, 5-10 Jun 2016, doi:10.1109/RTC.2016.7543102.

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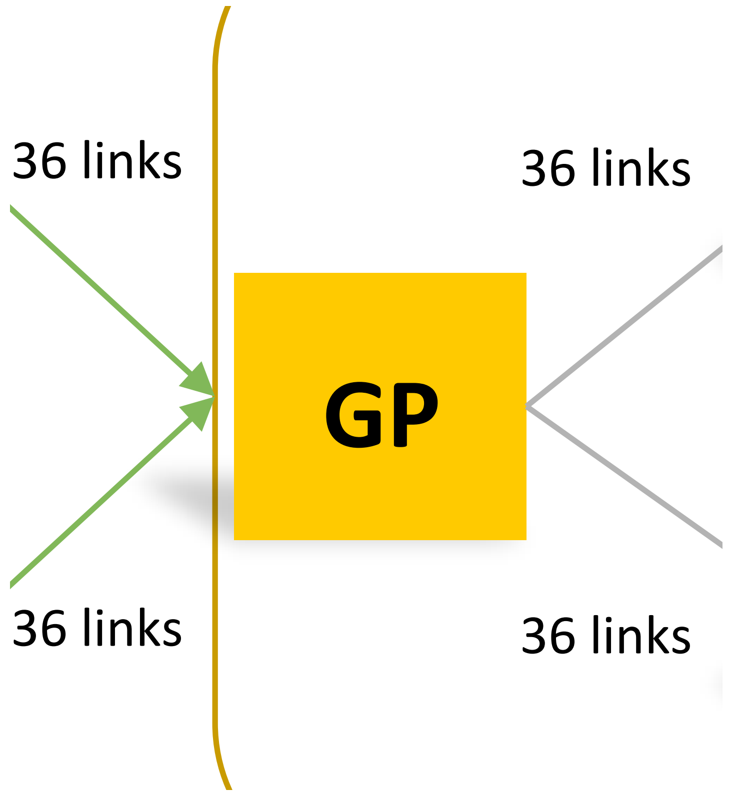
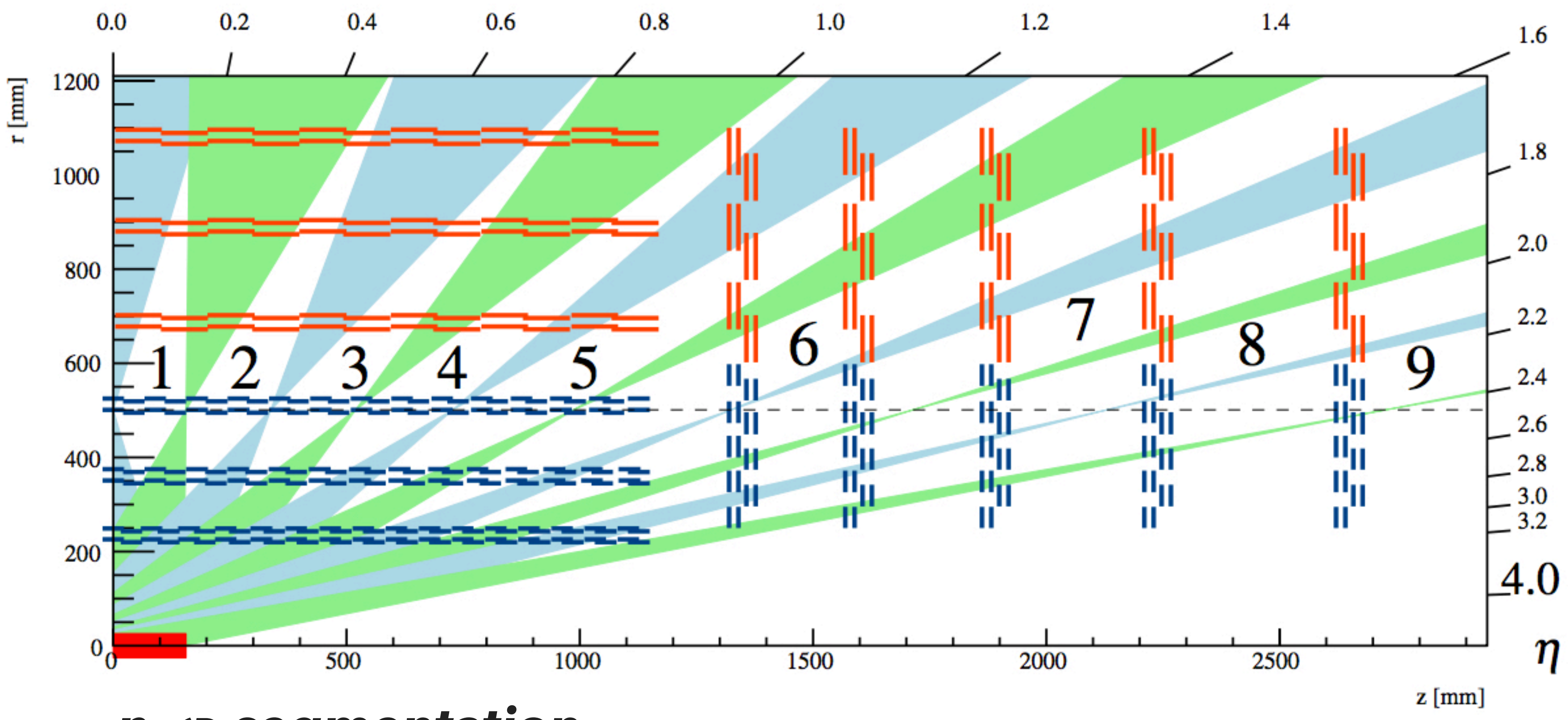
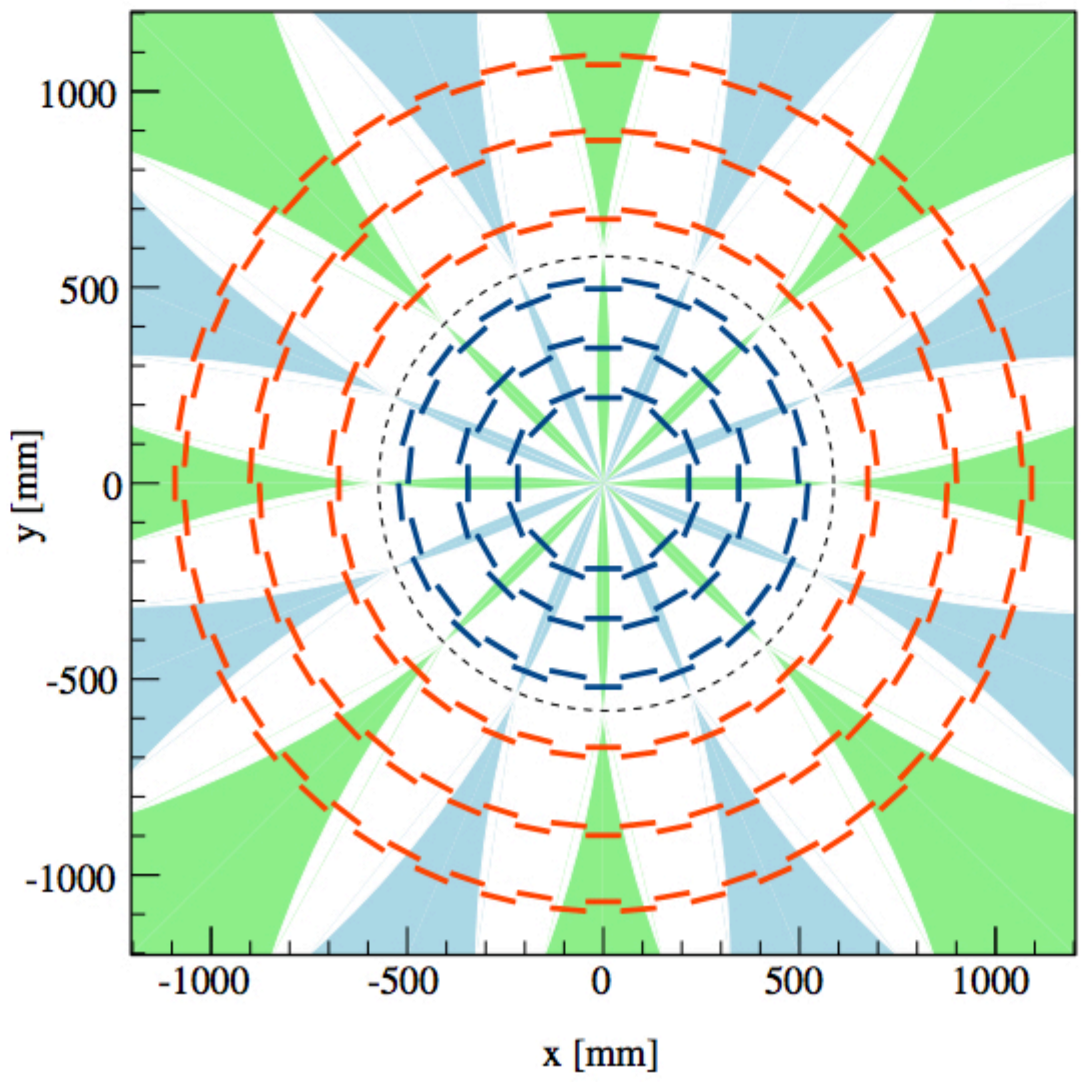
  - Maxeler Technologies
  - The Worshipful Company of Scientific Instrument Makers (UK)

GEOMETRIC PROCESSOR (GP)



- **Assigns stubs to 2 φ x 18 η sub-sectors**, **duplicating** across boundaries when necessary
  - Simplifies the track-finding task and allow for increased parallelisation downstream



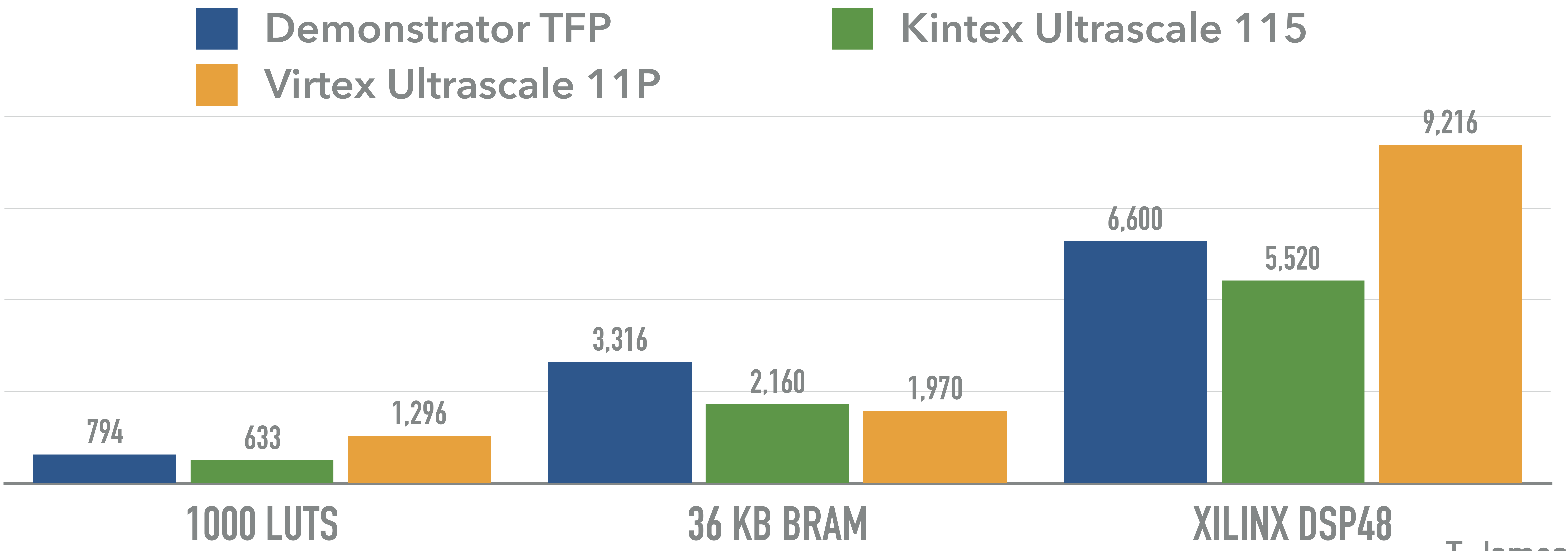


η, φ segmentation

- **Routes all stubs** in a given sector to **dedicated output link pairs**
  - 72 inputs -> 36 outputs
- Highly configurable arbitrator blocks

RESOURCE USAGE & FUTURE FPGA CHIPS

- Overall **resource usage** of the system shows that with some optimisations, a future TFP could feasibly consist of **two** KU115 or **one** VU11P FPGA
- Future work will be to build a system using the **KU115 FPGA** and **16.3 Gbps optical links** with a target latency of 2 μs



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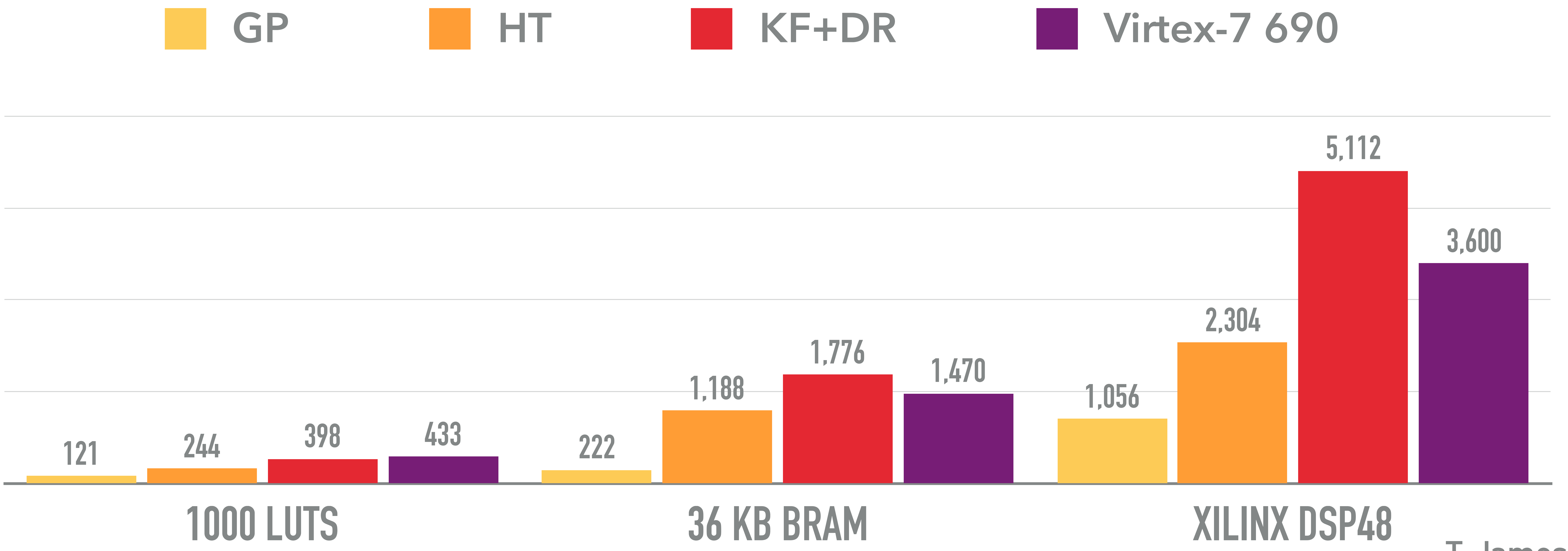

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	LUTs [10^3]	DSPs	FFs [10^3]	BRAM (36 Kb)
GP	121	1056	205	222
HT	244	2304	299	1188
KF and DR	398	5112	316	1776
Infrastructure per MP7	90	0	91	291
TFP Total (excl. infrastructure)	763	8472	820	3186
Virtex 7 690	433	3600	866	1470
Kintex Ultrascale 115	633	5520	1266	2160
Virtex Ultrascale+ 11P	1296	9216	2592	2016

SIMULATION RESULTS

Stage	Efficiency [%]	# of tracks	# of fakes	# of duplicates
HT	97.1	331	139	126
KF	95.1	190	27	103
DR	94.4	79	16	3
Full chain	94.4	79	16	3

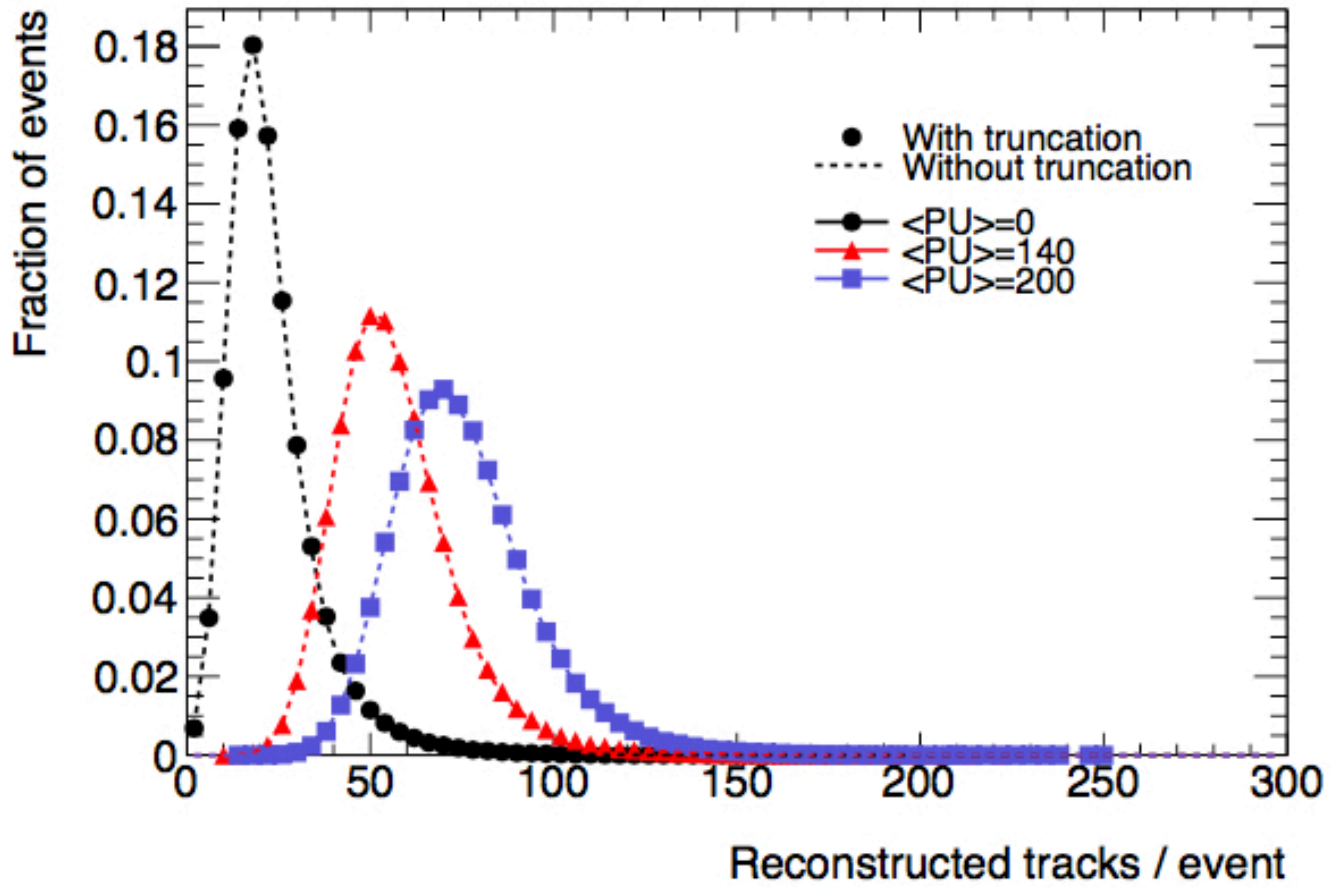


Figure 22: Total number of reconstructed tracks per event reconstructed in the tracker when processing $t\bar{t}$ events superimposed in 0, 140, and 200 PU events. These results are obtained from emulation, and are shown for when effects of truncation, caused by excess data flow through the system, are both included and excluded.

SIMULATION RESULTS

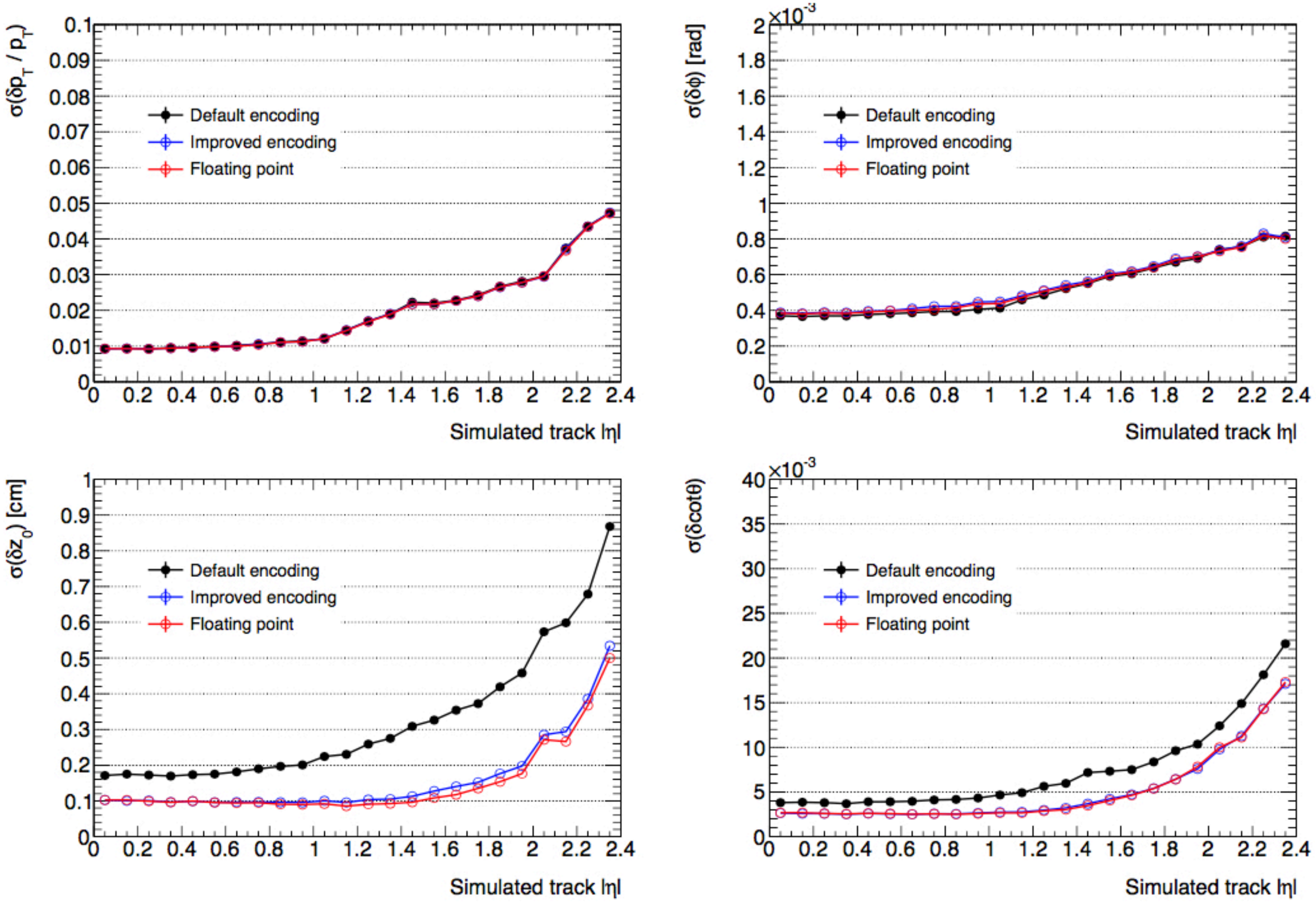
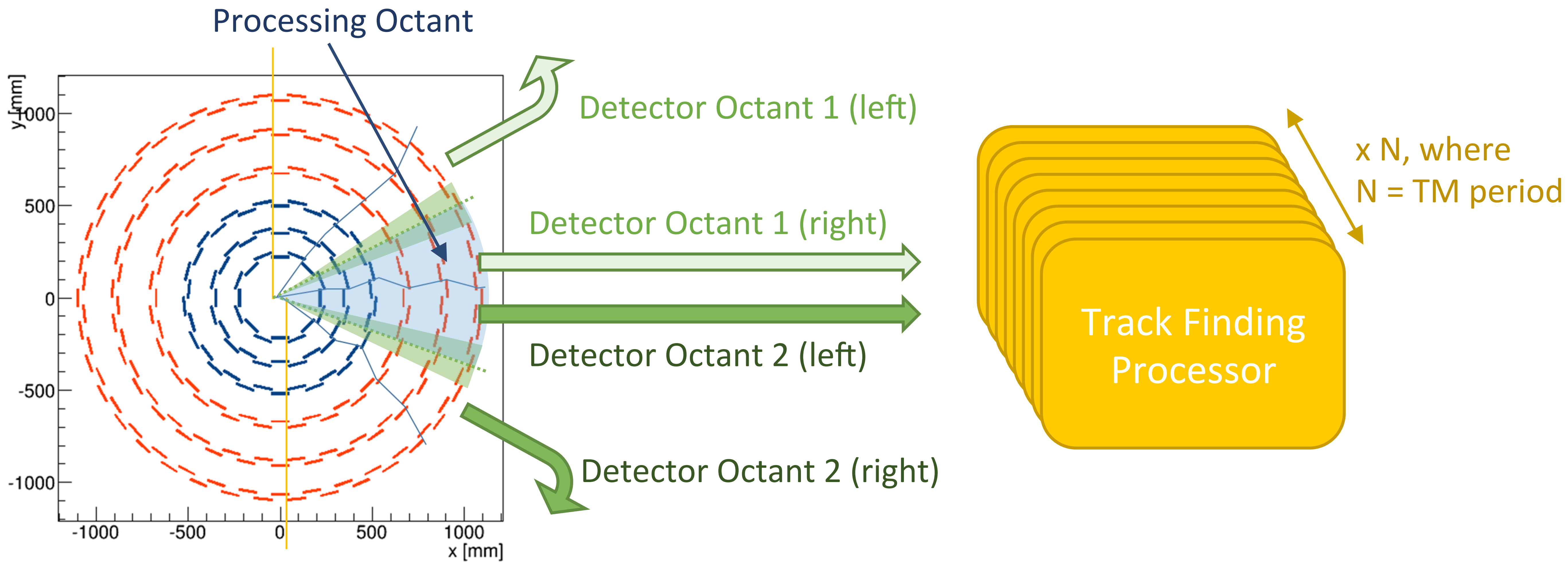


Figure 21: Relative p_T resolution, ϕ resolution [rad], z_0 resolution [cm] and $\cot\theta$ resolution measured for single isolated muons, with $5 < p_T^{\mu} < 15\,\text{GeV}$ obtained from emulation, using different levels of precision in simulation: Default encoding (10-bit r, 12-bit z, 15-bit ϕ stub coordinates); improved encoding (12-bit r, 14-bit z, 15-bit ϕ stub coordinates); and full floating-point simulation.

TRACK TRIGGER PROPOSAL

- Total available L1 time will be 12.5 μs, but **only ~4 μs is available for track finding**
- Must construct a track finder that is capable of processing **very high data rates (~20,000 stubs per event)** down to the O(10) genuine/interesting tracks expected on average, within this latency target
- **Proposal**: **Track Finding Processor (TFP) (FPGA data stream processing boards)** receive **data links from adjacent detector octants in φ**
- Fully **time-multiplexed** system
  - Processing of subsequent events done on parallel independent nodes
- **No further duplication or sharing between regions is required downstream**
  - **Highly scalable** system



- Each **TFP processes 1/8 in φ and 1/tmp** (time multiplex period) in time
- **One TFP becomes the demonstrator slice unit**

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