



### Thermal Mockup Studies of Belle II Vertex Detector

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## SuperKEKB/Belle II Upgrade





• The Belle II detector was rolled in in April 2017.

1980

1990

2000

2010

2020 Year

10<sup>30</sup>

10<sup>29</sup>

# Belle II Vertex Detector (VXD)



#### Silicon Vertex Detector(SVD)

- 4 layers of 172 double-sided silicon strip detectors (DSSDs)
- r=3.8/8.0/11.5/14cm; L=60cm
- ~1m<sup>2</sup>

Pixel Detector (PXD)

- 2 layers of 40 DEPFET sensors
- r=1.4/2.2cm; L=12cm
- ~0.027m<sup>2</sup>

Beam pipe

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### Belle II PXD: Ladder Design



- 2 layers pixel detector with 40 DEPFET sensors
- 7.68 million pixels with the pitch size:  $50x(55/60/70/85) \ \mu m^2$
- sensitive area size:
  - 12.50 X 44.80 mm<sup>2</sup> (layer.1)
  - 12.50 X 61.44 mm<sup>2</sup> (layer.2)
  - will be thinned down to 75  $\mu m.$
- Operated by 3 types of ASICs. Power consumption dominated by the ASICs at the end of sensor







Ladder formed from 2 sensors

- butt-face joint glueing
- ceramic mini-rods embedded in the thick rim of sensor



## **PXD Ladder Support**



Both layers are mounted on the combined support and cooling blocks (SCBs)

• connected by silver coated carbon fiber tubes for air cooling and grounding

Designed and produced by MPI

Ladders screwed on support

- elongated hole on the FWD side
- M1.2 screw with plastic washer o-ring to prevent electrical contact between screw and silicon.
- torque of 7mNm allows for compensating of thermal expansions.

SCB, manufactured using 3D printing technology, with enclosed  $CO_2$  and open N2 channels inside.

N<sub>2</sub> holes

 $N_2$  tube

 $CO_2$  inlet

 $CO_2$  outlet





## Belle II SVD Module



#### Silicon Vertex Detector

- Four layers (numbered from 3 to 6) from ladders with up to 5 DSSD modules in a row.
- p-strip pitch: 50(75)µm, n-strip pitch: 160(240)µm
- Supported by two ribs and Airex foam core sandwich.
- readout chip: APV25 (thinned down to 100 µm thickness)
- the Origami concept, all APV25 are aligned in a row and cooled by a single cooling pipe per ladder.



#### Modules in the barrel



### **SVD** Layout









#### Powder Consumption

CO <sub>2</sub> Circuit	Detector	Half	Layer	Туре	Side	Power [W]
1	PXD	up	1&2	endring	bwd	90
2			1&2	endring	fwd	90
3		down	1&2	endring	bwd	90
4			1&2	endring	fwd	90
	360					
5	SVD	left	3-6	endring	bwd	93
6		right	3-6	endring	bwd	93
7		left	3-6	endring	fwd	93
8		right	3-6	endring	fwd	93
9		left	4&5	origami	bwd	68
10		right	4&5	origami	bwd	68
11		left	6	origami	bwd	96
12		right	6	origami	bwd	96
	700					
	1060					

#### Requirements

- PXD: Sensor < 25°C to minimize shot noise due to leakage current; ASICs < 50°C to avoid risk of electro-migration.
- □ SVD: APV25 readout chips surface@~0°C for SNR improvement.
- Power consumption: PXD 360W; SVD 700W, together with the heat load through 9m of vacuum isolated flex lines; required cooling capacity of 2-3kW.
- VXD needs to be thermally isolated against CDC and beam pipe. Room temperature at the inner surface of CDC is required for stable calibration and dE/ dx performance



### 2-phase CO<sub>2</sub> cooling





17

From B. Verlaat, SLAC Advanced Instrumentation Seminars in March 2012

The 2-phase  $CO_2$  cooling is an efficient concept for low-mass detector.

- > Heat removal by evaporating liquid  $CO_2$  at the constant temperature and pressure.
- > The temperature can be controlled and monitored by the pressure.
- Challenges: need to guarantee the 2-phase state, otherwise "dry-out".

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## VXD Cooling System







Belle II







## VXD Thermal Mockup@DESY







- The long and thin cooling lines cause pressure drops, which result in temperature gradients.
- □ Relatively big contribution of pressure drop in transfer flex line, to ensure balanced  $CO_2$  mass flow in each circuit.







□ Additional pressure drop of about 1 bar results from the heat load in PXD ASICs.

# Temperature Distribution on PXD



• CO<sub>2</sub>@-25°C; N<sub>2</sub> 20L/min Sensor Layer 2-fwo ensor Layer 2-bw Power consumption\*: • DCD/DHP 8W, Switcher 0.5W, Temperature(°C) no SVD cooling & heat L2.top (y~ 20mm) matrix 0.5W SVD cooling & heat L2.middle(y~ 0mm) Temperature is monitored by resistance thermometers. L2.bottom(y~ -20mm) • With SVD cooling and power on, L2.average in y temperature on PXD changes ~2°C. 10 Layer 2 .2.3 \_\_\_L2.5 L.2 top -50 50 0 z(mm) L.1 top L2.1 ★ L1.top (y~ 13mm) L.2 middle-L2.7 L1.8 L1.bottom(y~ -13mm) Lemperatul 15 L.1 bottom Layer.1 L1.average in y L.2 bottom-2.11 L2.9• By changing the CO<sub>2</sub> set point, the temperature distribution gets shifted, while <sup>10</sup> the gradients stay. -50 0 50 • By increasing the N<sub>2</sub> flow, the gradient gets z(mm)  $\Delta T_v \sim 5^{\circ}C, \Delta T_7 \sim 7^{\circ}C$ improved.

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\* Based on the initial numbers for the first versions of chips for DEPFET, the final numbers need to be confirmed in future.



### Vibration v.s. N<sub>2</sub> flow





Vibration with RMS amplitude about 0.2um.





- A peak at about 175 Hz is observed, amplitude increases with the flow rate reaching about  $0.02 \mu m$  when 20L/min of N2 is injected.
- Flat background indicated by the measurements at the fixation screws on the SCB.

### **Temperature in SVD**





- Temperature in the middle of L.3 sensors is strongly influenced by PXD, therefore relies on the injected N2 flow.
- For L4/5/6, with nominal load, the maximum temperature on FW/BW edges reaches about 20°C, and module ASICs reach about 25-30°C.

L3 thermal mangement problem

 Finite Element (FE) Simulation indicates most of the gradient (~45°C in FW) is in the endring finger, made of stainless steel.



Update with copper insert, under testing in Melbourne.



Belle I

# **Temperature in VXD Volume**

DESY

Temperature on the top/bottom of inner side of VXD CFRP shield and CDC inner surface (AI shield).

CO2@-25°C



	VXD shield inner surface	CDC inner cover
top	10	15
bottom	4	8

About 6°C's gradient.

#### Thermal transfer through cables





- Electronic cables are insert to FW +x half endring, contacting L5&6.
- Little influence from cables' thermal conductivity.



### Dew Point in Dry Volume v.s. N2 flow







### Dew Point in Dry Volume v.s. N<sub>2</sub> flow







## Summary



- Operating environment of Belle II PXD and SVD are strongly coupled, meanwhile, it will influence the surrounding drift-chamber (CDC). Evaporative 2-phase CO<sub>2</sub> and airflow injection perform VXD cooling.
- □ A full-size thermal mock-up is built at DESY, to verify and optimize the cooling concept of Belle II VXD.

#### PXD

- With CO2 set at -25°C and N2 flow of 20L/min, temperature on PXD ladders is determined as <25°C.
- Temperature gradient along the sensitive area is  $\Delta Tz ~7^{\circ}C$ , top-bottom gradient  $\Delta Ty ~5^{\circ}C$ .
- N2 flow of 20L/min induces negligible vibrations on PXD sensors.

#### SVD

- ASICs on L3 suffer from high temperature, modifications are underway.
- Other ASICs temperature is <30°C.
- Heat transport through SVD electronic cables has minor effect to temperature distribution.

#### Dry Volume

• N2 injection >20L/min into the dry volume is required to avoid condensation.

#### CDC

• Temperature on the inner surface of CDC cylinder range from 15°C(top) to 8°C(bottom).

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Backup

# Temperature Distribution on PXD



- CO<sub>2</sub>@-30°C; N<sub>2</sub> 23L/min
- A plastic cylinder (ID 18cm, length 70cm) act as dry volume.
- Temperature is monitored by resistance thermometers, Pt100s and infrared camera



- By changing the CO<sub>2</sub> set point, the temperature distribution gets shifted, while the gradients stay.
- By increasing the N<sub>2</sub> flow, the gradient gets improved.



### Study Onset of Dry-out



When the vapor quality gets too high, there will be no liquid film on the capillary walls, then result in a shape increase of the cooling block temperature.



### The dry out happens in the last 6 sensors

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Estimated mass flow to get rid of 'dry out' ➤ CO<sub>2</sub>@-30°C, mass flow in the mockup should not be lower than 5.4 g/s, giving the pressure drop of about 1.7 bar in the cooling circuit.